

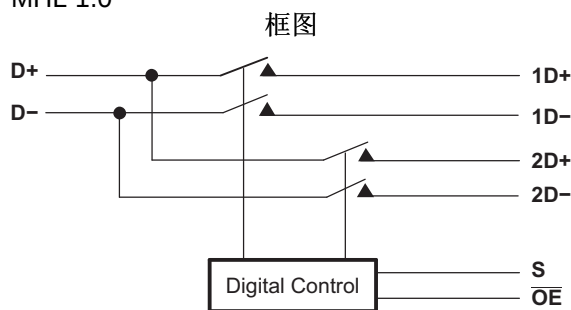
具有单使能端和 IEC 3 级 ESD 保护的 TS3USB221E 高速 USB 2.0 (480Mbps) 1:2 多路 复用器 – 多路信号分离器

1 特性

- V_{CC} 工作范围: 2.3V 至 3.6V
- 开关 I/O 支持高达 5.5V 的信号
- 1.8V 兼容控制引脚输入
- $\overline{OE}$ 禁用时采用低功耗模式 (1 μ A)
- $r_{ON} = 6\Omega$ (最大值)
- $\Delta r_{ON} = 0.2\Omega$ (典型值)
- $C_{io(on)} = 7pF$ (最大值)
- 低功耗 (最大值为 30 μ A)
- ESD 性能测试符合 JESD 22 标准
 - 7000V 人体放电模型 (A114-B, II 类)
 - 1000V 充电器件模型 (C101)
- ESD 性能 I/O 端口接地
 - 12kV 人体放电模型 (A114-B, II 类)
 - $\pm 7kV$ 接触放电 (IEC 61000-4-2)
- 高带宽 (典型值为 1GHz)

2 应用

- 为 USB 1.0、1.1 和 2.0 路由信号
- 手机
- 数码相机
- 笔记本电脑
- USB I/O 扩展
- MHL 1.0



3 说明

TS3USB221E 是一款高带宽开关, 专为电话和消费型应用 (如具有 USB I/O 受限的集线器或控制器的手机、数码相机和笔记本电脑) 中高速 USB 2.0 信号的开关而设计。此开关具有较宽的带宽 (1GHz), 这一特性使得信号传递具有最少的边缘失真和相位失真。该器件将 USB 主器件差动输出复用到一个相应的输出 (共两个输出)。此开关为双向开关, 输出端高速信号具有极少或零衰减。TS3USB221E 专为低位间偏移和高通道间噪声隔离而设计, 并且与高速 USB 2.0 (480Mbps) 等各种标准兼容。

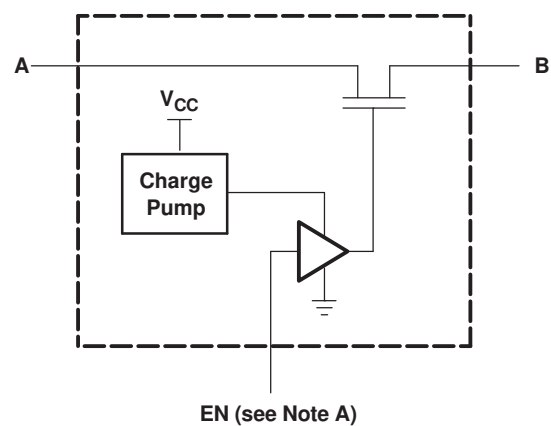
TS3USB221E 在所有引脚上集成了 ESD 保护单元, 采用 SON 封装 (3mm × 3mm) 和小型 μ QFN 封装 (2mm × 1.5mm), 自然通风条件下的工作温度范围为 -40°C 至 85°C 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TS3USB221E	VSON (10)	3.00mm × 3.00mm
	UQFN (10)	1.50mm × 2.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

每个 FET 开关 (SW) 的简化原理图



A. EN 是应用于开关的内部启用信号。



目录

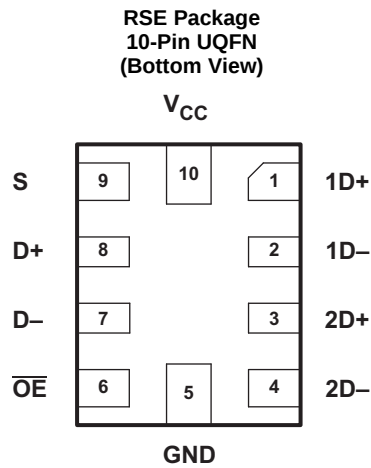
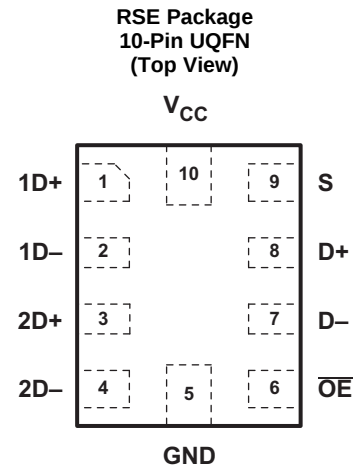
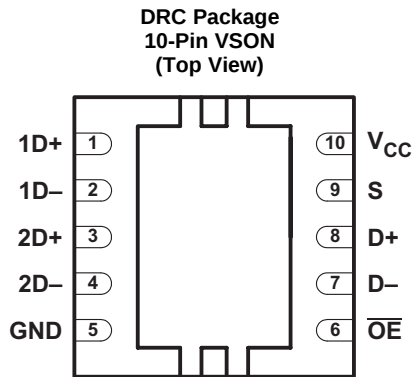
1	特性	1	8.1	Overview	12
2	应用	1	8.2	Functional Block Diagram	12
3	说明	1	8.3	Feature Description	12
4	修订历史记录	2	8.4	Device Functional Modes	12
5	Pin Configuration and Functions	3	9	Application and Implementation	13
6	Specifications	4	9.1	Application Information	13
6.1	Absolute Maximum Ratings	4	9.2	Typical Application	13
6.2	ESD Ratings	4	10	Power Supply Recommendations	15
6.3	Recommended Operating Conditions	4	11	Layout	15
6.4	Thermal Information	5	11.1	Layout Guidelines	15
6.5	Electrical Characteristics	5	11.2	Layout Example	16
6.6	Dynamic Electrical Characteristics, $V_{CC} = 3.3\text{ V}$ $\pm 10\%$	6	12	器件和文档支持	17
6.7	Dynamic Electrical Characteristics, $V_{CC} = 2.5\text{ V}$ $\pm 10\%$	6	12.1	文档支持	17
6.8	Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 10\%$	6	12.2	接收文档更新通知	17
6.9	Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 10\%$	6	12.3	支持资源	17
6.10	Typical Characteristics	7	12.4	商标	17
7	Parameter Measurement Information	8	12.5	静电放电警告	17
8	Detailed Description	12	12.6	Glossary	17
			13	机械、封装和可订购信息	17

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (April 2015) to Revision D	Page
• 已更改 将 V_{CC} 工作范围从 2.5V 至 3.3V 更改成了 2.3V 至 3.6V	1
Changes from Revision B (July 2012) to Revision C	Page
• 已添加 引脚配置和功能 部分、ESD 额定值 表、热性能信息 表、特性 说明 部分、器件功能模式、应用和 实施 部分、 电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分	1
• 删除了 订购信息 表	1
Changes from Revision A (February 2010) to Revision B	Page
• 更新了 订购信息 表中 RSE 封装的顶部标记	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1D+	1	I/O	USB port 1
1D-	2	I/O	
2D+	3	I/O	USB port 2
2D-	4	I/O	
GND	5	—	Ground
$\overline{\text{OE}}$	6	I	Bus-switch enable
D-	7	I/O	Common USB port
D+	8	I/O	
S	9	I	Select input
V _{CC}	10	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		–0.5	4.6	V
V _{IN}	Control input voltage ⁽²⁾⁽³⁾		–0.5	7	V
V _{I/O}	Switch I/O voltage ⁽²⁾⁽³⁾⁽⁴⁾		–0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		–50	mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		–50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±120	mA
	Continuous current through V _{CC} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	DRC package		48.7	°C/W
		RSE package		243	
T _{stg}	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except GND, $\overline{OE}$, S and V _{CC}	±12000
			Pins GND, $\overline{OE}$, S and V _{CC}	±7000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All pins except GND, $\overline{OE}$, S and V _{CC}	±7000
			Pins GND, $\overline{OE}$, S and V _{CC}	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See ⁽¹⁾.

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0.46 × V _{CC}		V
		V _{CC} = 2.7 V to 3.6 V	0.46 × V _{CC}		
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V		0.25 × V _{CC}	V
		V _{CC} = 2.7 V to 3.6 V		0.25 × V _{CC}	
V _{I/O}	Data input/output voltage		0	5.5	V
T _A	Operating free-air temperature		–40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3USB221E		UNIT
		DRC (VSON)	RSE (UQFN)	
		10 PINS	10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	57.7	169.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	87.7	84.7	
R _{θJB}	Junction-to-board thermal resistance	32.6	94.9	
ψ _{JT}	Junction-to-top characterization parameter	8.2	5.7	
ψ _{JB}	Junction-to-board characterization parameter	32.8	94.9	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	18.5	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}	V _{CC} = 3.6 V, 2.7 V,	I _I = –18 mA			–1.8	V
I _{IN} Control inputs	V _{CC} = 3.6 V, 2.7 V, 0 V,	V _{IN} = 0 V to 3.6 V			±1	μA
I _{OZ} ⁽³⁾	V _{CC} = 3.6 V, 2.7 V, V _O = 0 V to 5.25 V, V _I = 0 V,	V _{IN} = V _{CC} or GND, Switch OFF			±1	μA
I _{OFF}	V _{CC} = 0 V	V _{I/O} = 0 V to 5.25 V			±2	μA
		V _{I/O} = 0 V to 3.6 V			±2	
		V _{I/O} = 0 V to 2.7 V			±1	
I _{CC}	V _{CC} = 3.6 V, 2.7 V, V _{IN} = V _{CC} or GND,	I _{I/O} = 0 V, Switch ON or OFF			30	μA
I _{CC} (low power mode)	V _{CC} = 3.6 V, 2.7 V, V _{IN} = V _{CC} or GND	Switch disabled (OE in high state)			1	μA
I _{CC} ⁽⁴⁾ Control inputs	One input at 1.8 V, Other inputs at V _{CC} or GND	V _{CC} = 3.6 V			20	μA
		V _{CC} = 2.7 V			0.5	
C _{in} Control inputs	V _{CC} = 3.3 V, 2.5 V,	V _{IN} = 3.3 V or 0 V		1.5	2.5	pF
C _{IO(OFF)}	V _{CC} = 3.3 V, 2.5 V,	V _{I/O} = 3.3 V or 0 V, Switch OFF		3.5	5	pF
C _{IO(ON)}	V _{CC} = 3.3 V, 2.5 V,	V _{I/O} = 3.3 V or 0 V, Switch ON		6	7.5	pF
r _{ON} ⁽⁵⁾	V _{CC} = 3 V, 2.3 V	V _I = 0 V, I _O = 30 mA		3	6	Ω
		V _I = 2.4 V, I _O = –15 mA		3.4	6	
Δr _{ON}	V _{CC} = 3 V, 2.3 V	V _I = 0 V, I _O = 30 mA		0.2		Ω
		V _I = 1.7, I _O = –15 mA		0.2		
r _{ON(flat)}	V _{CC} = 3 V, 2.3 V	V _I = 0 V, I _O = 30 mA		1		Ω
		V _I = 1.7, I _O = –15 mA		1		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Dynamic Electrical Characteristics, $V_{CC} = 3.3\text{ V} \pm 10\%$

 over operating range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 3.3\text{ V} \pm 10\%$, $\text{GND} = 0\text{ V}$

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
X_{TALK}	Crosstalk	$R_L = 50$, $f = 250\text{ MHz}$	-40	dB
O_{IRR}	OFF isolation	$R_L = 50$, $f = 250\text{ MHz}$	-40	dB
BW	Bandwidth (-3 dB)	$R_L = 50$	1	GHz

 (1) For Maximum or Minimum conditions, use the appropriate value specified under [Electrical Characteristics](#) for the applicable device type.

6.7 Dynamic Electrical Characteristics, $V_{CC} = 2.5\text{ V} \pm 10\%$

 over operating range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 2.5\text{ V} \pm 10\%$, $\text{GND} = 0\text{ V}$

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
X_{TALK}	Crosstalk	$R_L = 50$, $f = 250\text{ MHz}$	-39	dB
O_{IRR}	OFF isolation	$R_L = 50$, $f = 250\text{ MHz}$	-40	dB
BW	Bandwidth (3 dB)	$R_L = 50$	1	GHz

 (1) For Maximum or Minimum conditions, use the appropriate value specified under [Electrical Characteristics](#) for the applicable device type.

6.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 10\%$

 over operating range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 3.3\text{ V} \pm 10\%$, $\text{GND} = 0\text{ V}$

PARAMETER		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pd}	Propagation delay ^{(2) (3)}		0.25		ns
t_{ON}	Line enable time	S to D, nD		30	ns
		$\overline{\text{OE}}$ to D, nD		17	
t_{OFF}	Line disable time	S to D, nD		12	ns
		$\overline{\text{OE}}$ to D, nD		10	
$t_{\text{SK(O)}}$	Output skew between center port to any other port ⁽²⁾		0.1	0.2	ns
$t_{\text{SK(P)}}$	Skew between opposite transitions of the same output ($t_{\text{PHL}} - t_{\text{PLH}}$) ⁽²⁾		0.1	0.2	ns

 (1) For Maximum or Minimum conditions, use the appropriate value specified under [Electrical Characteristics](#) for the applicable device type.

(2) Specified by design

(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Because this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 10\%$

 over operating range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 2.5\text{ V} \pm 10\%$, $\text{GND} = 0\text{ V}$

PARAMETER		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pd}	Propagation delay ^{(2) (3)}		0.25		ns
t_{ON}	Line enable time	S to D, nD		50	ns
		$\overline{\text{OE}}$ to D, nD		32	
t_{OFF}	Line disable time	S to D, nD		23	ns
		$\overline{\text{OE}}$ to D, nD		12	
$t_{\text{SK(O)}}$	Output skew between center port to any other port ⁽²⁾		0.1	0.2	ns
$t_{\text{SK(P)}}$	Skew between opposite transitions of the same output ($t_{\text{PHL}} - t_{\text{PLH}}$) ⁽²⁾		0.1	0.2	ns

 (1) For Maximum or Minimum conditions, use the appropriate value specified under [Electrical Characteristics](#) for the applicable device type.

(2) Specified by design

(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Because this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

6.10 Typical Characteristics

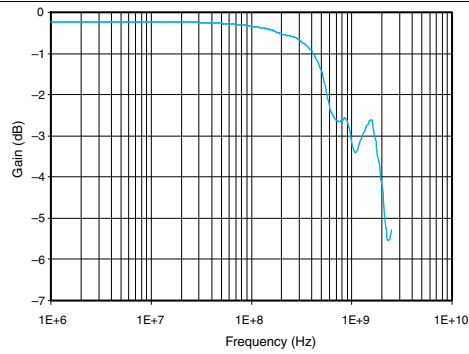


Figure 1. Gain vs Frequency

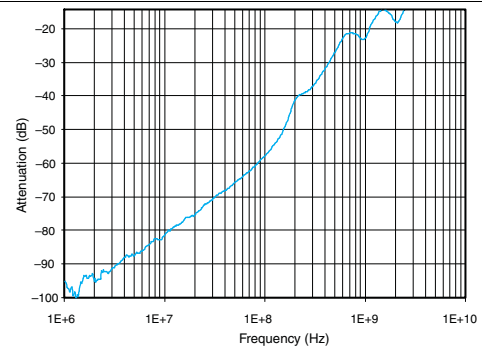


Figure 2. OFF Isolation vs Frequency

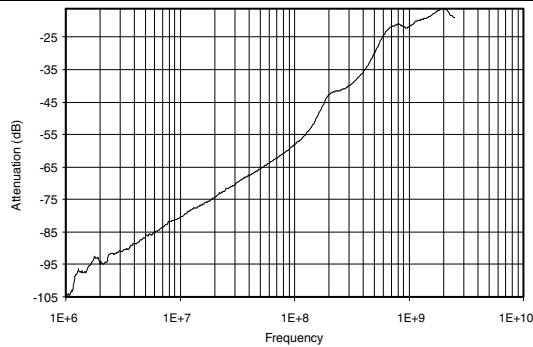


Figure 3. Crosstalk vs Frequency

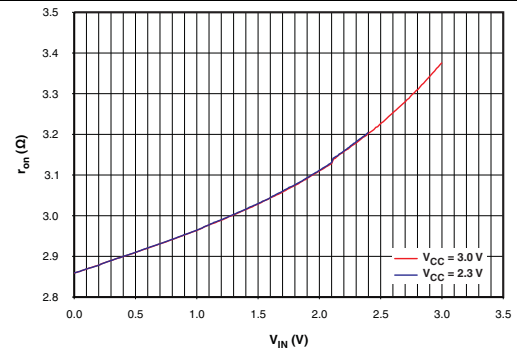


Figure 4. R_{on} vs V_{IN} ($I_{OUT} = -15$ mA)

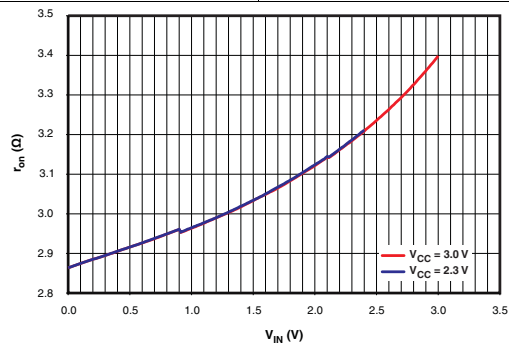
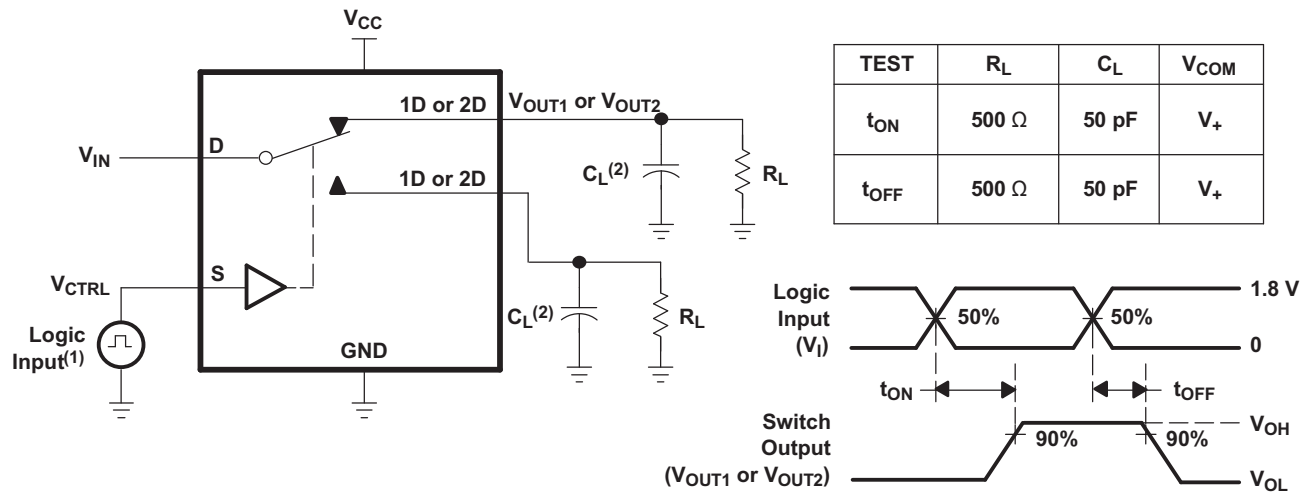


Figure 5. R_{on} vs V_{IN} ($I_{OUT} = -30$ mA)

7 Parameter Measurement Information



(1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

(2) C_L includes probe and jig capacitance.

Figure 6. Turnon (T_{ON}) and Turnoff Time (T_{OFF})

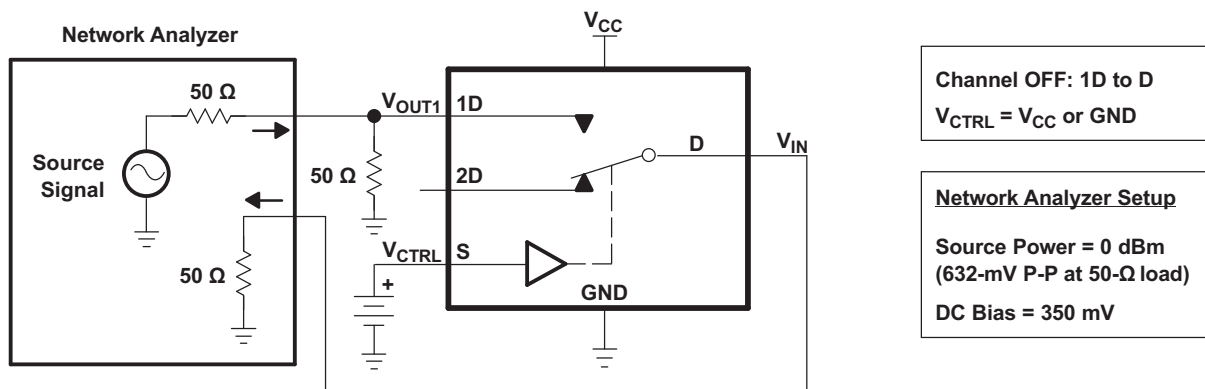


Figure 7. OFF Isolation (O_{ISO})

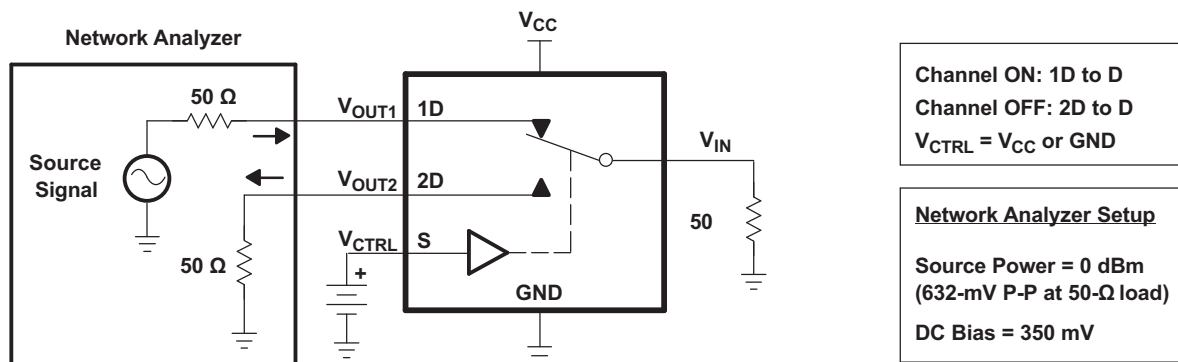


Figure 8. Crosstalk (X_{TALK})

Parameter Measurement Information (continued)

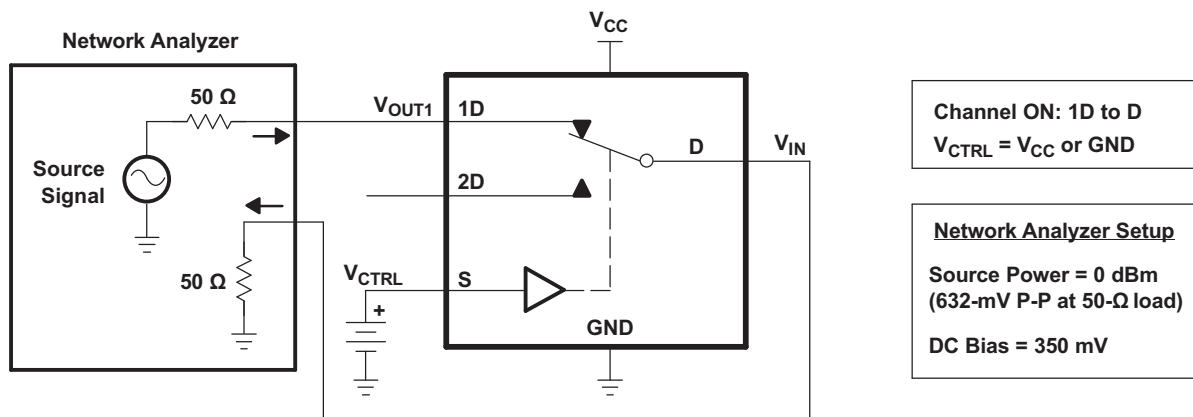


Figure 9. Bandwidth (BW)

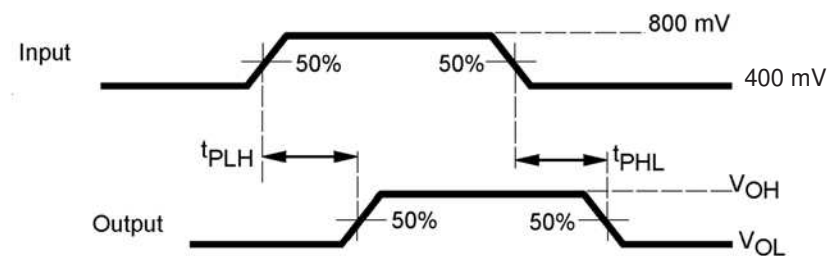
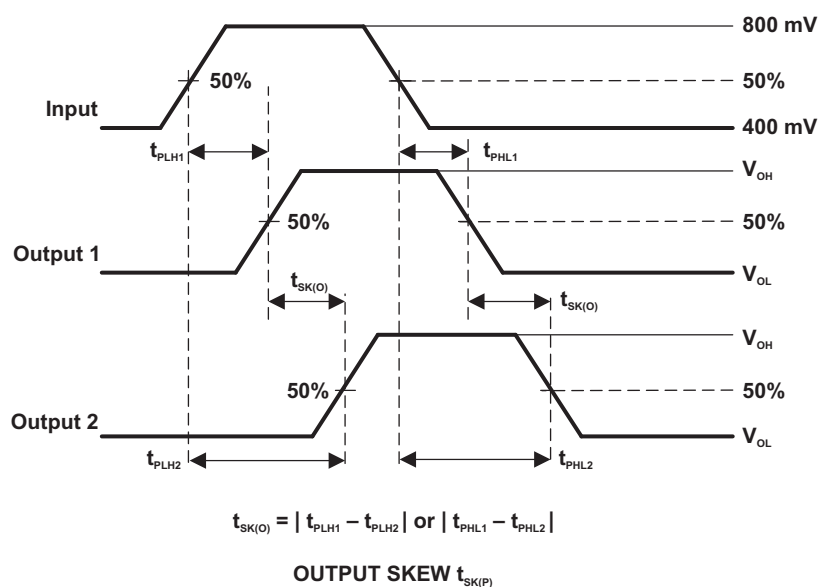
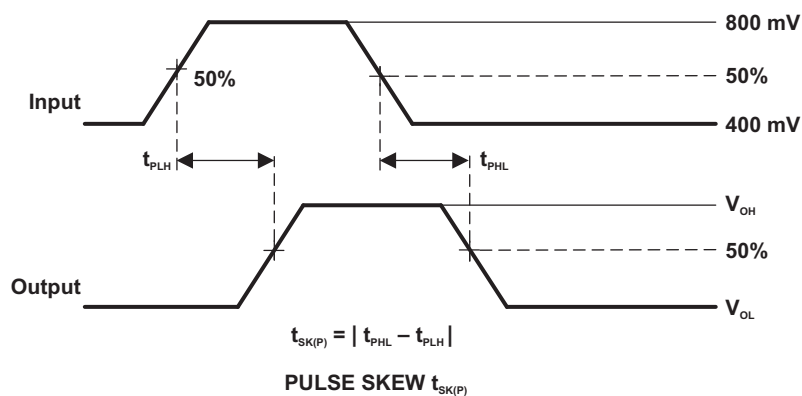
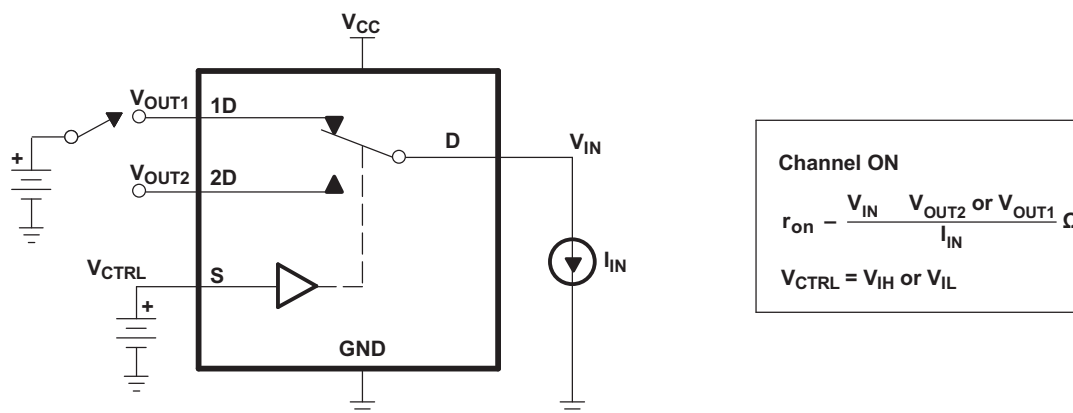


Figure 10. Propagation Delay

Parameter Measurement Information (continued)

Figure 11. Skew Test

Figure 12. ON-State Resistance (R_{on})

Parameter Measurement Information (continued)

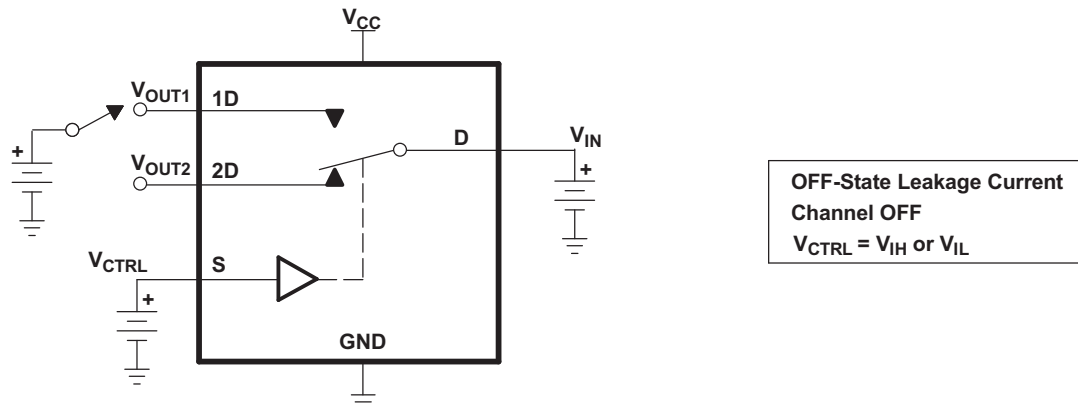


Figure 13. OFF-State Leakage Current

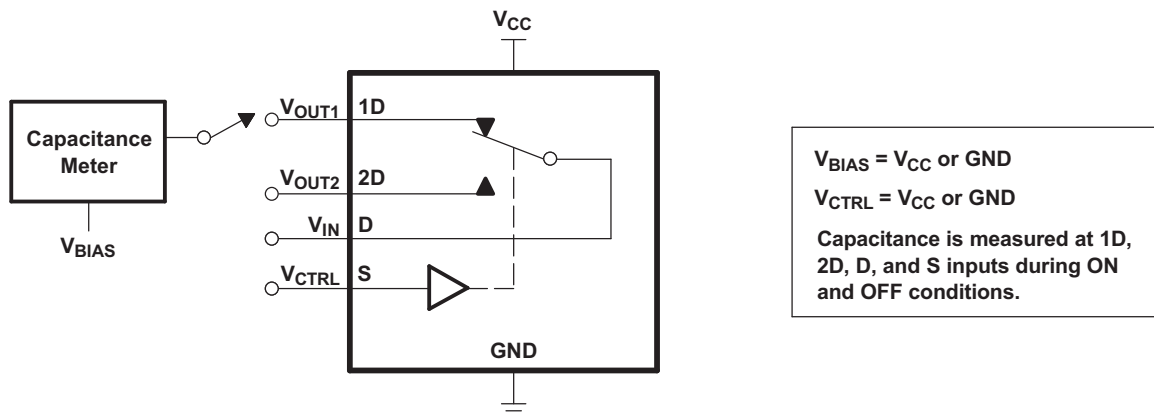


Figure 14. Capacitance

8 Detailed Description

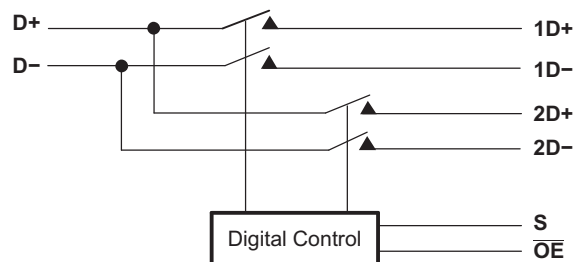
8.1 Overview

The TS3USB221E device is a 2-channel SPDT switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (1 GHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that reduces the power consumption to 1 μ A for portable applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221E device integrates ESD protection cells on all pins, is available in a tiny μ QFN package (2 mm $\times$ 1.5 mm) and is characterized over the free-air temperature range from -40°C to 85°C .

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low Power Mode

The TS3USB221E has a low power mode that reduces the power consumption to 1 μ A when the device is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{\text{OE}}$ must be supplied with a logic high signal.

8.4 Device Functional Modes

Table 1. Truth Table

S	$\overline{\text{OE}}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB221E solution can effectively expand the limited USB I/Os by switching between multiple USB buses in order to interface them to a single USB hub or controller. TS3USB221E can also be used to connect a single controller to two USB connectors.

9.2 Typical Application

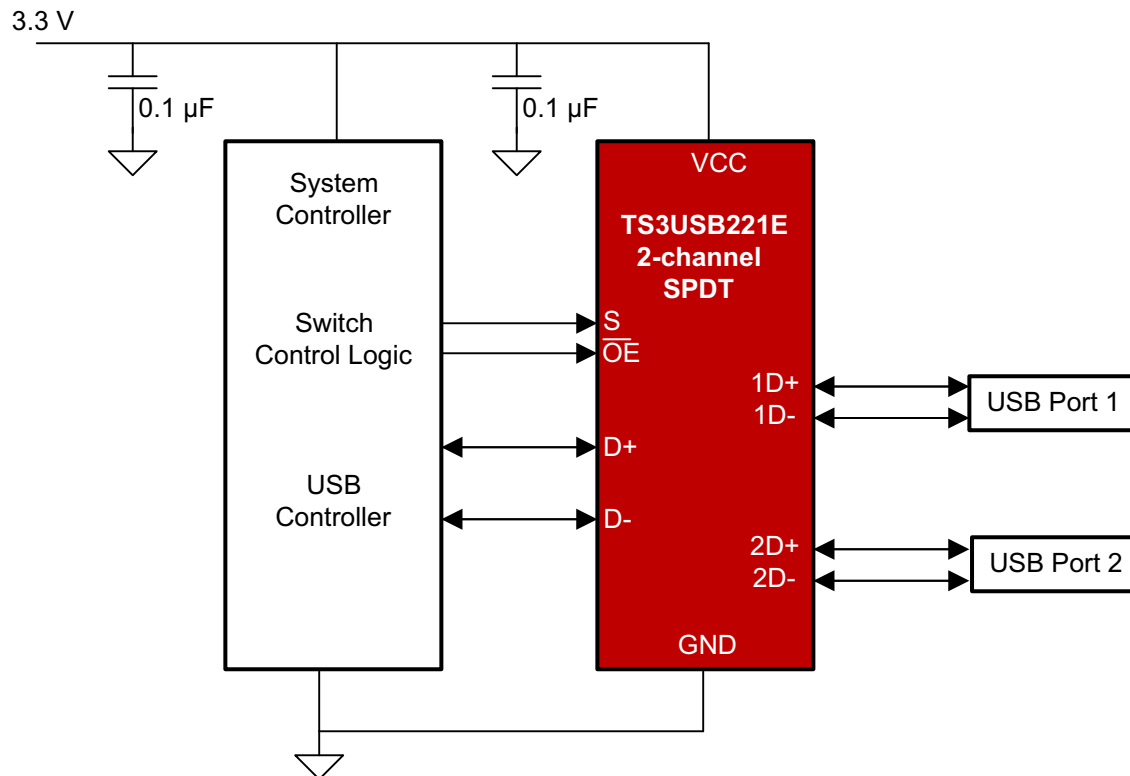


Figure 15. Simplified Schematic

9.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed.

TI recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure

The TS3USB221E can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

Typical Application (continued)

9.2.3 Application Curves

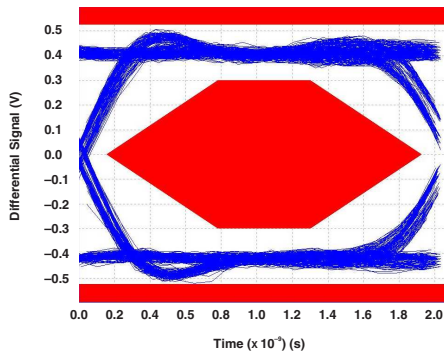


Figure 16. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

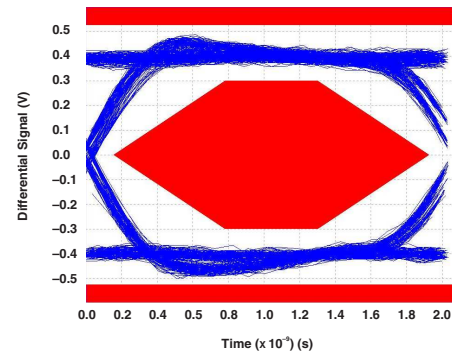


Figure 17. Eye Pattern: 480-Mbps USB Signal With Switch 1D Path

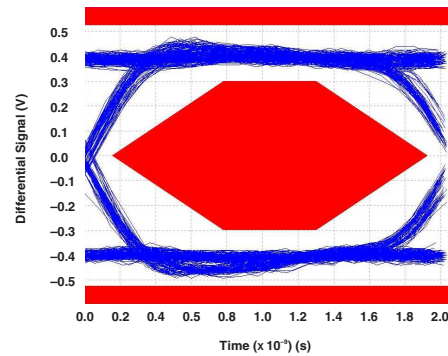


Figure 18. Eye Pattern: 480-Mbps USB Signal With Switch 2D Path

10 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin and should follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the D+/D– traces.

The high speed D+/D– traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (V_{CC} or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 19.

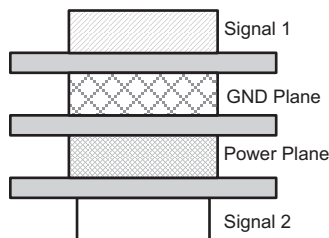


Figure 19. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082) and *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7).

11.2 Layout Example

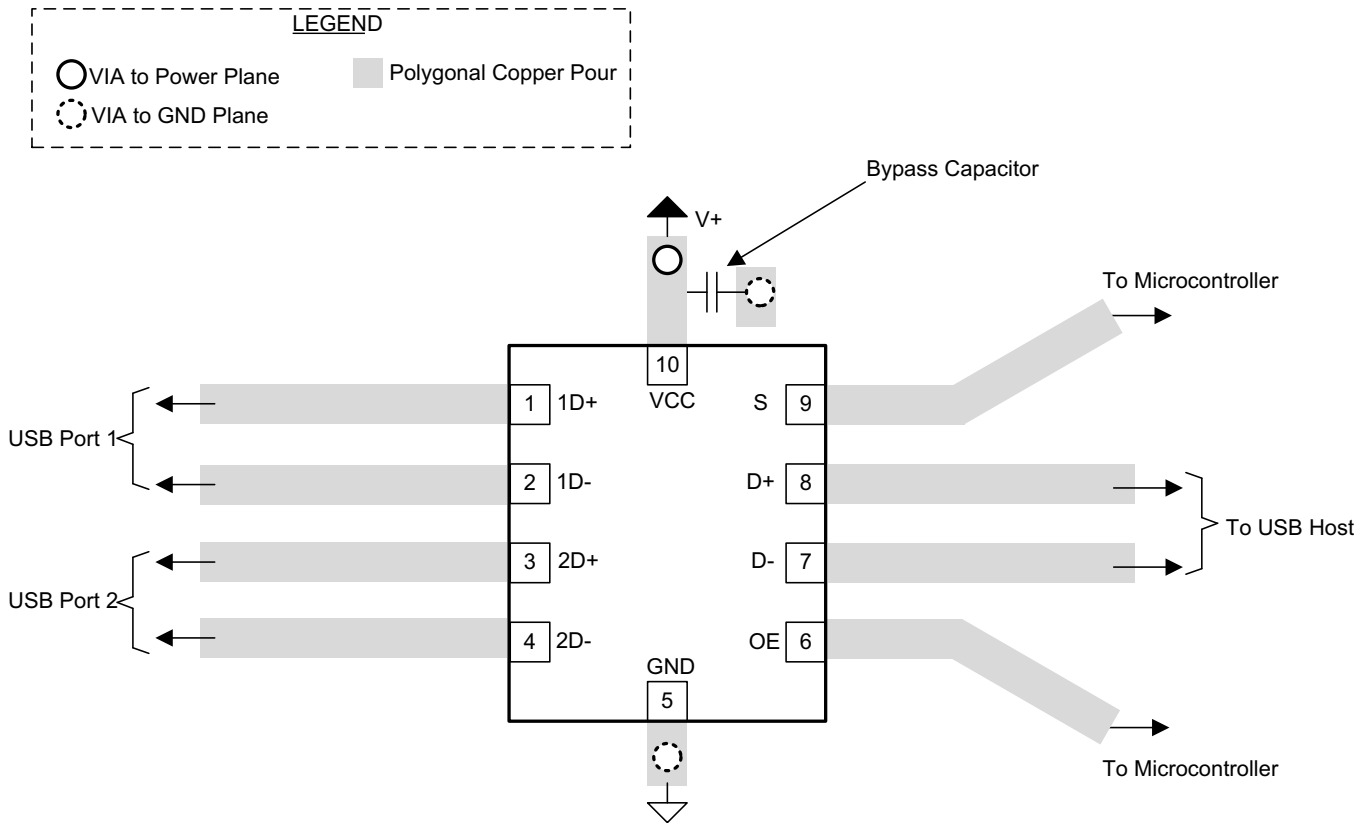


Figure 20. Package Layout Diagram

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

如需相关文档，请参阅：

- 《CMOS 输入缓慢变化或悬空的影响》，[SCBA004](#)
- 《高速布局指南》，[SCAA082](#)
- 《USB 2.0 电路板设计和布局指南》，[SPRAAR7](#)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB221EDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVM	Samples
TS3USB221ERSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(LGO, LGR, LGV)	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

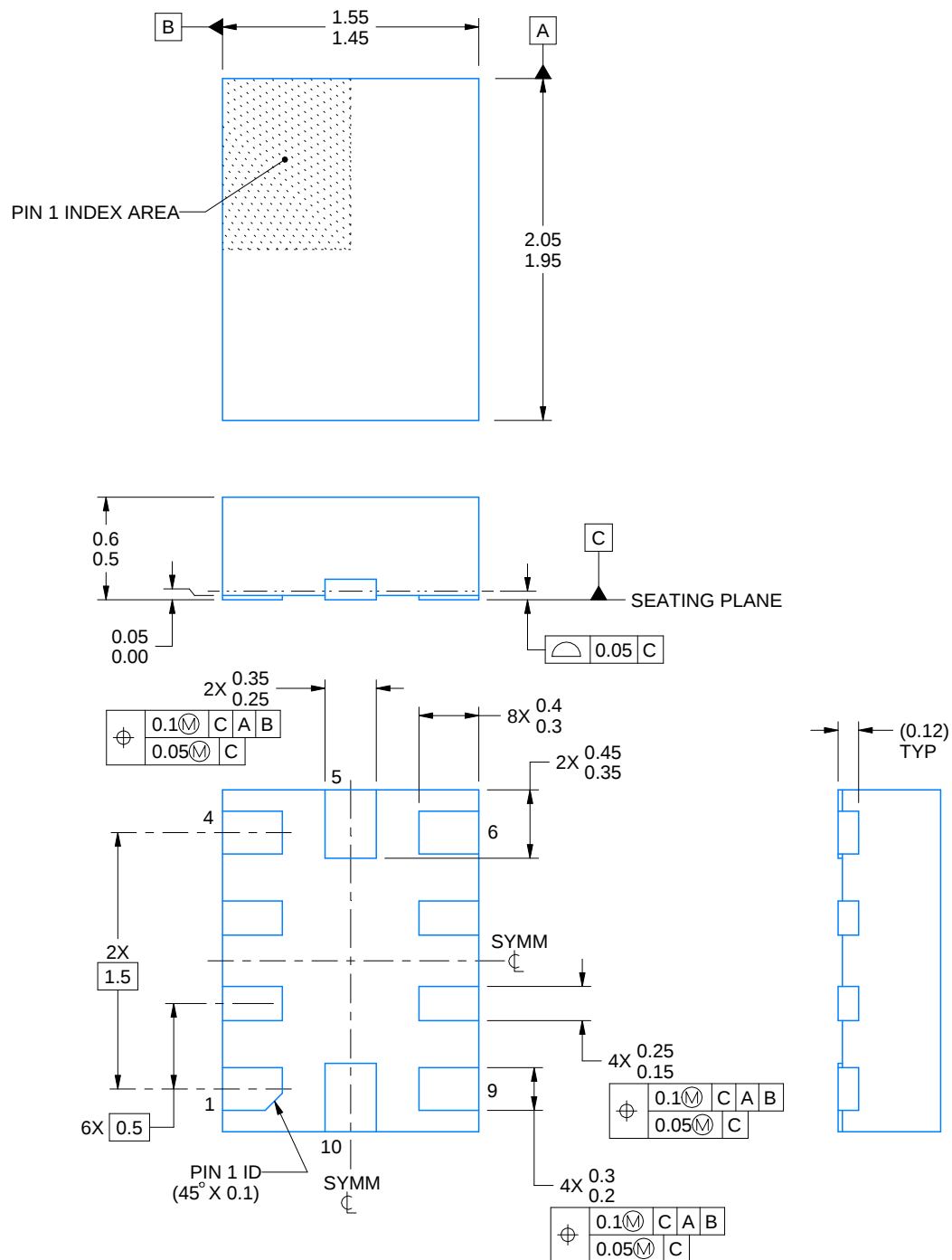
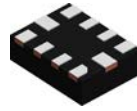
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB221EDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3USB221ERSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1
TS3USB221ERSER	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB221EDRCR	VSON	DRC	10	3000	853.0	449.0	35.0
TS3USB221ERSER	UQFN	RSE	10	3000	189.0	185.0	36.0
TS3USB221ERSER	UQFN	RSE	10	3000	202.0	201.0	28.0



4220307/A 03/2020

NOTES:

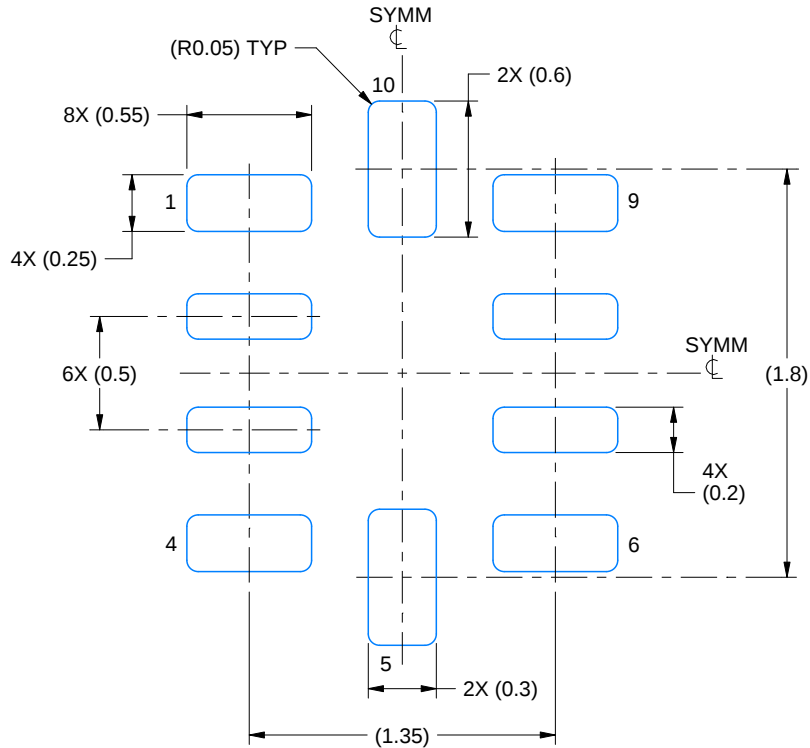
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

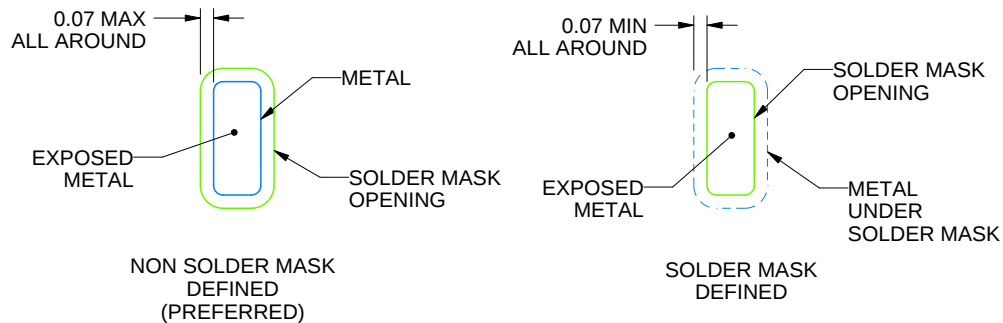
RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

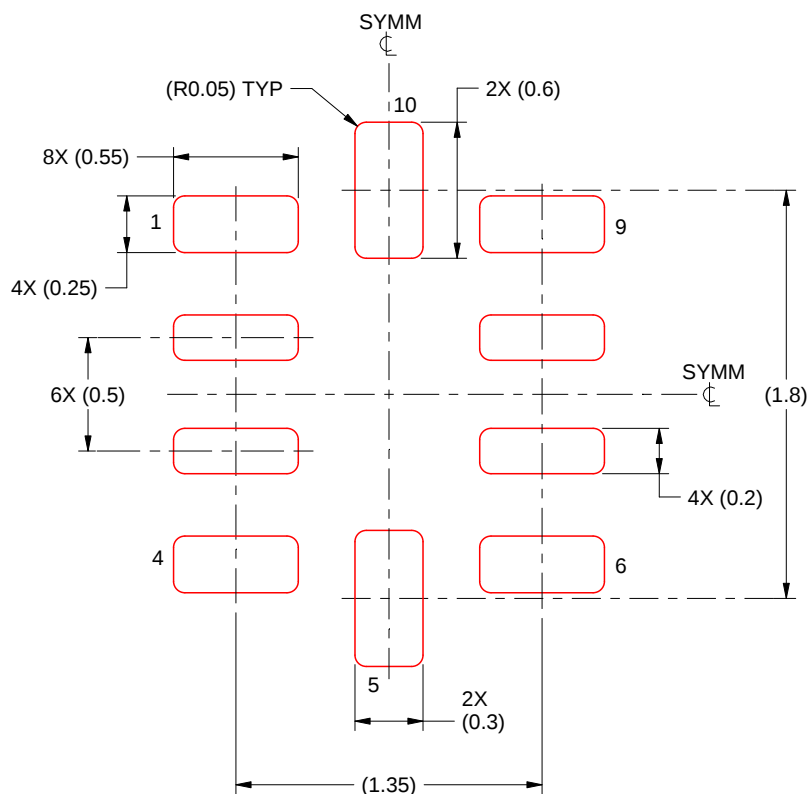
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

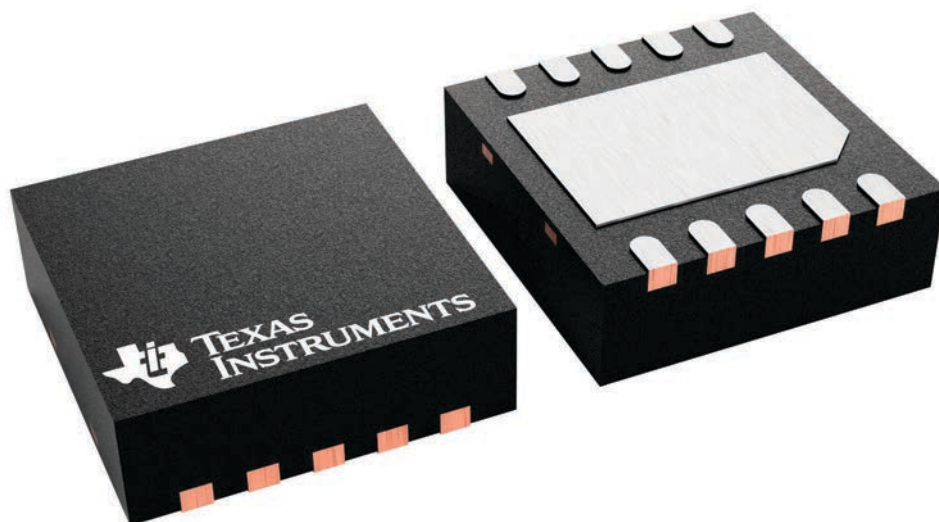
DRC 10

VSON - 1 mm max height

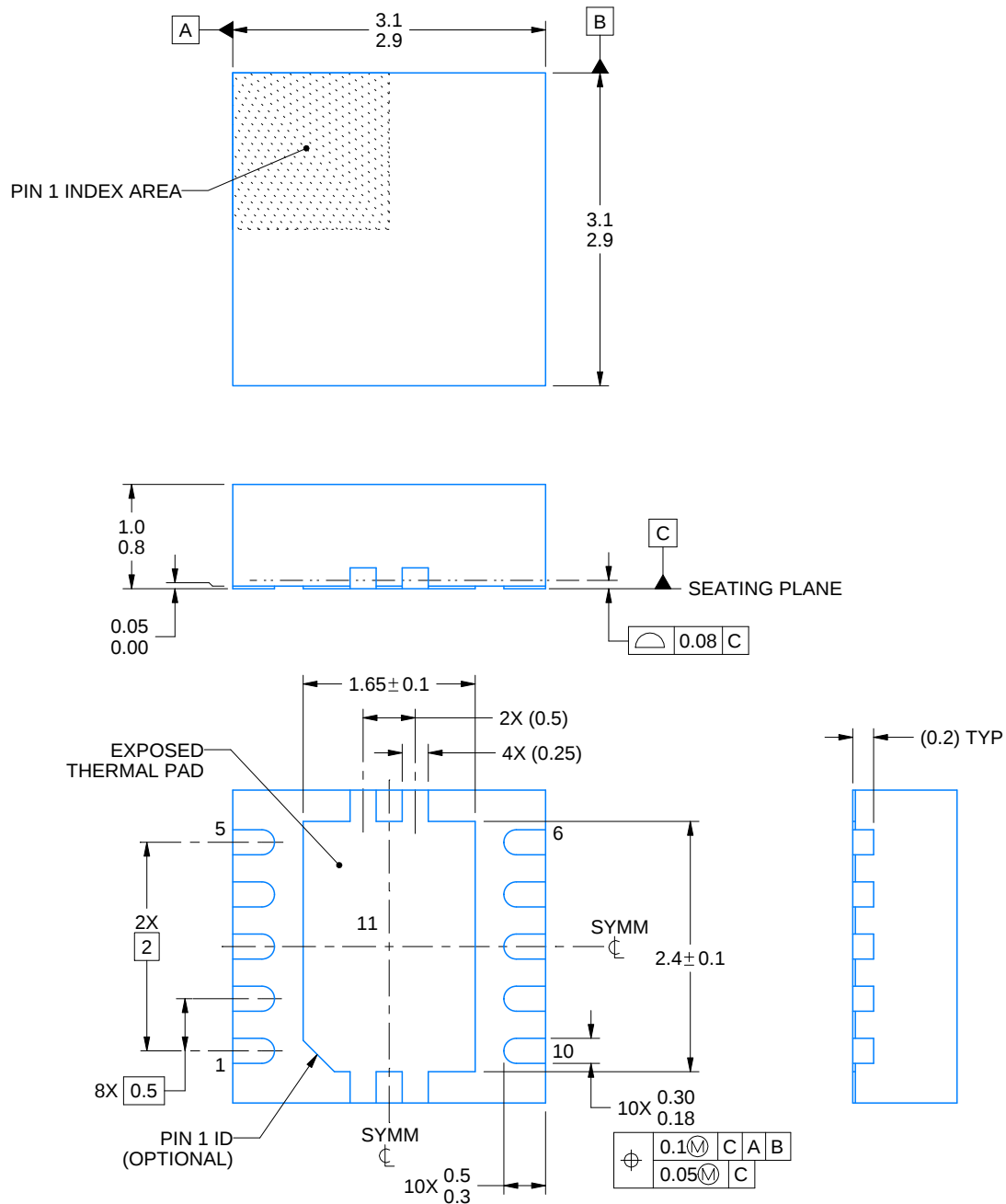
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A



4218878/B 07/2018

NOTES:

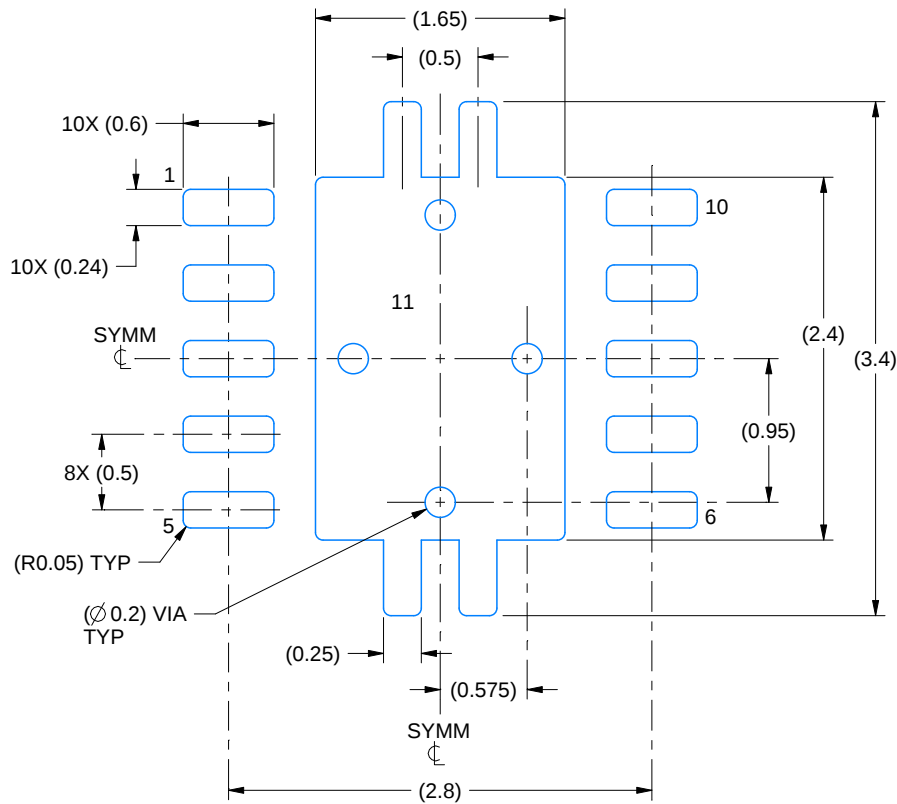
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

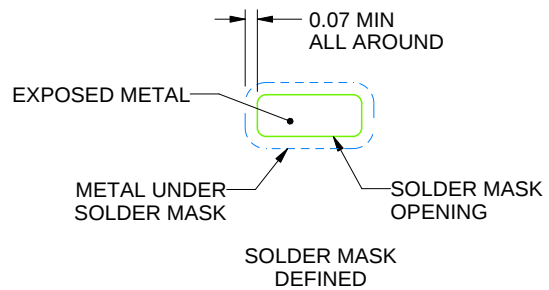
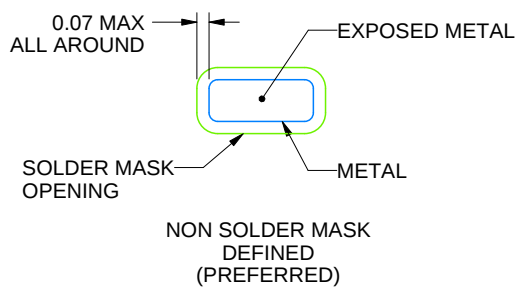
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

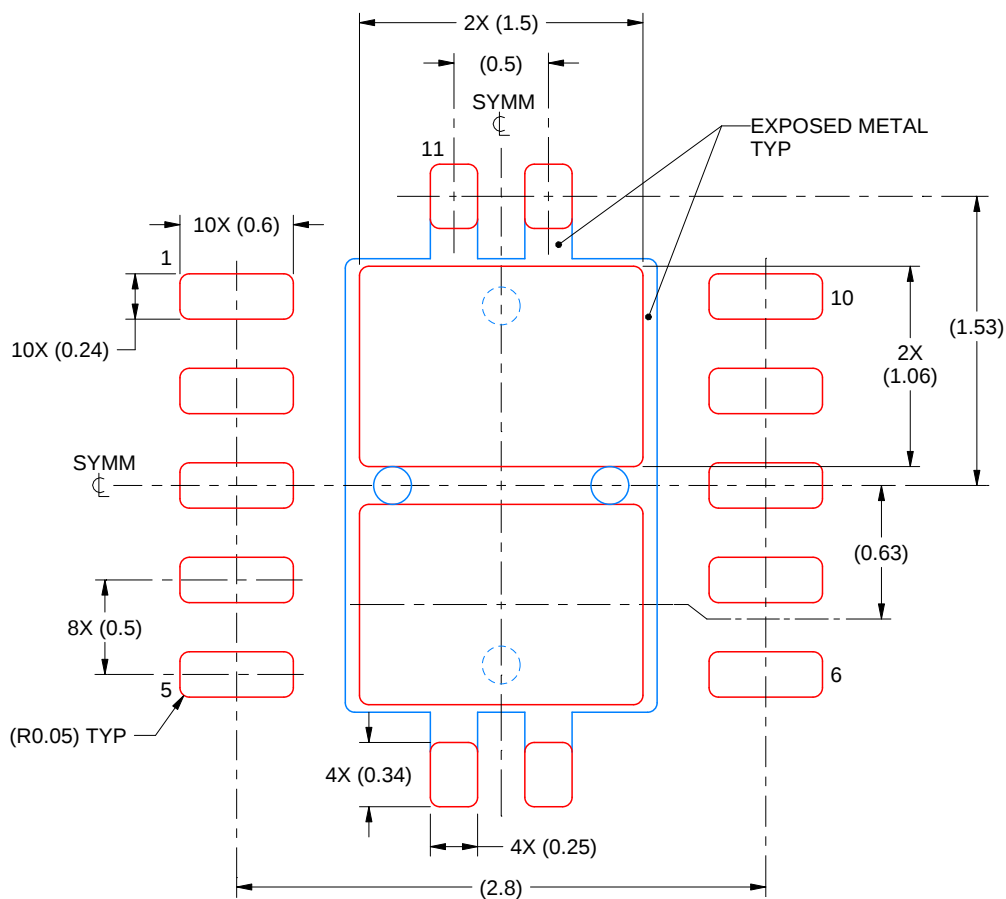
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 或 [ti.com.cn](https://www.ti.com.cn) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2021 德州仪器半导体技术（上海）有限公司