

具有 $\pm 8\text{kV}$ IEC ESD 保护功能的 THVD1520 10Mbps RS-485 收发器

1 特性

- 符合或超出 TIA/EIA-485A 标准要求
- 4.5V 至 5.5V 电源电压
- 10Mbps 半双工 RS-422/RS-485
- 总线 I/O 保护
 - $\pm 16\text{kV}$ HBM ESD
 - $\pm 8\text{kV}$ IEC 61000-4-2 接触放电
 - $\pm 8\text{kV}$ IEC 61000-4-2 空气间隙放电
 - $\pm 4\text{kV}$ IEC 61000-4-4 快速瞬变脉冲
- 工业工作温度范围: -40°C 至 125°C
- 用于噪声抑制的较大接收器滞后
- 低功耗
 - 低待机电源电流: $< 1\mu\text{A}$
 - 运行期间静态电流: $< 840\mu\text{A}$
- 适用于热插拔功能的无干扰上电/断电
- 开路、短路和空闲总线失效防护
- 1/8 单位负载 (多达 256 个总线节点)

2 应用

- 工厂自动化和控制
- 楼宇自动化
- HVAC 系统
- 视频监控
- 智能仪表

3 说明

THVD1520 是适用于工业应用的强大半双工 RS-485 收发器。这些总线引脚可耐受高级别的 IEC 接触放电 ESD 事件, 因此无需使用其他系统级保护组件。

该器件由 5V 单电源供电。总线引脚具备宽共模电压范围和低输入泄漏, 因此 THVD1520 适用于长电缆上的多点应用。

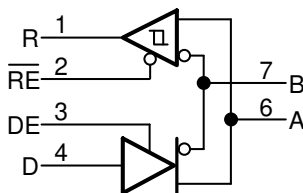
THVD1520 采用可实现快插兼容性的业界通用 8 引脚 SOIC 封装。该器件的额定温度范围为 -40°C 至 125°C 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
THVD1520	SOIC (8)	4.90mm $\times$ 3.91mm

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

简化原理图



目录

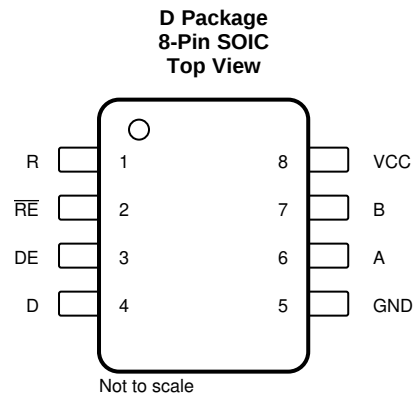
1	特性	1	8.3	Feature Description	11
2	应用	1	8.4	Device Functional Modes	11
3	说明	1	9	Application and Implementation	13
4	修订历史记录	2	9.1	Application Information	13
5	Pin Configuration and Functions	3	9.2	Typical Application	13
6	Specifications	4	10	Power Supply Recommendations	18
6.1	Absolute Maximum Ratings	4	11	Layout	19
6.2	ESD Ratings	4	11.1	Layout Guidelines	19
6.3	ESD Ratings [IEC]	4	11.2	Layout Example	19
6.4	Recommended Operating Conditions	5	12	器件和文档支持	20
6.5	Thermal Information	5	12.1	器件支持	20
6.6	Electrical Characteristics	6	12.2	第三方产品免责声明	20
6.7	Power Dissipation Characteristics	7	12.3	接收文档更新通知	20
6.8	Switching Characteristics	7	12.4	社区资源	20
6.9	Typical Characteristics	8	12.5	商标	20
7	Parameter Measurement Information	9	12.6	静电放电警告	20
8	Detailed Description	11	12.7	Glossary	20
8.1	Overview	11	13	机械、封装和可订购信息	20
8.2	Functional Block Diagrams	11			

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 10 月	*	初始发行版。

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low (internal 5-M Ω pull-up)
DE	3	Digital input	Driver enable, active high (internal 5-M Ω pull-down)
D	4	Digital input	Driver data input (internal 5-M Ω pull-up)
GND	5	Ground	Device ground
A	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	Bus input/output	Bus I/O port, B (complementary to A)
V _{CC}	8	Power	5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	−0.5	7	V
V _L	Input voltage at any logic pin (D, DE or $\overline{RE}$)	−0.3	5.7	V
V _A , V _B	Voltage at A or B inputs, as differential or common-mode with respect to GND	−18	18	V
I _O	Receiver output current	−24	24	mA
T _J	Junction temperature		170	°C
T _{STG}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Bus terminals and GND	±16,000
			All other pins	±4,000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1,500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND	±8,000	V
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND	±8,000	
		IEC 61000-4-4 EFT (Fast transient or burst), bus terminals and GND	±4,000	

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{ID}	Differential input voltage	–12		12	V
V_I	Input voltage at any bus terminal ⁽¹⁾	–7		12	V
V_{IH}	High-level input voltage (driver, driver-enable, and receiver-enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver-enable, and receiver-enable inputs)	0		0.8	V
I_O	Output current	Driver		60	mA
		Receiver		8	
R_L	Differential load resistance	54	60		Ω
$1/t_{UI}$	Signaling rate			10	Mbps
T_J	Junction temperature	–40		150	°C
$T_A^{(2)}$	Operating ambient temperature	–40		125	°C

- (1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
- (2) Operation is specified for internal (junction) temperatures upto 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown (TSD) circuit which disables the device when the junction temperature reaches 170°C.

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		THVD1520	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
V _{OD}	Driver differential-output voltage magnitude	V _{test} from −7 to +12 V	See 图 7	1.5	2.5	V	
		R _L = 54 Ω (RS-485), C _L = 50 pF	See 图 8	1.5	2.5		
		R _L = 100 Ω (RS-422), C _L = 50 pF		2	3		
Δ V _{OD}	Change in magnitude of driver differential-output voltage	R _L = 54 Ω or 100 Ω, C _L = 50 pF	See 图 8	−50		50	mV
V _{OC(SS)}	Steady-state common-mode output voltage	R _L = 54 Ω or 100 Ω, C _L = 50 pF	See 图 8	1	V _{CC} / 2	3	V
ΔV _{OC}	Change in differential driver common-mode output voltage			−50		50	mV
V _{OC(PP)}	Peak-to-peak driver common-mode output voltage				220		mV
I _{OS}	Driver short-circuit output current	DE = V _{CC} , -7 V ≤ [V _A or V _B] ≤ 12 V, or A pin shorted to B pin				150	mA
C _{OD}	Differential output capacitance				8		pF
Receiver							
I _I	Bus input current (driver disabled)	DE = 0 V, V _{CC} = 0 V or 5.5 V	V _I = 12 V		75	110	μA
			V _I = −7 V	−90	−70		
R _A , R _B	Bus input impedance	V _A = -7 V, V _B = 12 V and V _A = 12 V, V _B = -7 V	See 图 12	96			kΩ
V _{IT+}	Positive-going receiver differential-input voltage threshold				−90	−50	mV
V _{IT−}	Negative-going receiver differential-input voltage threshold				−200	−150	mV
V _{HYS} ⁽¹⁾	Receiver differential-input voltage threshold hysteresis (V _{IT+} − V _{IT−})				40	60	mV
V _{OH}	Receiver high-level output voltage	I _{OH} = −8 mA		4	V _{CC} − 0.3		V
V _{OL}	Receiver low-level output voltage	I _{OL} = 8 mA			0.2	0.4	V
I _{OZ}	Receiver high-impedance output current	V _O = 0 V or V _{CC} , $\overline{RE}$ = V _{CC}		−1		1	μA
I _{OSR}	Receiver output short-circuit current	$\overline{RE}$ = 0, DE = 0	See 图 13			95	mA
Logic							
I _{IN}	Input current (D, DE, $\overline{RE}$)				−2.5	2.5	μA
Supply							
I _{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V _{CC} , $\overline{RE}$ = 0, no load		600	840	μA
		Driver enabled, receiver disabled	DE = V _{CC} , $\overline{RE}$ = V _{CC} , no load		440	580	
		Driver disabled, receiver enabled	DE = 0, $\overline{RE}$ = 0, no load		530	680	
		Driver and receiver disabled	DE = 0, $\overline{RE}$ = V _{CC} , no load		0.1	1	

 (1) Under any specific conditions, V_{IT+} is specified to be at least V_{HYS} higher than V_{IT-} .

6.7 Power Dissipation Characteristics

PARAMETER			TEST CONDITIONS	VALUE	UNIT
PD	Power dissipation, driver and receiver enabled, $V_{CC} = 5.5\text{ V}$, $T_A = 125^\circ\text{C}$, 50% duty cycle square-wave signal at maximum signaling rate	Unterminated	$R_L = 300\ \Omega$, $C_L = 50\text{ pF}$	100	mW
		RS-422 load	$R_L = 100\ \Omega$, $C_L = 50\text{ pF}$	135	
		RS-485 load	$R_L = 54\ \Omega$, $C_L = 50\text{ pF}$	190	

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t _r , t _f	Driver differential output rise and fall times		See 图 9	10	17	30	ns
t _{PHL} , t _{PLH}	Driver propagation delay		See 图 9		20	35	ns
t _{SK(P)}	Driver pulse skew, t _{PHL} – t _{PLH}		See 图 9		0.8	4	ns
t _{PHZ} , t _{PLZ}	Driver disable time		See 图 10 and 图 11		25	100	ns
t _{PHZ} , t _{PLZ}	Driver enable time	Receiver enabled	See 图 10 and 图 11		25	100	ns
		Receiver disabled	See 图 10 and 图 11		1.5	3	μs
Receiver							
t _r , t _f	Receiver output rise and fall times		See 图 14		5	15	ns
t _{PHL} , t _{PLH}	Receiver propagation delay time		See 图 14		50	95	ns
t _{SK(P)}	Receiver pulse skew, t _{PHL} – t _{PLH}		See 图 14		3	15	ns
t _{PHZ} , t _{PLZ}	Receiver disable time		See 图 15		15	30	ns
t _{PZL(1)} , t _{PZH(1)} t _{PZL(2)} , t _{PZH(2)}	Receiver enable time	Driver enabled	See 图 15		25	170	ns
		Driver disabled	See 图 16		1	5	μs

6.9 Typical Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

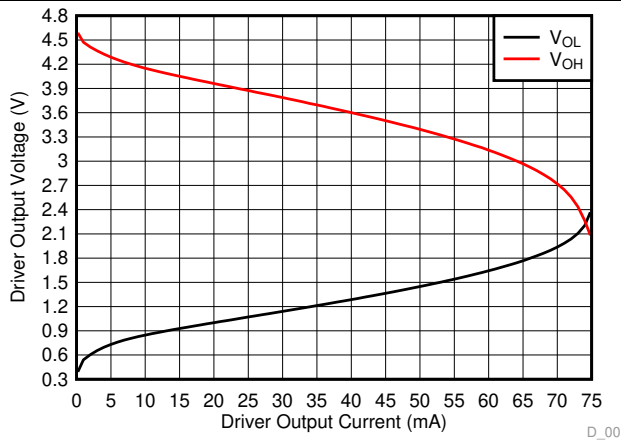


图 1. Driver Output Voltage vs Driver Output Current

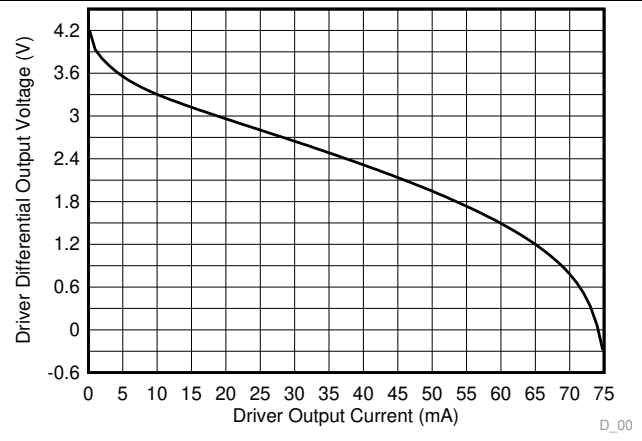


图 2. Driver Differential Output Voltage vs Driver Output Current

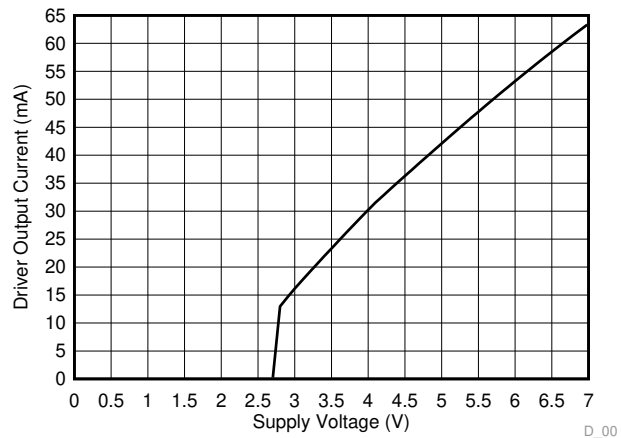


图 3. Driver Output Current vs Supply Voltage

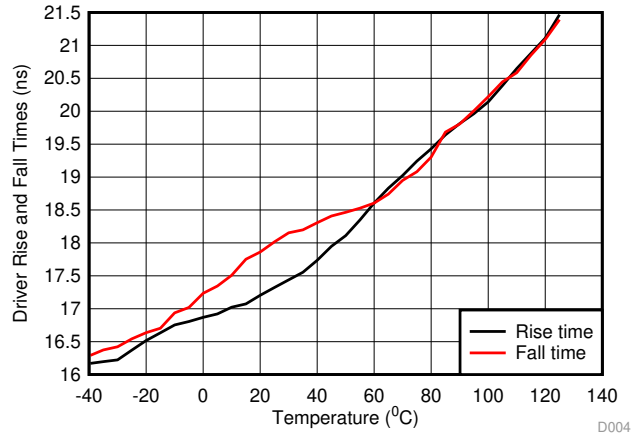


图 4. Driver Rise or Fall Time vs Temperature

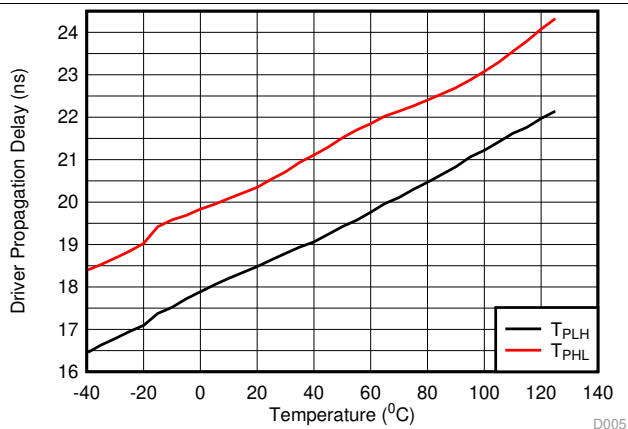


图 5. Driver Propagation Delay vs Temperature

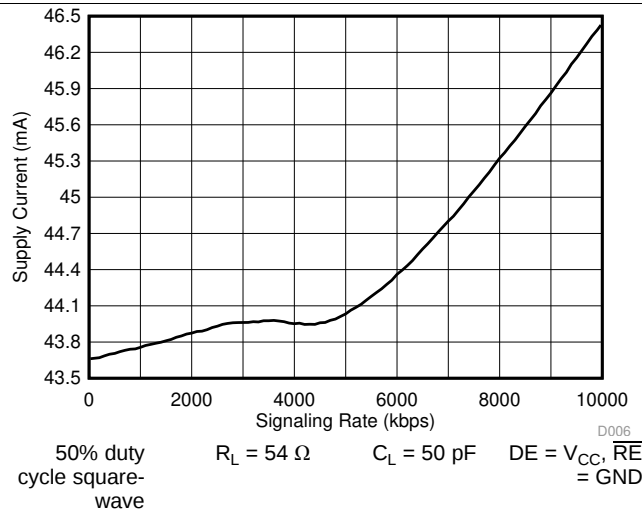


图 6. Supply Current vs Signaling Rate

7 Parameter Measurement Information

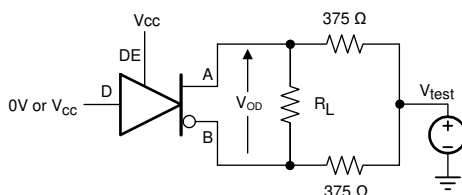


图 7. Measurement of Driver Differential Output Voltage With Common-Mode Load



图 8. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

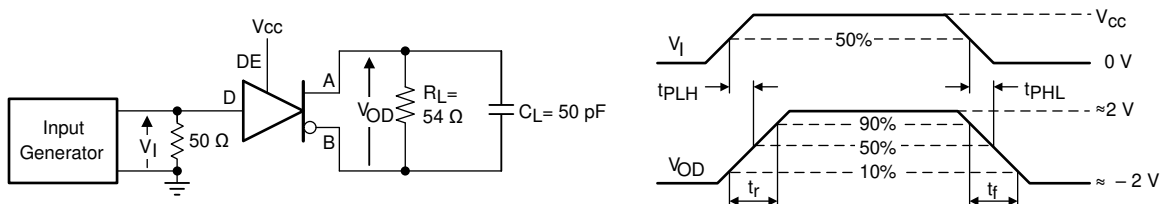


图 9. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

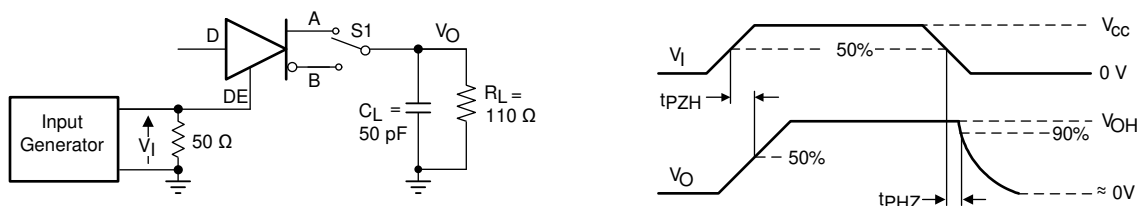


图 10. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

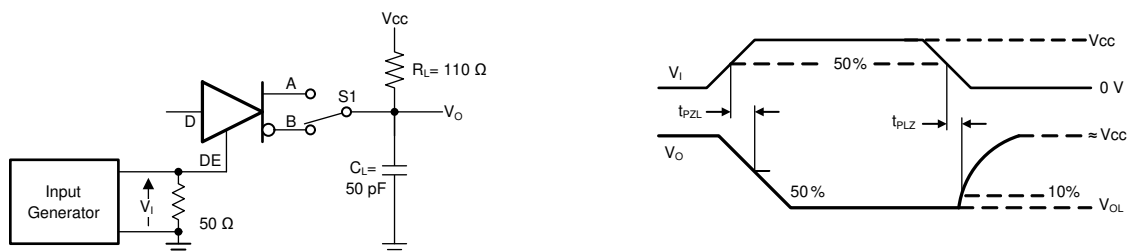


图 11. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

Parameter Measurement Information (接下页)

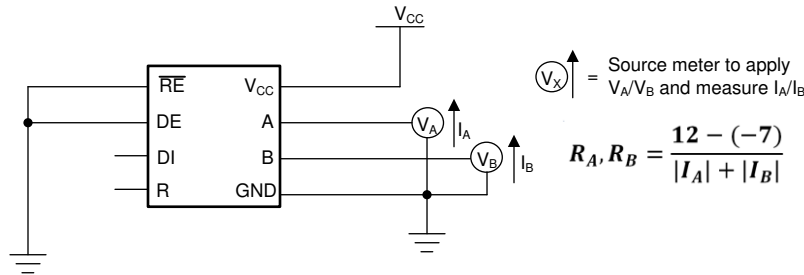


图 12. Measurement of Bus Impedance

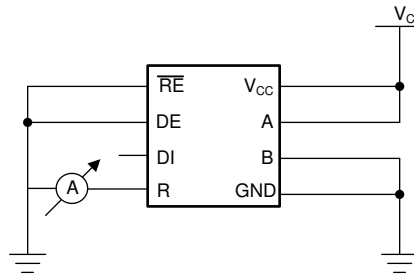


图 13. Measurement of Receiver Output Short Circuit Current

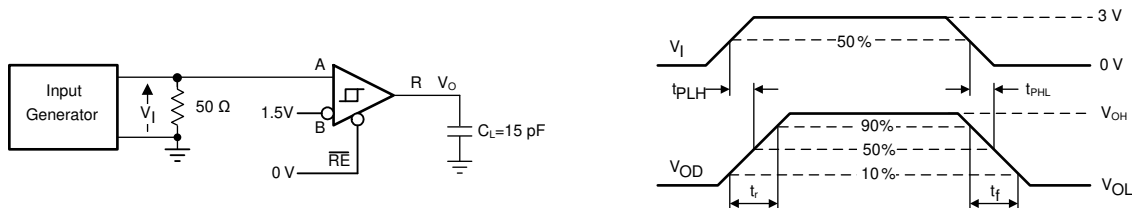


图 14. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

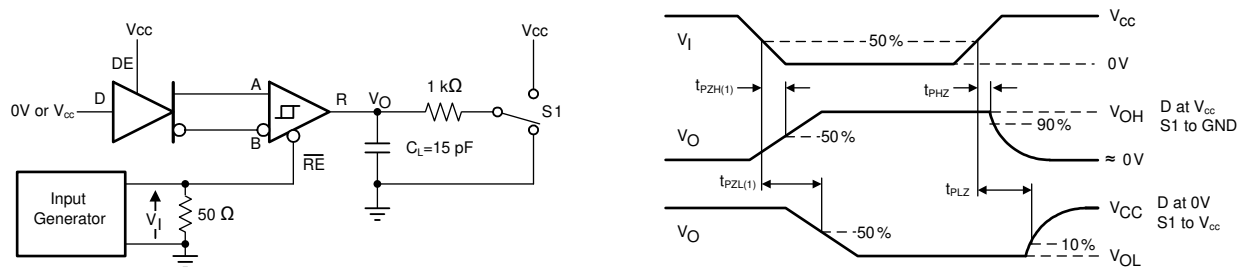


图 15. Measurement of Receiver Enable/Disable Times With Driver Enabled

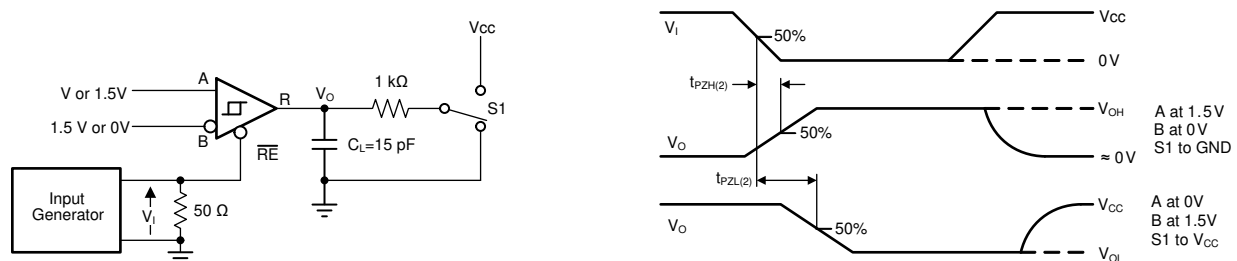


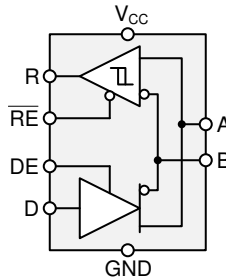
图 16. Measurement of Receiver Enable Times With Driver Disabled

8 Detailed Description

8.1 Overview

The THVD1520 is a low-power, half-duplex RS-485 transceiver suitable for data transmission up to 10 Mbps.

8.2 Functional Block Diagrams



8.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ± 8 kV (contact discharge), ± 8 kV (air gap discharge) and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ± 4 kV.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC} , thus, when left open while the driver is enabled, output A turns high and B turns low.

表 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+} , the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-} , the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} , the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The THVD1520 is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

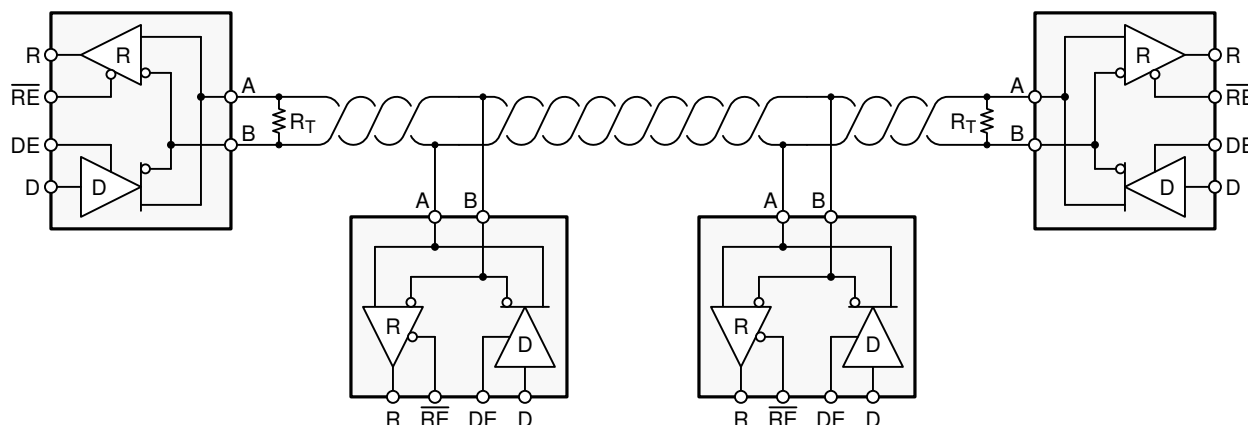


图 17. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

Typical Application (接下页)

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 公式 1.

$$L_{(\text{STUB})} \leq 0.1 \times t_r \times v \times c$$

where

- t_r is the 10/90 rise time of the driver
 - c is the speed of light (3×10^8 m/s)
 - v is the signal velocity of the cable or trace as a factor of c
- (1)

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 k Ω . Because the THVD1520 consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

9.2.1.4 Receiver Failsafe

The differential receivers of the THVD1520 are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} , V_{IT-} , and V_{HYS} (the separation between V_{IT+} and V_{IT-}). As shown in the table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{IT+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS} , as well as the value of V_{IT+} .

Typical Application (接下页)

9.2.1.5 Transient Protection

The bus pins of the THVD1520 transceiver family include on-chip ESD protection against ± 16 -kV HBM and ± 8 -kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

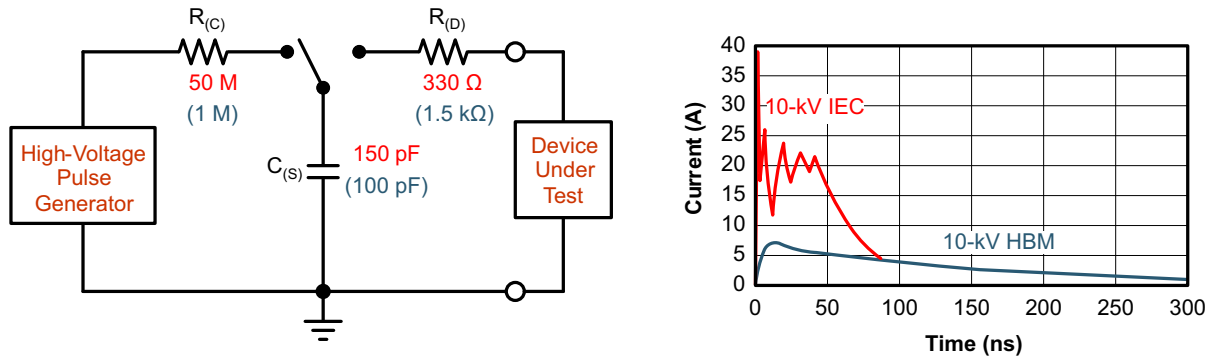


图 18. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

图 19 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

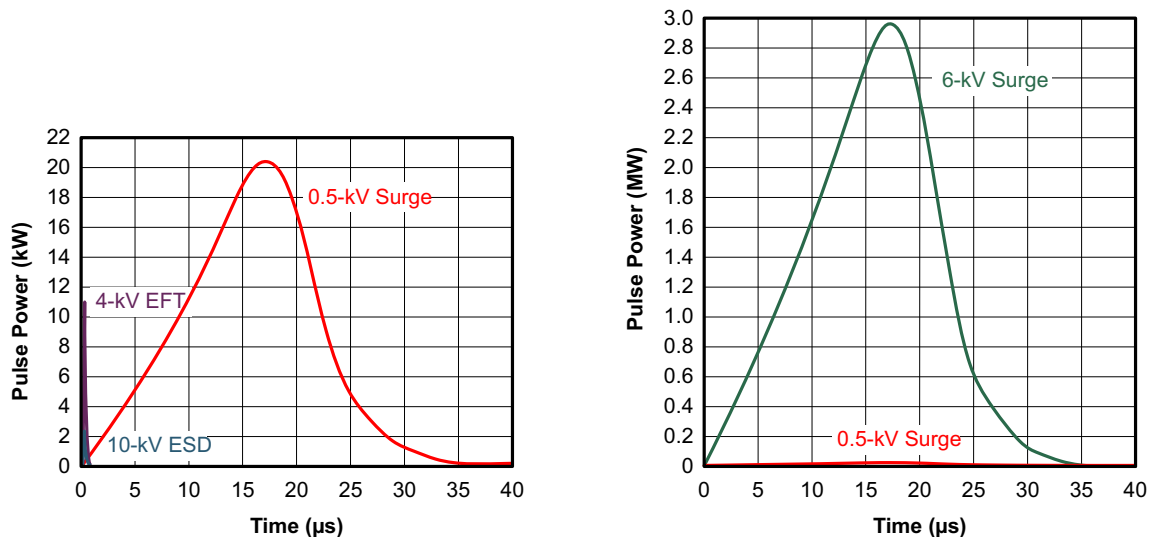


图 19. Power Comparison of ESD, EFT, and Surge Transients

Typical Application (接下页)

In the event of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 图 20 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

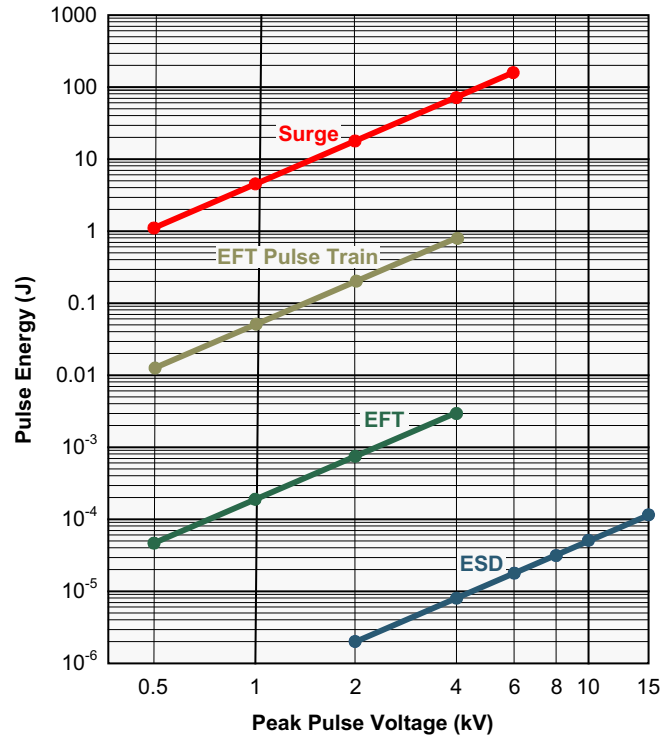


图 20. Comparison of Transient Energies

Typical Application (接下页)

9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. 图 21 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. 表 3 shows the associated bill of materials.

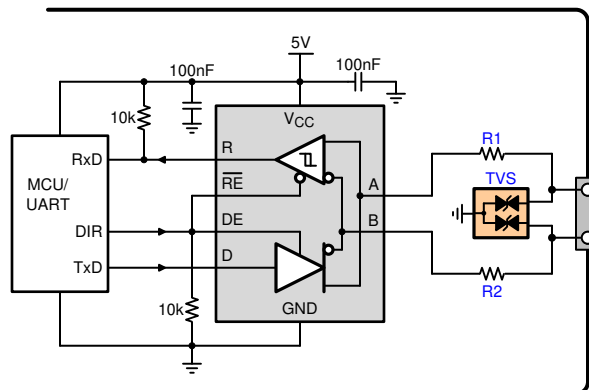


图 21. Transient Protection Against Surge Transients for Half-Duplex Devices

表 3. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 transceiver	THVD1520	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

9.2.3 Application Curves

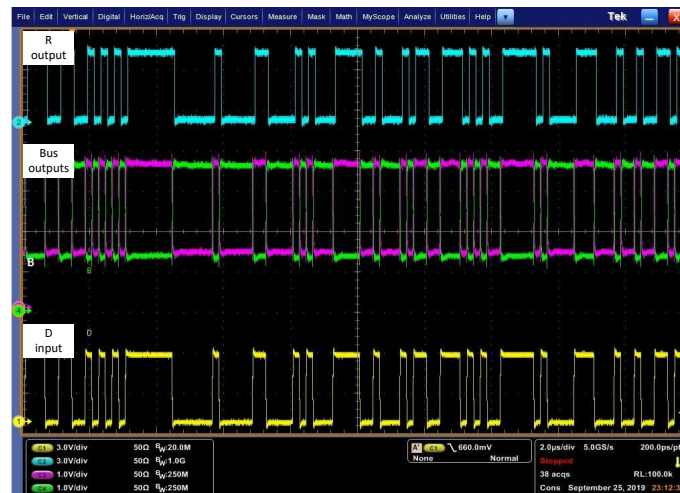


图 22. Waveforms at 10 Mbps Operation, PRBS7 Data Pattern

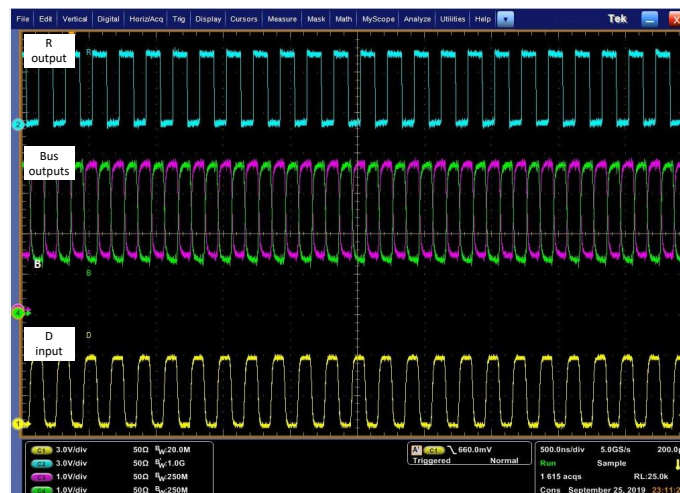


图 23. Waveforms at 10 Mbps Operation, Clock Data Pattern

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-k Ω to 10-k Ω pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example

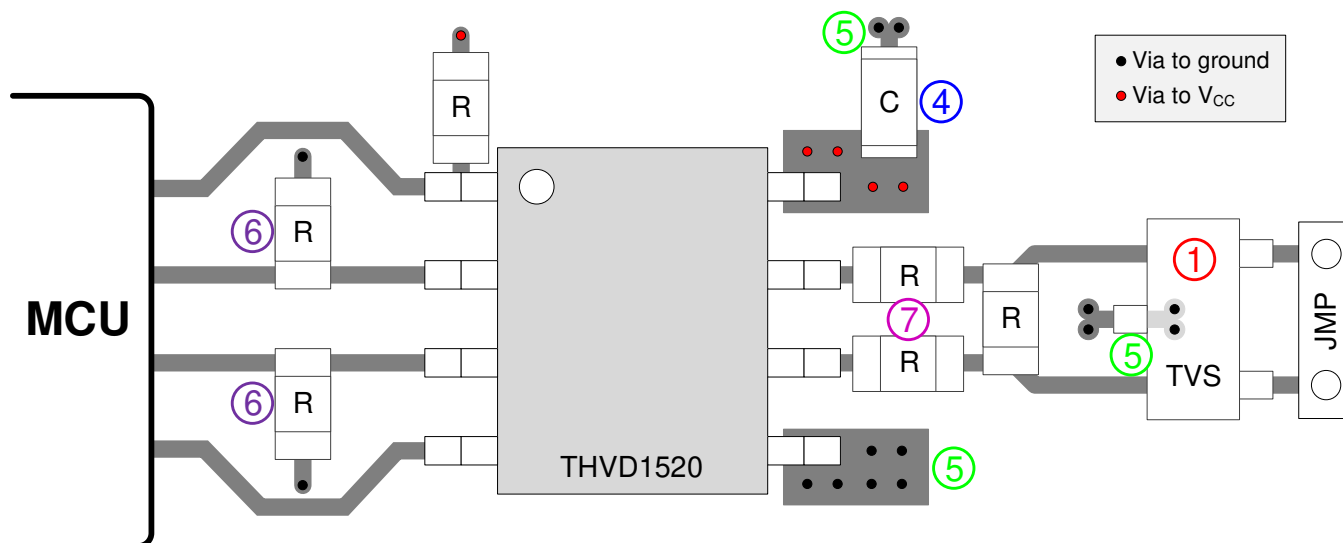


图 24. Layout Example

12 器件和文档支持

12.1 器件支持

12.2 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.5 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD1520DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1520DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1520DR	SOIC	D	8	2500	853.0	449.0	35.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司