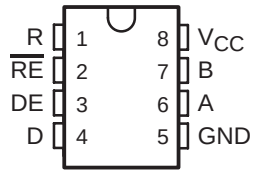
- **Qualified for Automotive Applications**
- **Bidirectional Transceiver**
- **Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **High-Speed Low-Power LinBiCMOS™ Circuitry**
- **Designed for High-Speed Operation in Both Serial and Parallel Applications**
- **Low Skew**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Very Low Disabled Supply-Current Requirements . . . 200 μA Maximum**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal-Shutdown Protection**
- **Driver Positive-and Negative-Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operate From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

D PACKAGE
(TOP VIEW)



Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A−B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description/ordering information

The SN65LBC176 differential bus transceiver is a monolithic, integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard RS-485 and ISO 8482:1987(E).

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC − D	Tape and reel	SN65LBC176QDRQ1	L176Q1

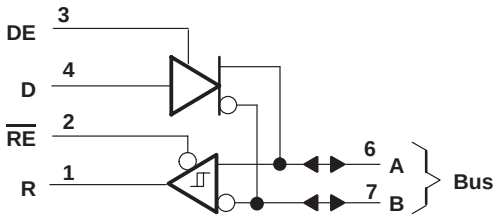
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

description (continued)

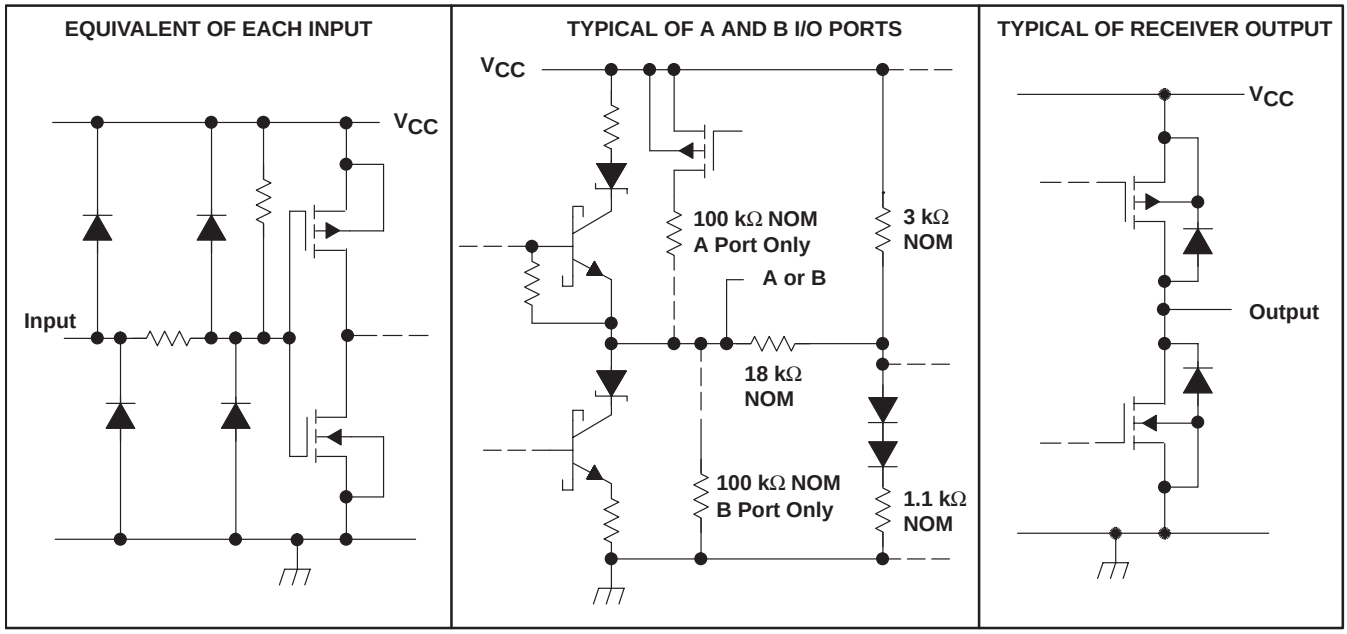
The SN65LBC176 combines a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver. Both the driver and receiver are available as cells in the Texas Instruments LinASIC™ Library.

This transceiver is suitable for ANSI Standard RS-485 and ISO 8482:1987 (E) applications to the extent that they are specified in the operating conditions and characteristics section of this data sheet. Certain limits contained in the ANSI Standard RS-485 and ISO 8482:1987 (E) are not met or cannot be tested over the entire extended temperature range.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . −10 V to 15 V
Input voltage, V_I (D, DE, R, or $\overline{RE}$) . . . . . −0.3 V to V_{CC} + 0.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A SN65LBC176Q . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65LBC176Q	−40		125	°C

NOTE 2: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0			0	6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0			1.5	6	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2,	See Note 3	1.1		V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 54 Ω,	See Figure 1,	See Note 3	1.1		V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage†	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,	See Figure 1			3	V
						−1	
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage†	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
I_O	Output current	Output disabled, See Note 4	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				−100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	µA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V					
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver disabled and driver enabled			1.75	mA
			Receiver and driver disabled			0.25	

† $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

NOTES: 3. This device meets the ANSI Standard RS-485 V_{OD} requirements above 0°C only.
4. This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		8		31	ns
$t_{t(OD)}$	Differential output transition time				12		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)					6	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4			65	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5			65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4			105	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5			105	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-485
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$	V_t (test termination measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	None
I_O	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$) (see Figure 4)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV,	I_{OL} = 8 mA,	See Figure 6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V				1	mA
			V_I = −7 V				−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					−100	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	μA
r_I	Input resistance				12			kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled				3.9	mA
			Receiver and driver disabled				0.25	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 5: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level single-ended output	V_{ID} = −1.5 V to 1.5 V, See Figure 7	11	37	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output		11	37	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)			10	ns
t_{PZH}	Output enable time to high level	See Figure 8		35	ns
t_{PZL}	Output enable time to low level			35	ns
t_{PHZ}	Output disable time from high level	See Figure 8		35	ns
t_{PLZ}	Output disable time from low level			35	ns

PARAMETER MEASUREMENT INFORMATION

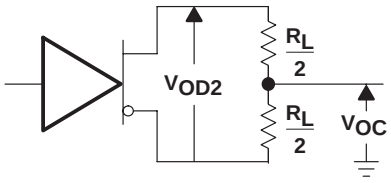


Figure 1. Driver V_{OD} and V_{OC}

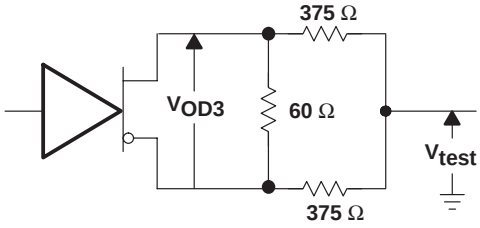


Figure 2. Driver V_{OD3}

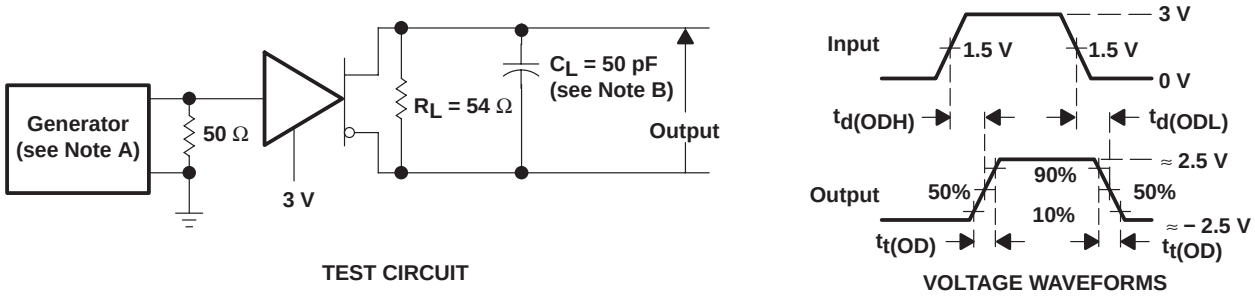


Figure 3. Driver Test Circuit and Voltage Waveforms

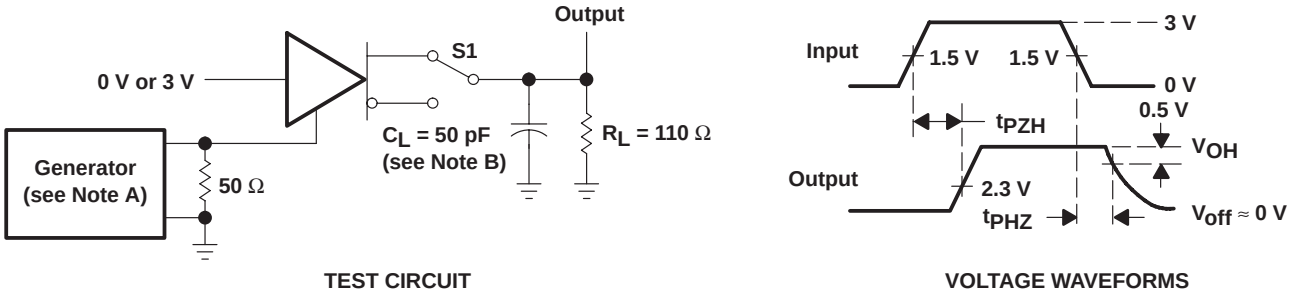


Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

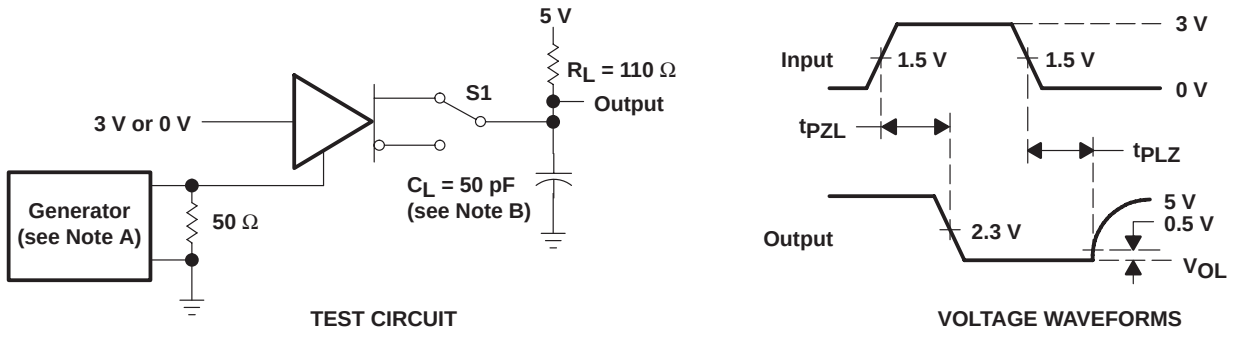


Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

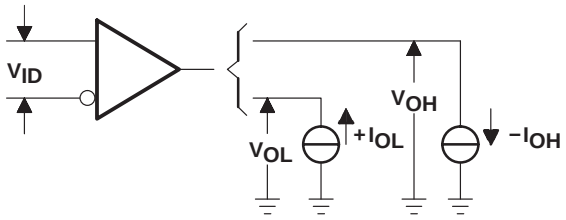
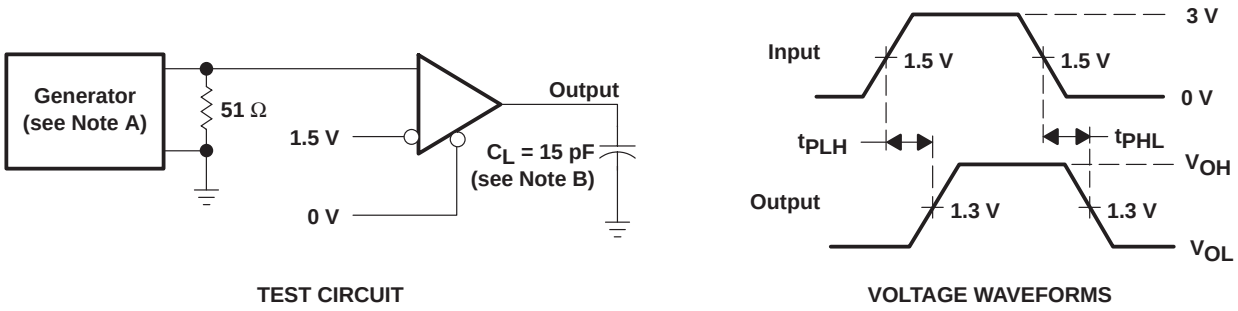


Figure 6. Receiver V_{OH} and V_{OL}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

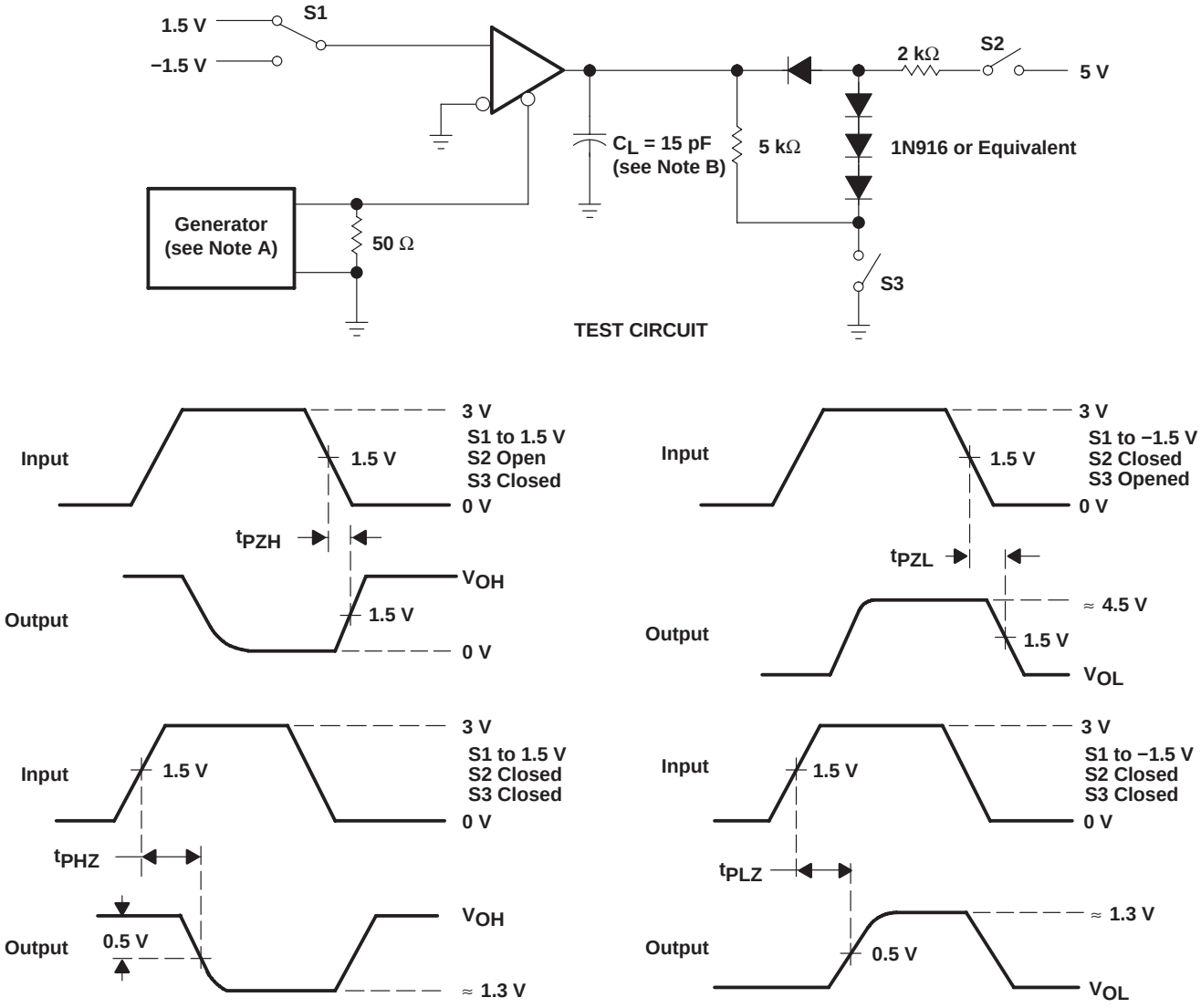


Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC176QDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J176Q1	Samples
SN65LBC176QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J176Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN65LBC176-Q1 :

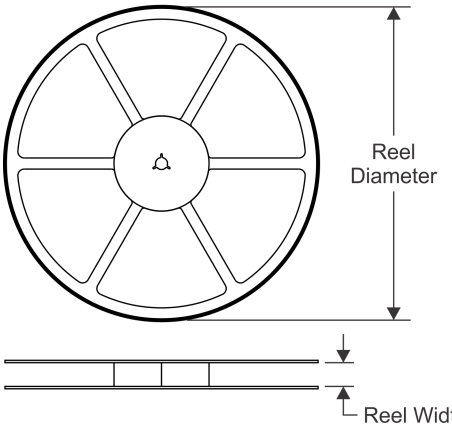
- Catalog: SN65LBC176

NOTE: Qualified Version Definitions:

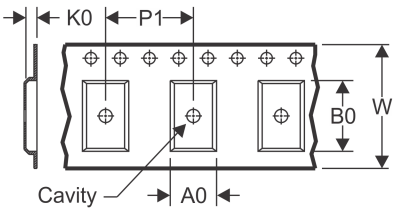
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

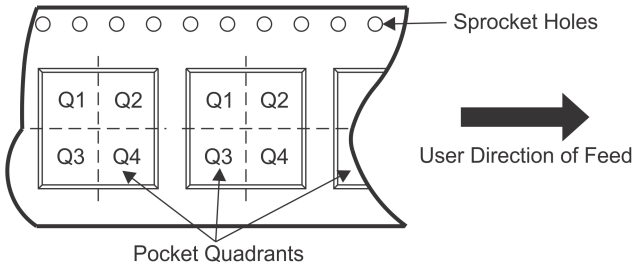


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

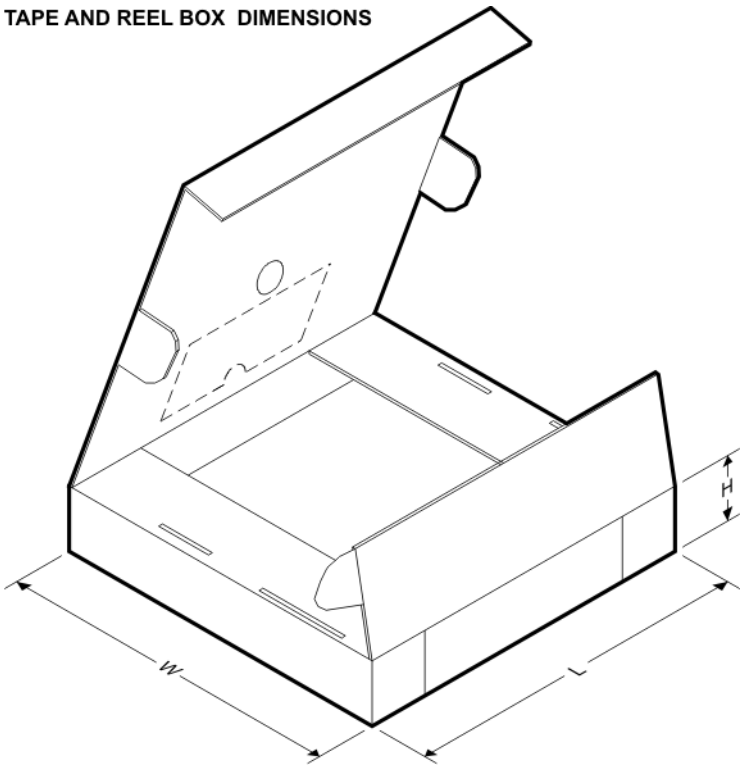
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

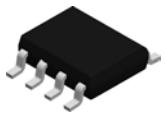
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176QDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176QDRG4Q1	SOIC	D	8	2500	340.5	338.1	20.6

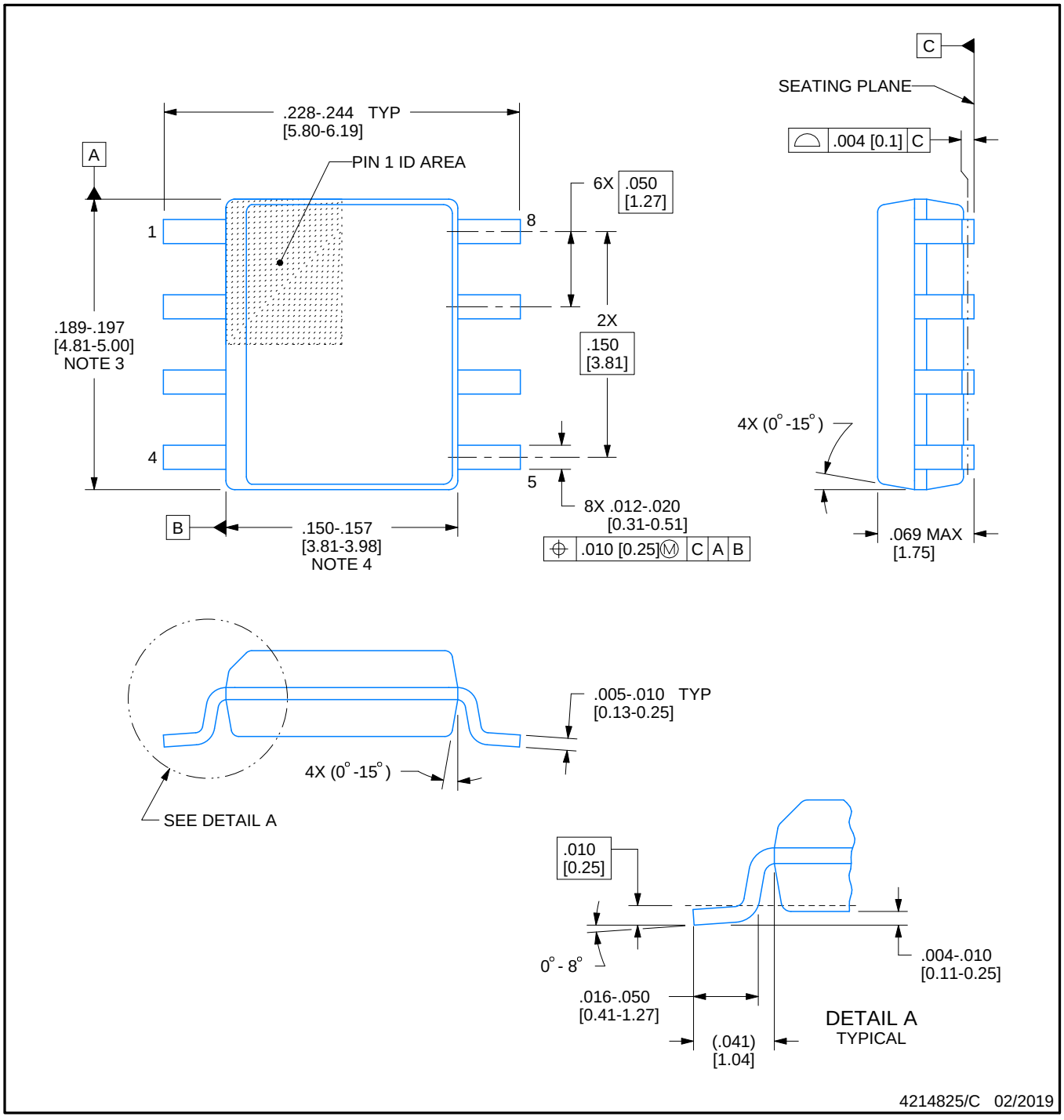


PACKAGE OUTLINE

D0008A

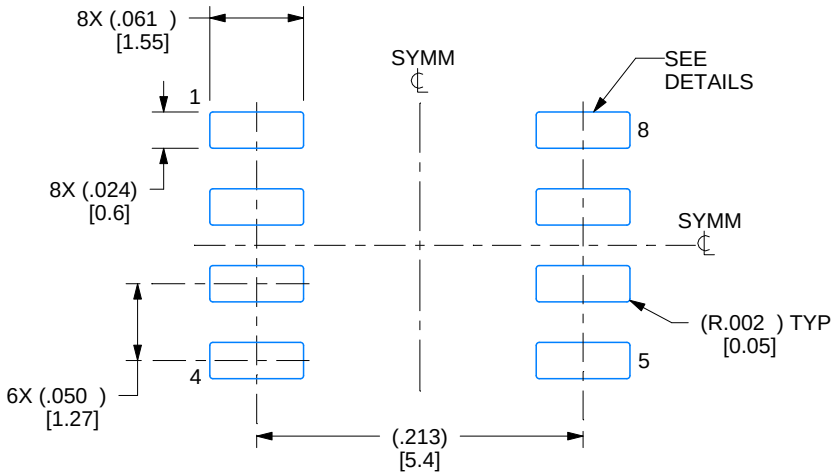
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

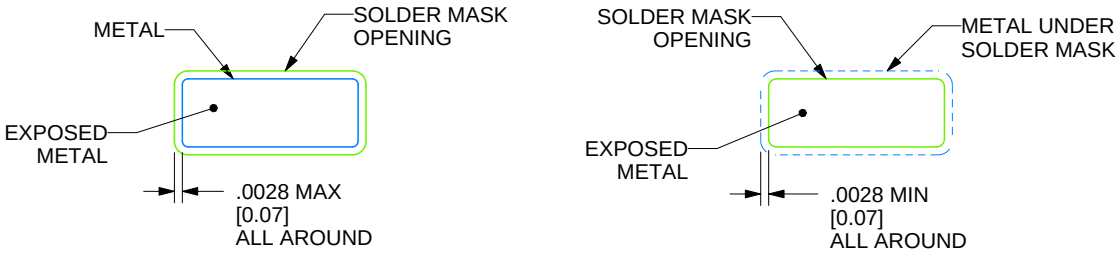


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

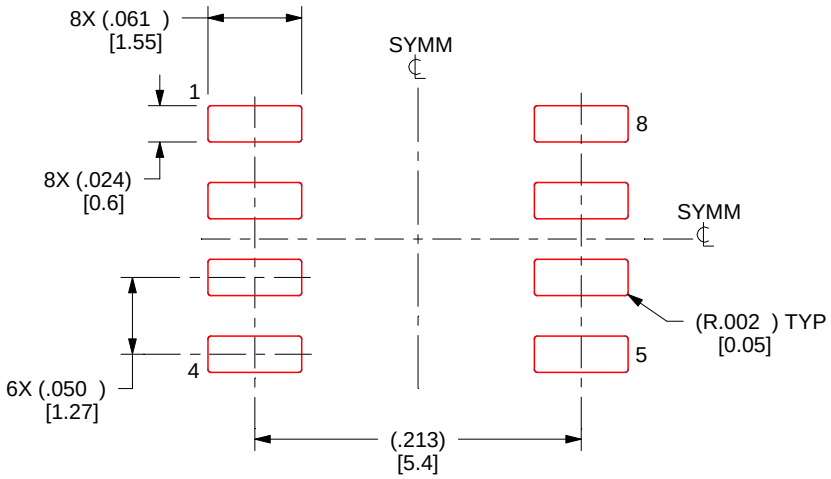
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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