9 通道 RS-422/RS-485 收发器

查询样品: **SN65HVD09-EP**

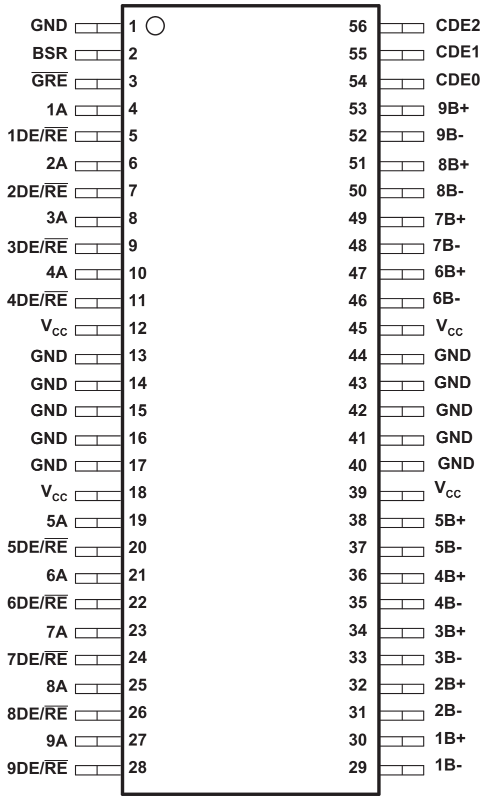
特性

- 每个 **RS-422/RS-485** 通道上的设计每秒数据传输速率高达 **2** 千万
- **SN65HVD09** 封装在引脚间距为 **0.5mm** 的薄型小外形尺寸封装内
- 超过 **12KV** 的总线引脚上的静电放电 **(ESD)** 保护
- 低失效电源电流 **8mA** （典型值）
- 具有热关断保护功能
- 正负电流限制
- 上电**/**断电毛刺脉冲保护

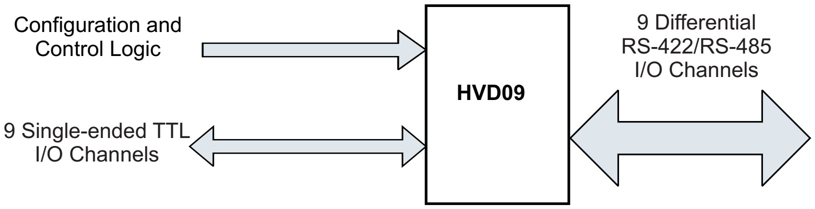
支持国防，航空航天，和医疗应用

- 可控基线
- 一个组装**/**测试场所
- 一个制造场所
- 延长的产品生命周期
- 延长产品的变更通知周期
- 产品可追溯性

SN65HVD09 DGG
(TOP VIEW)



Terminals 13 through 17, and 40 through 44 are connected together to the package lead frame and signal ground.



说明

SN65HVD09 是一款 9 通道适合于工业应用的 RS-422/RS-485 收发器。 它提供改进的开关性能，小型封装，和高静电放电 (ESD) 保护。 精确的压摆范围限制确保了传播延迟时间，不仅仅是通道到通道也包括器件到器件，

薄型小外形尺寸封装 (TSSOP) 使用了获得专利权的耐热增强技术，此技术可使器件工作在工业用温度范围内。 TSSOP 封装对主板面积要求很小，同时将封装高度减少到 1mm。 这样将提供更多的主板面积，对于小尺寸硬盘驱动等薄型并对空间要求严格的应用，允许将组件贴装在印刷电路板的两面。

English Data Sheet: SLLSEA3

使用人体模式，HVD09 能够承受超过 12kV 的静电放电，而使用 RS-485I/O 终端上的机器模式，HVD09 能够承受 600V 的静电放电。 这提供可耦合在外部线路内的噪音的保护。 此器件的另外终端可分别承受超过 4kV 和 400V 的放电。

HVD09 的 9 个半双工通道中每一个都设计运行在 RS-422 或者 RS-485 通信网络中。

SN65HVD09 额定工作温度 –40°C 至 85°C。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 85°C	TSSOP-DGG	SN65HVD09IDGGREP	SN65HVD09EP	V62/12607-01XE

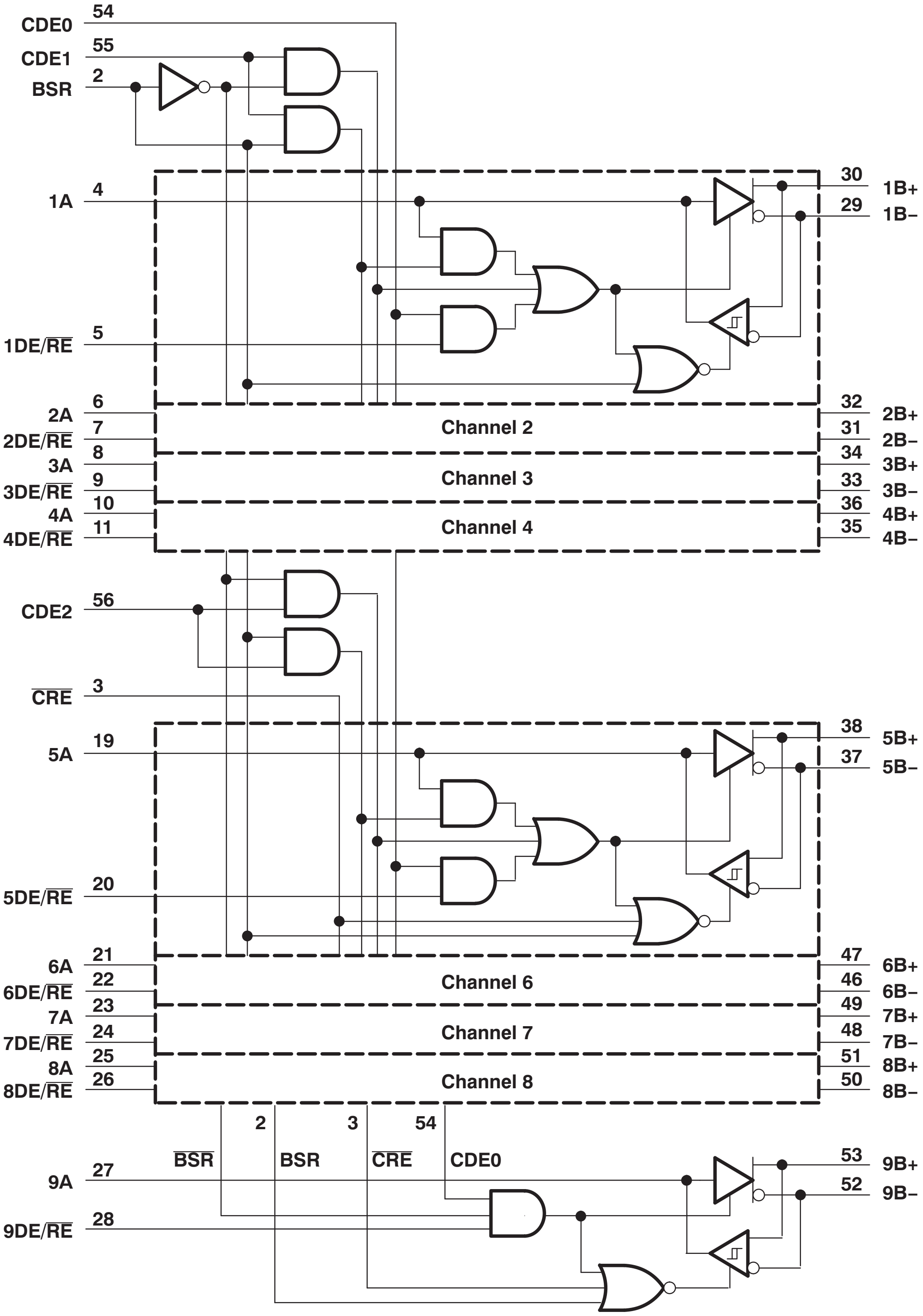
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PIN FUNCTIONS

PIN		LOGIC LEVEL	I/O	TERMINATION	DESCRIPTION
NAME	NO.				
1A to 9A	4,6,8,10, 19,21,23, 25,27	TTL	I/O	Pullup	1A to 9A carry data to and from the communication controller.
1B– to 9B–	29,31,33, 35,37,.46 , 48,50,52	RS-485	I/O	Pulldown	1B– to 9B– are the inverted data signals of the balanced pair to/from the bus.
1B+ to 9B+	30,32,34, 36,38,47, 49,51,53	RS-485	I/O	Pullup	1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus.
BSR	2	TTL	Input	Pullup	BSR is the bit significant response. BSR disables receivers 1 through 8 and enables wired-OR drivers when BSR and DE/$\overline{\text{RE}}$ and CDE1 or CDE2 are high. Channel 9 is placed in a high-impedance state with BSR high.
CDE0	54	TTL	Input	Pulldown	CDE0 is the common driver enable 0. Its input signal enables all drivers when CDE0 and 1DE/$\overline{\text{RE}}$ – 9DE/$\overline{\text{RE}}$ are high.
CDE1	55	TTL	Input	Pulldown	CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when CDE1 is high and BSR is low.
CDE2	56	TTL	Input	Pulldown	CDE2 is the common driver enable 2. When CDE2 is high and BSR is low, drivers 5 to 8 are enabled.
$\overline{\text{CRE}}$	3	TTL	Input	Pullup	$\overline{\text{CRE}}$ is the common receiver enable. When high, CRE disables receiver channels 5 to 9.
1DE/$\overline{\text{RE}}$ to 9DE/$\overline{\text{RE}}$	5,7,9,11, 20,22,24, 26,28	TTL	Input	Pullup	1DE/$\overline{\text{RE}}$–9DE/$\overline{\text{RE}}$ are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when 1DE/$\overline{\text{RE}}$–9DE/$\overline{\text{RE}}$ and CRE and BSR are low and CDE1 and CDE2 are low.
GND	1,13,14, 15,16,17, 40,41,42, 43,44	NA	Power	NA	GND is the circuit ground. All GND terminals except terminal 1 are physically tied to the die pad for improved thermal conductivity.[1]
V_{CC}	12,18,39, 45	NA	Power	NA	Supply voltage

(1) Terminal 1 must be connected to signal ground for proper operation.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

			VALUE	UNIT
V_{CC}	Supply voltage range(2)		–0.3 to 6	V
	Bus voltage range		–10 to 15	V
	Data I/O and control (A side) voltage range		–0.3 to V_{CC} +0.5	V
I_O	Receiver output current		±40	mA
	Electrostatic discharge	B side and GND, ESD HBM	12	kV
		B side and GND, ESD MM	400	V
		All terminals, ESD HBM	4	kV
		All terminals, ESD MM	400	V
	Continuous total power dissipation (3)		Internally Limited	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under r*ecommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.r

(2) All voltage values are with respect to the GND terminals.

(3) The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.

DISSIPATION RATINGS

PACKAGE	TA ≤ 25°C	OPERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGG	2500 mW	20 mW/°C	1600 mW	1300 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

PACKAGE THERMAL CHARACTERISTICS

			MIN	NOM	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	DGG, board-mounted, no air flow		50		°C/W
θ_{JC}	Junction-to-case thermal resistance	DGG		27		°C/W
T_{SD}	Thermal shutdown temperature			165		°C

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	Except nB+, nB–(1)	2			V
V_{IL}	Low-level input voltage				0.8	V
V_O, V_I, or V_{IC}	Voltage at any bus terminal (separately or common-mode)	nB+ or nB–	–7		12	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	mA
T_A	Operating free-air temperature		–40		85	°C

(1) n = 1 - 9

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN65HVD09			UNIT
					MIN	TYP[1]	MAX	
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	RS-422 load,	R_L = 100 Ω	See Figure 1	0.56	1.6		V
		RS-485 load,	R_L = 54 Ω			1.4		
		Pull-Up Pull-Down Load		See Figure 2	1	1.5		
V_{OH}	High-level output voltage	A side, I_{OH} = –8 mA, V_{ID} = 200 mV,		See Figure 4	4	4.5		V
		B side,		See Figure 2		3		V
V_{OL}	Low-level output voltage	A side, I_{OH} = 8 mA, V_{ID} = –200 mV,		See Figure 4		0.6	0.8	V
		B side,		See Figure 2		1		V
V_{IT+}	Receiver positive-going differential input threshold voltages	I_{OH} = –8 mA,		See Figure 4			0.2	V
V_{IT-}	Receiver negativegoing differential input threshold voltage	I_{OL} = 8 mA,		SeeFigure 4	–0.2			V
V_{hys}	Receiver input hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 5 V,	T_A = 25°C		24	45		mV
I_I	Bus input current	V_{IH} = 12 V	V_{CC} = 5 V,	Other input at 0 V			1	mA
		V_{IH} = 12 V	V_{CC} = 0,				1	mA
		V_{IH} = –7 V	V_{CC} = 5 V,		–0.8	–0.4		mA
		V_{IH} = –7 V	V_{CC} = 0,		–0.8	–0.3		mA
I_{IH}	High-level input current	nA, BSR, DE/$\overline{\text{RE}}$, and $\overline{\text{CRE}}$,		V_{IH} = 2 V	–100			µA
		CDE0, CDE1, and CDE2,		V_{IH} = 2V			100	µA
I_{IL}	Low-level input current	nA, BSR, DE/$\overline{\text{RE}}$, and $\overline{\text{CRE}}$,		V_{IL} = 0.8 V	–100			µA
		CDE1, CDE1, and CDE2,		V_{IL} = 0.8 V			100	µA
I_{OS}	Short circuit output current	nB+ or nB–					±260	mA
I_{OZ}	High-impedance-state output current	nA			See I_{IH} and I_{IL}			
		nB+ or nB–			See I_{II}			
I_{CC}	Supply current	Disabled					10	mA
		All drivers enabled, no load					60	
		All receivers enabled, no load					45	
C_O	Output capacitance	nB+ or nB– to GND				18		pF
C_{pd}	Power dissipation capacitance (2)	Receiver				40		pF
		Driver				100		

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) C_{pd} determines the no-load dynamic supply current consumption, $I_S = C_{PD} \times V_{CC} \times f + I_{CC}$

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65HVD09			UNIT
			MIN	TYP[1]	MAX	
t_{pd}	Propagation delay time, t_{PHL} or t_{PLH} (see Figure 2 and Figure 3)		2.5		13.5	ns
$t_{sk(p)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$				5	ns
t_f	Fall time	S1 to B, See Figure 3		4		ns
t_r	Rise time	See Figure 3		8		ns
t_{en}	Enable time, control inputs to active output				50	ns
t_{dis}	Disable time, control inputs to high-impedance output				225	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	See Figure 6 and Figure 7		17	225	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output			25	225	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output			17	50	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output			17	50	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

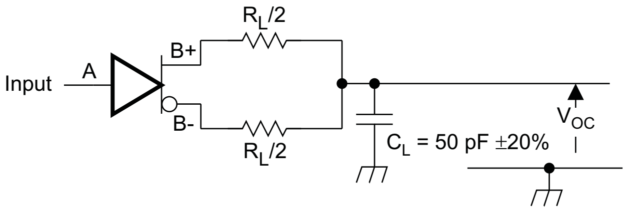
RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65HVD09			UNIT
			MIN	TYP[1]	MAX	
t_{pd}	Propagation delay time, t_{PHL} or t_{PLH} (see Figure 2 and Figure 3)		8		14.5	ns
$t_{sk(lim)}$	Skew limit, maximum t_{pd} – minimum t_{pd} [2]				5	ns
$t_{sk(p)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$			0.6	5	ns
t_t	Transition time (t_r or t_f)	See Figure 5		2		ns
t_{en}	Enable time, control inputs to active output			31		ns
t_{dis}	Disable time, control inputs to high-impedance output			41		ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	See Figure 8 and Figure 9		34		ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output			14		ns
t_{PZH}	Propagation delay time, high-impedance to high-level output			30		ns
t_{PZL}	Propagation delay time, high-impedance to low-level output			30		ns

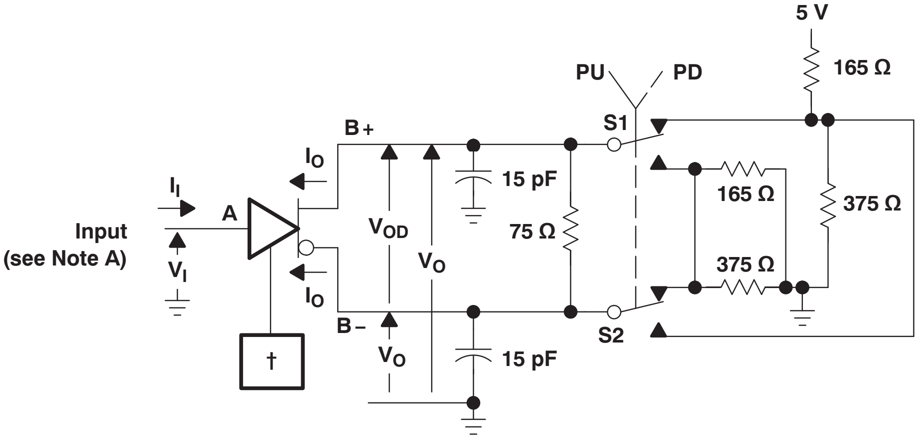
(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions and to any two devices.

PARAMETER MEASUREMENT INFORMATION



C_L Includes Fixture and
Instrumentation Capacitance

Figure 1. Driver Test Circuit, RS-422 and RS-485 Loading



† CDEO and DE/$\overline{RE}$ are at 2 V, BSR is at 0.8V, and all others are open.
‡ All nine drivers are enabled, similarly loaded, and switching.

Figure 2. Driver Test Circuit, Pull-Up and Pull-Down Loading‡

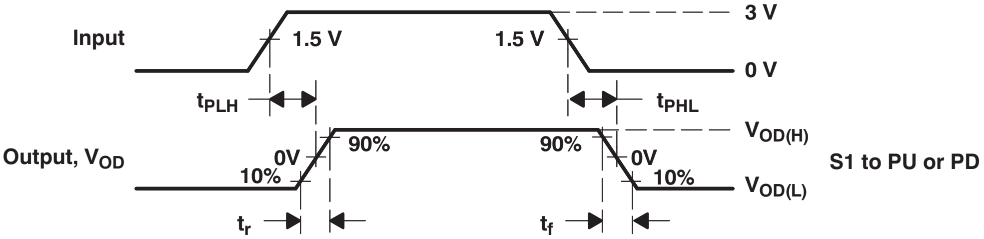
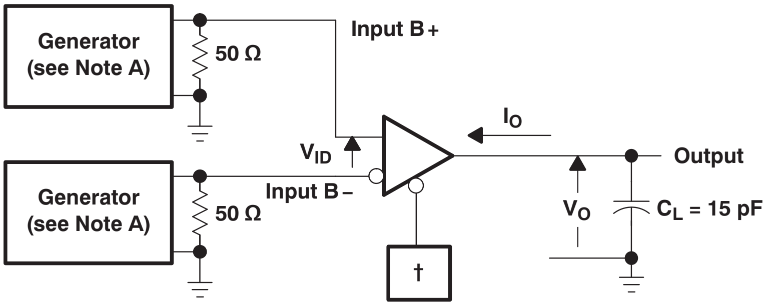


Figure 3. Driver Delay and Transition Time Test Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



† CDEO, CDE1, CDE2, BSR, CRE, and DE/$\overline{RE}$ at 0.8 V

‡ All nine receivers are enabled and switching.

Figure 4. Receiver Propagation Delay and Transition Time Test Circuit

A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.

B. All resistances are in Ω and ±5%, unless otherwise indicated.

C. All capacitances are in pF and ±10%, unless otherwise indicated.

D. All indicated voltages are ±10 mV.

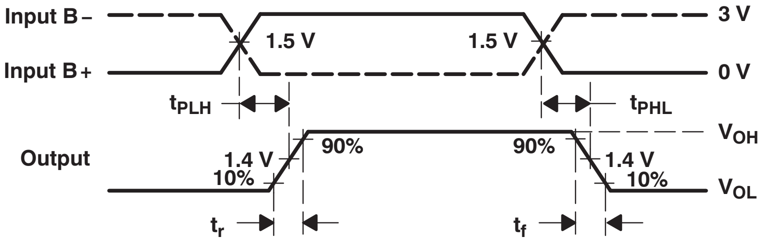
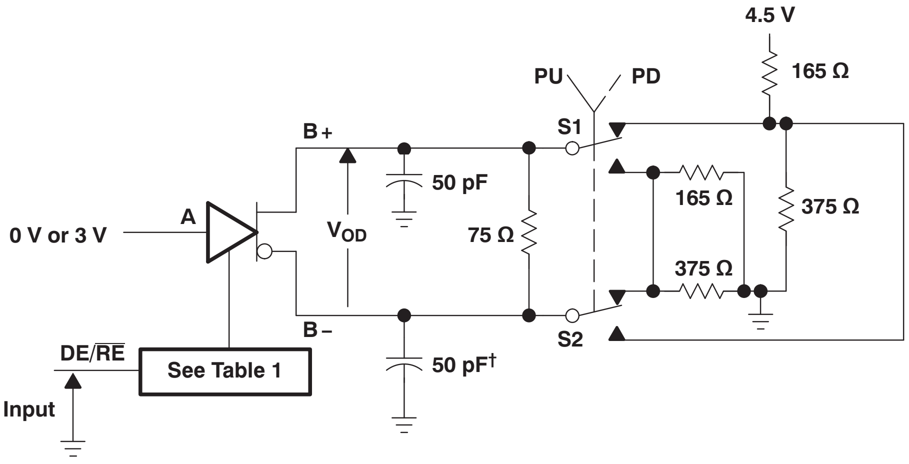


Figure 5. Receiver Delay and Transition Time Waveforms



† Includes probe and jig capacitance in two places.

Figure 6. Driver Enable and Disable Time Test Circuit

Table 1. Enabling for Driver Enable and Disable Time

DRIVER	BSR	CDE0	CDE1	CDE2	$\overline{\text{CRE}}$
1–8	H	H	L	L	X
9	L	H	H	H	H

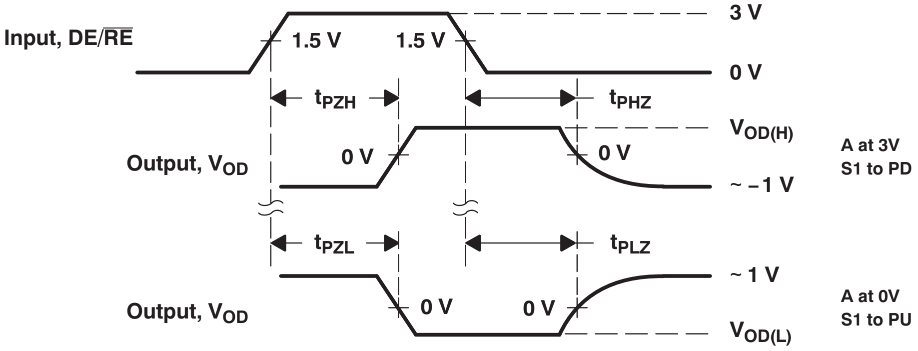
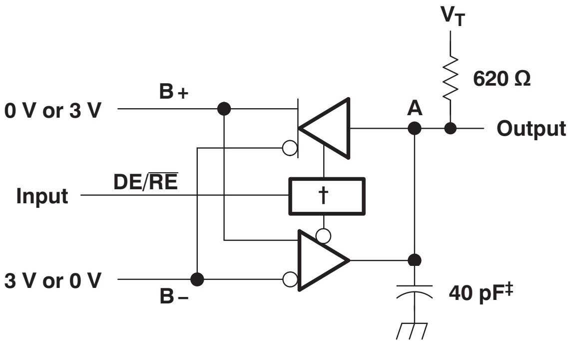


Figure 7. Driver Enable Time Waveforms

NOTES:
A. All input pulses are supplied by a generator having the following characteristics: $t_r \le 6$ ns, $t_f \le 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in Ω and ±5%, unless otherwise indicated.
C. All capacitances are in pF and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.



† CDEO is high, CDE1, CDE2, BSR, and $\overline{\text{CRE}}$ are low, all others are open.

‡ Includes probe and jig capacitance.

Figure 8. Receiver Enable and Disable Time Test Circuit

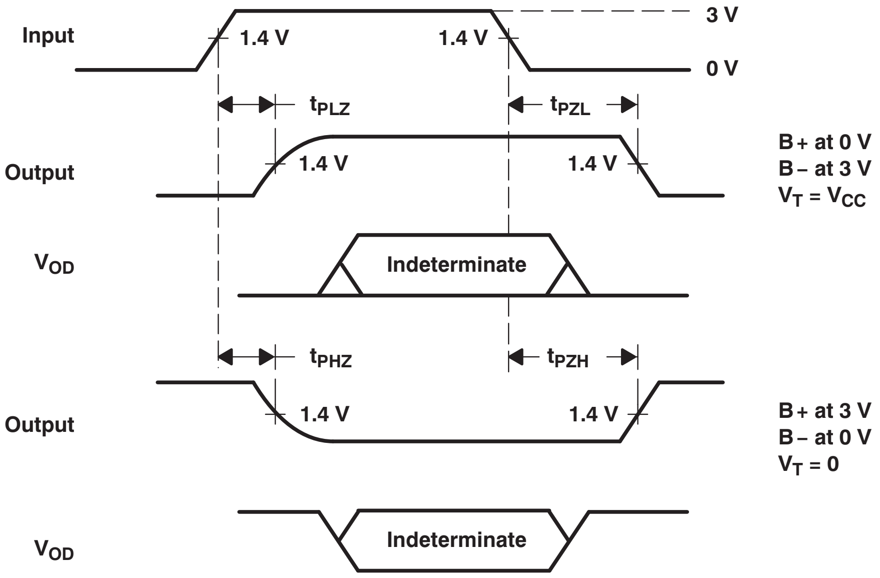


Figure 9. Receiver Enable and Disable Time Waveforms

NOTES:

A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.

B. All resistances are in Ω and ±5%, unless otherwise indicated.

C. All capacitances are in pF and ±10%, unless otherwise indicated.

D. All indicated voltages are ±10 mV.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

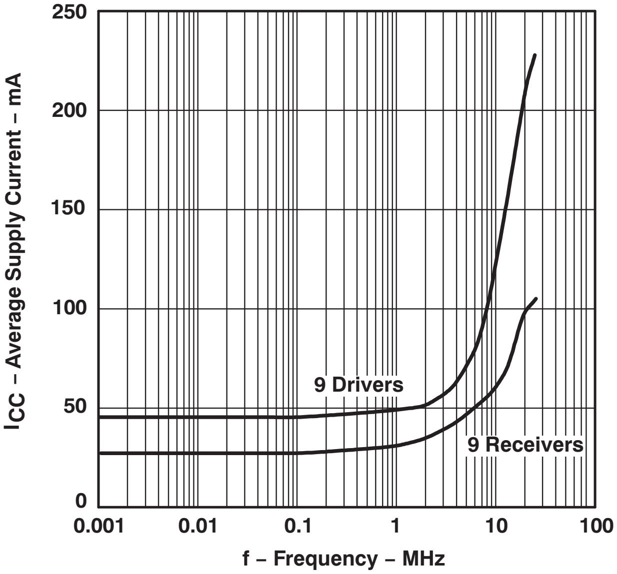


Figure 10.

LOGIC INPUT CURRENT
vs
INPUT VOLTAGE

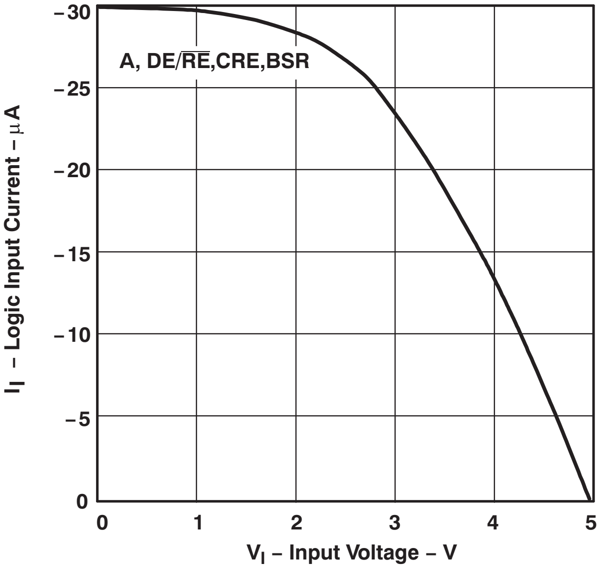


Figure 11.

BUS
INPUT CURRENT
vs
INPUT VOLTAGE

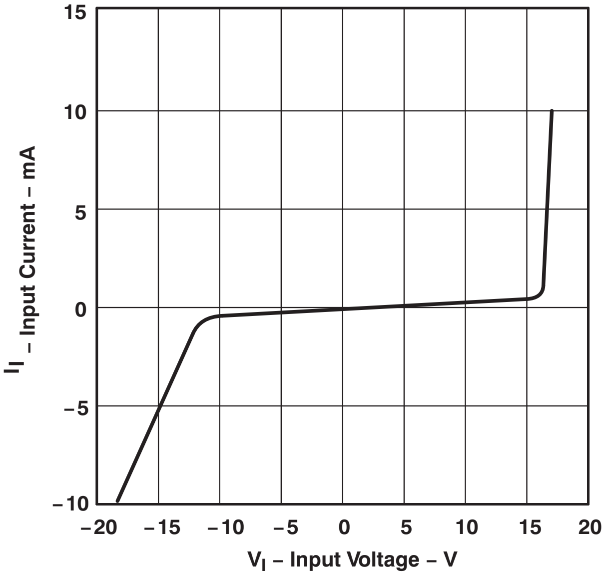


Figure 12.

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

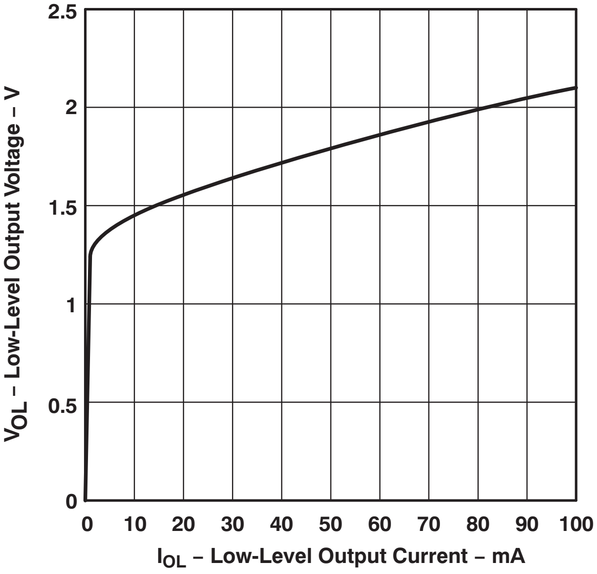


Figure 13.

TYPICAL CHARACTERISTICS (continued)

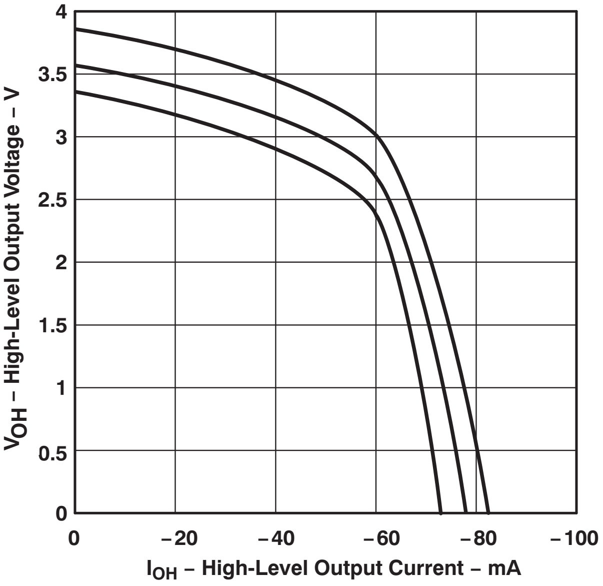

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 14.

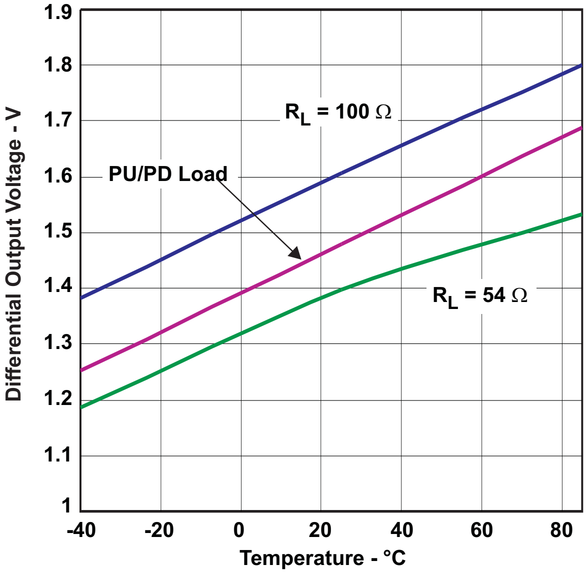

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
TEMPERATURE

Figure 15.

RECEIVER
PROPAGATION DELAY TIME
vs
TEMPERATURE

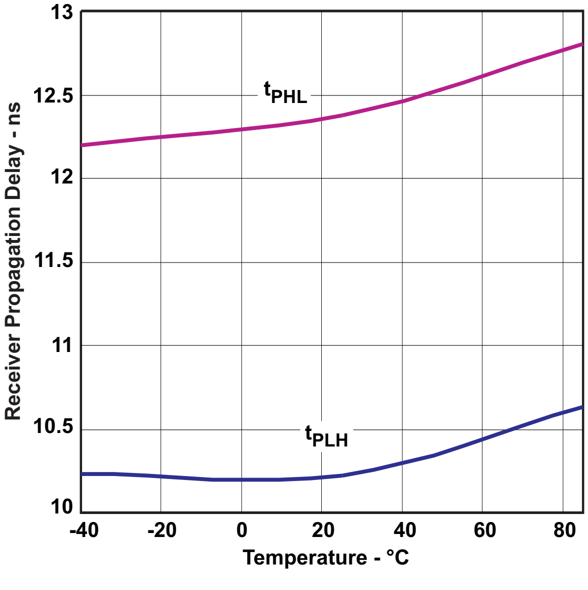


Figure 16.

DRIVER
PROPAGATION DELAY TIME
vs
TEMPERATURE

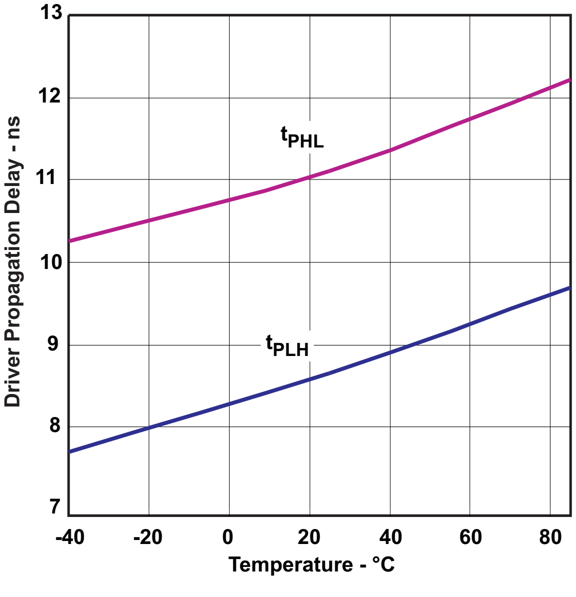


Figure 17.

TYPICAL CHARACTERISTICS (continued)

DRIVER
OUTPUT CURRENT
vs
SUPPLY VOLTAGE

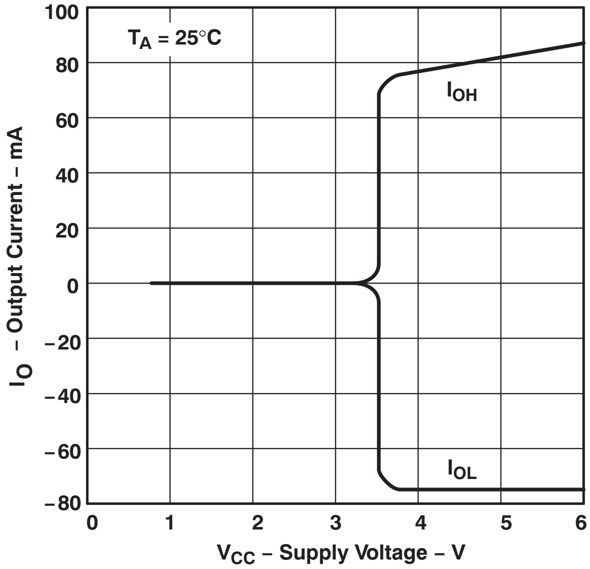
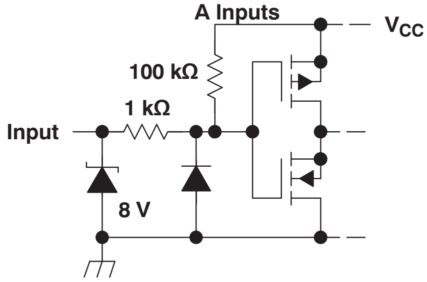


Figure 18.

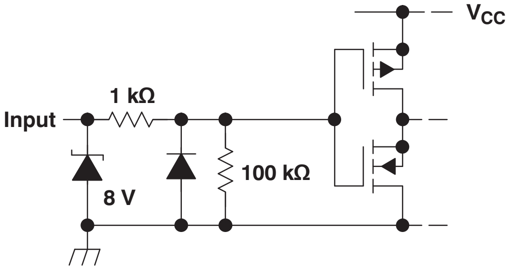
TYPICAL CHARACTERISTICS (continued)

SCHEMATICS OF INPUTS AND OUTPUTS

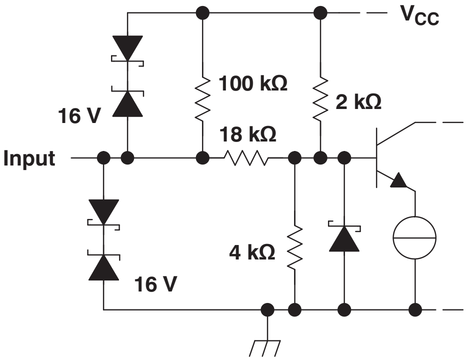
DE/$\overline{RE}$, $\overline{CRE}$, BSR, AND A Inputs



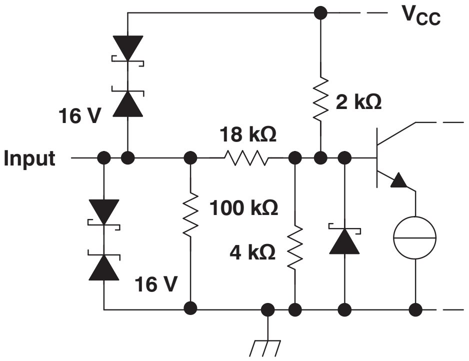
CDE0, CDE1, AND CDE2 Inputs



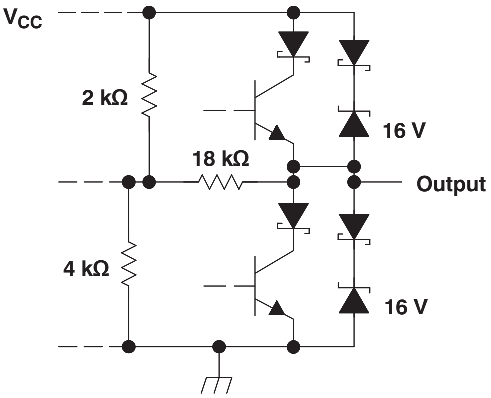
B + Input



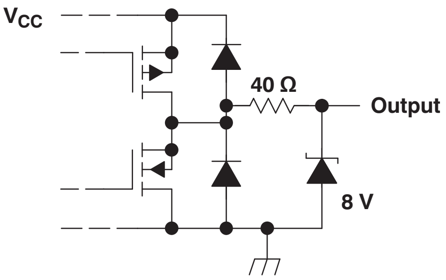
B – Input



B + AND B – Outputs



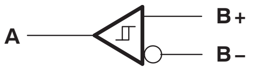
A Output



APPLICATION INFORMATION

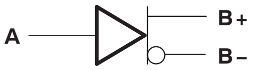
FUNCTION TABLES

RECEIVER



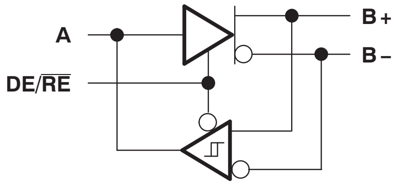
INPUTS		OUTPUT
B+[1]	B−[1]	A
L	H	L
H	L	H

DRIVER



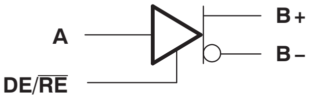
INPUT	OUTPUTS	
A	B+	B−
L	L	H
H	H	L

TRANSCEIVER



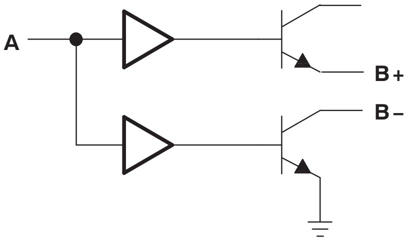
INPUTS				OUTPUTS		
DE/$\overline{\text{RE}}$	A	B+[1]	B−[1]	A	B+	B−
L	–	L	H	L	–	–
L	–	H	L	H	–	–
H	L	–	–	–	L	H
H	H	–	–	–	H	L

DRIVER WITH ENABLE



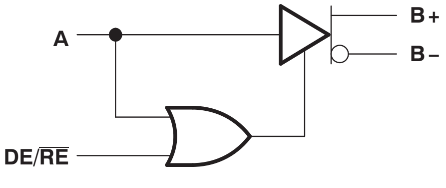
INPUTS		OUTPUTS	
DE/$\overline{\text{RE}}$	A	B+	B−
L	L	Z	Z
L	H	Z	Z
H	L	L	H
H	H	H	L

WIRED-OR DRIVER



INPUT	OUTPUTS	
A	B+	B−
L	Z	Z
H	H	L

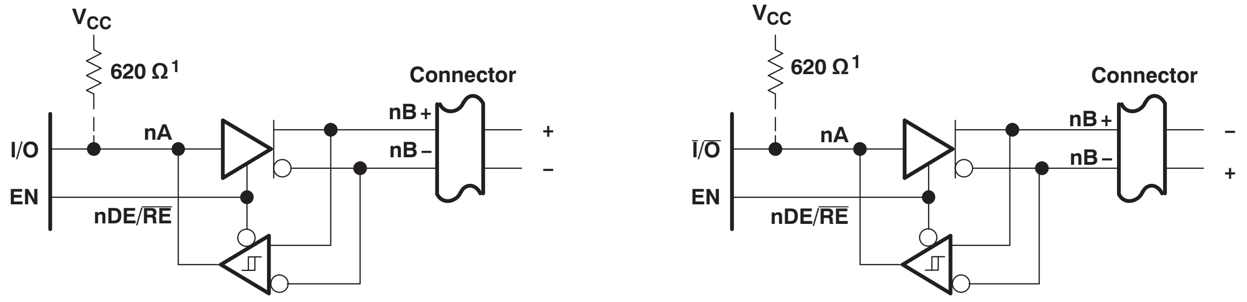
TWO-ENABLE INPUT DRIVER



INPUTS		OUTPUTS	
DE/$\overline{\text{RE}}$	A	B+	B−
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	H	L

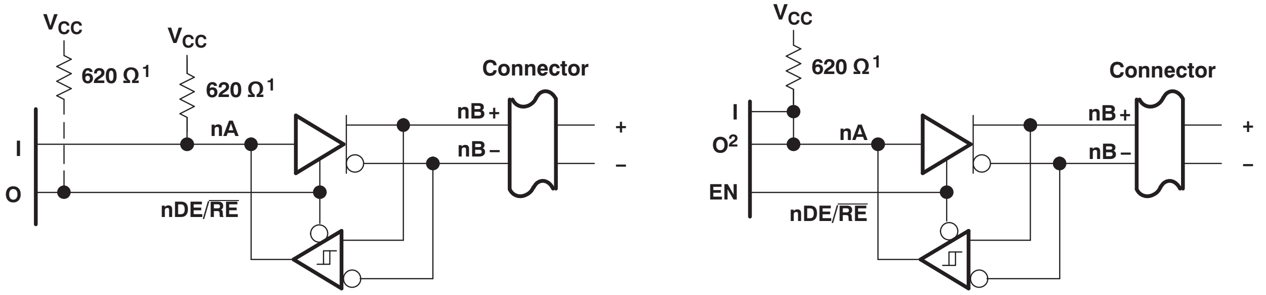
NOTE: H = high level, L = low level, X = irrelevant, Z = high impedance (off)

(1) An H in this column represents a voltage of 200 mV or higher than the other bus input. An L represents a voltage of 200 mV or lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.



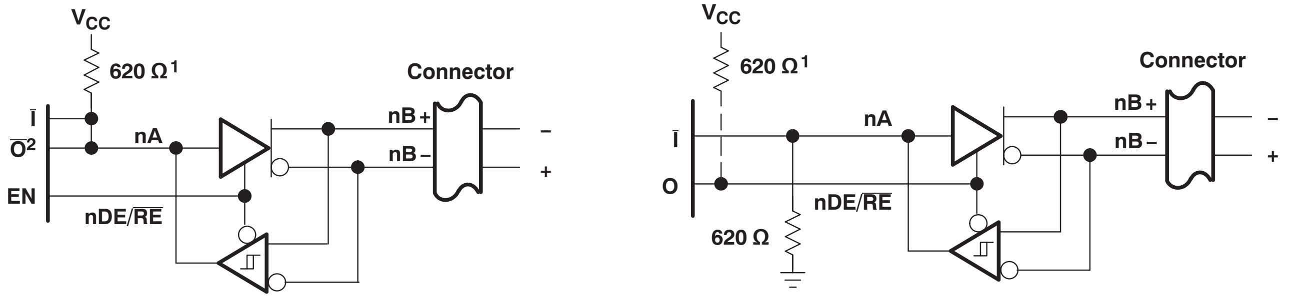
(a) ACTIVE-HIGH BIDIRECTIONAL I/O WITH SEPARATE ENABLE

(b) ACTIVE-LOW BIDIRECTIONAL I/O WITH SEPARATE ENABLE



(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT

(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT, AND ENABLE



(e) SEPARATE ACTIVE-LOW INPUT AND OUTPUT AND ACTIVE-HIGH ENABLE

(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

1: When 0 is open drain
2: Must be open-drain or 3-state output

(1) When 0 is open drain

(2) Must be open-drain or 3-state output

NOTE: The BSR, $\overline{\text{CRE}}$, A, and DE/$\overline{\text{RE}}$ inputs have internal pullup resistors. CDE0, CDE1, and CDE2 have internal pulldown resistors.

Figure 19. Typical Transceiver Connections

CHANNEL LOGIC CONFIGURATIONS WITH CONTROL INPUT LOGIC

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; the BSR, CDE0, CDE1, CDE2, and $\overline{\text{CRE}}$ bit values are shown below the diagrams. Channel 1 is at the top of the logic diagrams; channel 9 is at the bottom of the logic diagrams.

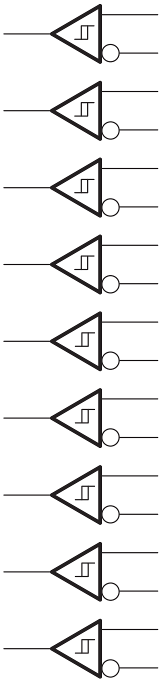


Figure 19. 00000

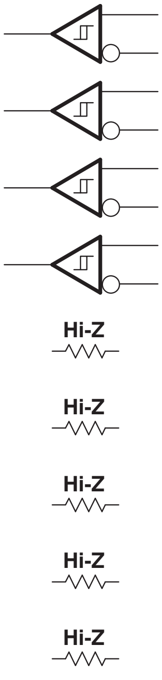


Figure 20. 00001

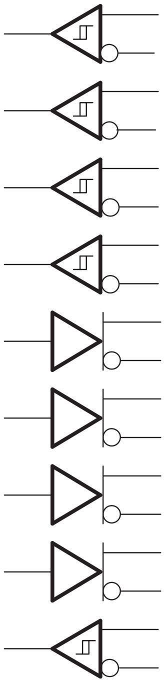


Figure 21. 00010

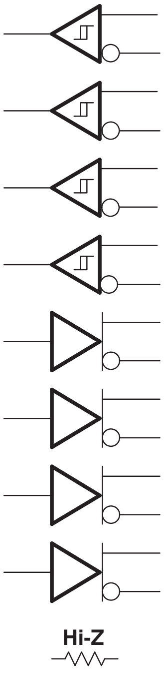


Figure 22. 00011

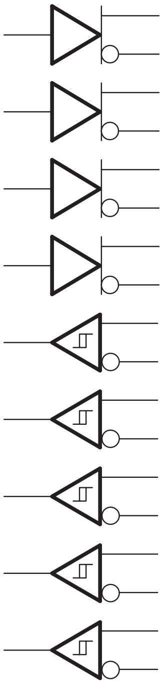


Figure 23. 00100

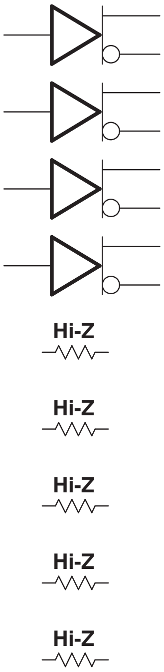


Figure 24. 00101

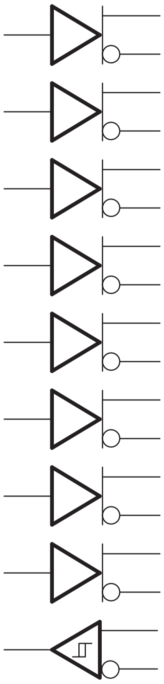


Figure 25. 00110

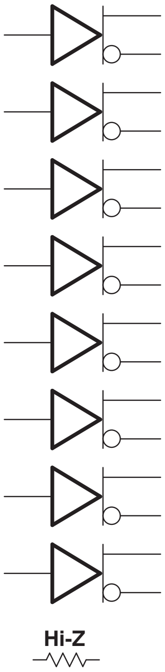


Figure 26. 00111

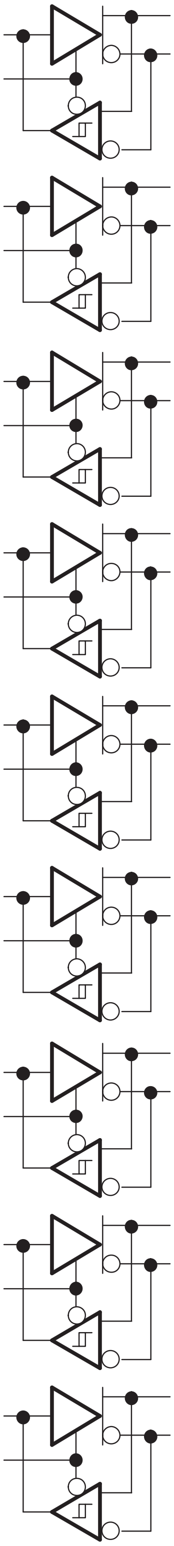


Figure 27. 01000

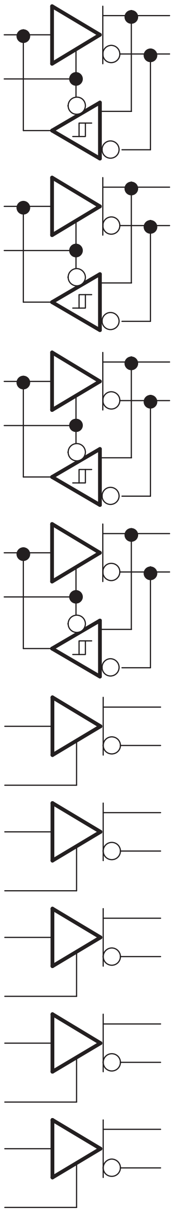


Figure 28. 01001

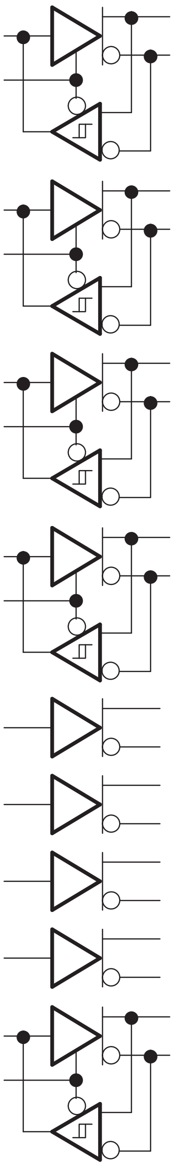


Figure 29. 01010

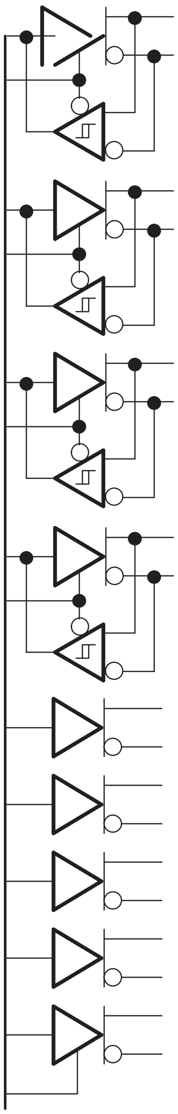


Figure 30. 01011

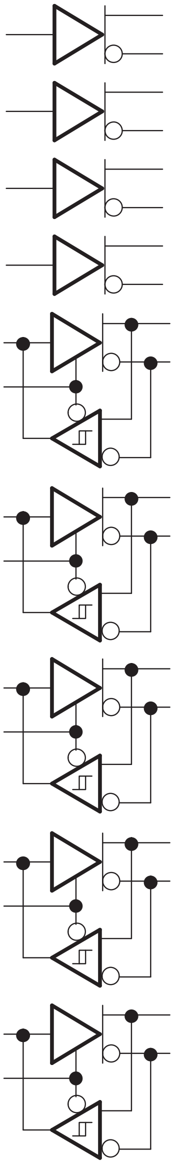


Figure 31. 01100

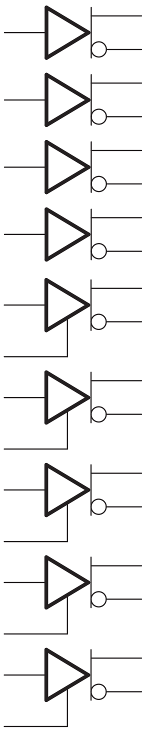


Figure 32. 01101

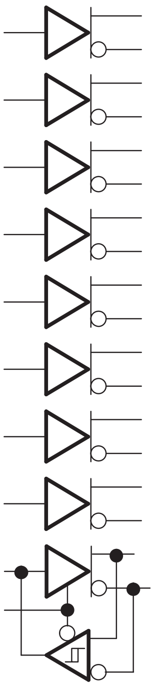


Figure 33. 01110

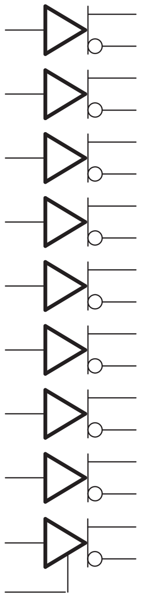


Figure 34. 01111

Figure 35. 10000 and 10001

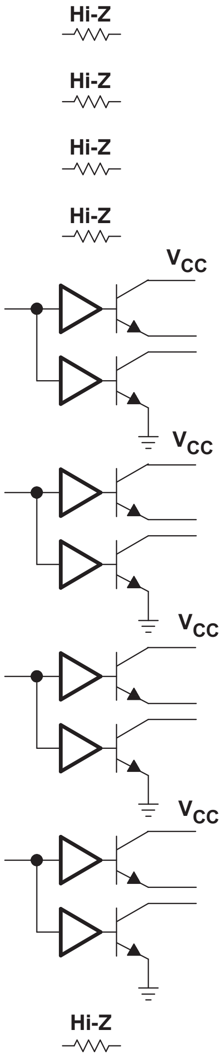


Figure 36. 10010 and 10011

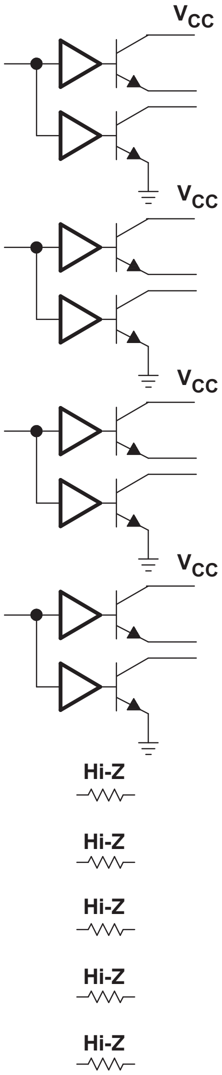


Figure 37. 10100 and 10101

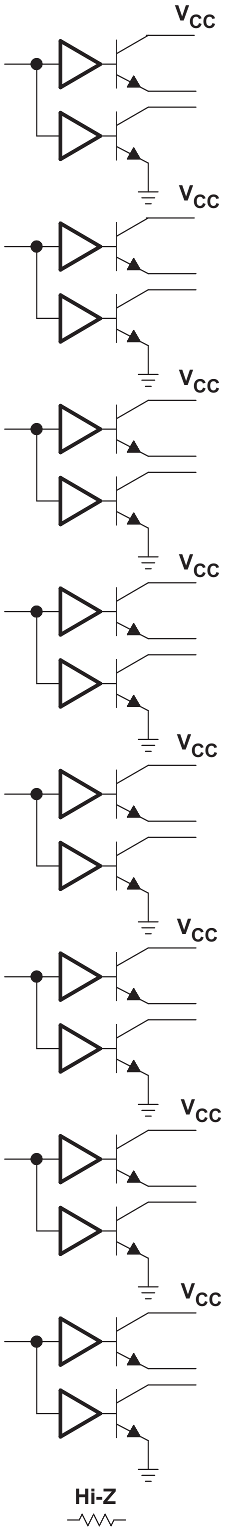


Figure 38. 10110 and 10111

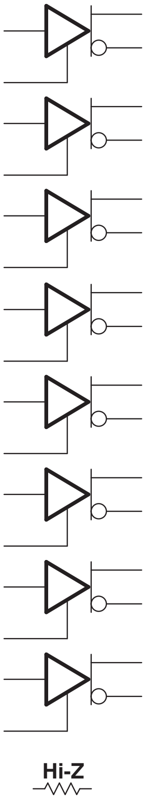


Figure 39. 11000 and 11001

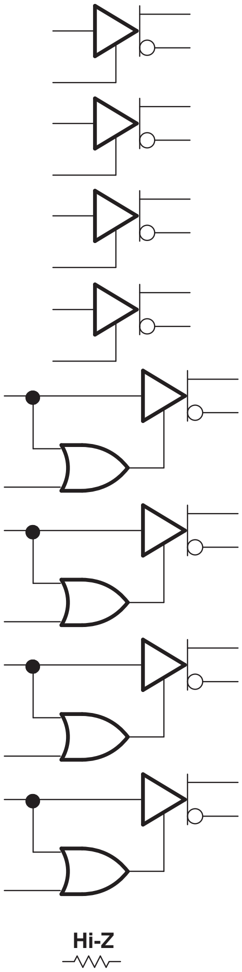


Figure 40. 11010 and 11011

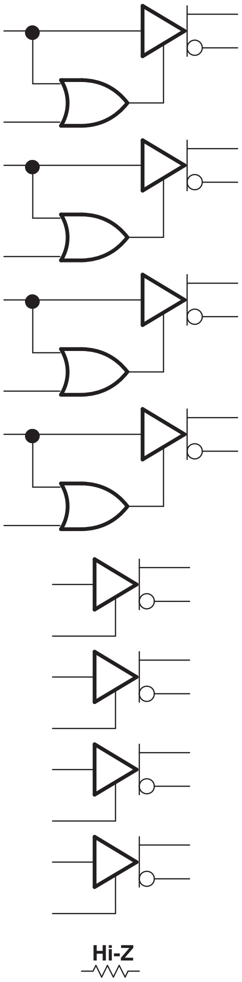


Figure 41. 11100 and 11101

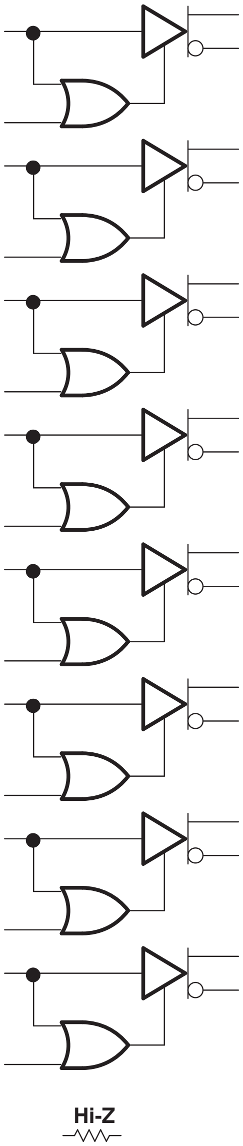


Figure 42. 11110 and 11111

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD09IDGGREP	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN65HVD09EP	Samples
V62/12607-01XE	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN65HVD09EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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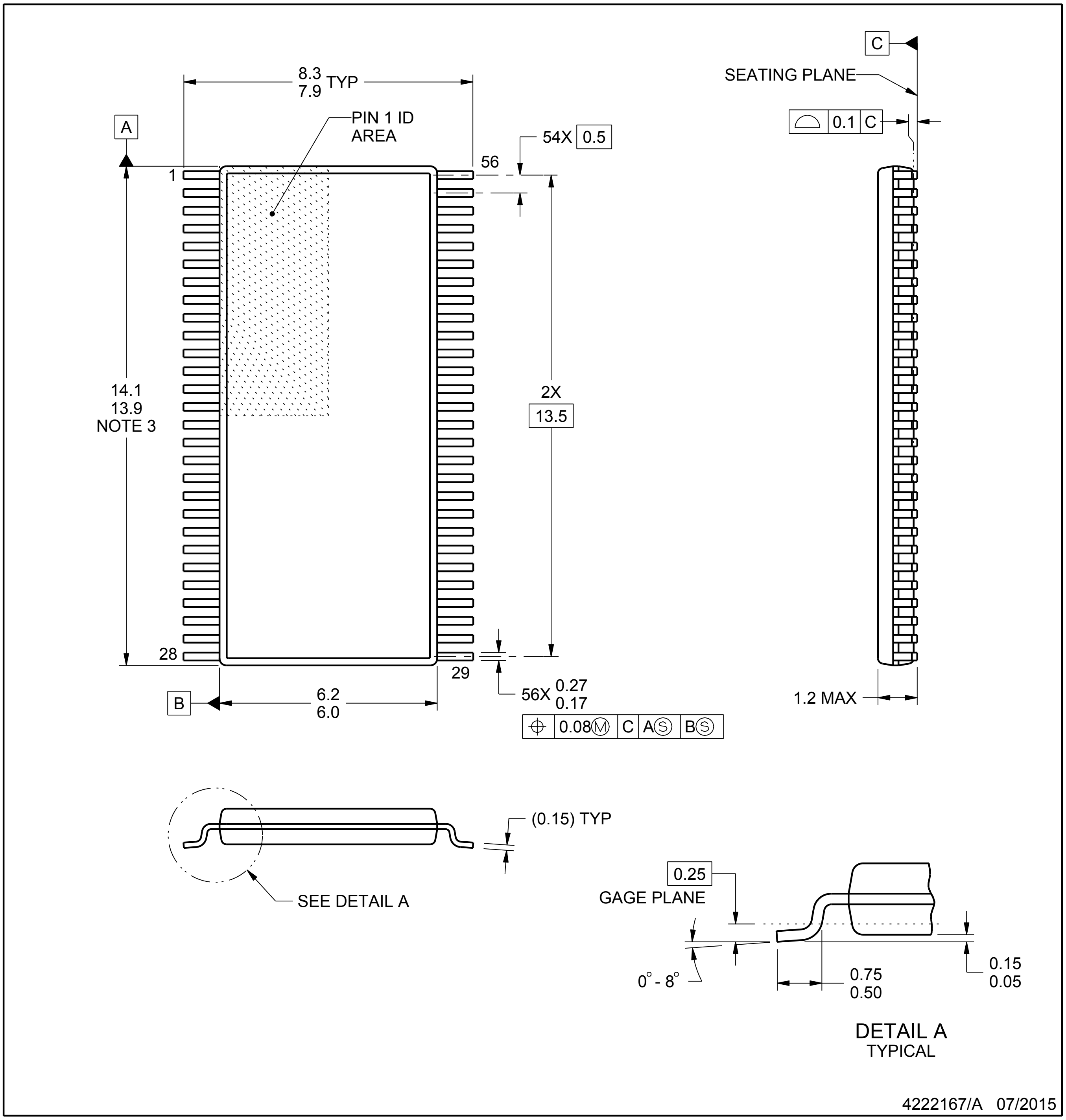
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

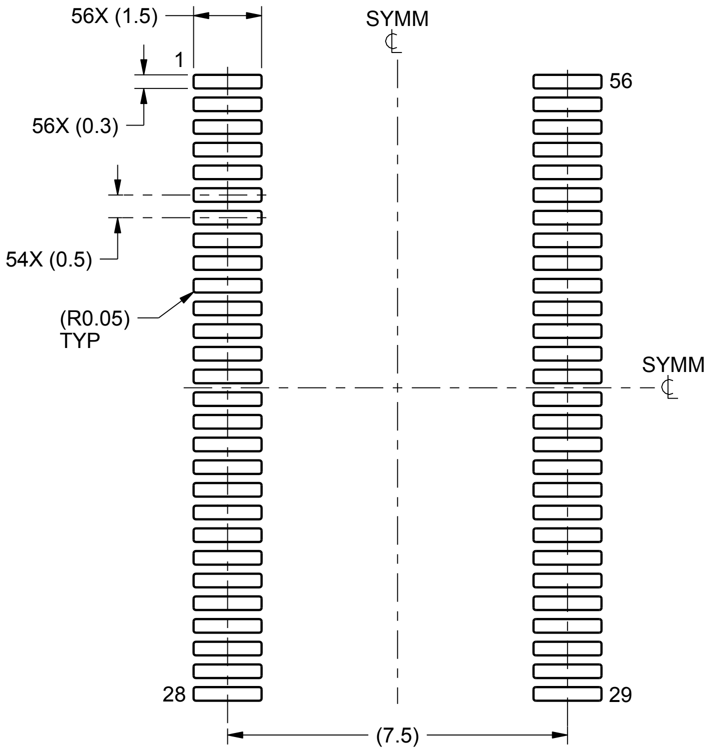
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

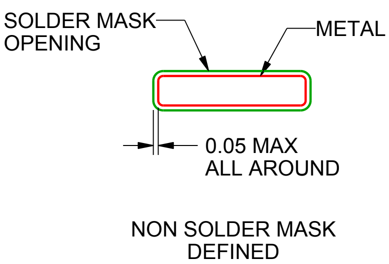


NOTES:

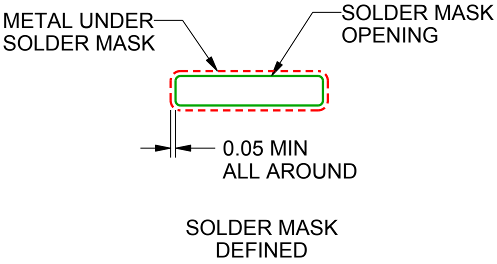
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED



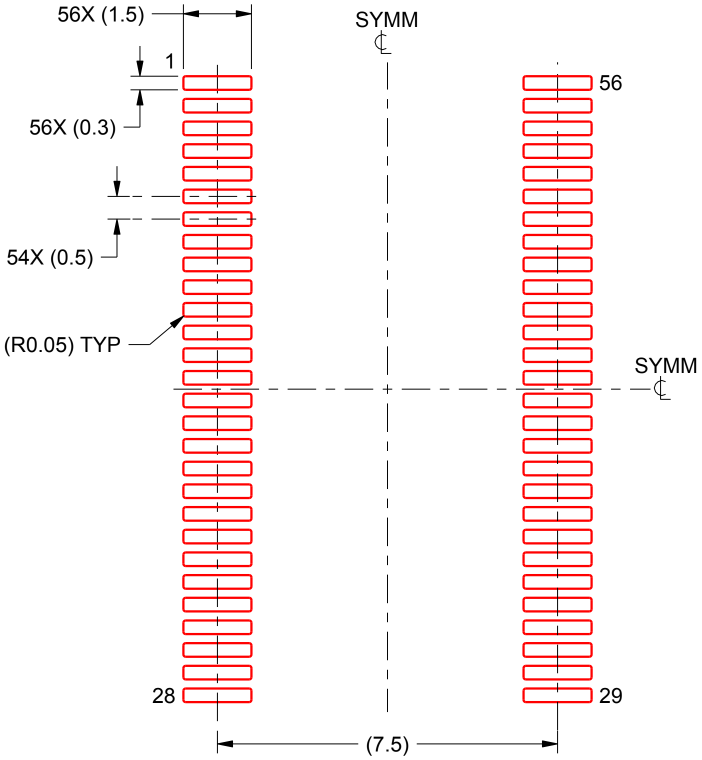
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122