具有 ±12kV ESD 保护的 SN65C1168E-SEP 双路差动驱动器和接收器

1 特性

- VID V62/19606
- 耐辐射
  - 单粒子锁定 (SEL) 在 125°C 下的抗扰度可达 43MeV-cm^2/mg
  - 在 30krad(Si) 的条件下无 ELDRS
  - 每个晶圆批次的 RLAT 总电离剂量 (TID) 高达 20krad(Si)
- 增强型航天塑料
  - 受控基线
  - 金线
  - NiPdAu 铅涂层
  - 一个组装和测试基地
  - 一个制造基地
  - 支持军用（–55°C 至 125°C）温度范围
  - 延长了产品生命周期
  - 延长了产品变更通知
  - 产品可追溯性
  - 采用增强型模塑化合物实现低释气
- 达到或超出 TIA/EIA-422-B 和 ITU Recommendation V.11 标准的要求
- 由一个 5V 电源供电
- 为 RS-422 总线引脚提供 ESD 保护
  - ±12kV 人体放电模型 (HBM)
  - ±8kV IEC 61000-4-2，接触放电
  - ±8kV IEC 61000-4-2，空气间隙放电
- 低脉冲偏斜
- 接收器输入阻抗 ... 17kΩ（典型值）
- 接收器输入灵敏度 ...±200mV
- -7V 至 7V 的接收器共模输入电压范围
- 无干扰上电/断电保护

2 应用

- 支持近地球轨道空间 应用
- 卫星通信
- 交流和伺服电机驱动器

3 说明

SN65C1168E-SEP 包含双驱动器和双接收器，具有 ±12kV ESD (HBM) 和 ±8kV ESD（IEC61000-4-2 空气间隙放电和接触放电），适用于 RS-422 总线引脚。此器件符合 TIA/EIA-422-B 和 ITU Recommendation V.11 标准的要求。经过 20krad(Si) TID 接触之后，有些参数不符合所有的 TIA/EIA-422-B 和 ITU Recommendation V.11 要求。

SN65C1168E-SEP 驱动器具有单独的高电平有效使能端。

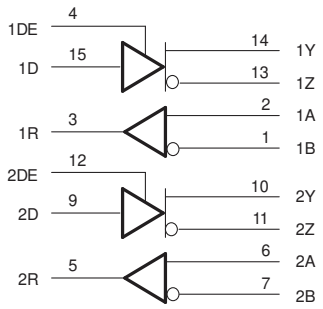
器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN65C1168EMPWTSEP	TSSOP (16)	5.00mm × 4.40mm
SN65C1168EMPWSEP		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

方框图

SN65C1168E-SEP



目录

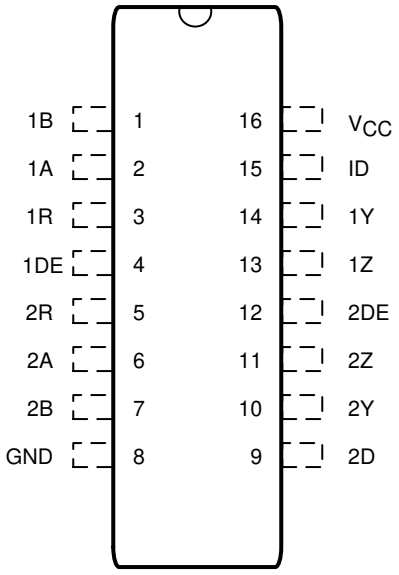
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 7 月	*	初始发行版。

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	RS422 differential input (noninverting) to receiver 1
2A	6	I	RS422 differential input (noninverting) to receiver 2
1B	1	I	RS422 differential input (inverting) to receiver 1
2B	7	I	RS422 differential input (inverting) to receiver 2
1D	15	I	Logic data input to RS422 driver 1
2D	9	I	Logic data input to RS422 driver 2
1DE	4	I	Driver 1 enable (active high)
2DE	12	I	Driver 2 enable (active high)
GND	8	—	Device ground
1R	3	O	Logic data output of RS422 receiver 1
2R	5	O	Logic data output of RS422 receiver 2
V_{CC}	16	—	Power supply
1Y	14	O	RS-422 differential (noninverting) driver output 1
2Y	10	O	RS-422 differential (noninverting) driver output 2
1Z	13	O	RS-422 differential (noninverting) driver output 1
2Z	11	O	RS-422 differential (noninverting) driver output 2

6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	7	V
V_I	Input voltage	Driver, DE, RE	–0.5	7	V
		A or B, Receiver	–14	14	
V_{ID}	Differential input voltage(3)	Receiver	–14	14	V
V_O	Output voltage	Driver	–0.5	7	V
		Receiver	–0.5	V_{CC} + 0.5	
I_{IK}	Input clamp current	Driver, V_I < 0		–20	mA
I_{OK}	Output clamp current	Driver, V_O < 0		–20	mA
		Receiver	–20	20	
I_O	Output current	Driver	–150	150	mA
		Receiver	–25	25	
I_{CC}	Supply current			200	mA
	GND current			–200	mA
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential input voltage are with respect to the network GND.
(3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±12000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		IEC 61000-4-2, air-gap discharge	±8000	
		IEC 61000-4-2, contact discharge	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IC}	Common-mode input voltage(1)	Receiver			±7	V
V_{ID}	Differential input voltage	Receiver			±7	V
V_I	Input voltage	Except A, B	0		5.5	V
V_O	Output voltage	Receiver	0		V_{CC}	V
V_{IH}	High-level input voltage	Except A, B	2			V
V_{IL}	Low-level input voltage	Except A, B			0.8	V
I_{OH}	High-level output current	Receiver			–6	mA
		Driver			–20	
I_{OL}	Low-level output current	Receiver			6	mA
		Driver			20	
T_A	Operating free-air temperature		–55		125	°C

(1) Refer to TIA/EIA-422-B for exact conditions.

6.4 Thermal Information

THERMAL METRIC(1)		SN65C1168E-SEP	UNIT
		PW (TSSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Driver Section Electrical Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –20 mA		2.4	3.5		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
$\|V_{OD1}\|$	Differential output voltage 1	I_O = 0 mA		2		6	V
$\|V_{OD2}\|$	Differential output voltage 2	R_L = 100 Ω, see Figure 1(2)		2	3.7		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	R_L = 100 Ω, see Figure 1(2)		–0.4		0.4	V
V_{OC}	Common-mode output voltage	R_L = 100 Ω, see Figure 1(2)		–3		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage	R_L = 100 Ω, see Figure 1(2)		–0.4		0.4	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0 V	V_O = 6 V			100	µA
			V_O = –0.25 V			100	
$I_{O(OFF)}$	Output current with power off(3)	V_{CC} = 0 V	V_O = 6 V			3	mA
			V_O = –0.25 V			3	
I_{OZ}	High-impedance-state output current	V_O = 2.5 V				20	µA
		V_O = 5 V				–20	
I_{OZ}	High-impedance-state output current(3)	V_O = 2.5 V				2	mA
		V_O = 5 V				–2	
I_{IH}	High-level input current	$V_I = V_{CC}$ or V_{IH}				1	µA
I_{IL}	Low-level input current	V_I = GND or V_{IL}				–36	µA
I_{OS}	Short-circuit output current	$V_O = V_{CC}$ or GND(4)		–30		–160	mA
I_{CC}	Supply current (total package)	No load, Enabled	$V_I = V_{CC}$ or GND		4	6	mA
			V_I = 2.4 or 0.5 V(5)		5	9	
I_{CC}	Supply current (total package)(3)	No load, Enabled	$V_I = V_{CC}$ or GND			17	mA
			V_I = 2.4 or 0.5 V(5)			16	
C_i	Input capacitance				6		pF

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Refer to TIA/EIA-422-B for exact conditions.
(3) 25°C only. Post 20-krad(Si) HDR TID using worst case static biasing.
(4) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(5) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

6.6 Receiver Section Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input					0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input			–0.2(2)			V
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})				60		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –6 mA		3.8	4.2		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 6 mA			0.1	0.3	V
I_I	Line input current	Other input at 0 V	V_I = 10 V			1.5	mA
			V_I = –10 V			–2.5	
r_I	Input resistance	V_{IC} = –7 V to 7 V, other input at 0 V		4	17		kΩ
I_{CC}	Supply current (total package)	No load, Enabled	V_I = V_{CC} or GND		4	6	mA
			V_{IH} = 2.4 V or 0.5 V(3)		5	9	
I_{CC}	Supply current (total package)(4)	No load	V_I = V_{CC} or GND			17	mA
			V_I = 2.4 or 0.5 V(5)			16	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) Refer to TIA/EIA-422-B for exact conditions.
(4) 25°C only. Post 20-krad(Si) HDR TID using worst case static biasing.
(5) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

6.7 Driver Section Switching Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see Figure 2		8	16	ns
t_{PLH}	Propagation delay time, low- to high-level output			8	16	ns
$t_{sk(p)}$	Pulse skew			1.5	4	ns
t_r	Rise time	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see Figure 3		5	8	ns
t_f	Fall time			5	8	ns
t_{PZH}	Output-enable time to high level	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is closed, see Figure 4		10	19	ns
t_{PZL}	Output-enable time to low level			10	19	ns
t_{PHZ}	Output-disable time from high level	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is closed, see Figure 4		7	16	ns
t_{PLZ}	Output-disable time from low level			7	16	ns
f_{SW}	Maximum switching frequency	R1 = R2 = 50 Ω, R3 = 500 Ω, C1 = C2 = C3 = 40 pF, S1 is open, see Figure 3	20			MHz

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

6.8 Receiver Section Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 5	9	15	27	ns
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 5	9	15	27	ns
t_{TLH}	Transition time, low- to high-level output	V_{IC} = 0 V, see Figure 5		4	9	ns
t_{PHL}	Transition time, high- to low-level output			4	9	ns

(1) Measured per input while the other inputs are at V_{CC} or GND.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

7 Parameter Measurement Information

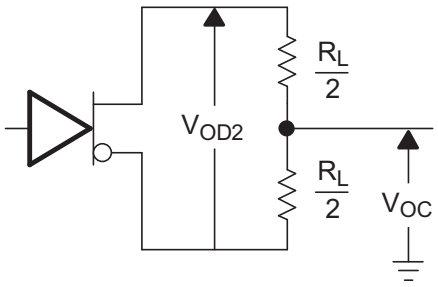
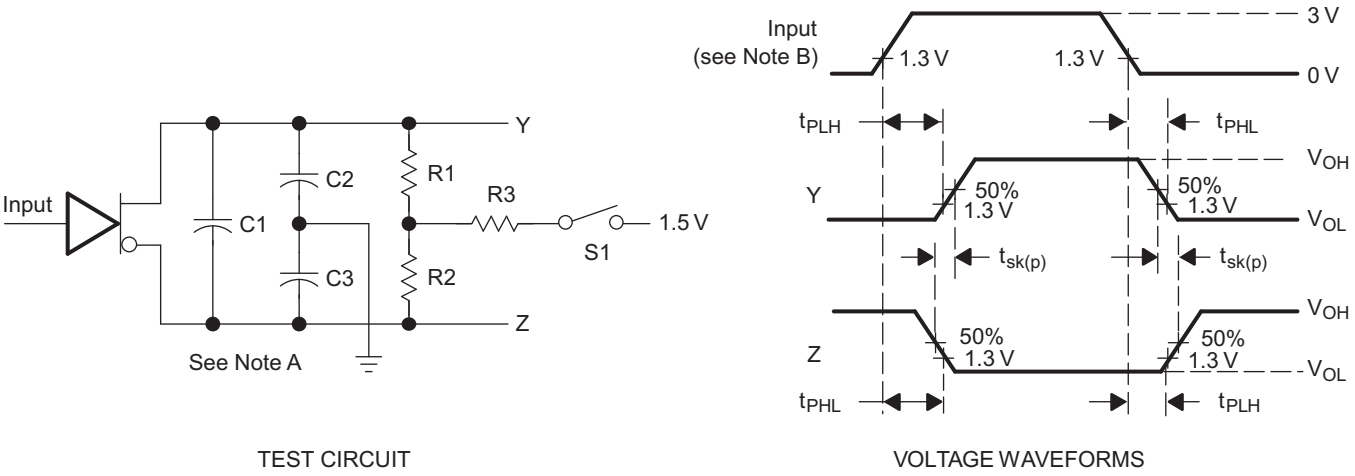


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

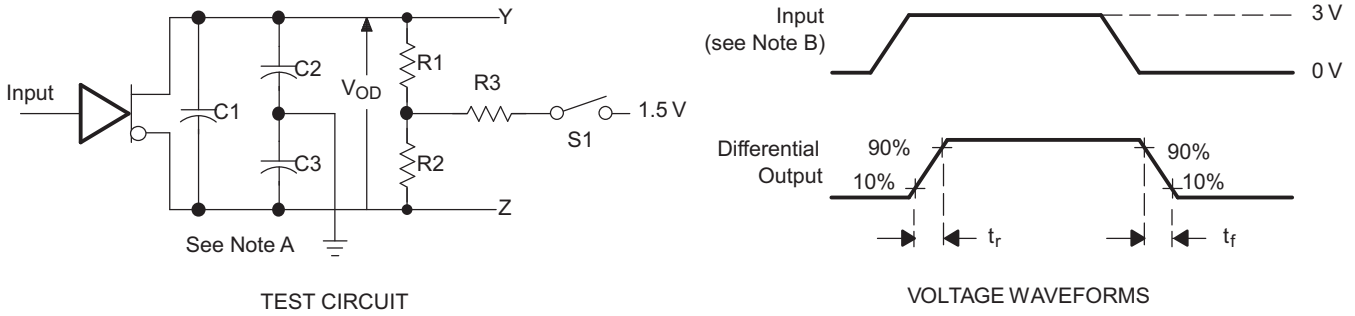


TEST CIRCUIT VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

Figure 2. Driver Test Circuit and Voltage Waveforms



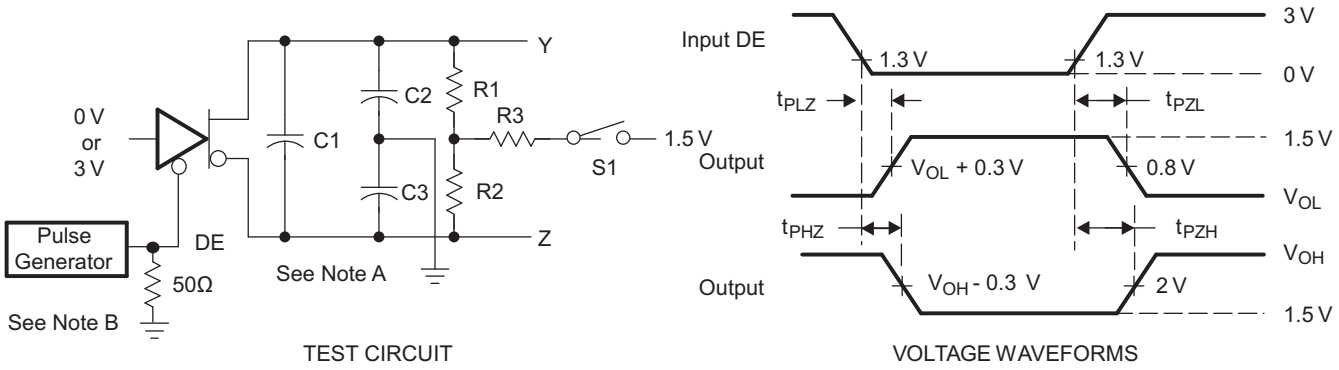
TEST CIRCUIT VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

Figure 3. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

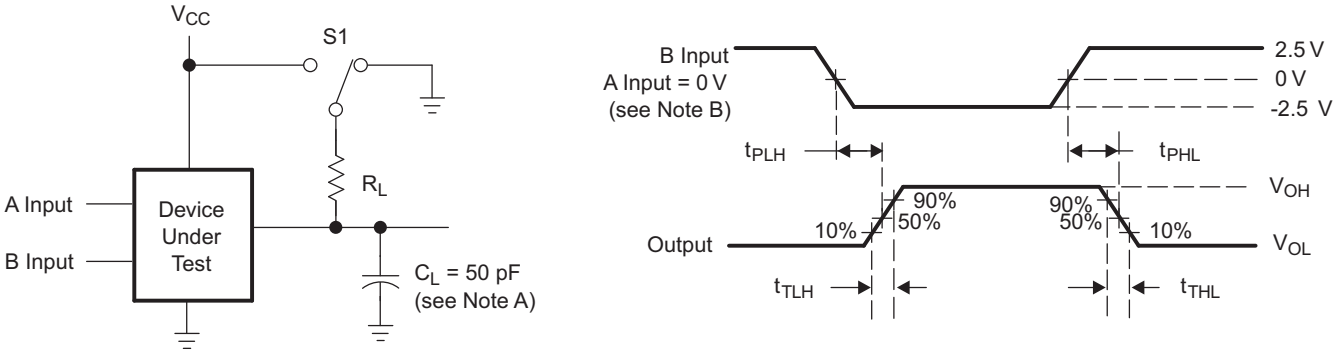


TEST CIRCUIT VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

Figure 4. Driver Test Circuit and Voltage Waveforms



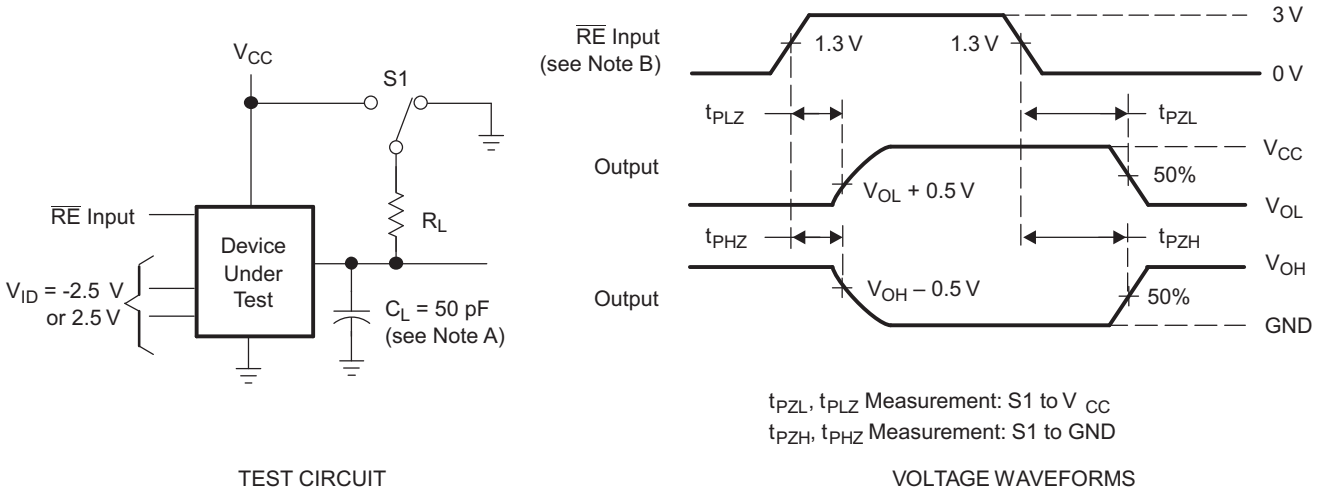
TEST CIRCUIT VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

Figure 5. Receiver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



TEST CIRCUIT VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

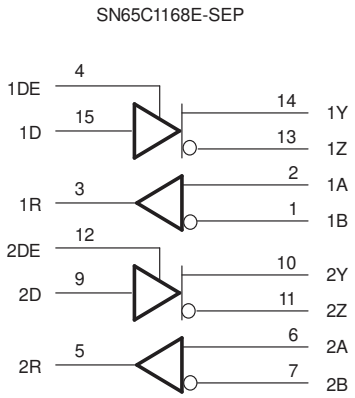
Figure 6. Receiver Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN65C1168E-SEP consist of dual drivers and dual receivers powered from a single 5-V supply. This device meets the requirements of TIA/EIA-422-B and ITU recommendation V.11.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Active High Driver Output Enables

SN65C1168E-SEP drivers can be configured individually by 1DE and 2DE logic inputs. Both drivers are set at high-impedance when disabled.

8.4 Device Functional Modes

Table 1 and Table 2 lists the functional modes of SN65C1168E-SEP.

Table 1. Each Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = High level, L = Low level, X = Irrelevant, Z = High impedance (off)

Table 2. Each Receiver(1)

DIFFERENTIAL INPUTS A–B	OUTPUT R
V_{ID} ≥ 0.2 V	H
–0.2 V < V_{ID} < 0.2 V	?
V_{ID} ≤ –0.2 V	L
Open	H

(1) H = High level, L = Low level, ? = Indeterminate

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 7 shows a typical RS-422 application. One transmitter is able to broadcast to multiple receiving nodes connected together over a shared differential bus. Twisted-pair cabling with a controlled differential impedance is used, and a termination resistance is placed at the farthest receive end of the cable in order to match the transmission line impedance and minimize signal reflections.

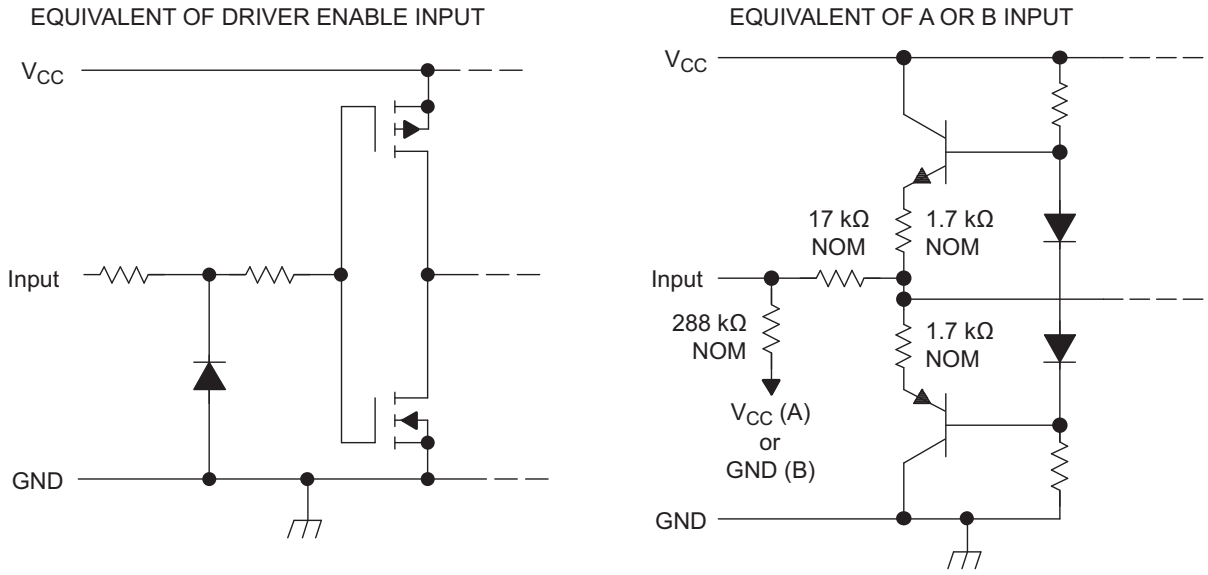


Figure 7. Schematic of Inputs

Application Information (continued)

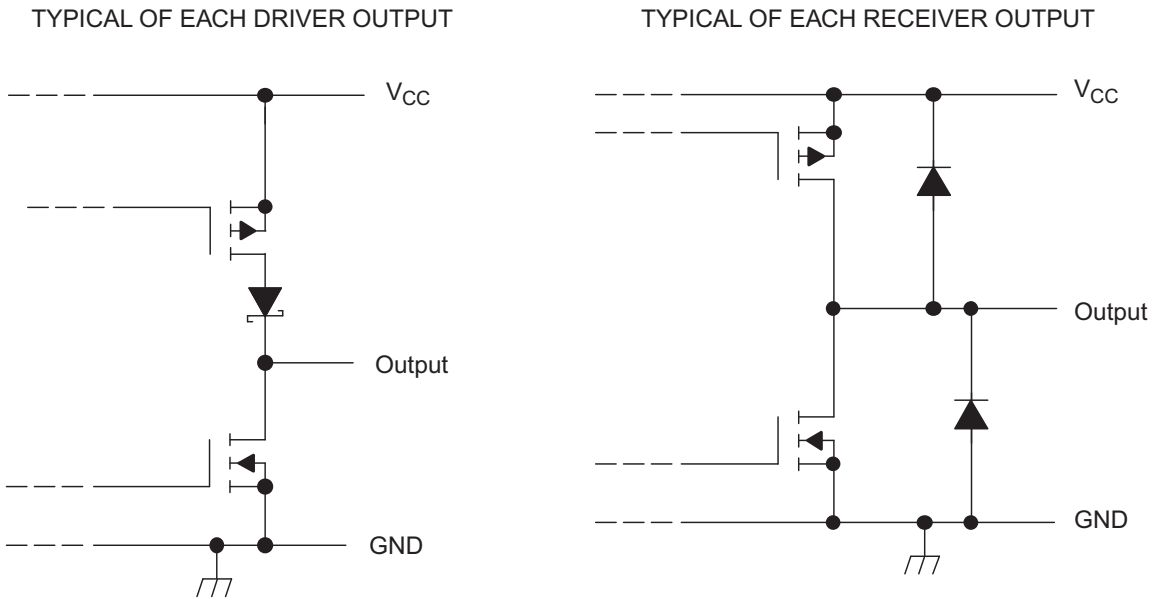


Figure 8. Schematic of Outputs

9.2 Typical Application

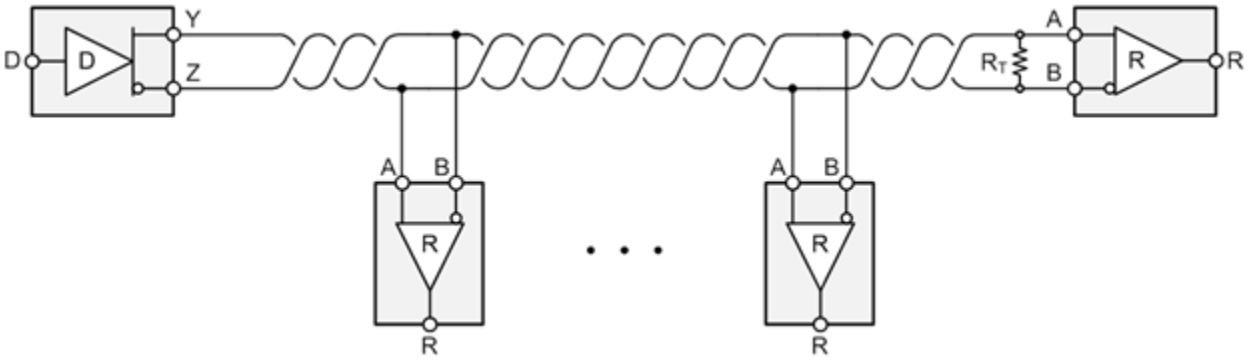


Figure 9. Typical RS-422 Application

9.2.1 Design Requirements

A typical RS-422 implementation using SN65C116xE requires the following:

- 5-V power source.
- Connector that ensures the correct polarity for port pins.
- Cabling that supports the desired operating rate and transmission distance.

9.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure ±200 mV on the A-B port when the driver circuit is disabled.

10 Power Supply Recommendations

Use a 5-V power supply for V_{CC} place 0.1-µF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high impedance power supplies.

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C1168EMPWSEP	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	1168SEP	Samples
SN65C1168EMPWTSEP	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	1168SEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

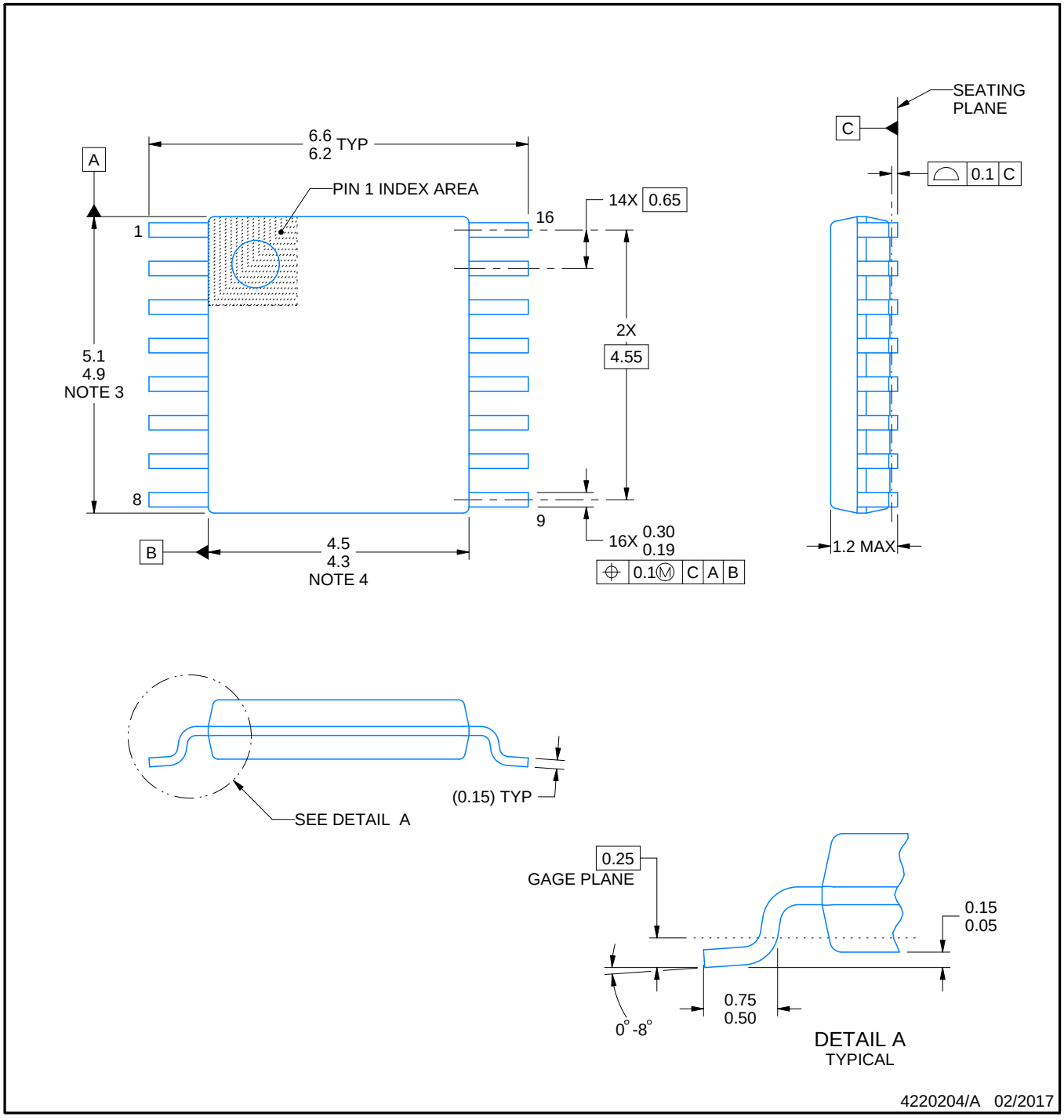
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PW0016A

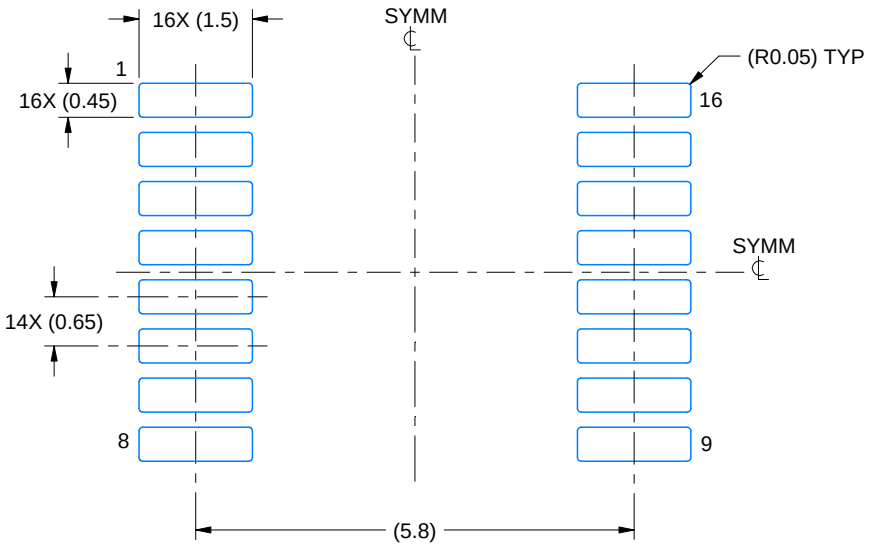
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

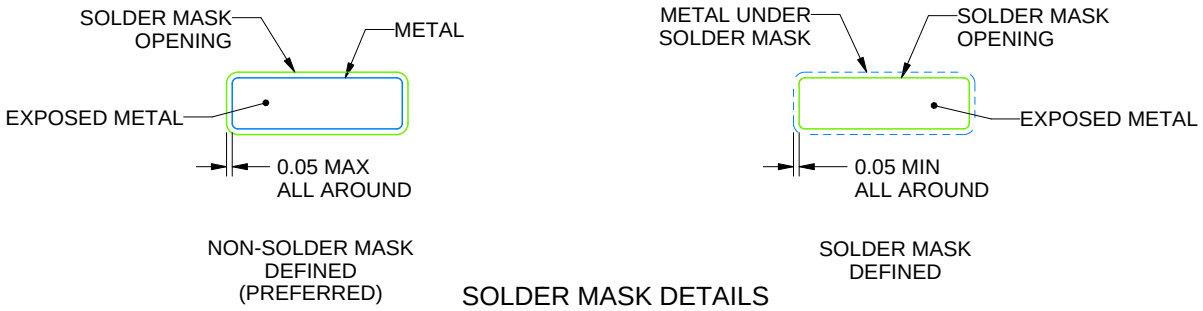


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

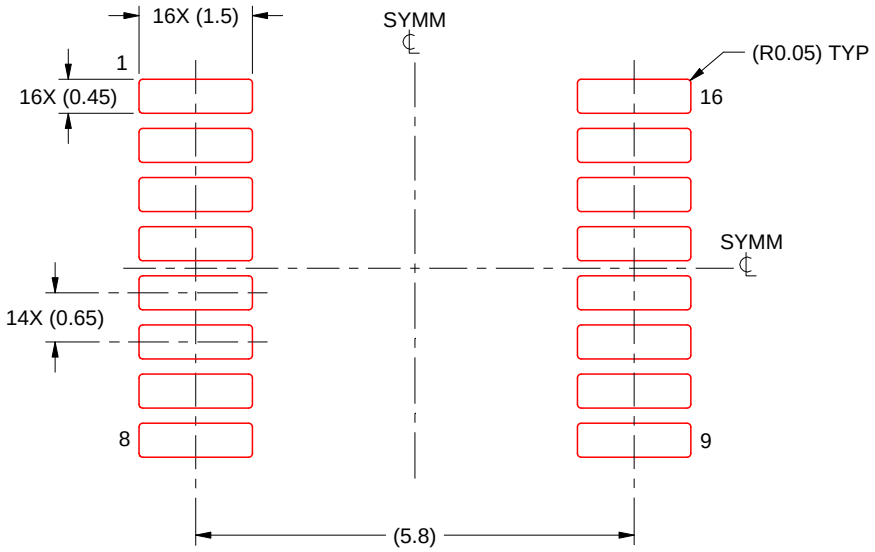


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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