

Description and Applications

The DML10M8LDS is a single channel load switch with very low on-resistance in a small package. It contains an N-channel MOSFET for up to V_{BIAS} -1.5V input voltage operation and 6A current channel with 3.2V to 5.5V bias supply. The load switch is controlled by a low voltage control signal through ON pin.

Applications

- Portable Electronics and Systems
- Notebook and Tablet Computers
- Telecom, Networking, Medical and Industrial Equipment
- Set-Top Boxes, Servers and Gateways
- SSD

Features and Benefits

- Low $R_{DS(ON)}$ – Ensures On State Losses are Minimized
- 0.8V to V_{BIAS} -1.5V Input Voltage Range
- 6A Continuous Current
- Low $R_{DS(ON)}$ Internal NFETs
 $8m\Omega$ at $V_{BIAS} = 5V$, $V_{IN} = 1.05V$, $T_A = +85^\circ C$
- 35 μA Low Quiescent Current
- 10 μs Turn On Rise Time
- 3.2V to 5.5V Bias Voltage
- Integrated Quick Output Discharge Resistor
- Moisture Sensitivity: Level 1 per J-STD-020
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.**
<https://www.diodes.com/quality/product-definitions/>

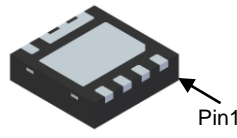
Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiPdAu Finish, Solderable per MIL-STD-202, Method 208@4
- Weight: 0.022 grams (Approximate)

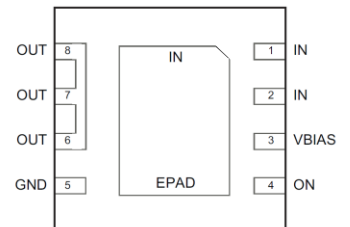
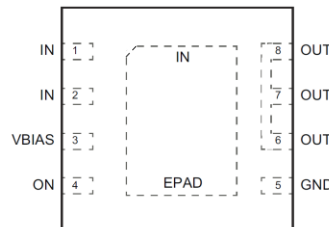
V-DFN3030-8 (Type R)



Top View



Bottom View



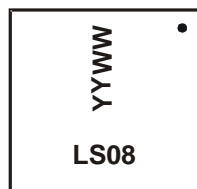
Ordering Information (Note 4)

Part Number	Case	Tape Width	Tape Pitch	Packaging
DML10M8LDS-7	V-DFN3030-8 (Type R)	8	4	3,000/Tape & Reel
DML10M8LDS-7A	V-DFN3030-8 (Type R)	12	8	1,500/Tape & Reel
DML10M8LDS-13	V-DFN3030-8 (Type R)	12	8	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

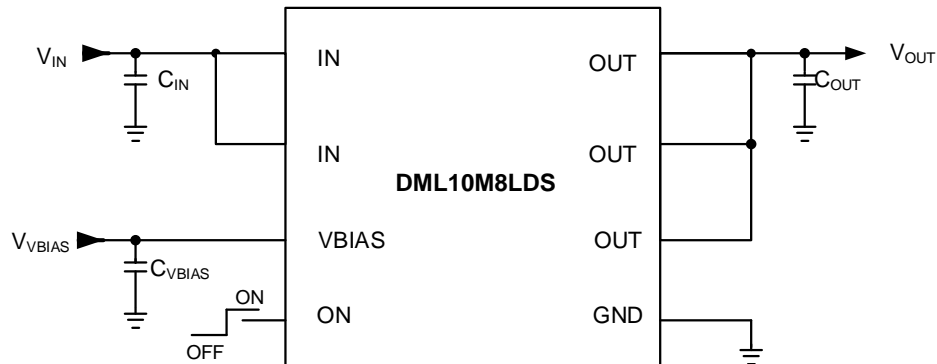
Marking Information

V-DFN3030-8 (Type R)



LS08 = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 20 = 2020)
WW = Week Code (01 to 53)

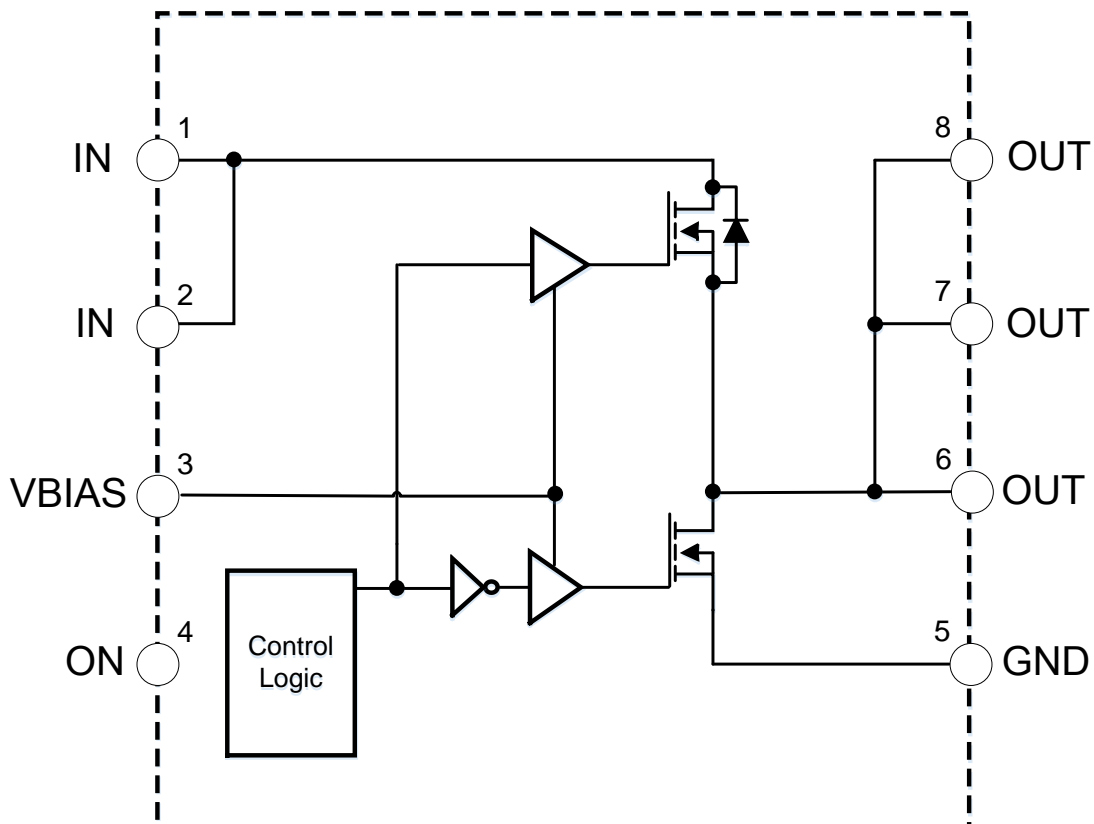
Typical Application Circuit



Pin Description

Pin Number	Pin Name	Pin Function
1, 2, EPAD	IN	Load switch input. Bypass capacitor is recommended to minimize input voltage dip.
3	VBIAS	Bias voltage. Power supply input for the device.
4	ON	Enable input. Load switch is on when ON is pulled high. Load switch is off when ON is pulled low. Do not leave floating.
5	GND	Ground.
6, 7, 8	OUT	Load switch output.

Functional Block Diagram



Absolute Maximum Rating

Parameter	Rating
Voltage from IN, ON, VBIAS, OUT to GND pin	-0.3V to 6V
Junction Temperature (T _J)	+150°C
I _{MAX}	12A
Storage Temperature (T _s)	-65°C to +150°C
ESD Rating HBM/CDM	2kV/1kV

Recommended Operating Ranges

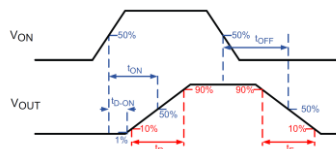
Parameter	Rating
Supply Voltage (V _{VBIAS})	3.2V to 5.5V
Input Voltage (V _{IN})	0.8V to V _{VBIAS} -1.5V
Ambient Temperature (T _A)	-40°C to +85°C
Package Thermal Resistance (θ _{JC})	8°C/W
Package Thermal Resistance (θ _{JA})	60°C/W

Electrical Characteristics (T_A = +25°C, V_{VBIAS} = 5V, V_{IN} = 1.05V, unless otherwise specified.)

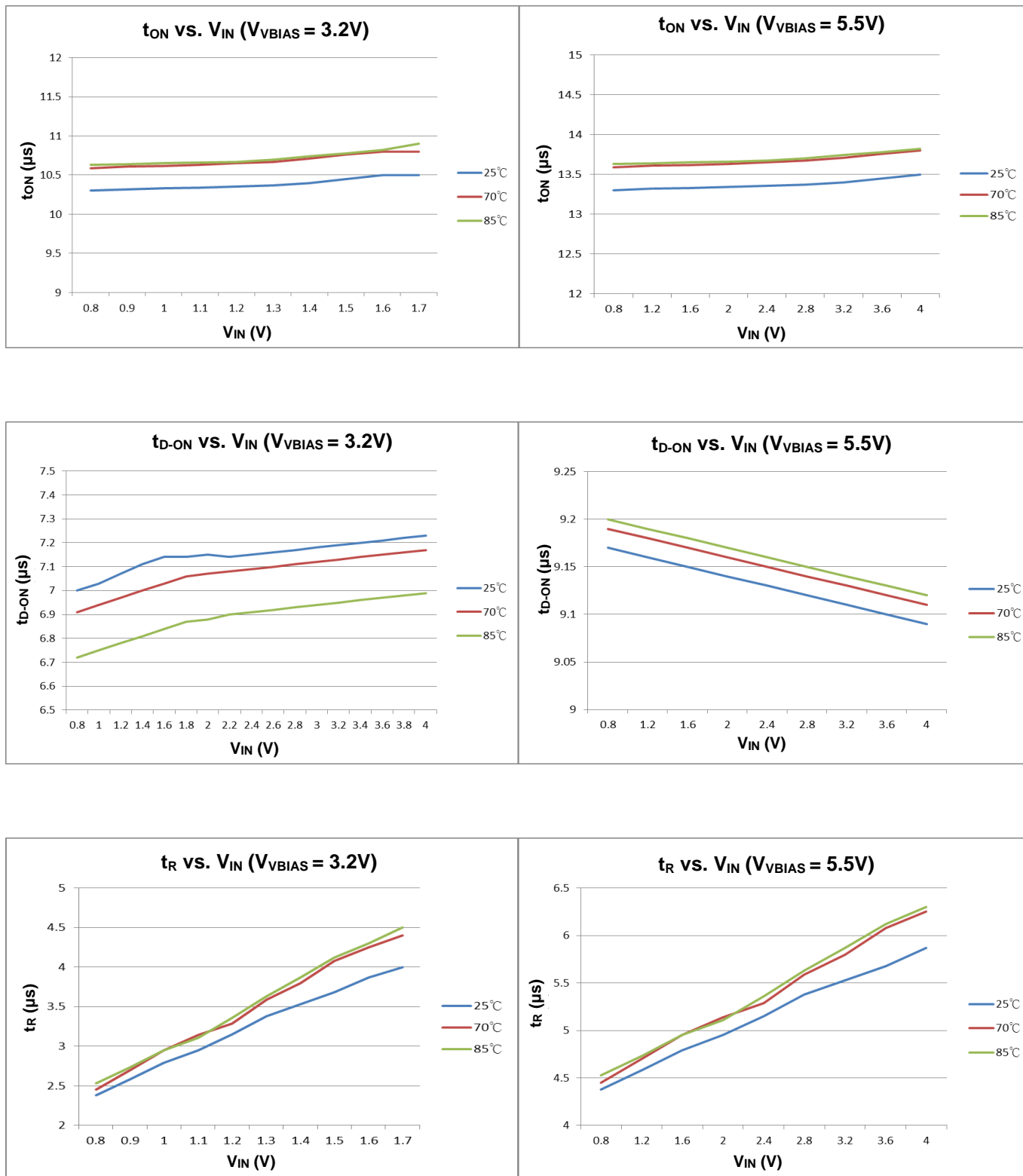
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IN}	In Supply Voltage	V _{ON} = 5V	0.8	1.05	V _{VBIAS} - 1.5	V
V _{VBIAS}	VBIAS Supply Voltage	—	3.2	5	5.5	V
I _D	Maximum Continuous Current	V _{ON} = 5V	—	6	—	A
I _{PLS}	Maximum Pulsed Switch Current	V _{IN} = V _{ON} = 5V Pulse < 300μs, 2% Duty Cycle	—	9	—	A
I _Q	Quiescent Supply Current of VBIAS	I _{OUT} = 0V, V _{ON} = 5V	—	35	—	μA
I _{OFF}	VBIAS Shutdown Supply Current	V _{ON} = 0V, V _{OUT} = 0V	—	—	2	μA
I _{INOFF}	IN Shutdown Supply Current	V _{ON} = 0V, V _{OUT} = 0V	—	—	2	μA
I _{ON}	On Leakage Current	V _{ON} = 5V	—	—	1	μA
V _{ONH}	On High Level Voltage	—	1.2	—	—	V
V _{ONL}	On Low Level Voltage	—	—	—	0.5	V
Switching On Resistance						
R _{ON}	Switch On-State Resistance	I _{OUT} = -200mA, V _{ON} = 5V, V _{VBIAS} = 5V	—	—	8	mΩ
		I _{OUT} = -200mA, V _{ON} = 5V, V _{VBIAS} = 3.3V	—	—	10	mΩ
R _{PD}	Output Pull-Down Resistance	I _{OUT} = 15mA, V _{ON} = 0V	—	—	200	Ω

Switching Electrical Characteristics (T_A = +25°C, V_{VBIAS} = V_{ON} = 5V, V_{IN} = 1.05V, C_{IN} = 1μF, C_{OUT} = 0.1μF, unless otherwise specified.)

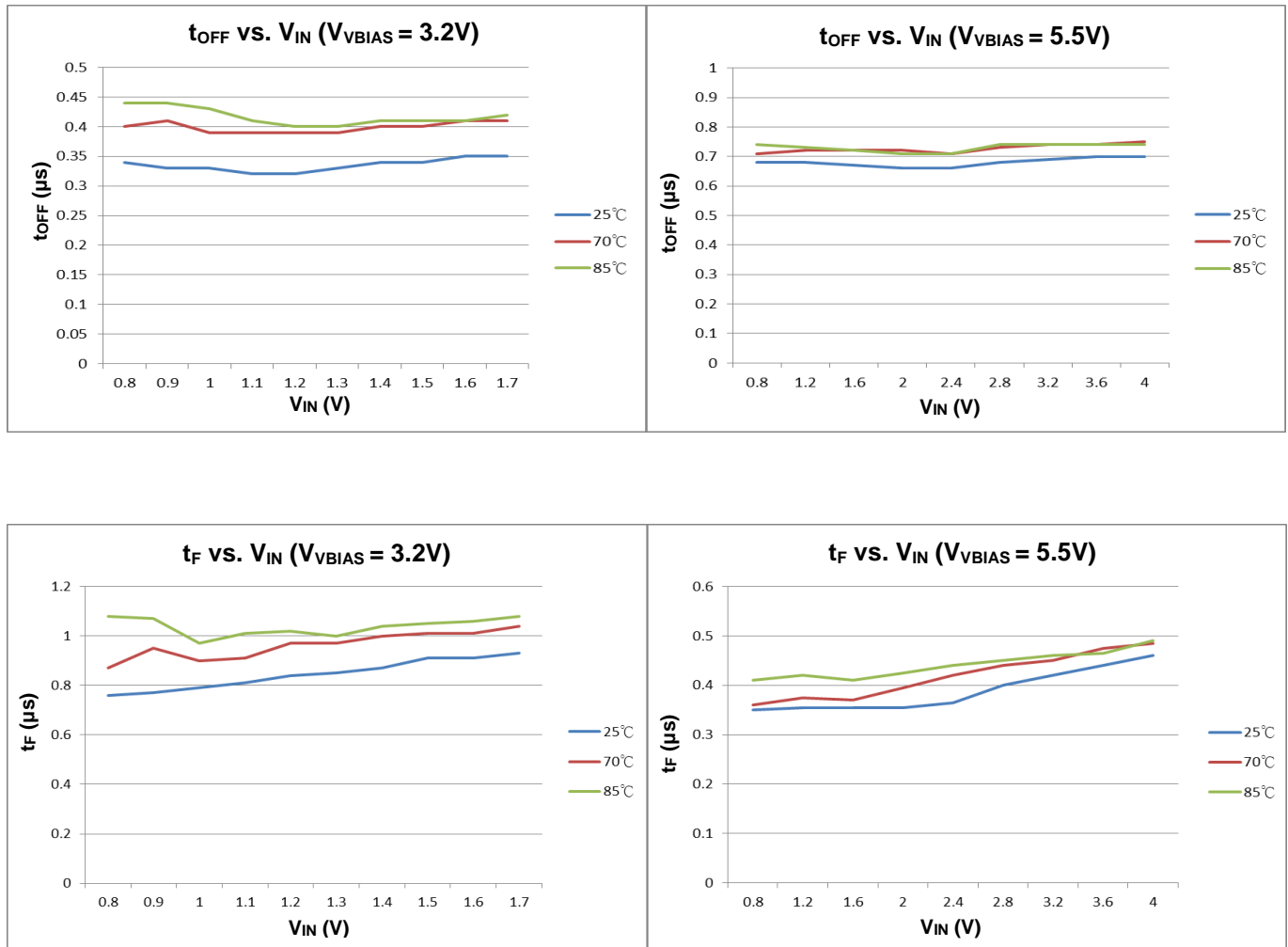
Symbol	Parameter	Min	Typ	Max	Unit
VIN = 1.5V, VVBIAS = VON = 5V					
tON	Turn-On Time	10	—	65	μs
tD-ON	Turn-On Delay Time	7.5	—	45	
tR	Turn-On Rise Time	5	—	33	
tOFF	Turn-Off Time	—	0.2	—	
tF	Turn-Off Fall Time	—	0.7	—	
VIN = 1.05V, VVBIAS = VON = 5V					
tON	Turn-On Time	10	—	65	μs
tD-ON	Turn-On Delay time	7.5	—	45	
tR	Turn-On Rise Time	5	—	33	
tOFF	Turn-Off Time	—	0.2	—	
tF	Turn-Off Fall Time	—	0.7	—	



Performance Characteristics (@T_A = +25°C, unless otherwise specified.)



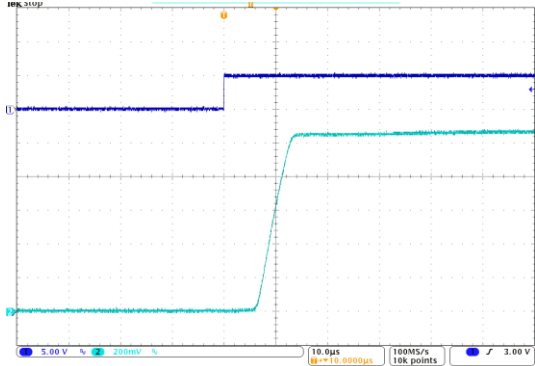
Performance Characteristics (@T_A = +25°C, unless otherwise specified. continued)



Performance Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified. continued)

Turn-On & Turn-On Rise Time

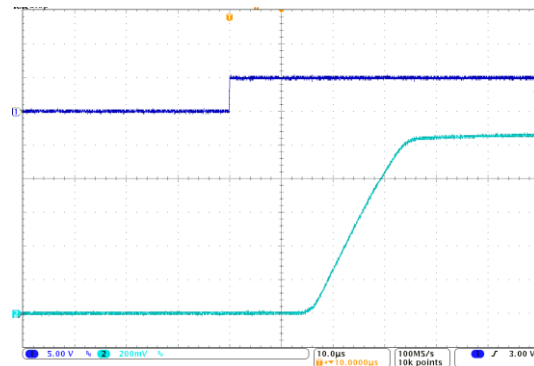
$V_{IN} = 1.05\text{V}$, $V_{BIAS} = 5\text{V}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 0.1\mu\text{F}$,
 $R_{OUT} = 10\Omega$



V_{ON}
(5V/div)
 V_{OUT}
(200mV/div)

Turn-On & Turn-On Rise Time

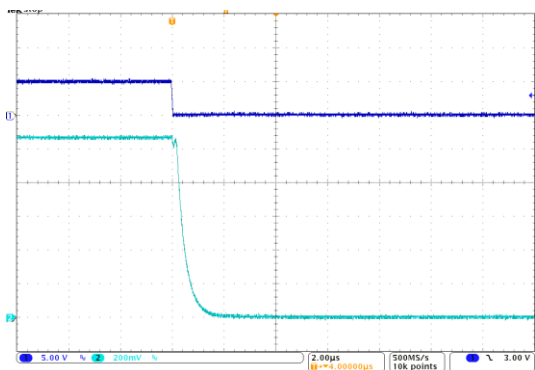
$V_{IN} = 1.05\text{V}$, $V_{BIAS} = 3.2\text{V}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 0.1\mu\text{F}$,
 $R_{OUT} = 10\Omega$



V_{ON}
(5V/div)
 V_{OUT}
(200mV/div)

Turn-Off & Turn-Off Fall Time

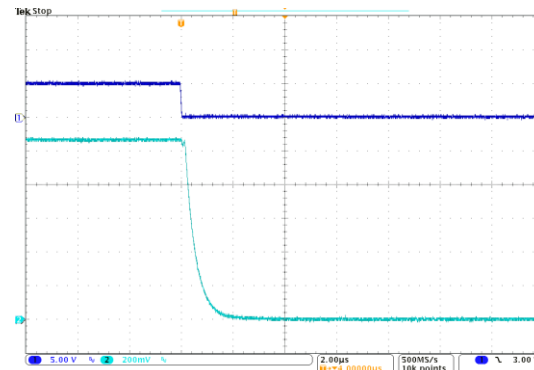
$V_{IN} = 1.05\text{V}$, $V_{BIAS} = 5\text{V}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 0.1\mu\text{F}$,
 $R_{OUT} = 10\Omega$



V_{ON}
(5V/div)
 V_{OUT}
(200mV/div)

Turn-Off & Turn-Off Fall Time

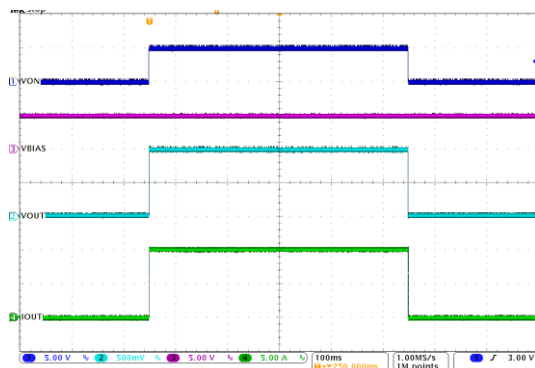
$V_{IN} = 1.05\text{V}$, $V_{BIAS} = 3.2\text{V}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 0.1\mu\text{F}$,
 $R_{OUT} = 10\Omega$



V_{ON}
(5V/div)
 V_{OUT}
(200mV/div)

Turn-On & Turn-Off at $I_{OUT} = -10\text{A}$

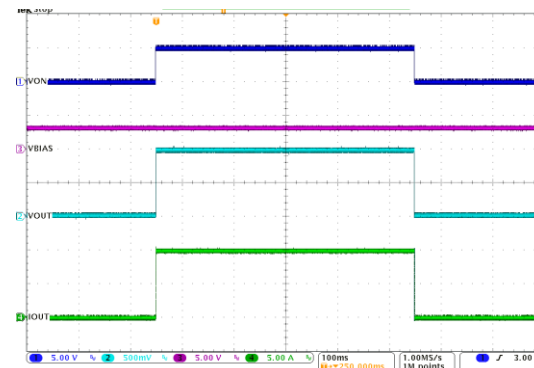
$V_{IN} = 1.05\text{V}$, $V_{BIAS} = 5\text{V}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 0.1\mu\text{F}$,
 $R_{OUT} = 0.1\Omega$



V_{ON}
(5V/div)
 V_{BIAS}
(5V/div)
 V_{OUT}
(500mV/div)
 I_{OUT}
(5A/div)

Turn-On & Turn-Off at $I_{OUT} = -10\text{A}$

$V_{IN} = 1.05\text{V}$, $V_{BIAS} = 3.2\text{V}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 0.1\mu\text{F}$,
 $R_{OUT} = 0.1\Omega$



V_{ON}
(5V/div)
 V_{BIAS}
(5V/div)
 V_{OUT}
(500mV/div)
 I_{OUT}
(5A/div)

Application Information

General Description

The DML10M8LDS is a single channel, 6A load switch in an 8-pin V-DFN3030-8 (Type R) package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET which can be operated input voltage range from 0.8V to 3.5V.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply and discharge FET eliminates the needs for any external components, which reduce solution size and bill of materials (BOM) count.

Enable Control

The DML10M8LDS device allows for enabling the MOSFET in an active-high configuration. When the VBIAS supply pin has an adequate voltage applied and the ON pin is at logic high level, the MOSFET will be enabled. Similarly, when the ON pin is at logic low level, the MOSFET will be disable.

Power Sequencing

The DML10M8LDS device will function with any power sequence, but the output turn-on delay performance may vary from what is specified. To archives the specified performance, there are two recommended power sequences:

- 1.) $V_{BIAS} \rightarrow V_{IN} \rightarrow V_{ON}$
- 2.) $V_{IN} \rightarrow V_{BIAS} \rightarrow V_{ON}$

Input Capacitor

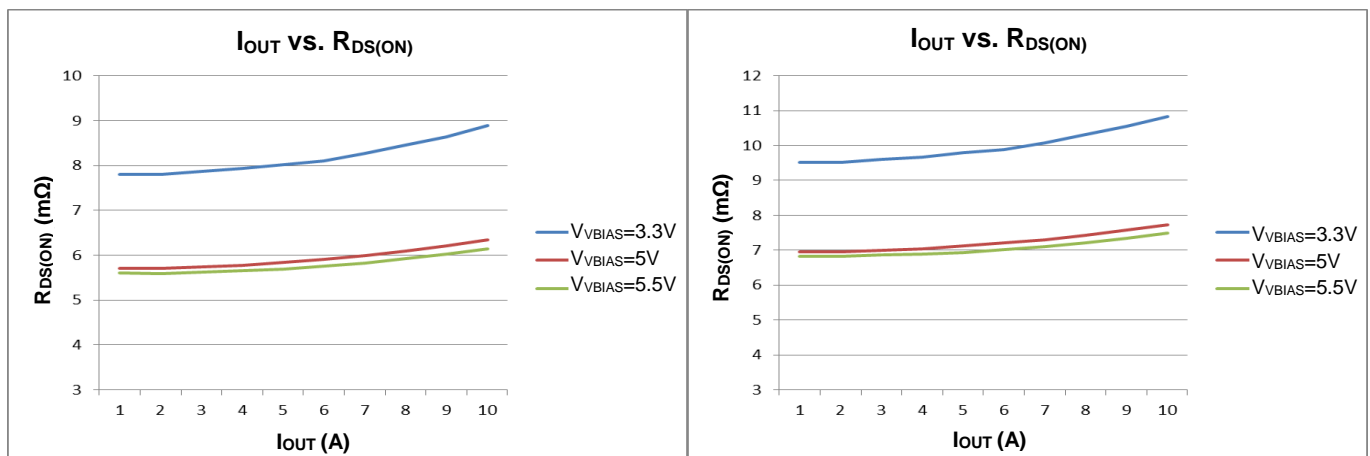
A capacitor of 10 μ F or higher value is recommended to be placed close to the IN pins of DML10M8LDS. This capacitor can reduce the voltage drop caused by the in-rush current during the turn-on transient of the load switch. A higher value capacitor can be used to further reduce the voltage drop during high-current application.

Output Capacitor

A capacitor of 0.1 μ F or higher value is recommended to be placed between the OUT pins and GND pin. The switching times are affected by the capacitance. A larger capacitor makes the initial turn-on transient smoother. This capacitor must be large enough to supply a fast transient load in order to prevent the output from dropping.

V_{IN} and V_{BIAS} Voltage Range

For optimal on-resistance of load switch, make sure $V_{IN} \leq 1.5V + V_{BIAS}$ and V_{BIAS} is within the voltage range from 3.2V to 5.5V. On-resistance of load switch will be higher if $V_{IN} + 1.5V > V_{BIAS}$. Resistance curves of a typical sample device at different $V_{BIAS} = V_{IN}$ at $I_{OUT} = -200mA$ are shown as below.



Application Information (continued)

Thermal Considerations

To ensure proper operation, the maximum junction temperature of the DML10M8LDS should not exceed +150°C. Several factors attribute to the junction temperature rise: load current, MOSFET on-resistance, junction-to-ambient thermal resistance, and ambient temperature. The maximum load current can be determined by:

$$I_{LOAD(MAX)} = \sqrt{\frac{T_{J(MAX)} - T_C}{\theta_{JC} \times R_{DS(ON)}}$$

Where

$I_{LOAD(MAX)}$ is the maximum allowable current on load (A). (6A for DML10M8LDS)

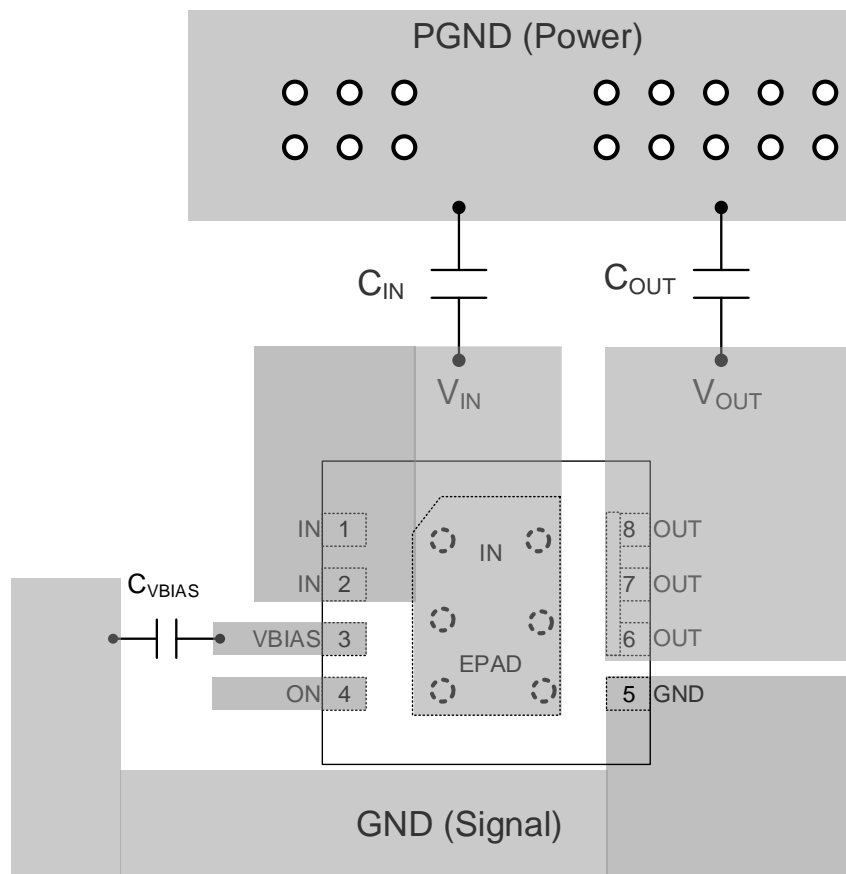
$T_{J(MAX)}$ is the maximum allowable junction temperature.

T_C is the case temperature of the device.

θ_{JC} = junction to case thermal impedance. This parameter is highly dependent upon PCB layout.

PCB Layout Consideration

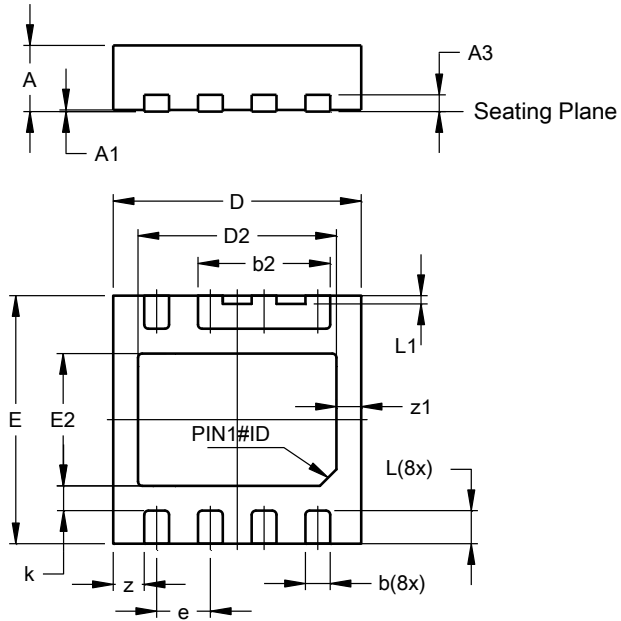
1. Place the input/output capacitors C_{IN} and C_{OUT} as close as possible to the IN and OUT pins.
2. The power traces which are IN trace, OUT trace and GND trace. They should be short, wide and directly for minimize parasitic inductance.
3. Place C_{VBIAS} capacitor near the device pin.
4. Connect the signal ground to the GND pin, and keep a single connection from GND pin to the power ground behind the input or output capacitors.
5. For better power dissipation, holes are recommended to connect to the exposed pad's landing area with a large copper polygon on the other side of the printed circuit board. The copper polygons and exposed pad shall connect to IN pin on the printed circuit board.



Package Outline Dimensions (All dimensions in mm.)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-DFN3030-8 (Type R)

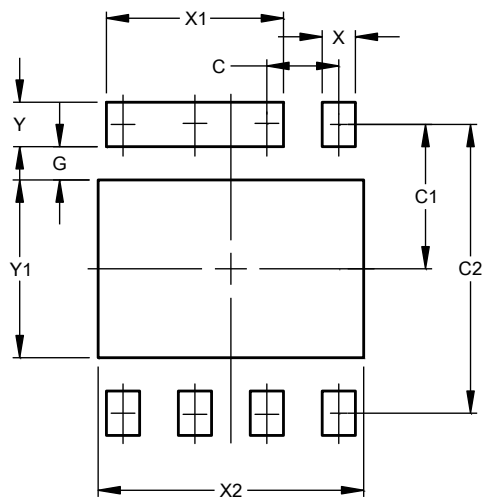


V-DFN3030-8 (Type R)			
Dim	Min	Max	Typ
A	0.77	0.83	0.80
A1	0.00	0.05	0.03
A3	--	--	0.203
b	0.25	0.35	0.30
b2	1.55	1.65	1.60
D	2.95	3.05	3.00
D2	2.30	2.50	2.40
E	2.95	3.05	3.00
E2	1.50	1.70	1.60
e	0.65 BSC		
k	--	--	0.30
L	0.35	0.45	0.40
L1	0.05	0.15	0.10
z	--	--	0.375
z1	--	--	0.30
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

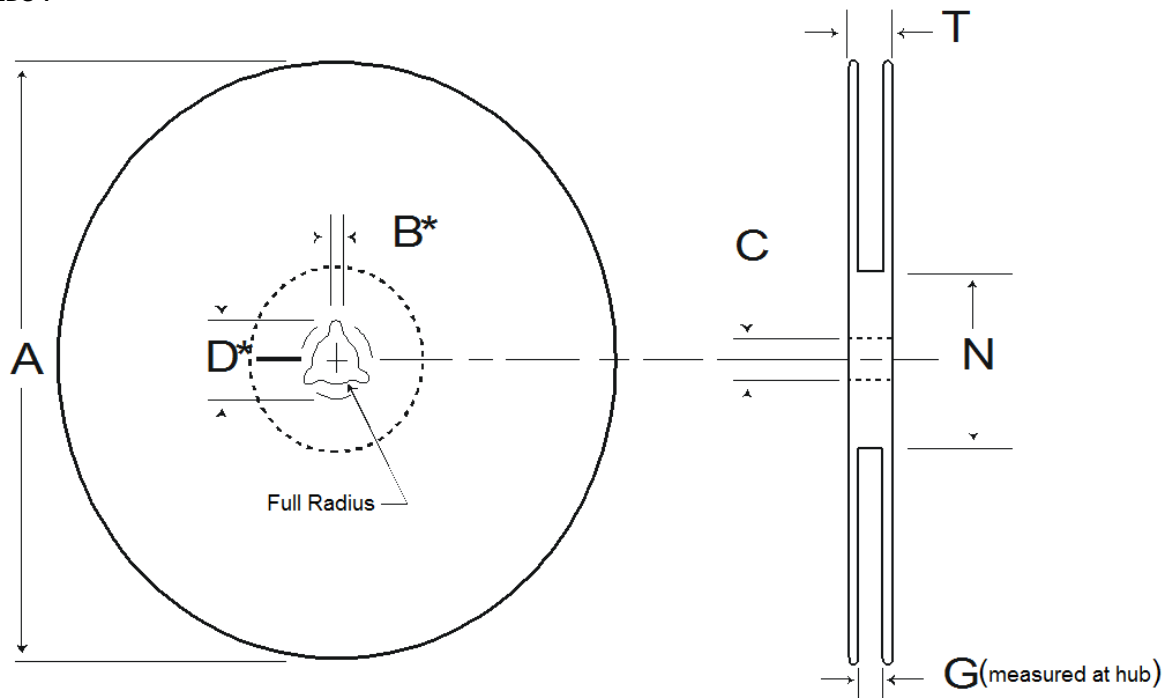
V-DFN3030-8 (Type R)



Dimensions	Value (in mm)
C	0.65
C1	1.30
C2	2.60
G	0.30
X	0.30
X1	1.60
X2	2.40
Y	0.40
Y1	1.60

Surface Mount Reel Specifications

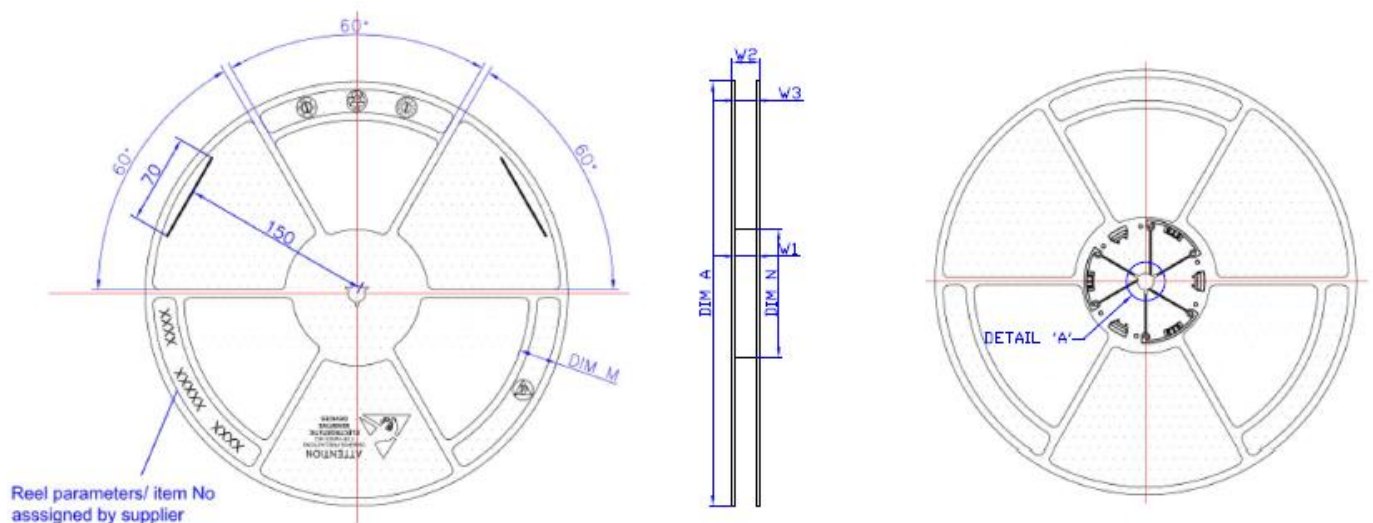
DML1008LDS-7



* Drive spokes optional. If used, dimensions with asterisks apply

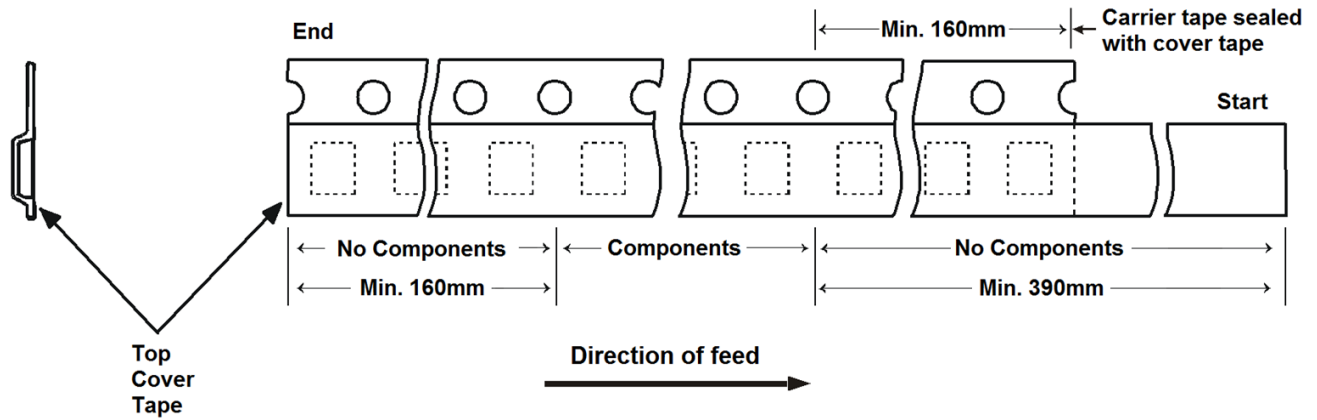
Tape Width	Reel Size	A (mm)	B Max (mm)	C (mm)	D Max (mm)	N Min (mm)	G (mm)	T Max (mm)
8mm	7"	178 ±2	2.0 +0.5 -0	13 +0.5 -0.2	20.5 ±0.2	55 ±5	8.4 +1.5 -0.0	14.4

DML1008LDS-13



Tape Width	Reel Size	DIM A (mm)	W1 (mm)	W2 (mm)	W3 (mm)	DIM N (mm)	DIM M (mm)
12mm	13"	330 ±2	12.4 +2 -0	18.4MAX.	11.9~15.4	100 ±2	65

Tape Leader and Trailer Specifications (Notes 5 and 6)



- Notes:**
5. There shall be a leader of at least 230mm which may consist of carrier tape and/or cover tape or a start tape followed by at least 160mm of empty carrier tape sealed with cover tape.
 6. There shall be a trailer of at least 160mm of empty carrier tape sealed with cover tape. The entire carrier tape must release from the reel hub as the last portion of the tape unwinds from the reel without damage to the carrier tape and the remaining components in the cavities.

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