

## Description

The DML1012LDS is a single channel load switch with very low on-resistance in a small package. It contains an N-channel MOSFET for up to  $V_{BIAS} - 1.5V$  input voltage operation and 6A current channel with 3.2V to 5.5V bias supply. The load switch is controlled by a low voltage control signal through ON pin.

## Applications

- Portable Electronics and Systems
- Notebook and Tablet Computers
- Telecom, Networking, Medical, and Industrial Equipment
- Set-Top Boxes, Servers, and Gateways
- SSD

## Features and Benefits

- Low  $R_{DS(ON)}$  – Ensures On State Losses Are Minimized
- 0.8V to  $V_{BIAS} - 1.5V$  Input Voltage Range
- 6A Continuous Current
- Low  $R_{DS(ON)}$  Internal NFETs  
8m $\Omega$  at  $V_{BIAS} = 5V$ ,  $V_{IN} = 1.05V$ ,  $T_A = +85^\circ C$
- 28 $\mu A$  Low Quiescent Current
- 10 $\mu s$  Turn On Rise Time
- 3.2V to 5.5V Bias Voltage
- Integrated Quick Output Discharge Resistor
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/contact-us) or your local Diodes representative.**  
<https://www.diodes.com/quality/product-definitions/>

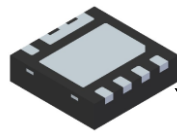
## Mechanical Data

- Case: V-DFN3030-8
- Case Material: Molded Plastic, "Green" Molding Compound.  
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish — NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 <sup>(e4)</sup>
- Weight: 0.022 grams (Approximate)

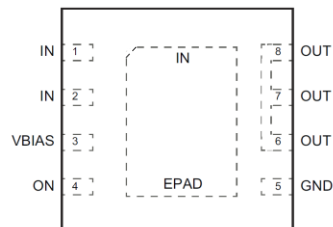
V-DFN3030-8 (Type R)



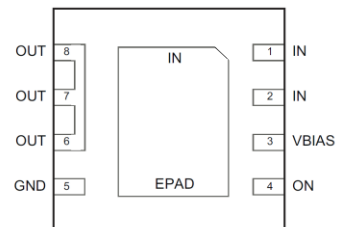
Top View



Bottom View



Top View



Bottom View

## Ordering Information (Note 4)

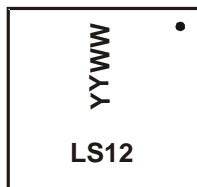
Part Number	Case	Tape Width	Tape Pitch	Packaging
DML1012LDS-7A	V-DFN3030-8 (Type R)	12mm	8mm	1500/Tape & Reel
DML1012LDS-13	V-DFN3030-8 (Type R)	12mm	8mm	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information

Site 1

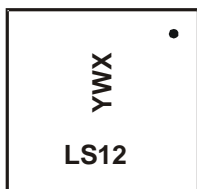
V-DFN3030-8 (Type R)



LS12 = Product Type Marking Code  
YYWW = Date Code Marking  
YY = Last Two Digits of Year (ex: 20 = 2020)  
WW = Week Code (01 to 53)

Site 2

V-DFN3030-8 (Type R)



LS12 = Product Type Marking Code  
YWX = Date Code Marking  
Y = Year (ex: 0 = 2020)  
W = Week (ex: a = Week 27; z Represents Week 52 and 53)  
X = Internal Code (ex: U = Monday)

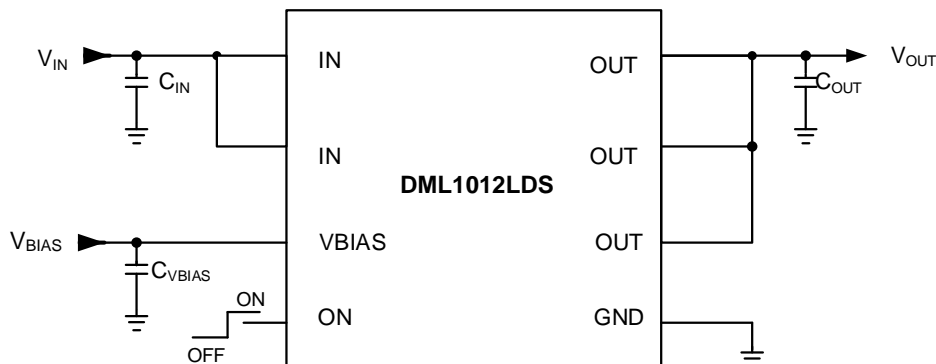
### Date Code Key

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	9	0	1	2	3	4	5	6	7	8	9	0

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

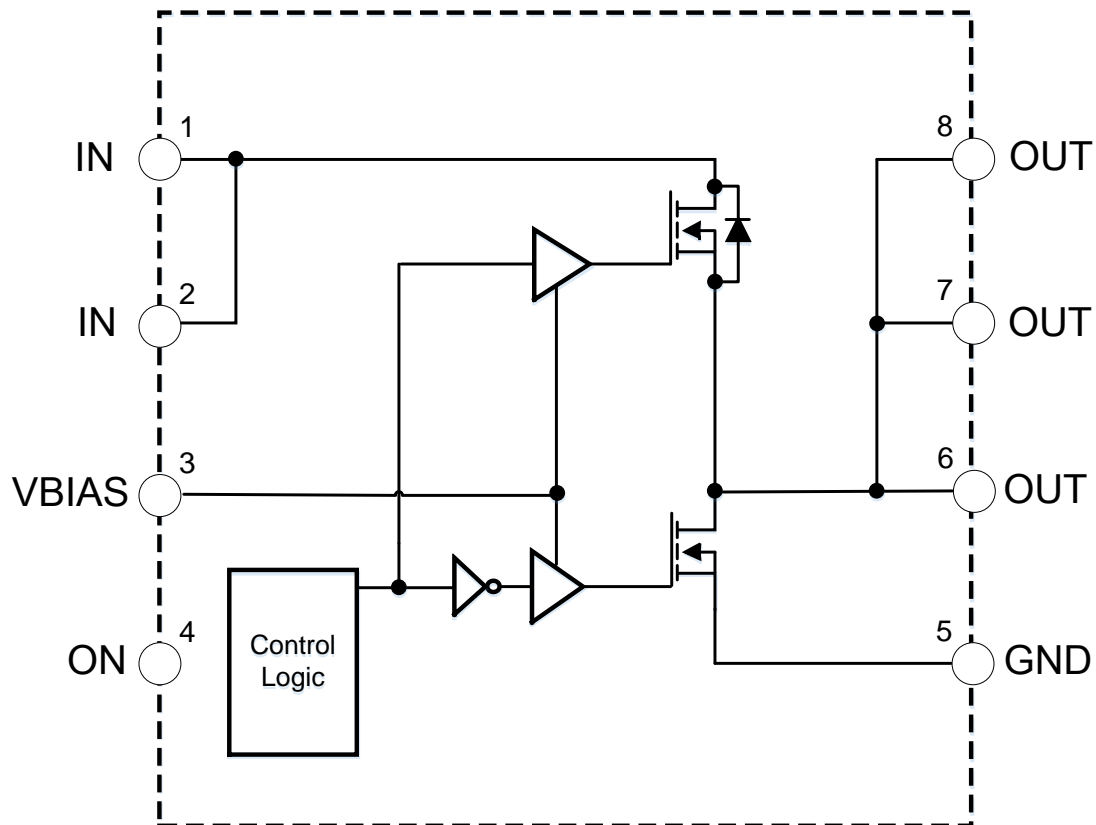
## Typical Application Circuit



## Pin Description

Pin Number	Pin Name	Pin Function
1, 2, EPAD	IN	Load Switch Input. Bypass capacitor is recommended to minimize input voltage dip.
3	VBIAS	Bias Voltage. Power supply input for the device.
4	ON	Enable Input. Load switch is on when ON is pulled high. Load switch is off when ON is pulled low. Do not leave floating.
5	GND	Ground.
6, 7, 8	OUT	Load switch output.

## Functional Block Diagram



## Absolute Maximum Rating

Parameter	Rating
Voltage from IN, ON, VBIAS, OUT to GND Pin	-0.3V to 6V
Junction Temperature (T <sub>J</sub> )	+150°C
I <sub>MAX</sub>	12A
Storage Temperature (T <sub>STG</sub> )	-65°C to +150°C
ESD Rating HBM/CDM	2kV/1kV

## Recommended Operating Ranges

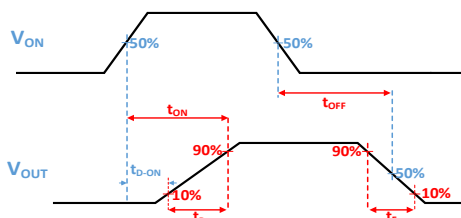
Parameter	Rating
Supply Voltage (V <sub>BIAS</sub> )	3.2V to 5.5V
Input Voltage (V <sub>IN</sub> )	0.8V to V <sub>BIAS</sub> - 1.5V
Ambient Temperature (T <sub>A</sub> )	-40°C to +85°C
Package Thermal Resistance (θ <sub>JC</sub> )	8°C/W
Package Thermal Resistance (θ <sub>JA</sub> )	60°C/W

## Electrical Characteristics (T<sub>A</sub> = +25°C, V<sub>BIAS</sub> = 5V, V<sub>IN</sub> = 1.05V, unless otherwise specified.)

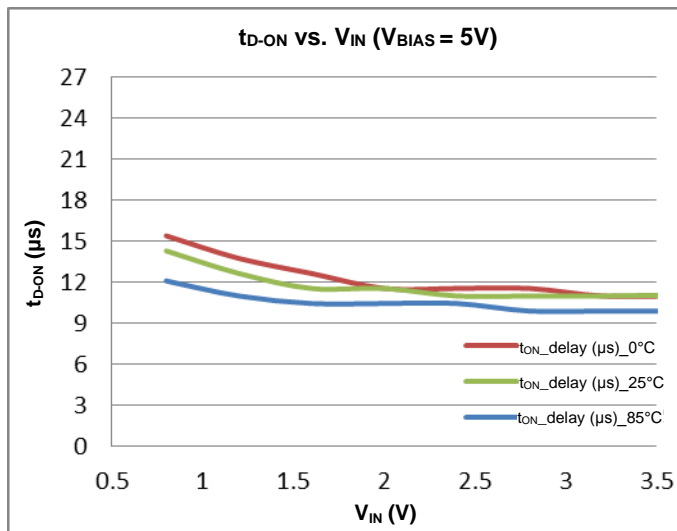
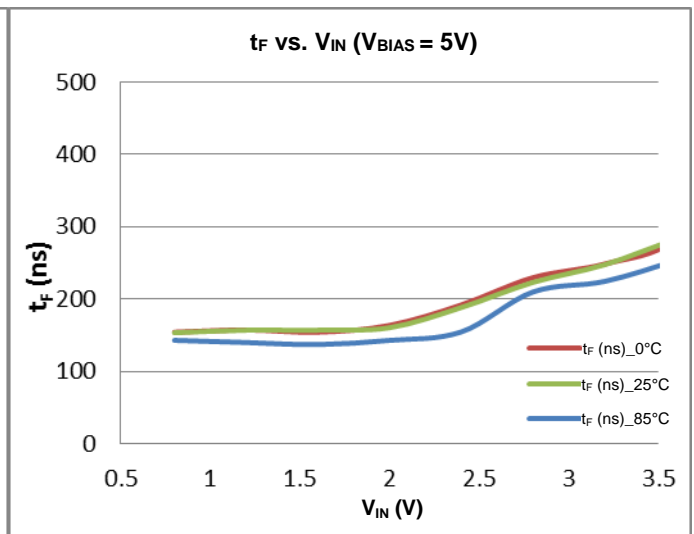
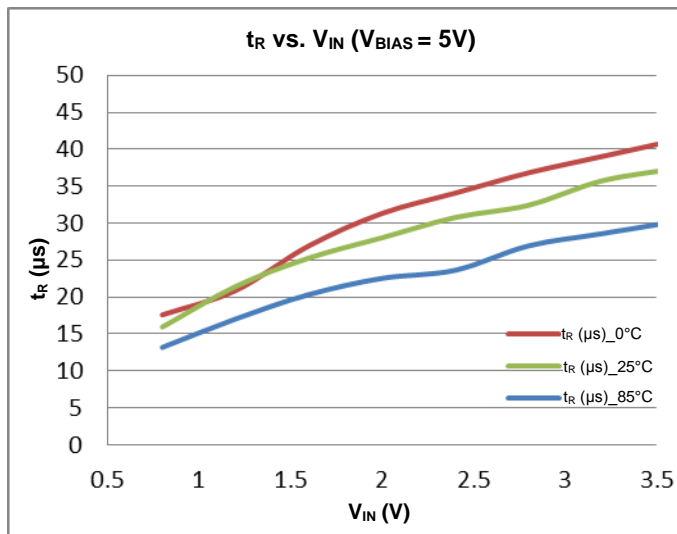
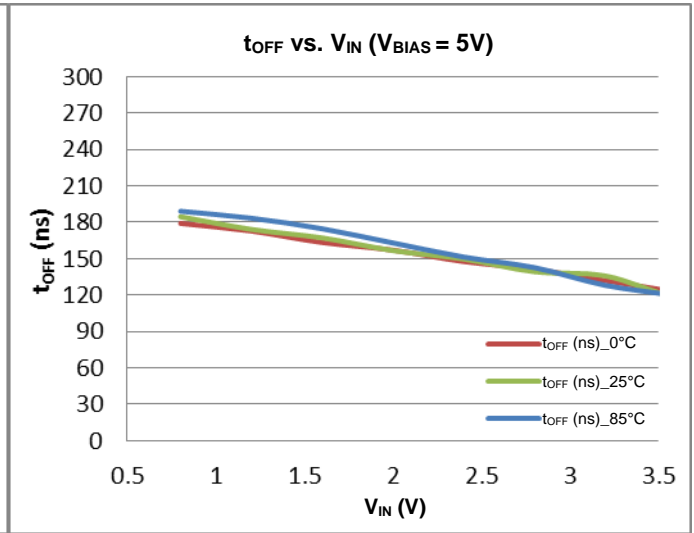
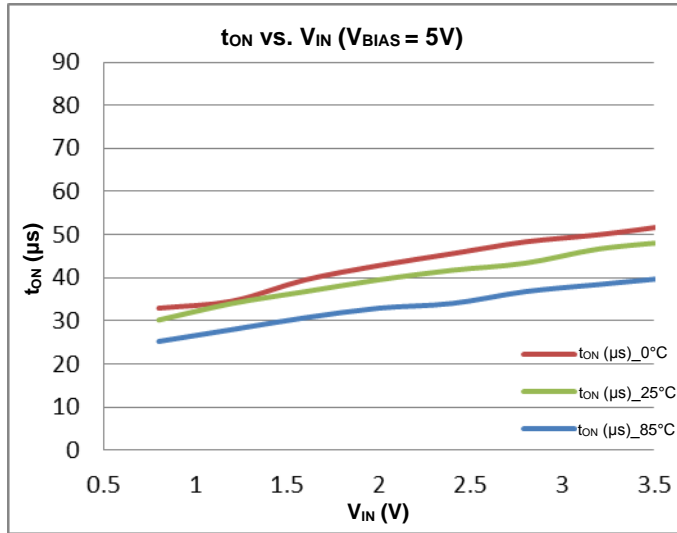
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IN</sub>	IN Supply Voltage	V <sub>ON</sub> = 5V	0.8	1.05	V <sub>BIAS</sub> - 1.5	V
V <sub>BIAS</sub>	VBIAS Supply Voltage	—	3.2	5	5.5	V
I <sub>D</sub>	Maximum Continuous Current	V <sub>ON</sub> = 5V	—	6	—	A
I <sub>PLS</sub>	Maximum Pulsed Switch Current	V <sub>IN</sub> = V <sub>ON</sub> = 5V Pulse < 300μs, 2% Duty Cycle	—	9	—	A
I <sub>Q</sub>	Quiescent Supply Current of VBIAS	I <sub>OUT</sub> = 0V, V <sub>ON</sub> = 5V	—	28	—	μA
I <sub>OFF</sub>	VBIAS Shutdown Supply Current	V <sub>ON</sub> = 0V, V <sub>OUT</sub> = 0V	—	—	2	μA
I <sub>INOFF</sub>	IN Shutdown Supply Current	V <sub>ON</sub> = 0V, V <sub>OUT</sub> = 0V	—	—	2	μA
I <sub>ON</sub>	ON Leakage Current	V <sub>ON</sub> = 5V	—	—	1	μA
V <sub>ONH</sub>	ON High Level Voltage	—	1.2	—	—	V
V <sub>ONL</sub>	ON Low Level Voltage	—	—	—	0.5	V
<b>Switching ON Resistance</b>						
R <sub>ON</sub>	Switch ON-State Resistance	I <sub>OUT</sub> = -200mA, V <sub>ON</sub> = 5V, V <sub>BIAS</sub> = 5V	—	—	8	mΩ
		I <sub>OUT</sub> = -200mA, V <sub>ON</sub> = 5V, V <sub>BIAS</sub> = 3.3V	—	—	10	mΩ
R <sub>PD</sub>	Output Pull-Down Resistance	I <sub>OUT</sub> = 15mA, V <sub>ON</sub> = 0V	—	—	200	Ω

## Switching Electrical Characteristics (T<sub>A</sub> = +25°C, V<sub>BIAS</sub> = V<sub>ON</sub> = 5V, C<sub>IN</sub> = 1μF, C<sub>OUT</sub> = 0.1μF, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
VIN = 1.5V, VBIAS = VON = 5V					
tON	Turn-On Time	15	—	55	μs
tD-ON	Turn-On Delay Time	5	—	30	
tR	Turn-On Rise Time	10	—	25	
tOFF	Turn-Off Time	—	0.2	—	
tF	Turn-Off Fall Time	—	0.7	—	
VIN = 1.05V, VBIAS = VON = 5V					
tON	Turn-On Time	15	—	55	μs
tD-ON	Turn-On Delay time	5	—	30	
tR	Turn-On Rise Time	10	—	25	
tOFF	Turn-Off Time	—	0.2	—	
tF	Turn-Off Fall Time	—	0.7	—	



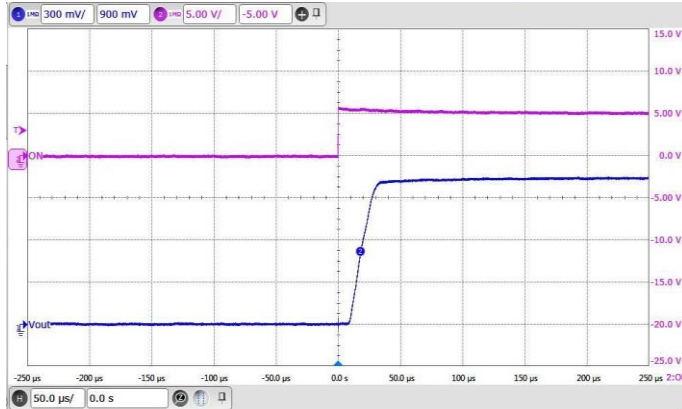
**Performance Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)



**Performance Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.) (continued)

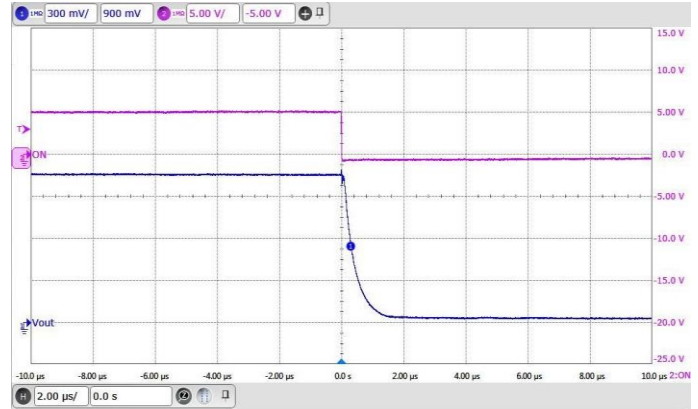
**Turn-On & Turn-On Rise Times**

V<sub>IN</sub> = 1.05V, V<sub>BIAS</sub> = 5V, C<sub>IN</sub> = 1μF, C<sub>OUT</sub> = 0.1μF,



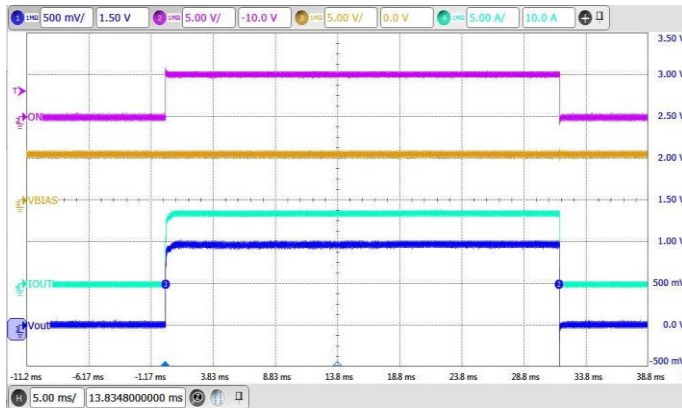
**Turn-Off & Turn-Off Fall Times**

V<sub>IN</sub> = 1.05V, V<sub>BIAS</sub> = 5V, C<sub>IN</sub> = 1μF, C<sub>OUT</sub> = 0.1μF,



**Turn-On & Turn-Off at I<sub>OUT</sub> = -10A**

V<sub>IN</sub> = 1.05V, V<sub>BIAS</sub> = 5V, C<sub>IN</sub> = 1μF, C<sub>OUT</sub> = 0.1μF, R<sub>OUT</sub> = 0.1Ω



## Application Information

### General Description

The DML1012LDS is a single channel, 6A load switch in an 8-pin V-DFN3030-8 (Type R) package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET operated input voltage range from 0.8V to 3.5V.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply and discharge FET eliminates the needs for any external components, which reduce solution size and bill of materials (BOM) count.

### Enable Control

The DML1012LDS device allows for enabling the MOSFET in an active-high configuration. When the VBIAS supply pin have an adequate voltage applied and the ON pin is at logic high level, the MOSFET enabled. Similarly, when the ON pin is at logic low level, the MOSFET is disabled.

### Power Sequencing

The DML1012LDS device will function with any power sequence, but the output turn-on delay performance may vary from what is specified. To archives the specified performance, there are two recommended power sequences:

$V_{BIAS} \rightarrow V_{IN} \rightarrow V_{ON}$

### Input Capacitor

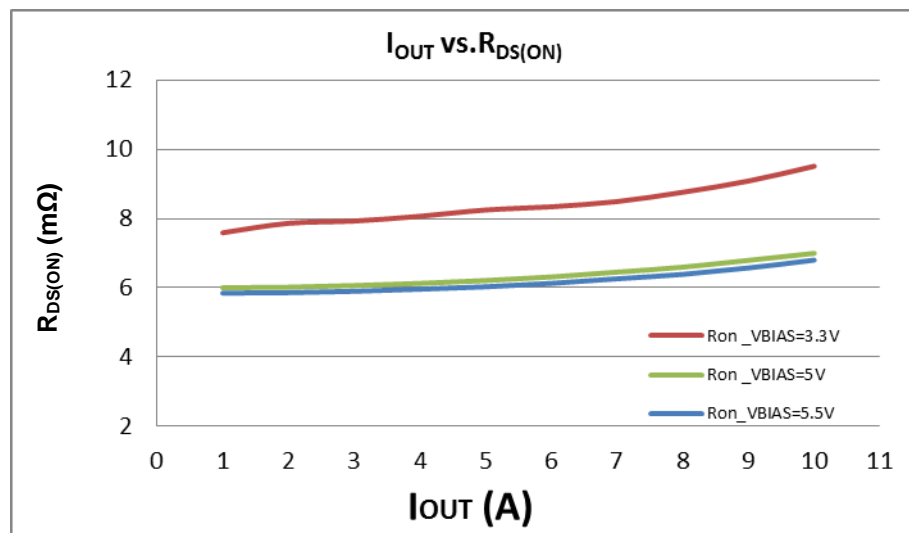
A capacitor of 10 $\mu$ F or higher value is recommended to be placed close to the IN pins of DML1012LDS. This capacitor can reduce the voltage drop caused by the in-rush current during the turn-on transient of the load switch. A higher value capacitor can further reduce the voltage drop during high-current application.

### Output Capacitor

A capacitor of 0.1 $\mu$ F or higher value is recommended to be placed between the OUT pins and GND pin. The switching times affected by the capacitance. A larger capacitor makes the initial turn-on transient smoother. This capacitor must be large enough to supply a fast transient load in order to prevent the output from dropping.

### V<sub>IN</sub> and V<sub>BIAS</sub> Voltage Range

For optimal on-resistance of load switch, make sure  $V_{IN} \leq 1.5V + V_{BIAS}$  and  $V_{BIAS}$  is within the voltage range from 3.2V to 5.5V. On-resistance of load switch will be higher if  $V_{IN} + 1.5V > V_{BIAS}$ . Resistance curves of a typical sample device at different  $V_{BIAS} = V_{IN}$  at  $I_{OUT} = -200mA$  are shown as below.



## Application Information (continued)

### Thermal Considerations

To ensure proper operation, the maximum junction temperature of the DML1012LDS should not exceed +150°C. Several factors attribute to the junction temperature rise: load current, MOSFET on-resistance, junction-to-ambient thermal resistance, and ambient temperature. The maximum load current can be determined by:

$$I_{LOAD(MAX)} = \sqrt{\frac{T_{J(MAX)} - T_C}{\theta_{JC} \times R_{DS(ON)}}}$$

Where

$I_{LOAD(MAX)}$  is the maximum allowable current on load (A). (6A for DML1012LDS)

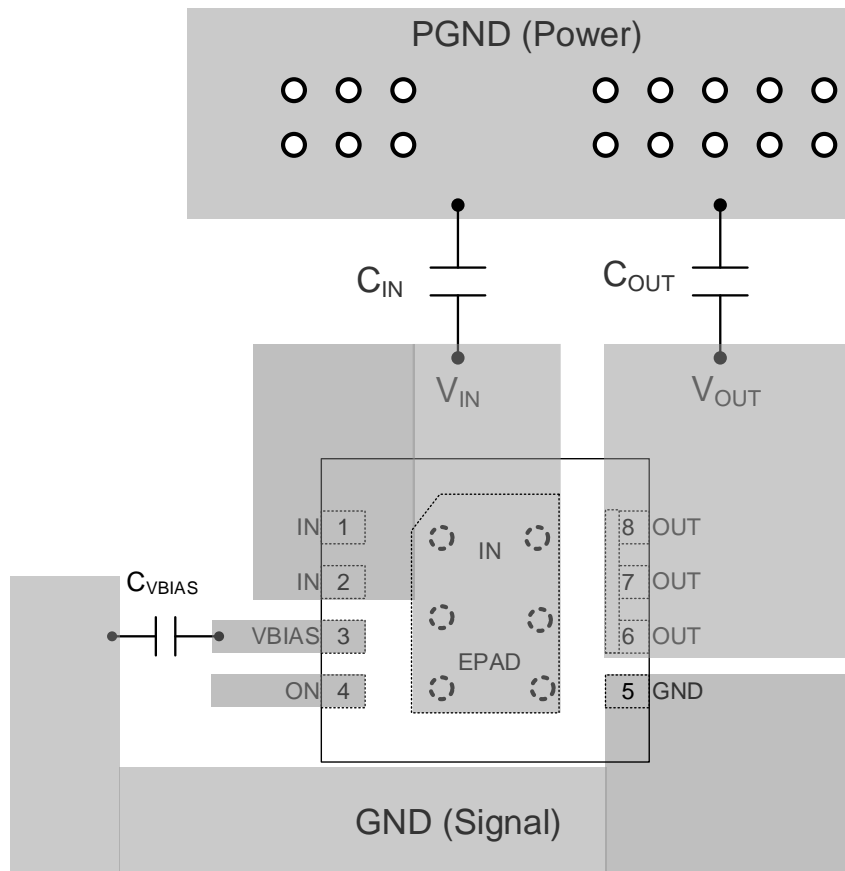
$T_{J(MAX)}$  is the maximum allowable junction temperature.

$T_C$  is the case temperature of the device.

$\theta_{JC}$  = junction to case thermal impedance. This parameter is highly dependent upon PCB layout.

### PCB Layout Consideration

1. Place the input/output capacitors  $C_{IN}$  and  $C_{OUT}$  as close as possible to the IN and OUT pins.
2. The power traces which are IN trace, OUT trace and GND trace. They should be short, wide and directly for minimize parasitic inductance.
3. Place  $C_{VBias}$  capacitor near the device pin.
4. Connect the signal ground to the GND pin, and keep a single connection from GND pin to the power ground behind the input or output capacitors.
5. For better power dissipation, holes are recommended to connect to the exposed pad's landing area with a large copper polygon on the other side of the printed circuit board. The copper polygons and exposed pad shall connect to IN pin on the printed circuit board.

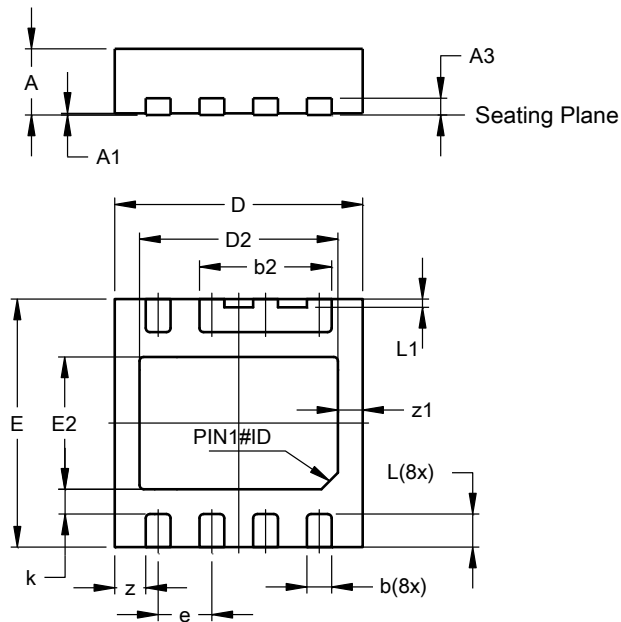




## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

### V-DFN3030-8 (Type R)

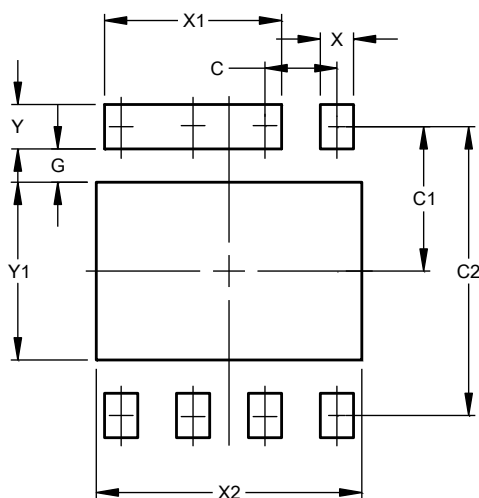


V-DFN3030-8 (Type R)			
Dim	Min	Max	Typ
A	0.77	0.83	0.80
A1	0.00	0.05	0.03
A3	--	--	0.203
b	0.25	0.35	0.30
b2	1.55	1.65	1.60
D	2.95	3.05	3.00
D2	2.30	2.50	2.40
E	2.95	3.05	3.00
E2	1.50	1.70	1.60
e	0.65 BSC		
k	--	--	0.30
L	0.35	0.45	0.40
L1	0.05	0.15	0.10
z	--	--	0.375
z1	--	--	0.30
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

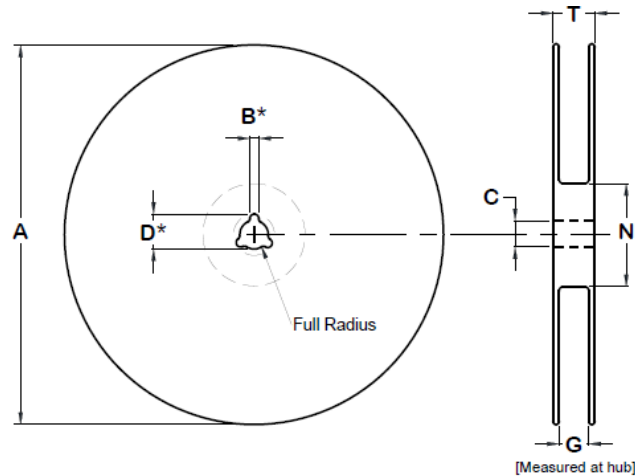
### V-DFN3030-8 (Type R)



Dimensions	Value (in mm)
C	0.65
C1	1.30
C2	2.60
G	0.30
X	0.30
X1	1.60
X2	2.40
Y	0.40
Y1	1.60

## Surface Mount Reel Specifications (All dimensions in mm.)

Please see <https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf> for the latest version.



### DML1012LDS-7A

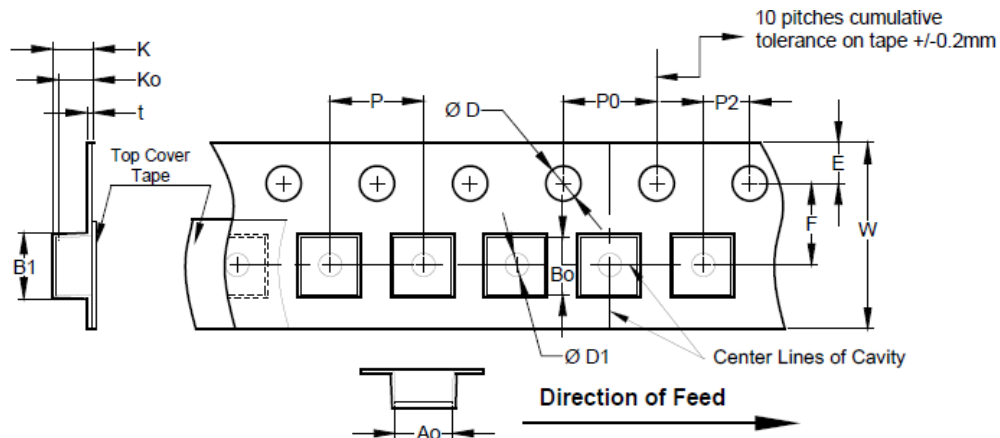
Tape Size	A Max	B* Max	C	D* Max	N Min	G	T Max
12mm	178 ±2	2.0 <sup>+0.5</sup> <sub>-0</sub>	13 <sup>+0.5</sup> <sub>-0.2</sub>	20.5 ±0.2	55 ±5	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4

### DML1012LDS-13

Tape Size	A Max	B* Max	C	D* Max	N Min	G	T Max
12mm	330 ±2	2.0 <sup>+0.5</sup> <sub>-0</sub>	13 <sup>+0.5</sup> <sub>-0.2</sub>	20.5 ±0.2	100 ±2	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4

## Embossed Carrier Tape Specifications

Please see <https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf> for the latest version.



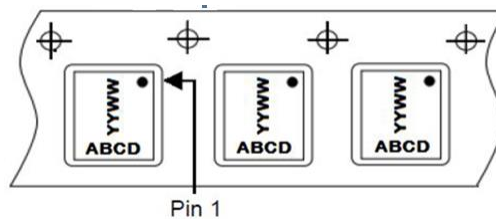
8, 12, 16, 24mm EMBOSSED TAPE DIMENSIONS IN mm						
Tape Width	D	E	P <sub>o</sub>	tmax	A <sub>o</sub> B <sub>o</sub> K <sub>o</sub>	
8, 12, 16, 24mm	1.50 +0.10 -0.0	1.75 ± 0.10	4.0 ± 0.10	0.400	(Note 5)	Constant Dimensions

Tape Width	B1 max	D1 min	F	K max	P2	W	P
12mm	8.2	1.5	5.5 ± 0.05	4.5	2.0 ± 0.05	12.0 ± 0.30	8.0 ± 0.10

Note: 5. A<sub>0</sub> B<sub>0</sub> K<sub>0</sub> are determined by component size.

## Tape Orientation

Please see <https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf> for the latest version.



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