16-CHANNEL LED DRIVER WITH DOT CORRECTION AND GRAYSCALE PWM CONTROL

Check for Samples: TLC59401

FEATURES

- **16 Channels**
- **12-Bit (4096 Steps) Grayscale PWM Control**
- **Dot Correction**
  - **6-Bit (64 Steps)**
- **Drive Capability (Constant-Current Sink)**
  - **0 mA to 80 mA (V_{CC} ≤ 3.6 V)**
  - **0 mA to 120 mA (V_{CC} > 3.6 V)**
- **LED Power-Supply Voltage up to 17 V**
- **V_{CC} = 3.0 V to 5.5 V**
- **Serial Data Interface**
- **Controlled Inrush Current**
- **30-MHz Data Transfer Rate**
- **CMOS Level I/O**
- **Error Information**
  - **LOD: LED Open Detection**
  - **TEF: Thermal Error Flag**

APPLICATIONS

- **Monocolor, Multicolor, Full-Color LED Displays**
- **LED Signboards**
- **Display Back-Lighting**

DESCRIPTION

The TLC59401 is a 16-channel, constant-current sink, LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED channels and other LED drivers. Both grayscale control and dot correction are accessible via a serial interface. A single external resistor sets the maximum current value of all 16 channels.

The TLC59401 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an over-temperature condition.

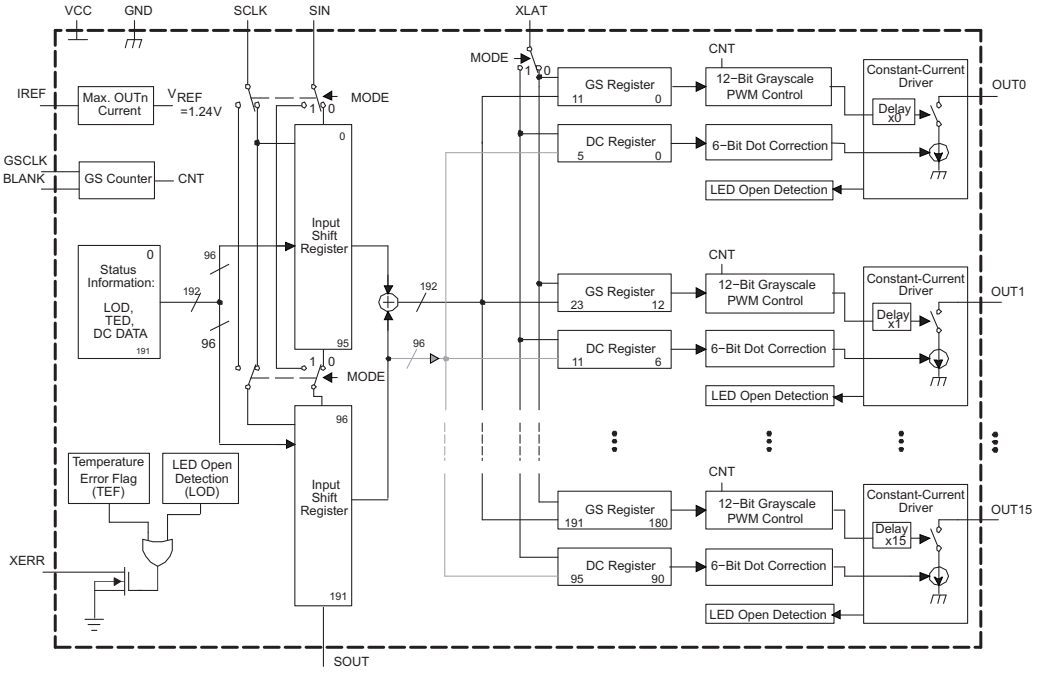


Figure 1. Functional Block Diagram

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	PART NUMBER
–40°C to +85°C	28-pin HTSSOP PowerPAD™	TLC59401PWP
–40°C to +85°C	32-pin 5 mm x 5 mm QFN	TLC59401RHB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			TLC59401	UNIT
V_I	Input voltage range(2)	V_{CC}	–0.3 to 6	V
I_O	Output current (dc)		130	mA
V_I	Input voltage range	$V_{(BLANK)}$, $V_{(SCLK)}$, $V_{(XLAT)}$, $V_{(MODE)}$, $V_{(SIN)}$, $V_{(GSCLK)}$, $V_{(IREF)}$, $V_{(TEST)}$	–0.3 to V_{CC} +0.3	V
V_O	Output voltage range	$V_{(SOUT)}$, $V_{(XERR)}$	–0.3 to V_{CC} +0.3	V
		$V_{(OUT0)}$ to $V_{(OUT15)}$	–0.3 to 18	V
	ESD rating	HBM (JEDEC JESD22-A114, human body model)	2	kV
		CDM (JEDEC JESD22-C101, charged device model)	500	V
$T_{J(max)}$	Operating junction temperature		+150	°C
T_{STG}	Storage temperature range		–55 to +150	°C
T_A	Operating ambient temperature range		–40 to +85	°C
	Package thermal impedance(3)	HTSSOP (PWP)(4)	31.58	°C/W
		QFN (RHB)(4)	35.9	°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) With PowerPAD soldered on PCB with 2-oz. trace of copper. See TI application report SLMA002 for further information.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DC CHARACTERISTICS						
V_{CC}	Supply Voltage		3		5.5	V
V_O	Voltage applied to output (OUT0 – OUT15)				17	V
V_{IH}	High-level input voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.2 V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 5 V at SOUT			–1	mA
I_{OL}	Low-level output current	V_{CC} = 5 V at SOUT, XERR			1	mA
I_{OLC}	Constant output current	OUT0 to OUT15, V_{CC} ≤ 3.6 V			80	mA
		OUT0 to OUT15, V_{CC} > 3.6 V			120	mA
T_J	Operating junction temperature		–40		+125	°C
T_A	Operating free-air temperature range		–40		+85	°C
AC CHARACTERISTICS At V_{CC} = 3 V to 5.5 V and T_A = –40°C to +85°C, unless otherwise noted.						
$f_{(SCLK)}$	Data shift clock frequency	SCLK			30	MHz
$f_{(GSCLK)}$	Grayscale clock frequency	GSCLK			30	MHz
t_{wh0}/t_{wl0}	SCLK pulse duration	SCLK = high/low (see Figure 12)	16			ns
t_{wh1}/t_{wl1}	GSCLK pulse duration	GSCLK = high/low (see Figure 12)	16			ns
t_{wh2}	XLAT pulse duration	XLAT = high (see Figure 12)	20			ns
t_{wh3}	BLANK pulse duration	BLANK = high (see Figure 12)	20			ns
t_{su0}	Setup time	SIN - SCLK↑ (see Figure 12)	5			ns
t_{su1}		SCLK↓ - XLAT↑ (see Figure 12)	10			
t_{su2}		MODE↑↓ - SCLK↑ (see Figure 12)	10			
t_{su3}		MODE↑↓ - XLAT↑ (see Figure 12)	10			
t_{su4}		BLANK↓ - GSCLK↑ (see Figure 12)	10			
t_{su5}		XLAT↑ - GSCLK↑ (see Figure 12)	30			
t_{h0}	Hold Time	SCLK↑ - SIN (see Figure 12)	3			ns
t_{h1}		XLAT↓ - SCLK↑ (see Figure 12)	10			
t_{h2}		SCLK↑ - MODE↑↓ (see Figure 12)	10			
t_{h3}		XLAT↓ - MODE↑↓ (see Figure 12)	10			
t_{h4}		GSCLK↑ - BLANK↑ (see Figure 12)	10			

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A < +25°C	DERATING FACTOR ABOVE T_A = +25°C	POWER RATING T_A = +70°C	POWER RATING T_A = +85°C
28-pin HTSSOP with PowerPAD soldered(1)	3958 mW	31.67 mW/°C	2533 mW	2058 mW
28-pin HTSSOP without PowerPAD soldered	2026 mW	16.21 mW/°C	1296 mW	1053 mW
32-pin QFN(1)	3482 mW	27.86 mW/°C	2228 mW	1811 mW

(1) The PowerPAD is soldered to the PCB with a 2-oz. copper trace. See application report SLMA002 for further information.

ELECTRICAL CHARACTERISTICS

At V_{CC} = 3 V to 5.5 V and T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC59401			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA, SOUT	V_{CC} – 0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND; BLANK, TEST, GSCLK, SCLK, SIN, XLAT pin	–1		1	µA
		V_I = GND; MODE pin	–1		1	µA
		V_I = V_{CC}; MODE pin			50	µA
I_{CC}	Supply current	No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ		0.9	6	mA
		No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		5.2	12	mA
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		16	25	mA
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω		30	60	mA
$I_{O(LC)}$	Constant output current	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω	54	61	69	mA
I_{lkg}	Leakage output current	All output OFF, V_O = 15 V, $R_{(IREF)}$ = 640 Ω , OUT0 to OUT15			0.1	µA
$\Delta I_{O(LC0)}$	Constant sink current error	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15, –20°C to +85°C(1)		±1	±4	%
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15(1)		±1	±8	
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 320 Ω, V_{CC} > 3.6 V, OUT0 to OUT15, –20°C to +85°C(1)		±1	±6	%
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 320 Ω, V_{CC} > 3.6 V, OUT0 to OUT15(1)		±1	±8	
$\Delta I_{O(LC1)}$	Constant sink current error	Device to device, averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 1920 Ω (20 mA)(2)		–2, +0.4	±4	%
$\Delta I_{O(LC2)}$	Constant sink current error	Device to device, averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 480 Ω (80 mA)(2)		–2.7, +2	±4	%
$\Delta I_{O(LC3)}$	Line regulation	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω OUT0 to OUT15, V_{CC} = 3 V to 5.5 V(3)		±1	±4	%/V
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 320 Ω OUT0 to OUT15, V_{CC} > 3.6 V(3)		±1	±6	%/V
$\Delta I_{O(LC4)}$	Load regulation	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15(4)		±2	±6	%/V
		All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 320 Ω, V_{CC} > 3.6 V, OUT0 to OUT15(4)		±2	±8	%/V
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature(5)	+150		+170	°C
$V_{(LED)}$	LED open detection threshold			0.3	0.4	V
$V_{(IREF)}$	Reference voltage output	$R_{(IREF)}$ = 640 Ω	1.20	1.24	1.28	V

(1) The deviation of each output from the average of OUT0-15 constant current. It is calculated by Equation 1 in Table 1.
(2) The deviation of average of OUT1-15 constant current from the ideal constant-current value. It is calculated by Equation 2 in Table 1. The ideal current is calculated by Equation 3 in Table 1.
(3) The line regulation is calculated by Equation 4 in Table 1.
(4) The load regulation is calculated by Equation 5 in Table 1.
(5) Not tested. Specified by design.

Table 1. Test Parameter Equations

$\Delta(\%) = \frac{I_{OUTn} - I_{OUTavg\_0-15}}{I_{OUTavg\_0-15}} \times 100$	**(1)**
$\Delta(\%) = \frac{I_{OUTavg} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \times 100$	**(2)**
$I_{OUT(IDEAL)} = 31.5 \times \left(\frac{1.24V}{R_{IREF}}\right)$	**(3)**
$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5V) - (I_{OUTn} \text{ at } V_{CC} = 3.0V)}{(I_{OUTn} \text{ at } V_{CC} = 3.0V)} \times \frac{100}{2.5}$	(4)
$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0V) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1.0V)} \times \frac{100}{2.0}$	(5)

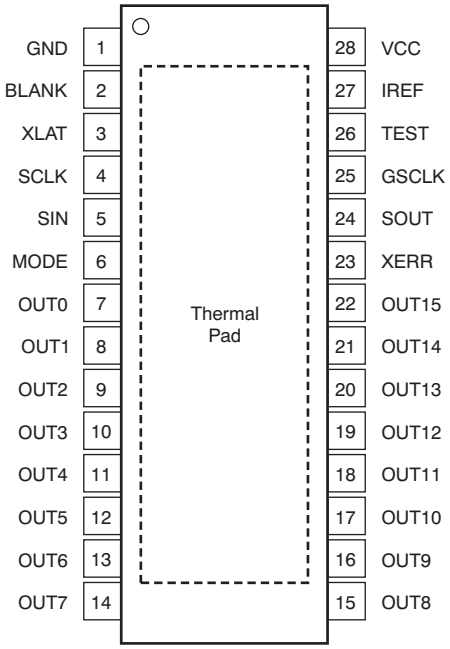
SWITCHING CHARACTERISTICS

At V_{CC} = 3 V to 5.5 V, C_L = 15 pF, and T_A = –40°C to 85°C, unless otherwise noted.

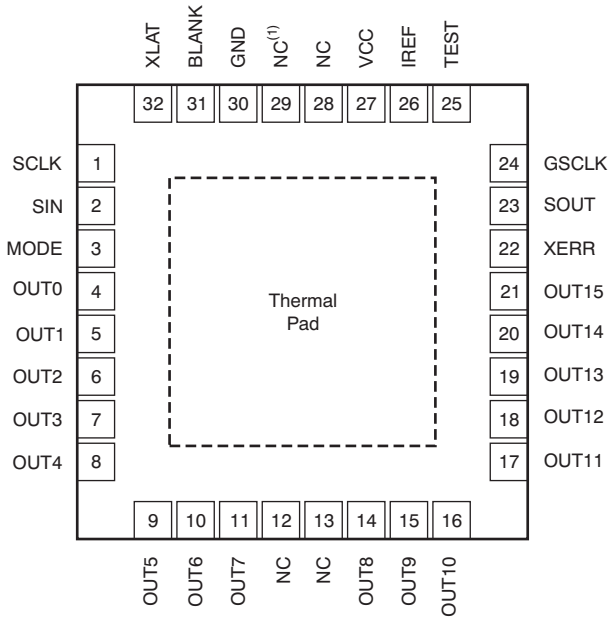
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT			16	ns
t_{r1}		OUTn, V_{CC} = 5 V, T_A = +60°C, DCn = 3Fh		10	30	
t_{f0}	Fall time	SOUT			16	ns
t_{f1}		OUTn, V_{CC} = 5 V, T_A = +60°C, DCn = 3Fh		10	30	
t_{pd0}	Propagation delay time	SCLK - SOUT (see Figure 12)			30	ns
t_{pd1}		BLANK - OUT0 (see Figure 12)			60	ns
t_{pd2}		OUTn - XERR (see Figure 12)			1000	ns
t_{pd3}		GSCLK - OUT0 (see Figure 12)			60	ns
t_{pd4}		XLAT - I_{OUT} (dot correction) (see Figure 12)			60	ns
t_d	Output delay time	OUTn - OUT(n+1) (see Figure 12)		20	30	ns
t_{on_err}	Output on-time error	t_{outon} – T_{gsclk} (see Figure 12), GSn = 01h, GSCLK = 11 MHz	–90	–50	10	ns

PIN CONFIGURATIONS

PWP PACKAGE
28-PIN HTSSOP PowerPAD
(TOP VIEW)



RHB PACKAGE
32-PIN 5 mm × 5 mm QFN
(TOP VIEW)



(1) NC = no connection.

TERMINAL FUNCTION

TERMINAL			I/O	DESCRIPTION
	PWP	RHB		
NAME	NO.	NO.		
BLANK	2	31	I	Blank all outputs. When BLANK is high, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK is low, OUTn are controlled by the grayscale PWM control.
GND	1	30	G	Ground
GSCLK	25	24	I	Reference clock for grayscale PWM control
IREF	27	26	I/O	Reference current terminal. The maximum current for the outputs OUT0-OUT15 is set with a resistor from IREF to GND. Any capacitance does not need to be connected between IREF and GND.
NC	-	12, 13, 28, 29		No connection
OUT0	7	4	O	Constant-current output. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUT1	8	5	O	Constant-current output
OUT2	9	6	O	Constant-current output
OUT3	10	7	O	Constant-current output
OUT4	11	8	O	Constant-current output
OUT5	12	9	O	Constant-current output
OUT6	13	10	O	Constant-current output
OUT7	14	11	O	Constant-current output
OUT8	15	14	O	Constant-current output
OUT9	16	15	O	Constant-current output
OUT10	17	16	O	Constant-current output
OUT11	18	17	O	Constant-current output
OUT12	19	18	O	Constant-current output
OUT13	20	19	O	Constant-current output
OUT14	21	20	O	Constant-current output
OUT15	22	21	O	Constant-current output
SCLK	4	1	I	Serial data shift clock
SIN	5	2	I	Serial data input
SOUT	24	23	O	Serial data output
TEST	26	25	I	Test pin: TEST must be connected to VCC
VCC	28	27	I	Power-supply voltage
MODE	6	3	I	Input mode-change pin. When MODE = GND, the device is in GS mode. When MODE = V_{CC}, the device is in DC mode.
XERR	23	22	O	Error output. XERR is an open-drain terminal. XERR goes low when LOD or TEF is detected.
XLAT	3	32	I	Level triggered latch signal. When XLAT is high, the TLC59401 writes data from the input shift register to either GS register (MODE is low) or DC register (MODE is high). When XLAT is low, the data in the GS or DC registers are held constant and do not change.

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

Resistor values are equivalent resistance and not tested.

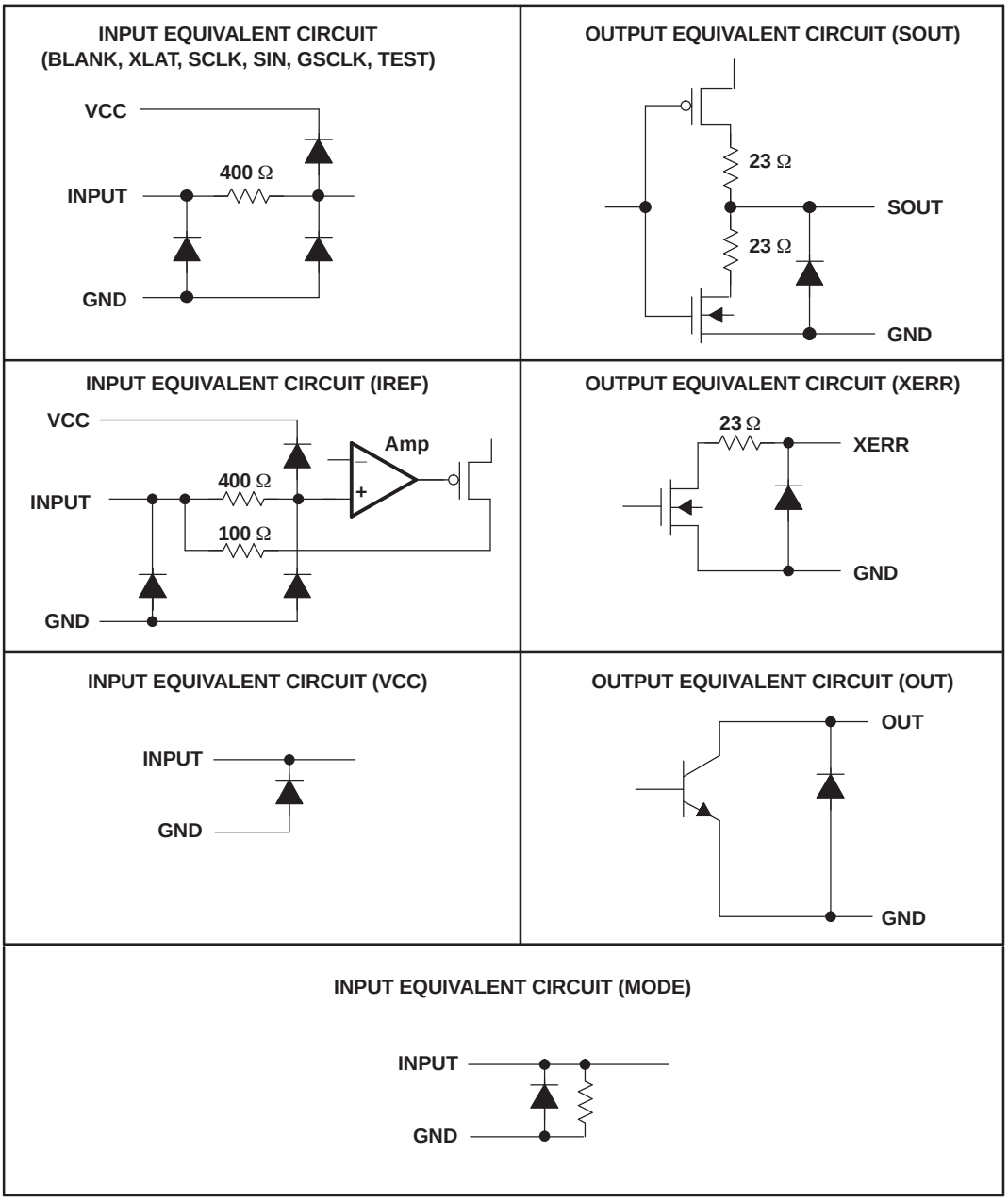


Figure 2. Input and Output Equivalent Circuits

PARAMETER MEASUREMENT INFORMATION (continued)

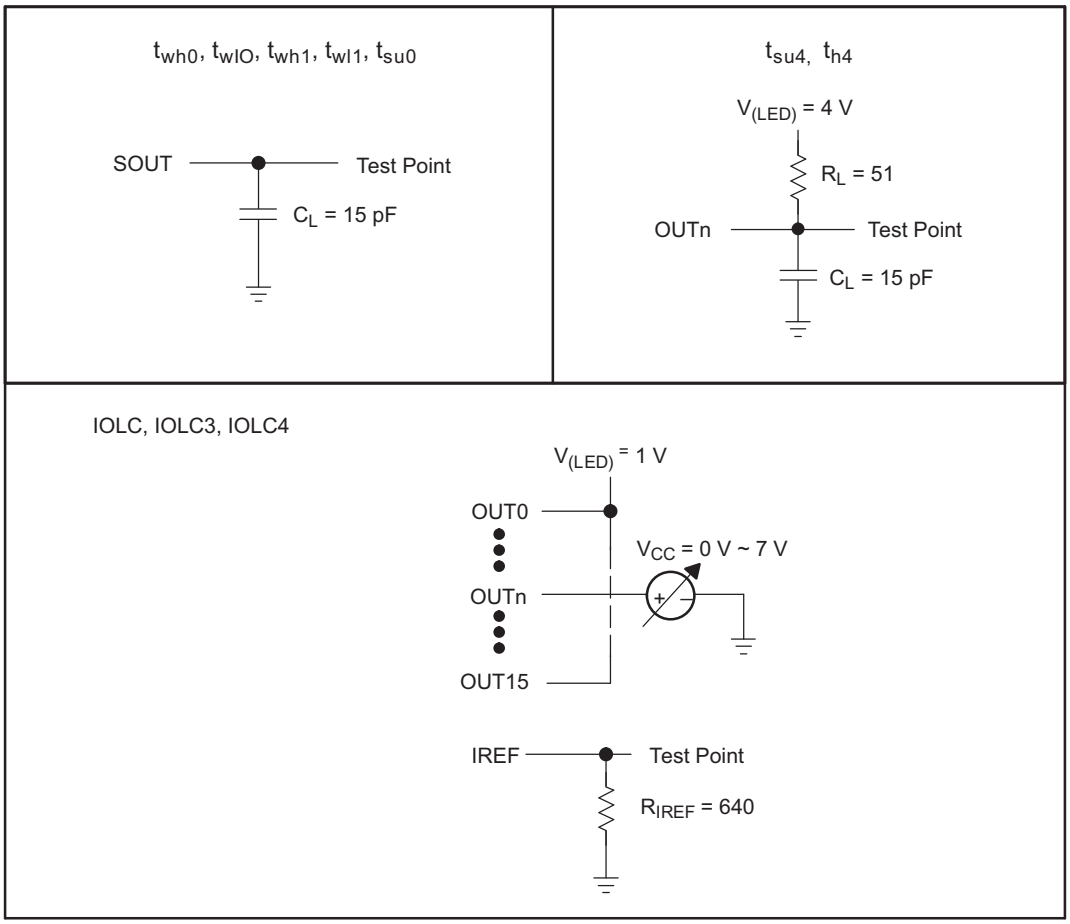


Figure 3. Parameter Measurement Circuits

TYPICAL CHARACTERISTICS

REFERENCE RESISTOR vs OUTPUT CURRENT

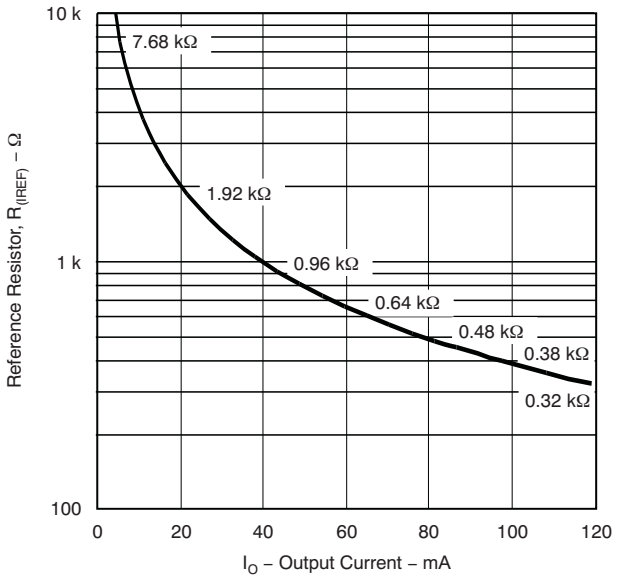


Figure 4.

POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE

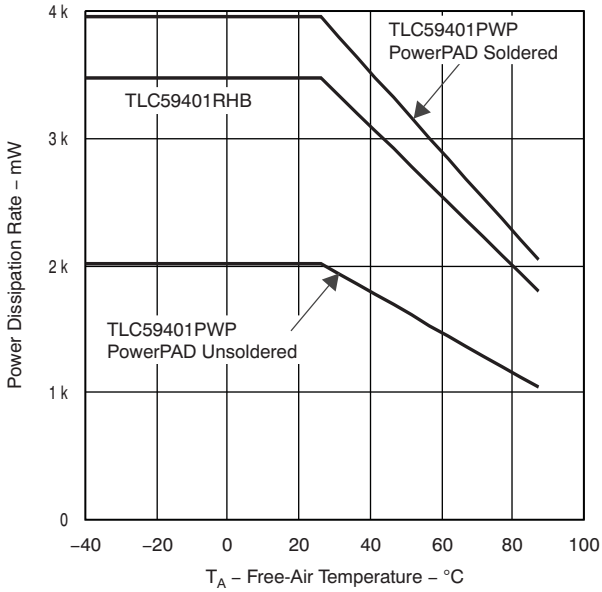


Figure 5.

OUTPUT CURRENT vs OUTPUT VOLTAGE

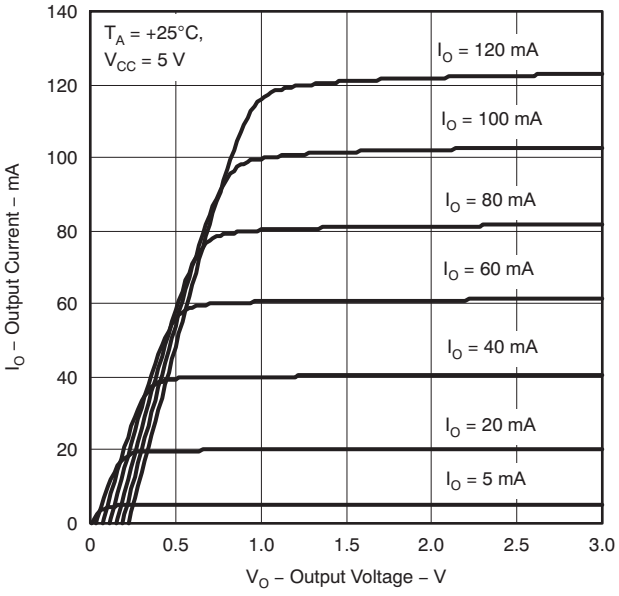


Figure 6.

OUTPUT CURRENT vs OUTPUT VOLTAGE

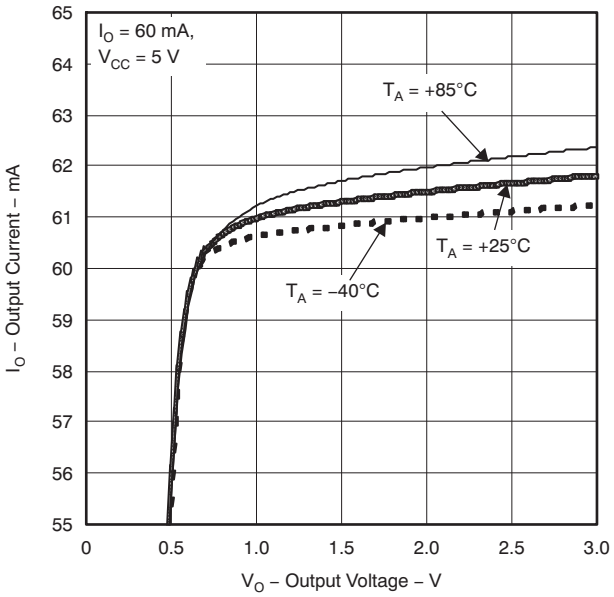


Figure 7.

TYPICAL CHARACTERISTICS (continued)

CONSTANT OUTPUT CURRENT, ΔI_{OLC} vs AMBIENT TEMPERATURE

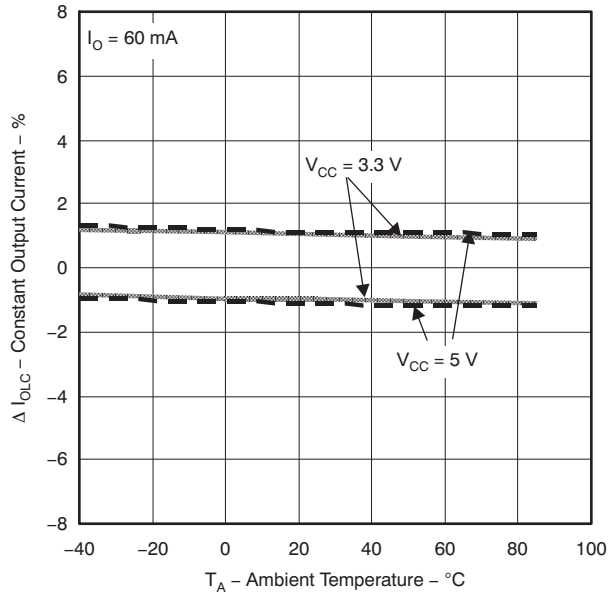


Figure 8.

CONSTANT OUTPUT CURRENT, ΔI_{OLC} vs OUTPUT CURRENT

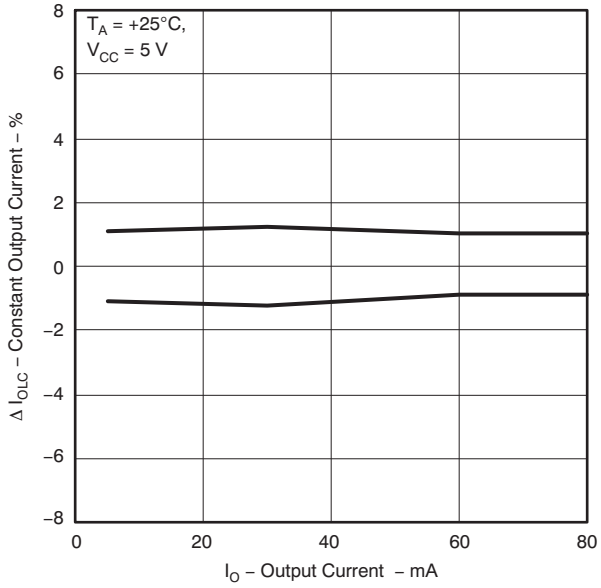


Figure 9.

OUTPUT CURRENT vs DOT CORRECTION LINEARITY (ABS Value)

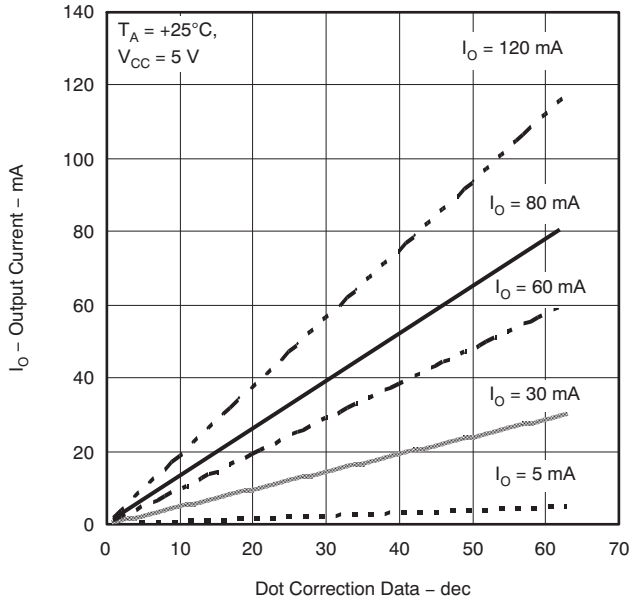


Figure 10.

OUTPUT CURRENT vs DOT CORRECTION LINEARITY (ABS Value)

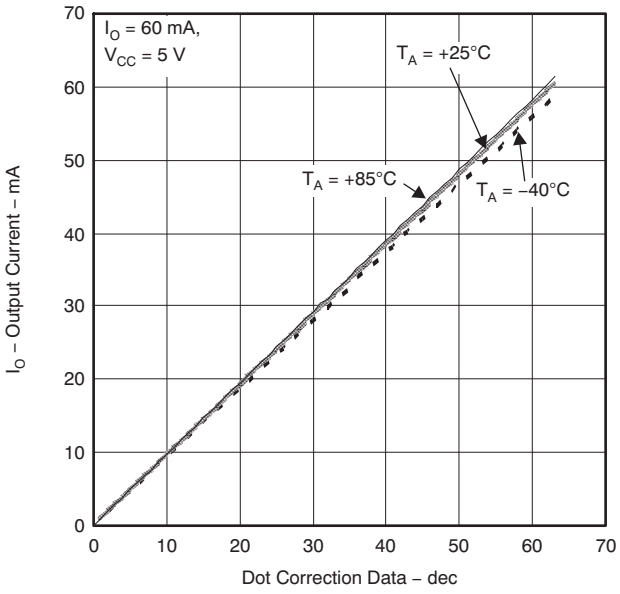


Figure 11.

PRINCIPLES OF OPERATION

SERIAL INTERFACE

The TLC59401 has a flexible serial interface, which can be connected to microcontrollers or digital signal processors in various ways. Only three pins are needed to input data into the device. The rising edge of SCLK signal shifts the data from the SIN pin to the internal register. After all data are clocked in, a high-level pulse of XLAT signal latches the serial data to the internal registers. The internal registers are level-triggered latches of XLAT signal. All data are clocked in MSB first. The length of serial data is 96 bit or 192 bit, depending on the programming mode. Grayscale data and dot correction data can be entered during a grayscale cycle. Although new grayscale data can be clocked in during a grayscale cycle, the XLAT signal should only latch the grayscale data at the end of the grayscale cycle. Latching in new grayscale data immediately overwrites the existing grayscale data. Figure 12 shows the serial data input timing chart. More than two TLC59401s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. An example of cascading two TLC59401s is shown in Figure 13 and the timing chart is shown in Figure 14. The SOUT pin can also be connected to the controller to receive status information from TLC59401, as shown in Figure 22.

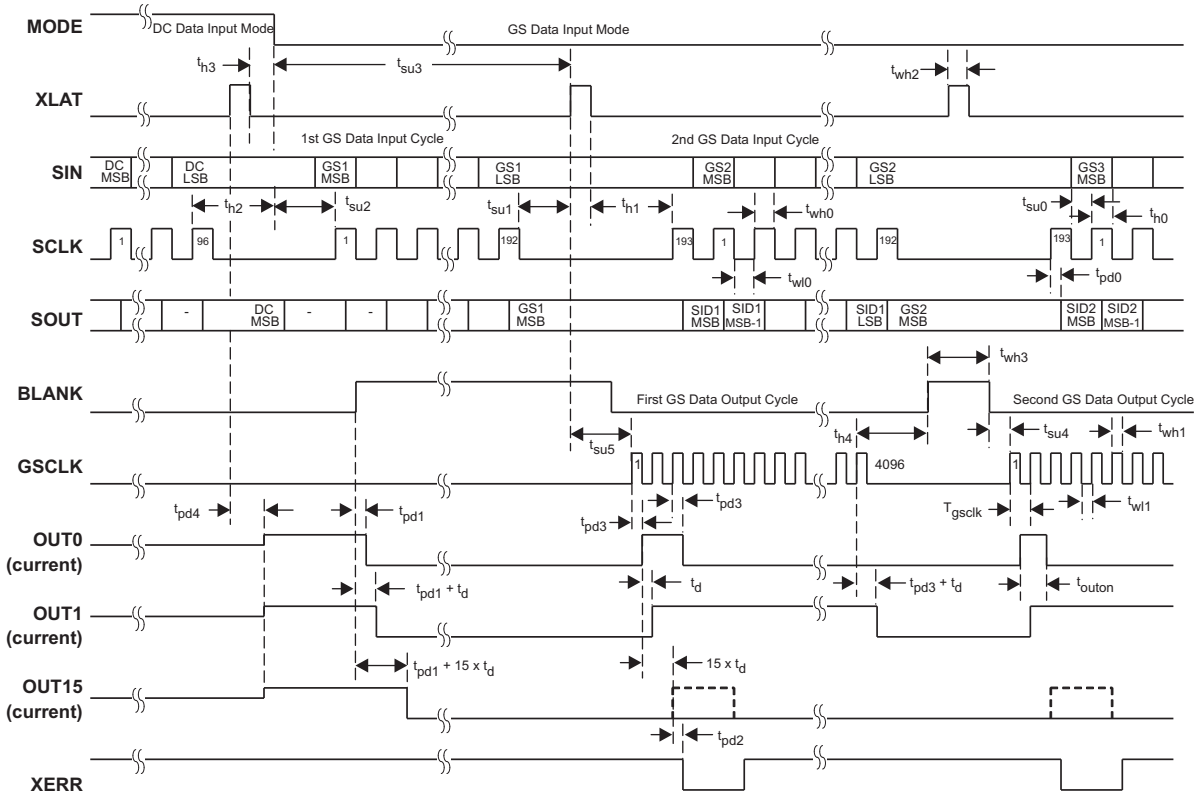


Figure 12. Serial Data Input Timing Chart

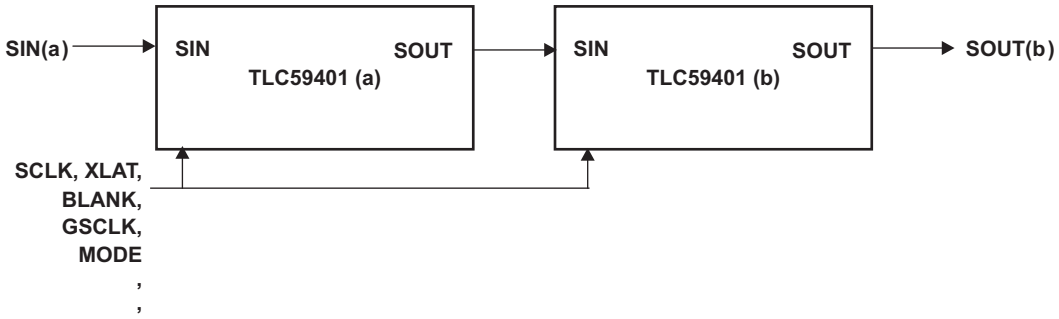


Figure 13. Cascading Two TLC59401 Devices

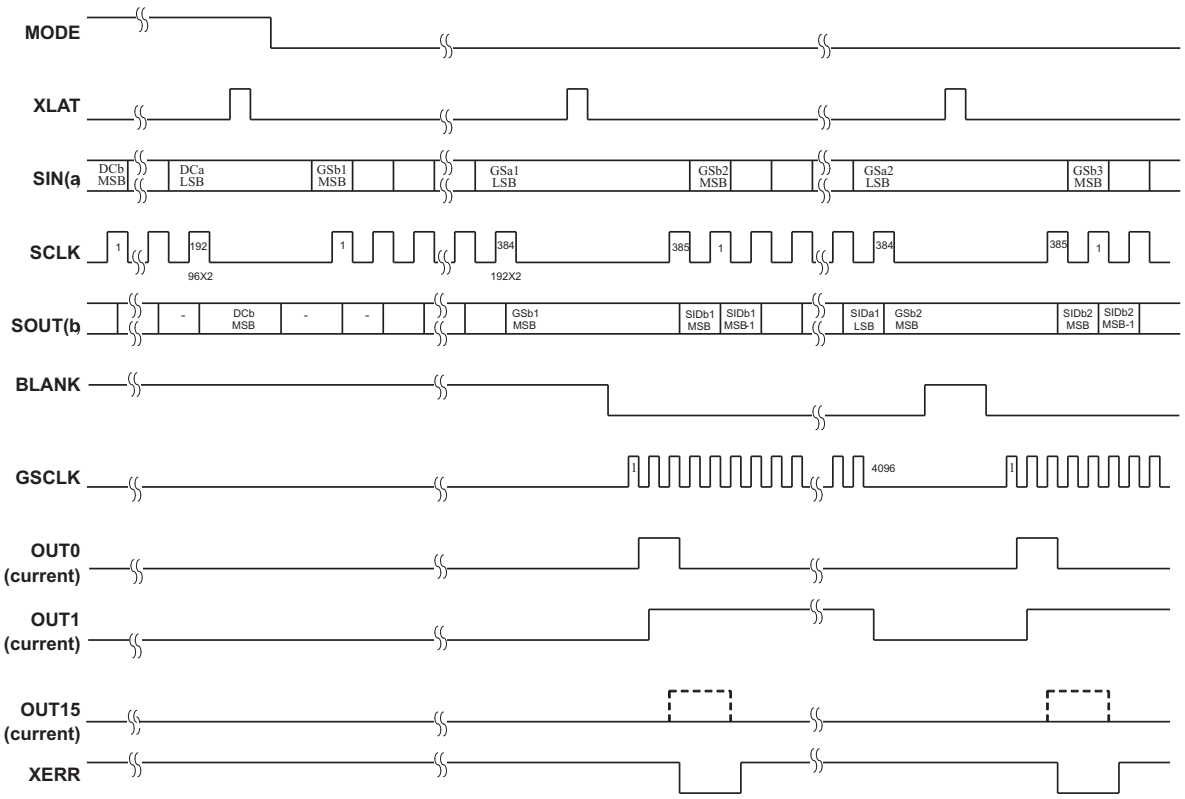


Figure 14. Timing Chart for Two Cascaded TLC59401 Devices

ERROR INFORMATION OUTPUT

The open-drain output XERR is used to report both of the TLC59401 error flags, TEF and LOD. During normal operation, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through an external pull-up resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Because XERR is an open-drain output, multiple ICs can be ORed together and pulled up to V_{CC} with a single pull-up resistor. This capability reduces the number of signals needed to report a system error (see Figure 22).

To differentiate the LOD and TEF signal from the XERR pin, LOD can be masked out with BLANK pulled high.

Table 2. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't care	Low	X	High	High
$T_J > T_{(TEF)}$	Don't care	High	X		Low
$T_J < T_{(TEF)}$	OUTn > $V_{(LED)}$	Low	Low	Low	High
	OUTn < $V_{(LED)}$	Low	High		Low
$T_J > T_{(TEF)}$	OUTn > $V_{(LED)}$	High	Low		Low
	OUTn < $V_{(LED)}$	High	High		Low

TEF: THERMAL ERROR FLAG

The TLC59401 provides a temperature error flag (TEF) circuit to indicate an over-temperature condition of the IC. If the junction temperature exceeds the threshold temperature (+160°C typical), TEF goes high and the XERR pin goes to a low level. When the junction temperature becomes lower than the threshold temperature, TEF goes low and the XERR pin becomes high impedance. The TEF status can also be read out from the TLC59401 status register.

LOD: LED OPEN DETECTION

The TLC59401 has an LED-open detection circuit that detects broken or disconnected LEDs. The LED open detector pulls the XERR pin to GND when an open LED is detected. XERR and the corresponding error bit in the Status Information Data is only active under the following open LED conditions:

1. OUTn is on and the time t_{pd2} (1 µs typical) has passed.
2. The voltage of OUTn is < 0.3V (typical)

The LOD status of each output can be also read out from the SOUT pin. See the *Status Information Output* section for details. The LOD error bits are latched into the Status Information Data when XLAT returns to a low state after a high state. Therefore, the XLAT pin must be pulsed high, then low while XERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

DELAY BETWEEN OUTPUTS

The TLC59401 has graduated delay circuits between outputs. These circuits can be found in the constant-current driver block of the device (see Figure 1). The fixed-delay time is 20 ns (typical), OUT0 has no delay, OUT1 has 20 ns delay, and OUT2 has 40 ns delay, etc. The maximum delay is 300 ns from OUT0 to OUT15. The delay works during switch on and switch off of each output channel. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

OUTPUT ENABLE

All OUTn channels of the TLC59401 can be switched off with one signal. When BLANK is set high, all OUTn channels are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When BLANK is set low, all OUTn channels work under normal conditions. If BLANK goes low and then back high again in less than 300 ns, all outputs programmed to turn on do so for either the programmed number of grayscale clocks or the length of time that the BLANK signal was low, whichever is lower. For example, if all outputs are programmed to turn on for 1 ms, but the BLANK signal is only low for 200 ns, all outputs turn on for 200 ns even though some outputs are turning on after the BLANK signal has already gone high.

Table 3. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
Low	Normal condition
High	Disabled

SETTING MAXIMUM CHANNEL CURRENT

The maximum output current per channel is programmed by a single resistor, $R_{(IREF)}$, which is placed between IREF pin and GND pin. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24 V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 31.5. The maximum output current can be calculated by Equation 6:

$$I_{max} = \frac{V_{(IREF)}}{R_{(IREF)}} \times 31.5 \quad (6)$$

where:

$V_{(IREF)}$ = 1.24 V

$R_{(IREF)}$ = User-selected external resistor.

I_{max} must be set between 5 mA and 120 mA. The output current may be unstable if I_{max} is set lower than 5 mA. Output currents lower than 5 mA can be achieved by setting I_{max} to 5 mA or higher and then using dot correction.

See Figure 4 for the maximum output current I_O versus $R_{(IREF)}$. $R_{(IREF)}$ is the value of the resistor between IREF terminal to GND, and I_O is the constant output current of OUT0 to OUT15. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per channel. The maximum output current per channel is 31.5 times the current flowing out of the IREF pin.

POWER DISSIPATION CALCULATION

The device power dissipation must be below the power dissipation rate of the device package to ensure correct operation. Equation 7 calculates the power dissipation of device:

$$P_D = \left(V_{CC} \times I_{CC}\right) + \left(V_{OUT} \times I_{MAX} \times N \times \frac{DC_n}{63} \times d_{PWM}\right) \quad (7)$$

where:

V_{CC}: device supply voltage

I_{CC}: device supply current

V_{OUT}: TLC59401 OUTn voltage when driving LED current

I_{MAX}: LED current adjusted by $R_{(IREF)}$ Resistor

DC_n: maximum dot correction value for OUTn

N: number of OUTn driving LED at the same time

d_{PWM}: duty cycle defined by BLANK pin or GS PWM value

OPERATING MODES

The TLC59401 has two operating modes defined by MODE as shown in Table 4. The GS and DC registers are set to random values that are not known immediately after power on. The GS and DC values must be programmed before turning on the outputs. Please note that when initially setting GS and DC data after power on, the GS data must be set before the DC data is set. Failure to set GS data before DC data may result in losing the first bit of GS data. XLAT must be low when the MODE pin goes high-to-low or low-to-high to change back and forth between GS mode and DC mode.

Table 4. TLC59401 Operating Modes Truth Table

MODE	INPUT SHIFT REGISTER	OPERATING MODE
GND	192 bit	Grayscale PWM Mode
V_{CC}	96 bit	Dot Correction Data Input Mode

SETTING DOT CORRECTION

The TLC59401 has the capability to fine-adjust the output current of each channel (OUT0 to OUT15) independently. This feature is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current I_{max}. The TEST pin must be connected to V_{CC} to ensure proper operation of the dot correction circuitry. Equation 8 determines the output current for each output n:

$$I_{OUTn} = I_{max} \times \frac{DCn}{63} \quad (8)$$

where:

I_{max} = the maximum programmable output current for each output.

DCn = the programmed dot correction value for output n (DCn = 0 to 63).

n = 0 to 15

Figure 15 shows the dot correction data packet format which consists of 6 bits x 16 channel, total 96 bits. The format is Big-Endian format. In this format, the MSB is transmitted first, followed by the MSB-1, etc. The DC 15.5 in Figure 15 stands for the fifth-most significant bit for output 15.

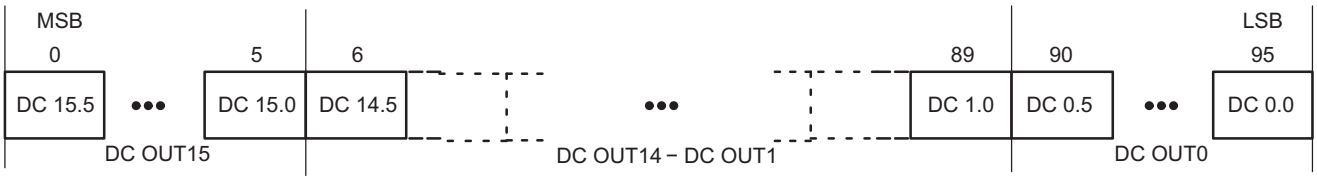


Figure 15. Dot Correction Data Packet Format

When MODE is set to V_{CC}, the TLC59401 enters the dot correction data input mode. The length of the input shift register becomes 96 bits. After all serial data are shifted in, the TLC59401 writes the data in the input shift register to the DC register when XLAT is high, and holds the data in the DC register when XLAT is low. The DC register is a level-triggered latch of the XLAT signal. Because XLAT is a level-triggered signal, SCLK and SIN must not be changed while XLAT is high. After XLAT goes low, data in the DC register are latched and do not change. The BLANK signal does not need to be high to latch in new data. When XLAT goes high, the new dot-correction data immediately become valid and change the output currents if BLANK is low. XLAT has a setup time (t_{su1}) and a hold time (t_{h1}) to SCLK, as shown in Figure 12.

To input data into the dot correction register, MODE must be set to V_{CC}. The internal input shift register is then set to 96-bit width. After all serial data are clocked in, a rising edge of XLAT is used to latch the data into the dot correction register. Figure 16 shows the dc data input timing chart.

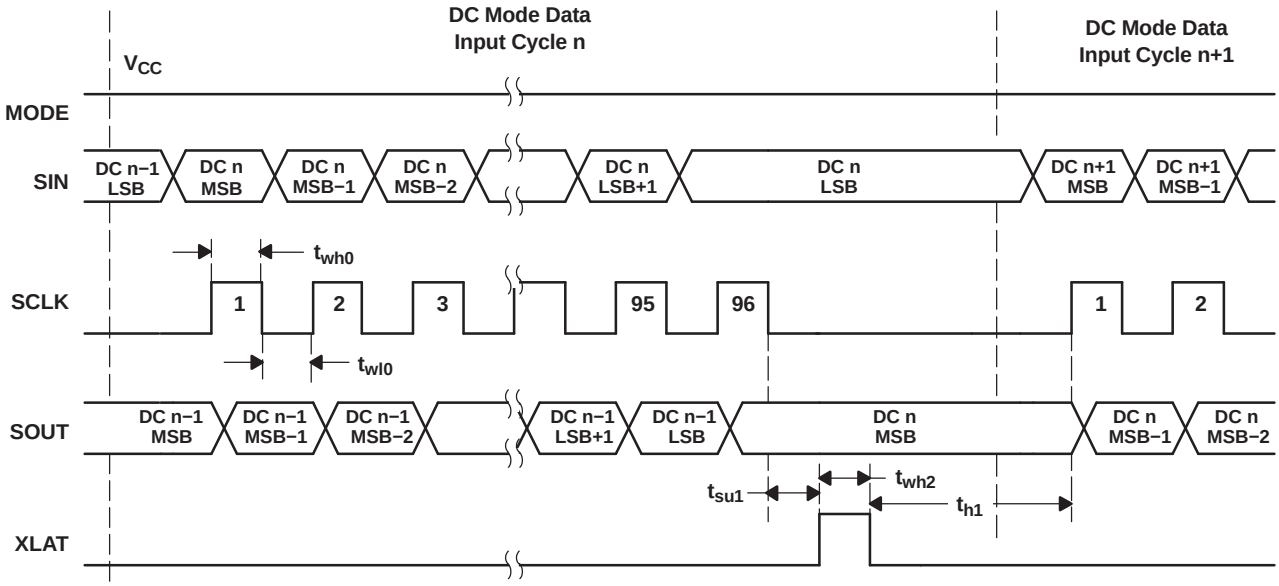


Figure 16. Dot Correction Data Input Timing Chart

When the IC is powered on, the data in the input shift register and DC register are not set to any default values. Therefore, DC data must be written to the DC register before turning on the constant-current output.

SETTING GRAYSCALE

The TLC59401 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, from 0% to 100% brightness. Equation 9 determines the brightness level for each output n:

$$\text{Brightness in \%} = \frac{GSn}{4095} \times 100 \tag{9}$$

where:

GSn = the programmed grayscale value for output n (GSn = 0 to 4095)

n = 0 to 15

Grayscale data for all OUTn

The input shift register enters grayscale data into the grayscale register for all channels simultaneously. The complete grayscale data format consists of 16 × 12 bit words, which forms a 192-bit wide data packet (see Figure 17). The data packet must be clocked in MSB first.

Figure 17. Grayscale Data Packet Format

When MODE is set to GND, the TLC59401 enters grayscale data input mode. The device switches the input shift register to 192-bit width. After all data are clocked in, a rising edge of the XLAT signal latches the data into the grayscale register (see Figure 18). New grayscale data immediately become valid at the rising edge of the XLAT signal; therefore, new grayscale data should be latched at the end of a grayscale cycle when BLANK is high. The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register are replaced with status information data (SID) after updating the grayscale register.

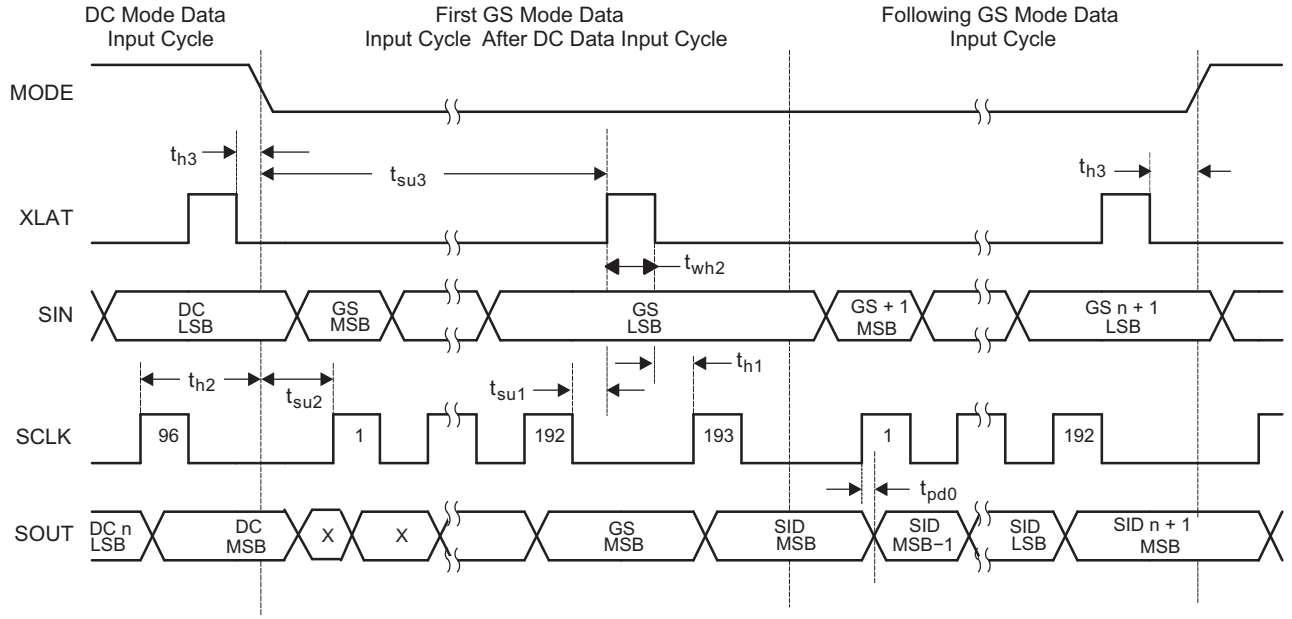


Figure 18. Grayscale Data Input Timing Chart

When the IC is powered on, the data in the input shift register and GS register are not set to any default values. Therefore, GS data must be written to the GS register before turning on the constant-current output.

STATUS INFORMATION OUTPUT

The TLC59401 has a status information register, which can be accessed in grayscale mode (MODE = GND). After the XLAT signal latches the data into the GS register, the input shift register data are replaced with the status information data (SID) of the device (see Figure 18). LOD, TEF, and dot-correction register data can be read out at the SOUT pin. The status information data packet is 192 bits wide. Bits 0 to 15 contain the LOD status of each channel. Bit 16 contains the TEF status. Bits 24 to 119 contain the data of the dot-correction register. The remaining bits are reserved. The complete status information data packet is shown in Figure 19.

SOUT outputs the MSB of the SID at the same time the SID are stored in the SID register, as shown in Figure 20. The next SCLK pulse, which is the clock for receiving the MSB of the next grayscale data, transmits MSB-1 of the SID. If the output voltage is less than 0.3 V (typical) when the output sink current turns on, the LOD status flag becomes active. The LOD status flag is an internal signal that pulls the XERR pin low when the LOD status flag becomes active. The delay time, t_{pd2} (1 µs maximum), is the period from the time of turning on the output sink current to the time the LOD status flag becomes valid. The timing for each channel LOD status to become valid is shifted by the 30-ns (maximum), channel-to-channel turn-on time. After the first GSCLK goes high, OUT0 LOD status is valid; $t_{pd3} + t_{pd2}$ = 60 ns + 1 µs = 1.06 µs. OUT1 LOD status is valid; $t_{pd3} + t_d + t_{pd2}$ = 60 ns + 30 ns + 1 µs = 1.09 µs. OUT2 LOD status is valid; $t_{pd3} + (2 \times t_d) + t_{pd2}$ = 1.12 µs, and so on. It takes 1.51 µs maximum ($t_{pd3} + (15 \times t_d) + t_{pd2}$) from the first GSCLK rising edge until all LOD become valid; $t_{su}LOD$ must be greater than 1.51 µs (see Figure 20) to ensure that all LOD data are valid.

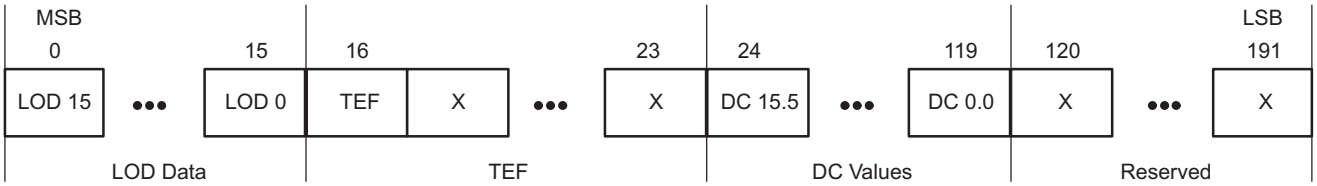


Figure 19. Status Information Data Packet Format

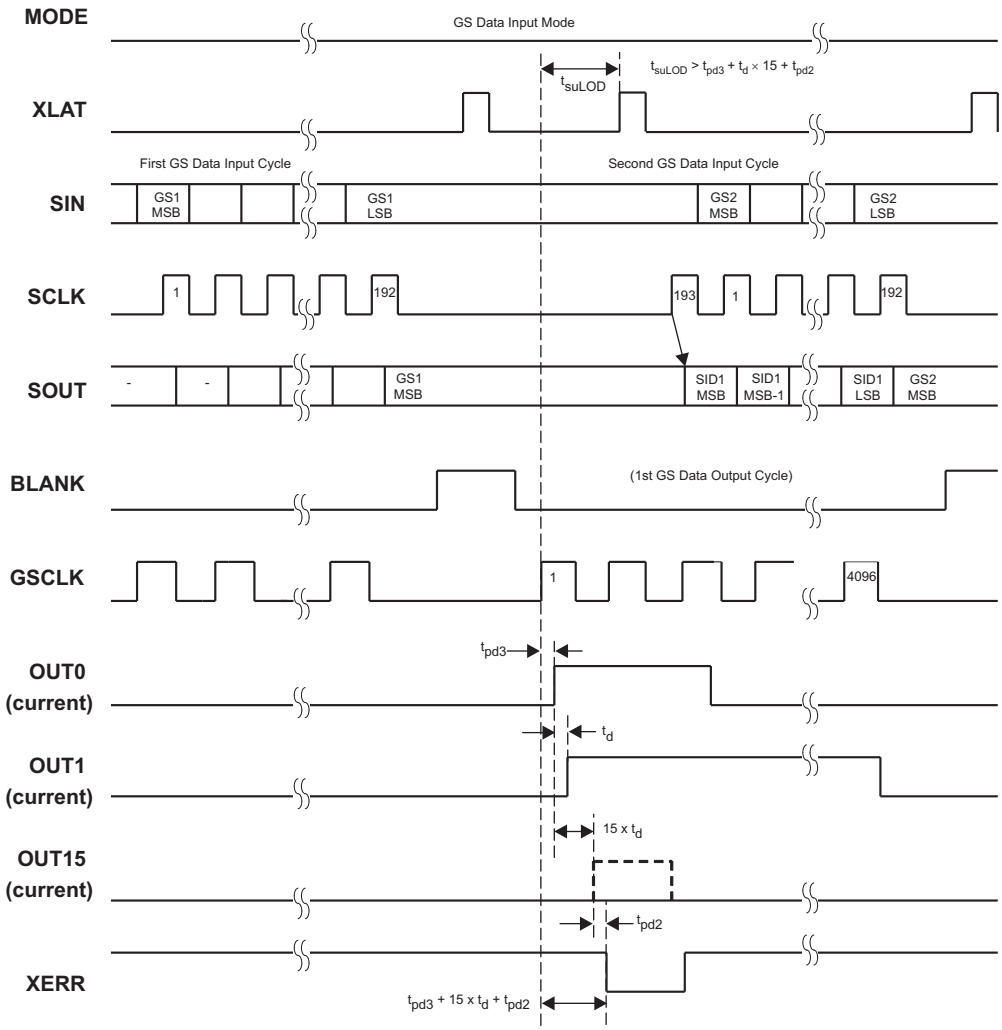


Figure 20. Readout Status Information Data (SID) Timing Chart

The LOD status of each output can be read out from the SOUT pin. The LOD error bits are latched into the Status Information Data when XLAT returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while XERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

GRAYSCALE PWM OPERATION

The grayscale PWM cycle starts with the falling edge of BLANK. The first GSCLK pulse after BLANK goes low increases the grayscale counter by one and switches on all OUTn with a grayscale value not equal to zero. Each following rising edge of GSCLK increases the grayscale counter by one. The TLC59401 compares the grayscale value of each output OUTn with the grayscale counter value. All OUTn with grayscale values equal to the counter values are switched off. A high BLANK signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle ,as Figure 21 shows. When the counter reaches a count of FFFh, the counter stops counting and all outputs turn off. Pulling BLANK high before the counter reaches FFFh immediately resets the counter to zero.

If there are any unconnected outputs (OUTn), including LEDs in a failed short or failed open condition, the GS data corresponding to the unconnected output should be set to '0' before turning on the LEDs. Otherwise, the VCC supply current (I_{CC}) increases while the constant-current output is on.

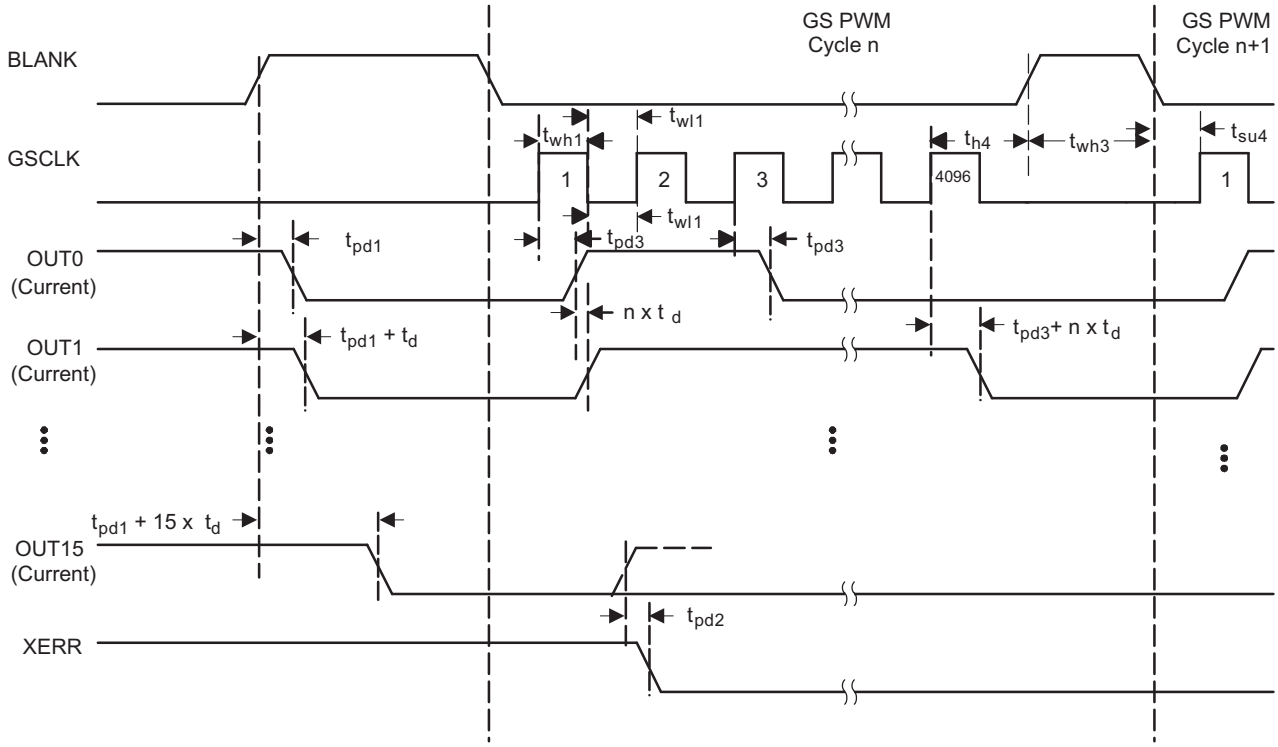


Figure 21. Grayscale PWM Cycle Timing Chart

Output On-Time

The amount of time that each output is turned on is a function of the grayscale clock frequency and the programmed grayscale PWM value. The on-time of each output can be calculated using Equation 10.

$$T\_on_n = \frac{GSn}{f_{(GSCLK)}} + t_{on\_err} \quad (10)$$

where:

T_on_n is the time that OUTn turns on and sinks current

GSn is the OUTn programmed grayscale PWM value between 0 and 4095

t_{on_err} is the output on-time error defined in the Switching Characteristics Table

When using Equation 10 with very high GSCLK frequencies and very low grayscale PWM values, the resulting T_on-time may be negative. If T_on is negative, the output does not turn on. For example, using $f_{(GSCLK)}$ = 30 MHz, GSn = 1, and the typical t_{on_err} = 50 ns, Equation 10 calculates that OUTn turns on for –16.6 ns. This output may not turn on under these conditions. Increasing the PWM value or reducing the GSCLK clock frequency ensures turn-on.

SERIAL DATA TRANSFER RATE

Figure 22 shows a cascading connection of *n* TLC59401 devices connected to a controller, building a basic module of an LED display system. There is no TLC59401 limitation to the maximum number of ICs that can be cascaded. The maximum number of cascading TLC59401 devices depends on the application system. Equation 11 calculates the minimum frequency needed:

$$f_{(GSCLK)} = 4096 \times f_{(update)}$$

$$f_{(SCLK)} = 193 \times f_{(update)} \times n \quad (11)$$

where:

$f_{(GSCLK)}$: minimum frequency needed for GSCLK

$f_{(SCLK)}$: minimum frequency needed for SCLK and SIN

$f_{(update)}$: update rate of whole cascading system

n: number cascaded of TLC59401 device

APPLICATION EXAMPLE

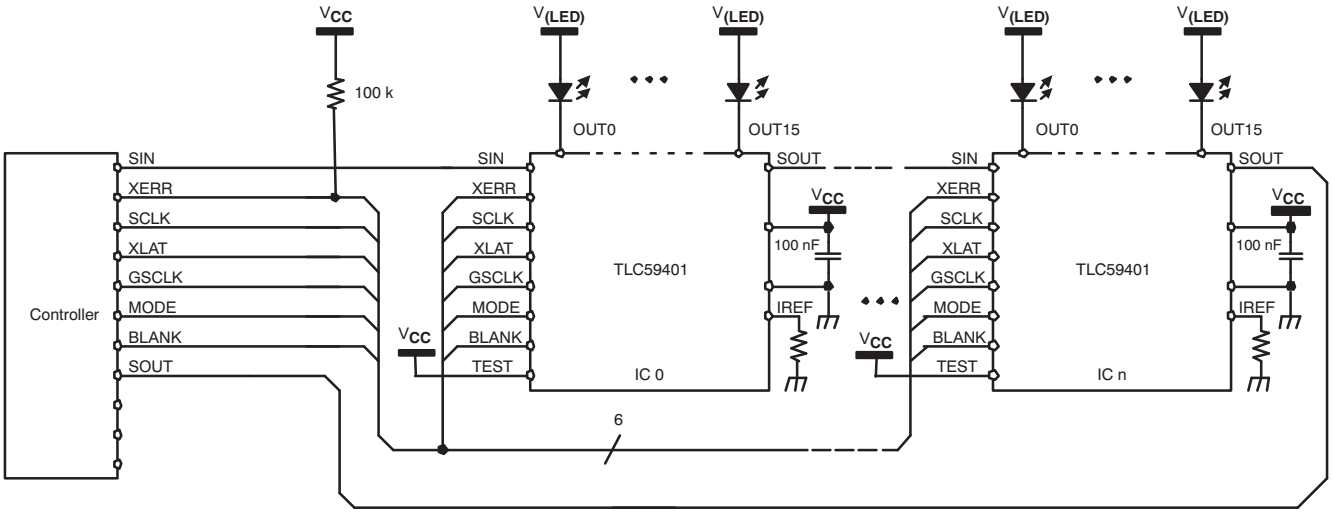


Figure 22. Cascading Devices

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59401PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59401	Samples
TLC59401PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59401	Samples
TLC59401RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 59401	Samples
TLC59401RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 59401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

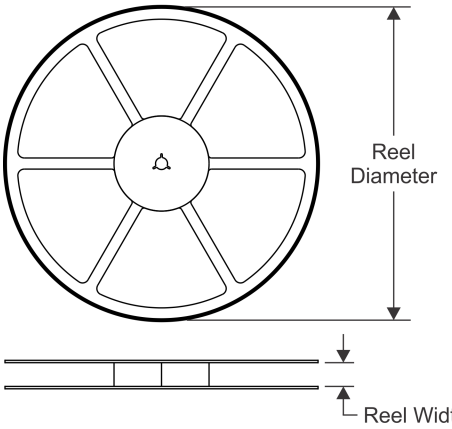
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

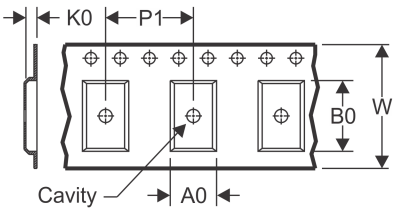
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

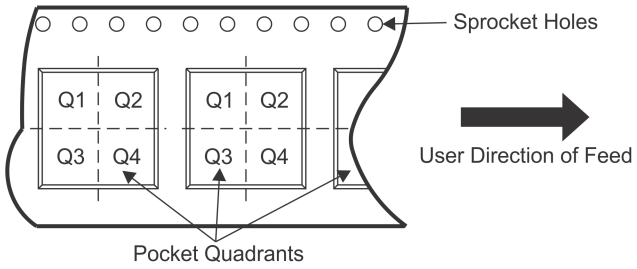


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

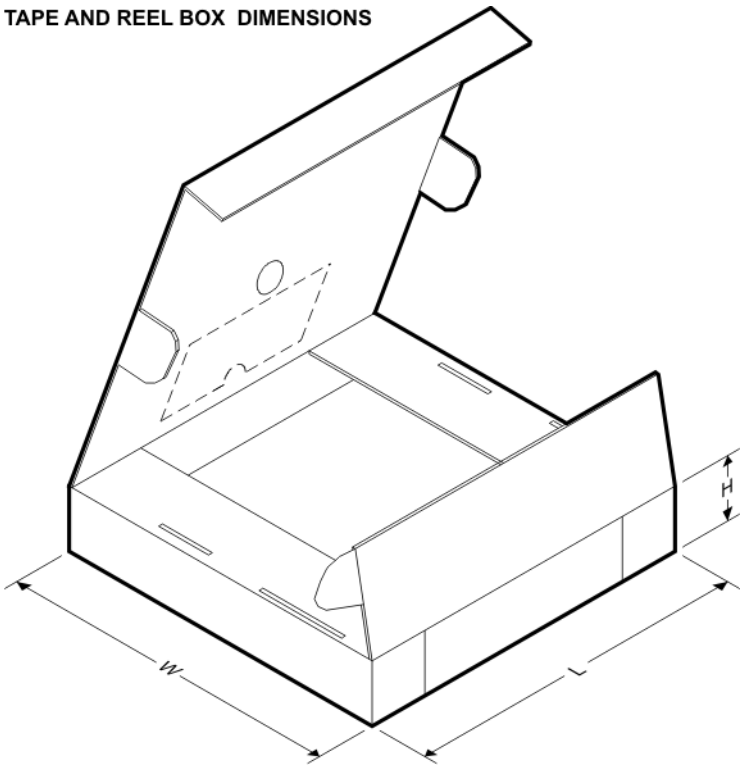
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59401PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC59401RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC59401RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59401PWPR	HTSSOP	PWP	28	2000	853.0	449.0	35.0
TLC59401RHBR	VQFN	RHB	32	3000	853.0	449.0	35.0
TLC59401RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

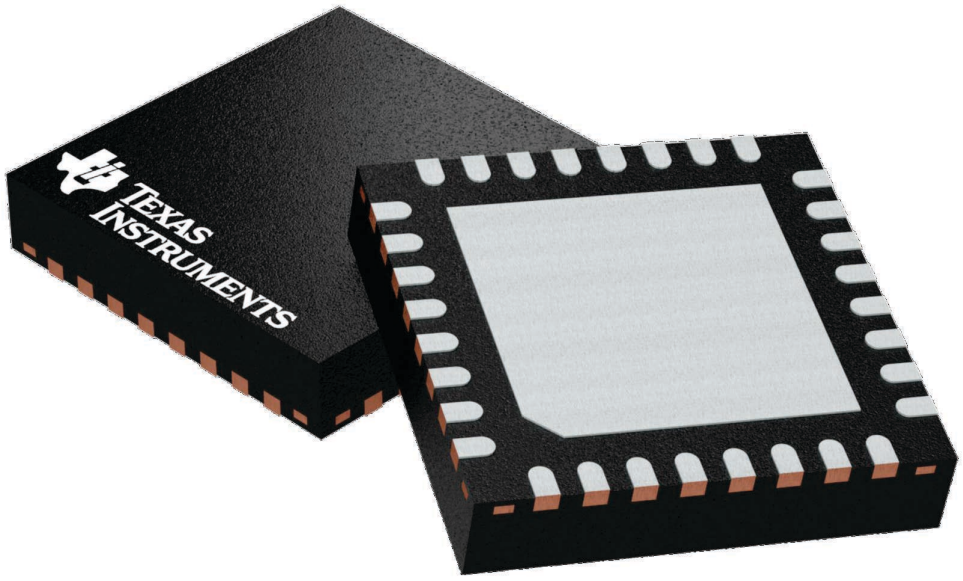
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

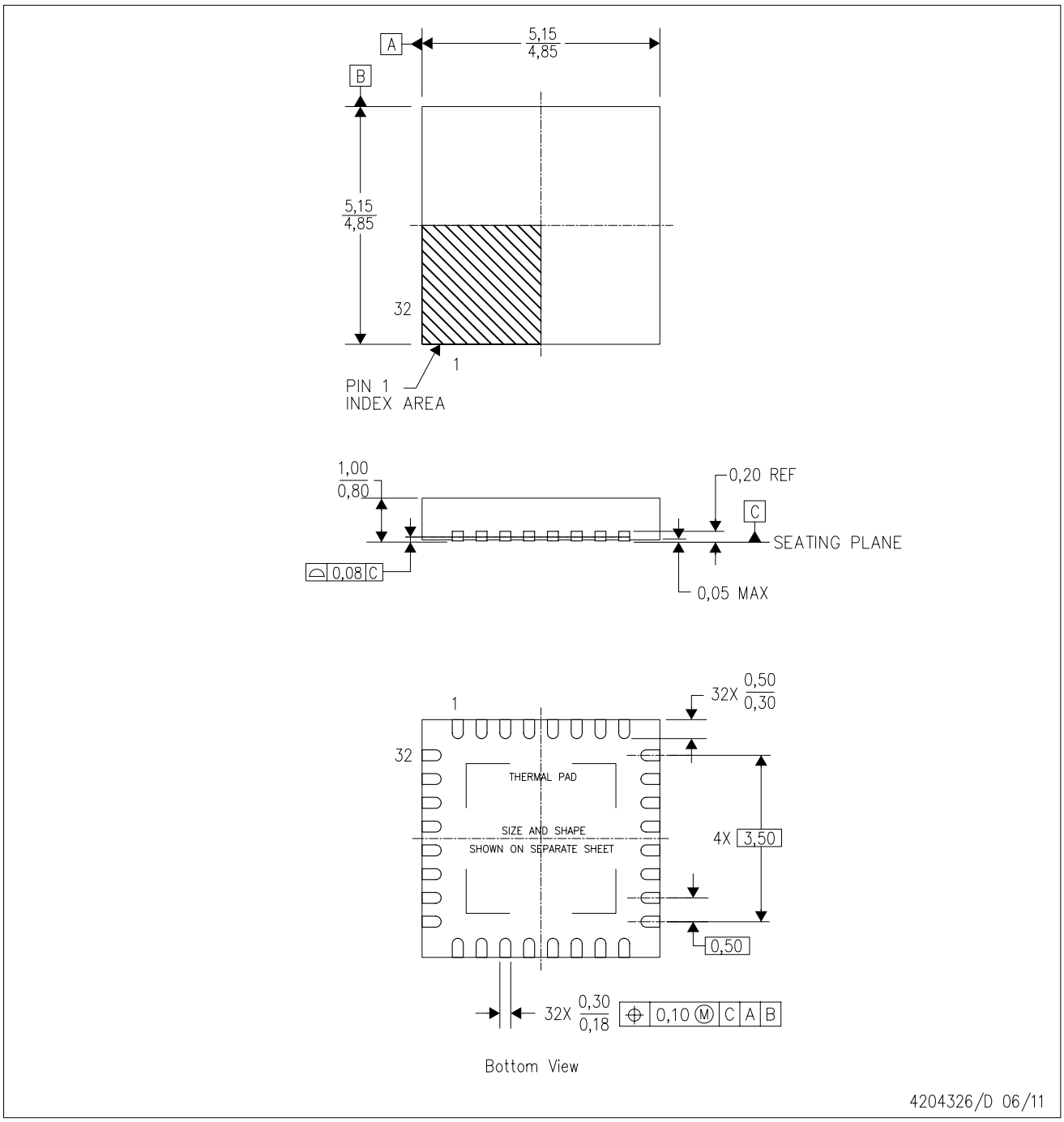
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

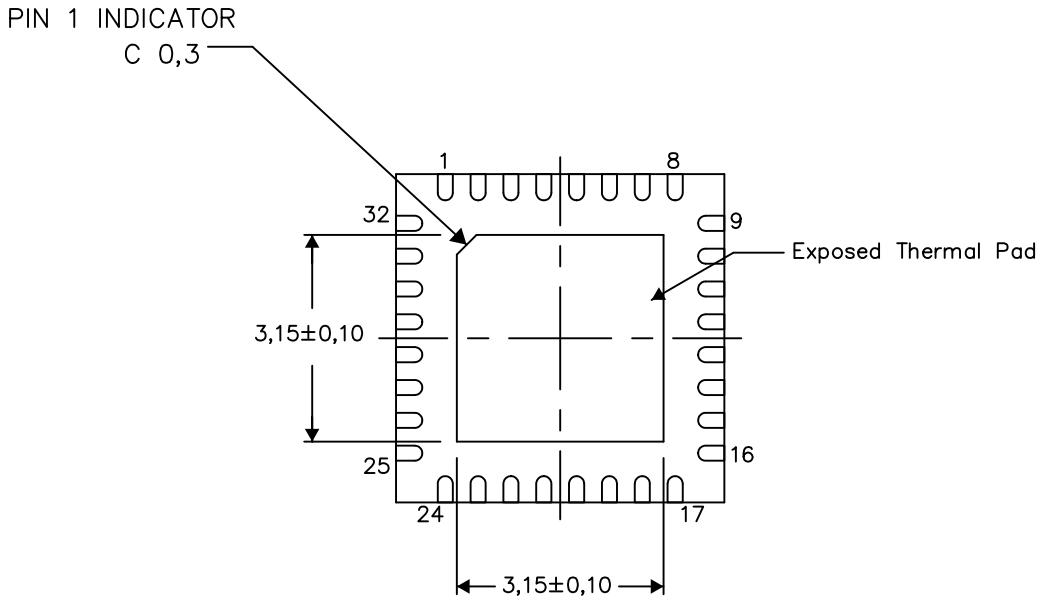
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



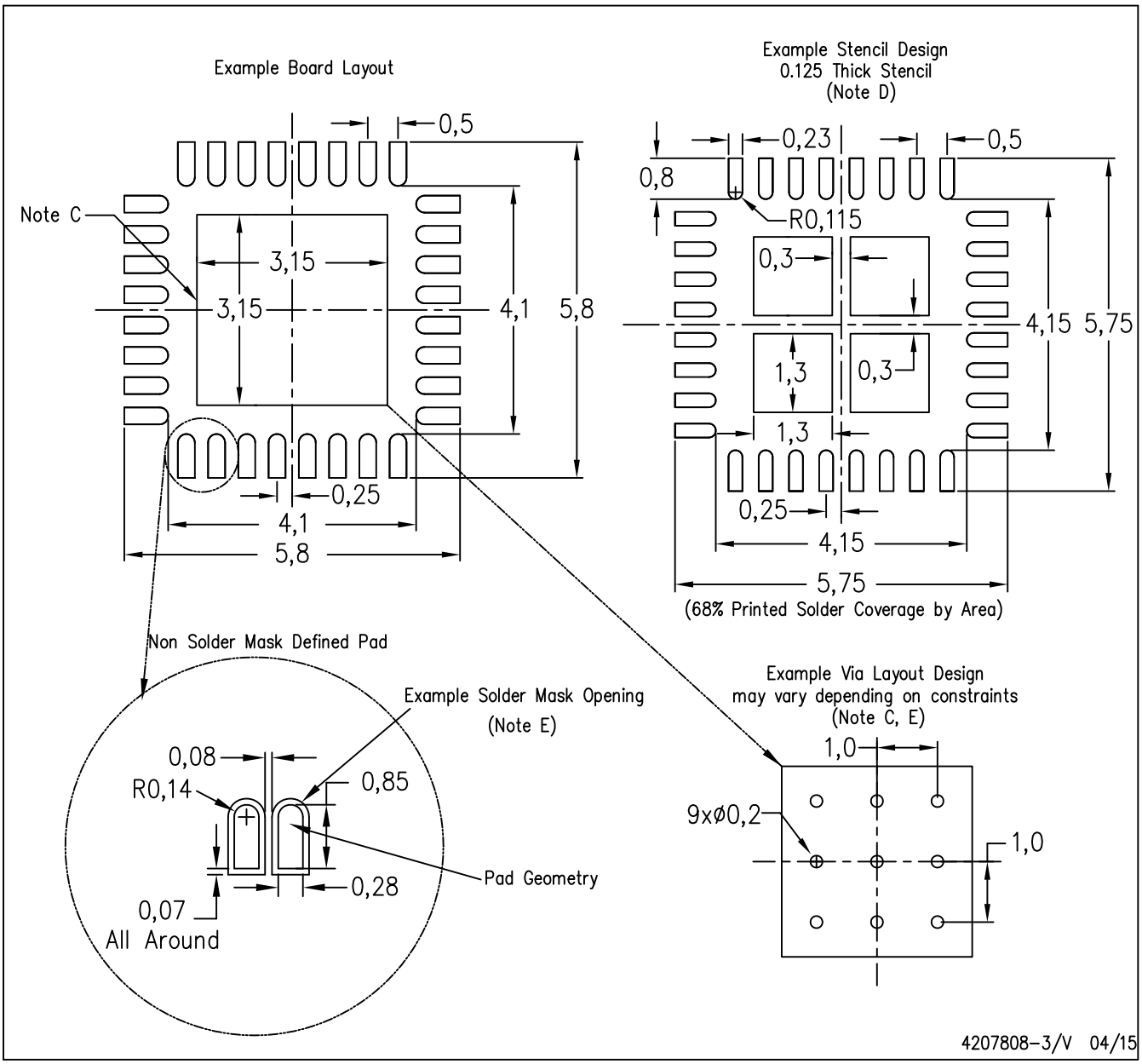
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

GENERIC PACKAGE VIEW

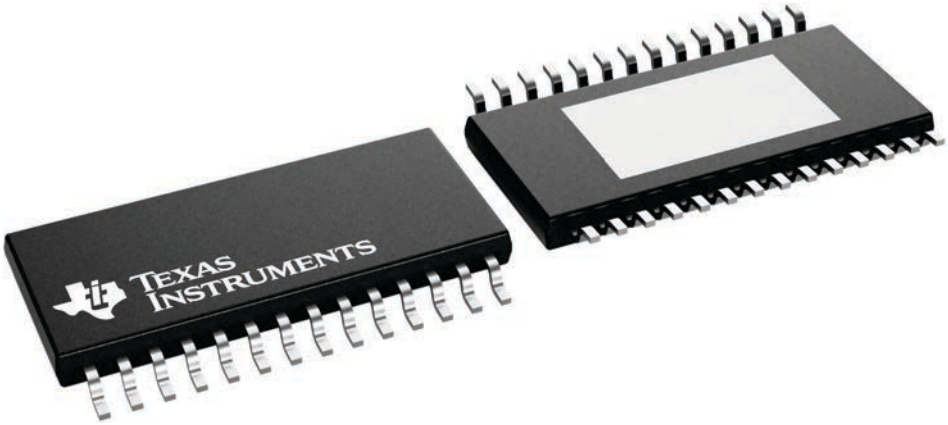
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

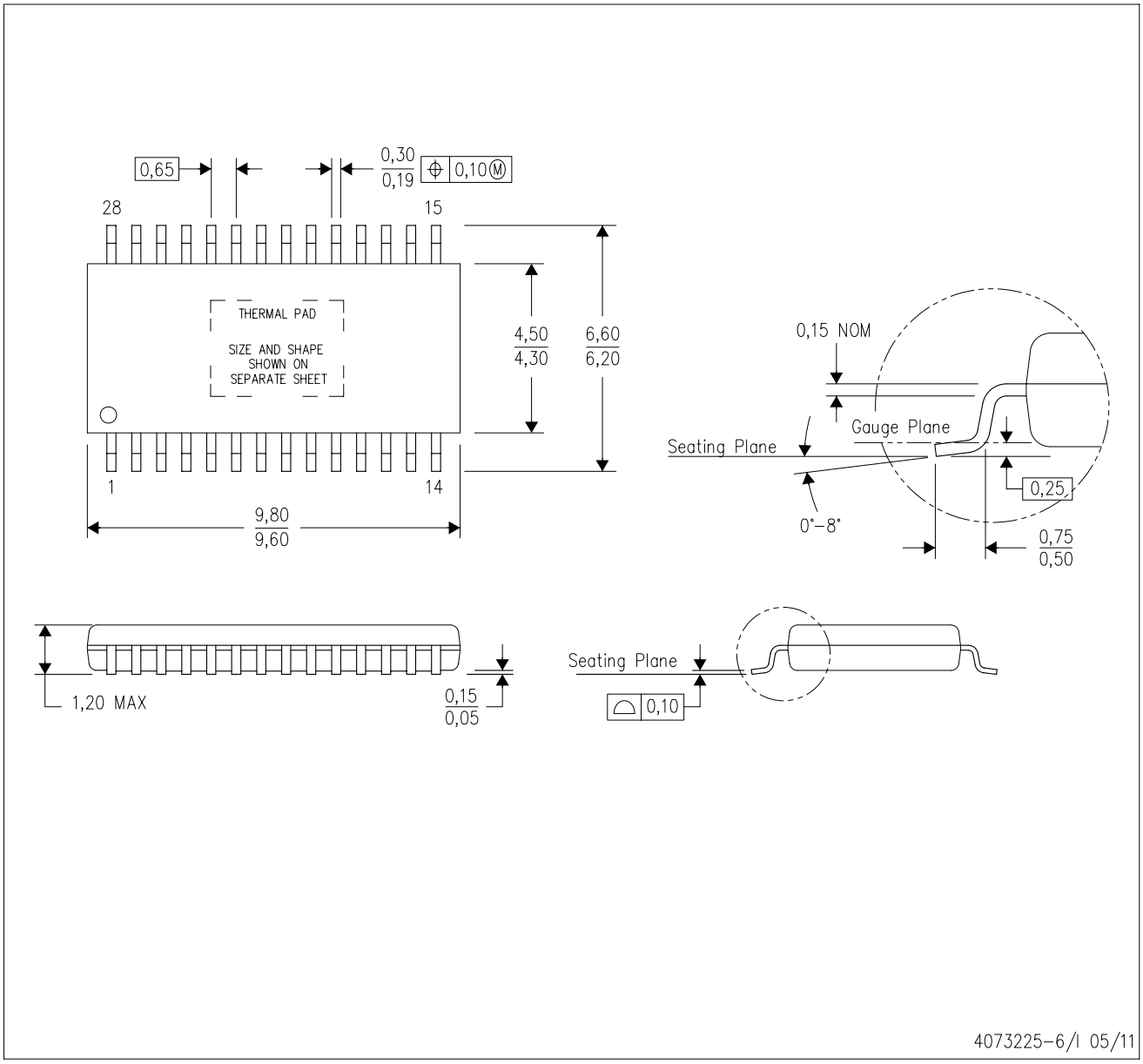
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

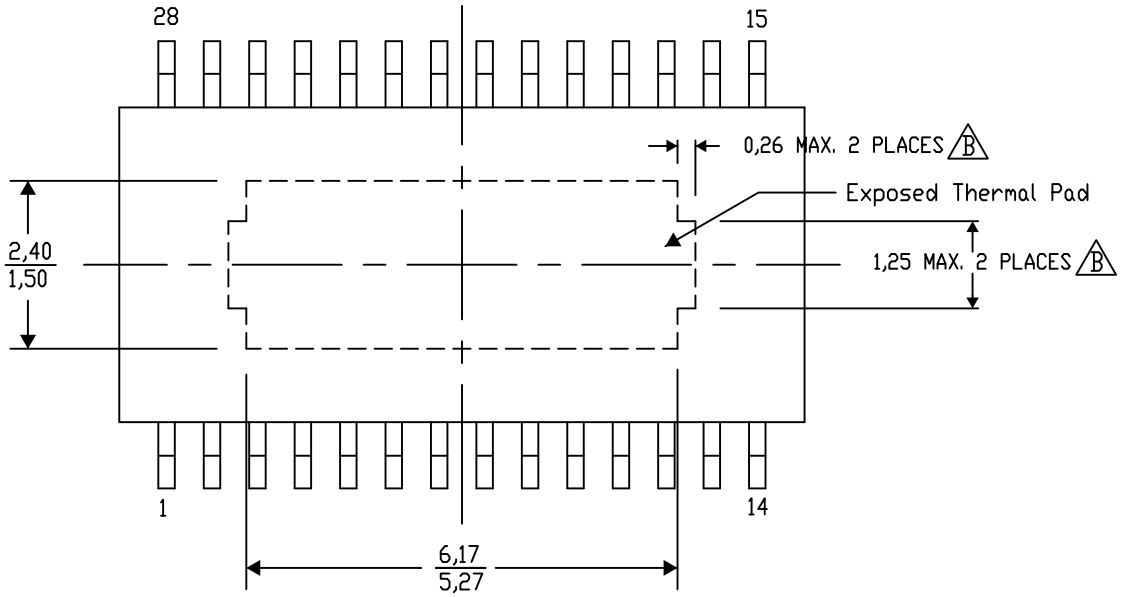
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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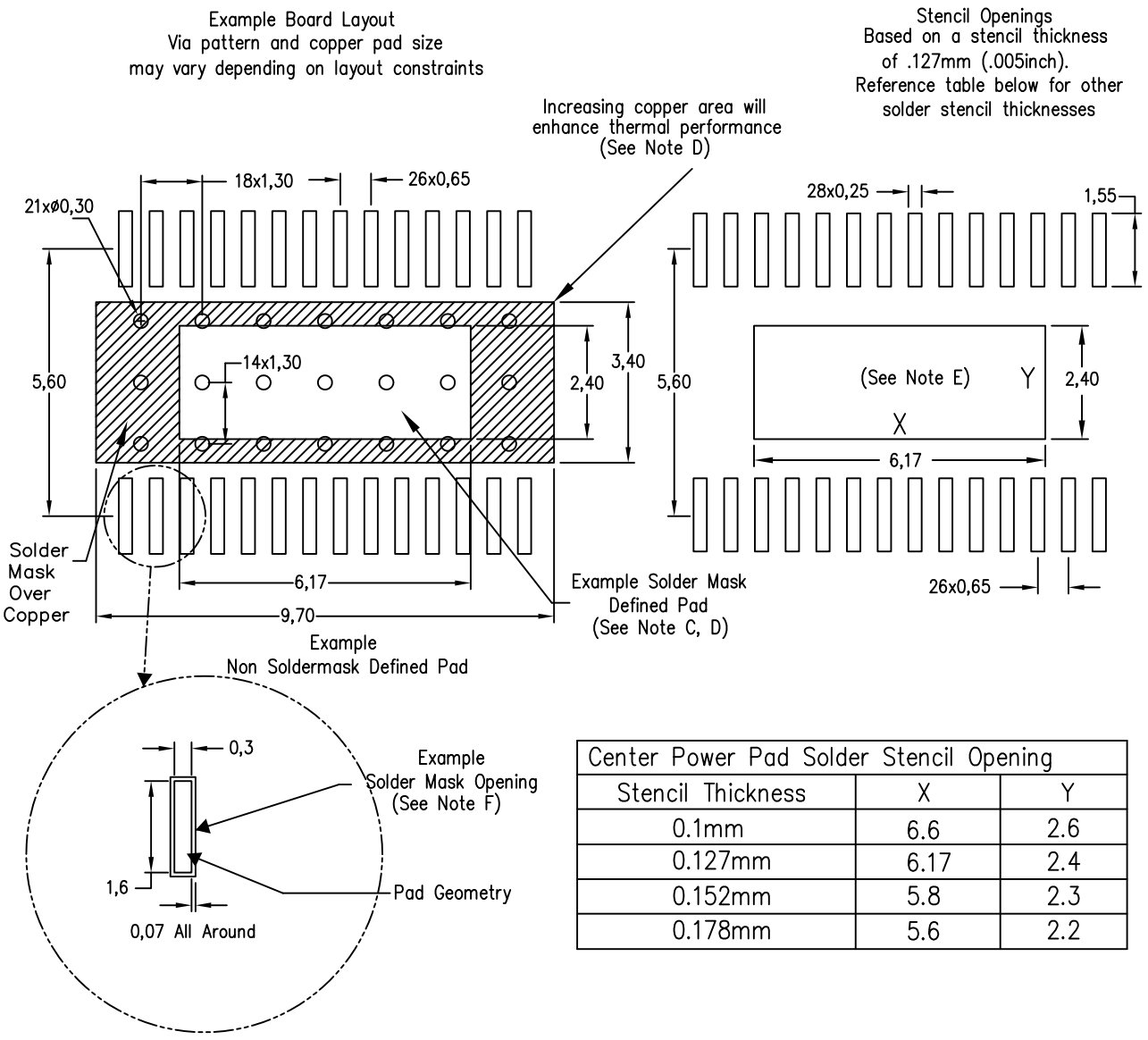

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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