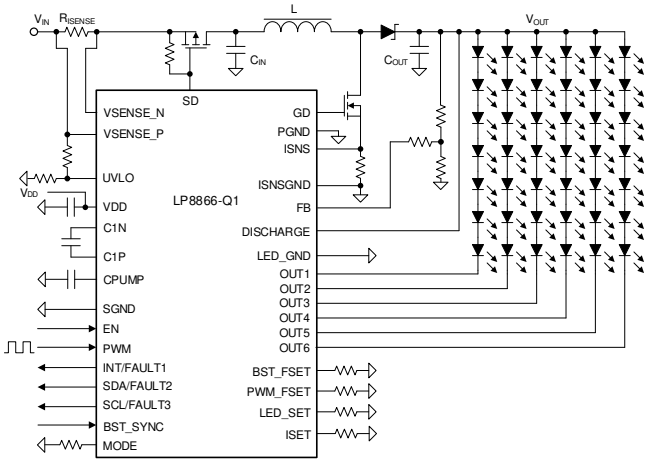
具有六个 200mA 通道LP8866-Q1 汽车显示 LED 背光驱动器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：
    –40°C 至 +125°C，T_A
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 输入电压工作范围：3V 至 48V
- 六路高精度电流阱
  - 各电流阱直流电流高达 200mA
  - 电流匹配度为 1%（典型值）
  - 使用 152Hz LED 输出 PWM 频率时，调光比为 32000:1
  - 使用 I2C 或 PWM 输入时，最高 16 位 LED 调光分辨率
  - 可配置 8 个 LED 灯串
- 自动移相 PWM 调光
- 最高 48V V_{OUT} 升压或 SEPIC 直流/直流控制器
  - 开关频率为 100kHz 至 2.2MHz
  - 升压扩频功能可降低 EMI
  - 升压同步输入，可通过外部时钟设置升压开关频率
  - 禁用升压时，输出电压自动放电
- 多种故障诊断功能

简化原理图



2 应用

- 为以下应用提供背光：
  - 汽车信息娱乐系统
  - 汽车仪表组
  - 智能车镜
  - 抬头显示屏 (HUD)
  - 中央信息显示屏 (CID)
  - 音视频导航 (AVN)

3 说明

LP8866-Q1 是一款具有升压控制器的汽车高效 LED 驱动器。六路高精度电流阱支持根据使用的通道数自动调整相移。可通过 I²C 接口或 PWM 输入对 LED 亮度进行全局控制。

升压控制器具有基于 LED 电流阱余量电压的自适应输出电压控制。该特性可在所有条件下将升压电压调节到能够满足需要的最低水平，从而最大限度降低功耗。凭借宽范围可调频率，LP8866-Q1 可避免调幅 (AM) 射频波段的干扰。

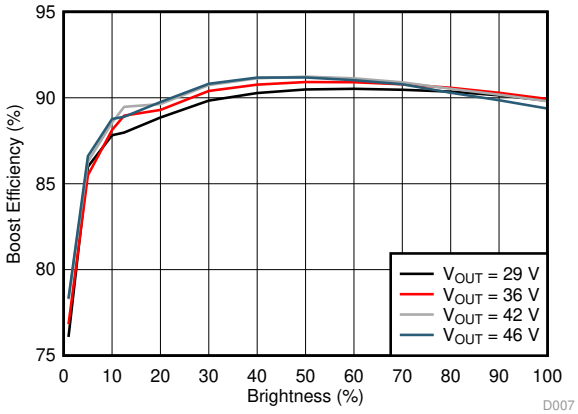
LP8866-Q1 支持内置混合 PWM 调光和模拟电流调光，从而可降低 EMI、延长 LED 使用寿命并提高总光学效率。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LP8866-Q1	HTSSOP (38)	9.70mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

系统效率



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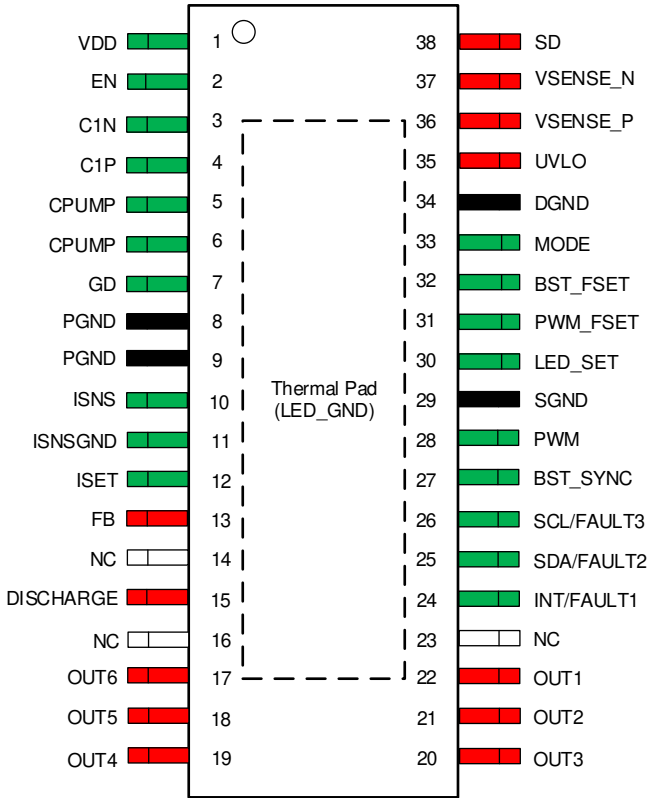
4 修订历史记录

日期	修订版本	说明
2019 年 12 月	*	初始发行版

5 Pin Configuration and Functions

DCP Package
38-Pin HTSSOP
Top View



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Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD	Power	Power supply input for internal analog and digital circuit. Connect a 10uF capacitor between the VDD pin to GND
2	EN	Analog	Enable input
3	C1N	Analog	Negative input for charge pump flying capacitor. If feature not used leave this pin floating.
4	C1P	Analog	Positive input for charge pump flying capacitor. If feature not used leave this pin floating.
5	CPUMP	Power	Charge pump output pin. Connect to VDD if charge pump is not used. A 4.7 µF decoupling capacitor is recommended on CPUMP pin.
6	CPUMP	Power	Charge pump output pin. Always connects with pin 5.
7	GD	Analog	Gate driver output for external N-FET
8	PGND	GND	Power ground
9	PGND	GND	Power ground
10	ISNS	Analog	Boost current sense pin
11	ISNSGND	GND	Current sense resistor GND.
12	ISET	Analog	LED full-scale current setup through external resistor
13	FB	Analog	Boost feedback input
14	NC	N/A	No connect - Leave floating.
15	DISCHARGE	Analog	Boost output voltage discharge pin. Connect to Boost output.
16	NC	N/A	No connect - Leave floating.
17	OUT6	Analog	LED current sink output. If unused tie to ground.
18	OUT5	Analog	LED current sink output. If unused tie to ground.
19	OUT4	Analog	LED current sink output. If unused tie to ground.
20	OUT3	Analog	LED current sink output. If unused tie to ground.
21	OUT2	Analog	LED current sink output. If unused tie to ground.
22	OUT1	Analog	LED current sink output. If unused tie to ground.
23	NC	N/A	No connect - Leave floating.
24	INT/FAULT1	Analog	Device fault interrupt output, open drain.FAULT1 output if I2C interface is disabled. A 10-kΩ pullup resistor is recommended.
25	SDA/FAULT2	Analog	SDA for I2C interface. FAULT2 output if I2C interface is disabled. A 10-kΩ pullup resistor is recommended.
26	SCL/FAULT3	Analog	SCL for I2C interface. FAULT3 output if I2C interface is disabled. A 10-kΩ pullup resistor is recommended.
27	BST_SYNC	Analog	Input for synchronizing boost. When synchronization is not used, connect this pin to ground to disable spread spectrum or to VDD to enable spread spectrum.
28	PWM	Analog	PWM input for brightness control. Tie to GND if unused.
29	SGND	GND	Signal ground
30	LED_SET	Analog	LED string configuration through external resistor. Do not leave floating.
31	PWM_FSET	Analog	LED dimming frequency setup through external resistor. Do not leave floating.
32	BST_FSET	Analog	Boost switching frequency setup through external resistor. Do not leave floating.
33	MODE	Analog	Dimming mode setup through external resistor. Do not leave floating.
34	DGND	GND	Digital ground
35	UVLO	Analog	Input voltage sense for programming input UVLO threshold through external resistor to VIN
36	VSENSE_P	Analog	Pin for input voltage detection for OVP protection and positive input for input current sense.
37	VSENSE_N	Analog	Negative input for input current sense. If input current sense is not used, please tie to VSENSE_P pin.
38	SD	Analog	Power line FET control. Open Drain output. If unused, leave this pin floating.
DAP	LED_GND	GND	LED ground connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Voltage on pins	VSENSE_P, VSENSE_N, UVLO, SD, FB, DISCHARGE, OUT1 to OUT6	–0.3	52	V
	C1N, C1P, VDD, EN, PWM, ISNS, ISNS_GND, FAULT1/INT, FAULT2/SDA, FAULT3/SCL, MODE, PWM_FSET, BST_FSET, LED_SET, ISET, GD and BST_SYNC, CPUMP	–0.3	6	V
	Continuous power dissipation(3)		Internally Limited	W
Thermal	Ambient temperature, TA(4)	–40	125	
	Junction temperature, TJ(4)	–40	150	°C
	Lead temperature (soldering)		260	°C
	Storage temperature, Tstg	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 150°C (typical).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX} = 150°C), the power dissipation of the device in the application (P), the junction-to-board thermal resistance and the temperature difference between the system board and the ambient (Δt_{BA}), which is given by the following equation: $T_{A-MAX} = T_{J-MAX} – (\Theta_{JB} \times P) - \Delta t_{BA}$

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 19, 20 and 38)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Voltage on pins	VSENSE_P, VSENSE_N, SD, UVLO	3	12	48	V
	FB, OUT1 to OUT6	0		48	
	ISNS, ISNSGND	0		5.5	
	EN, PWM, FAULT1/INT, FAULT2/SDA, FAULT3/SCL, BST_SYNC	0	3.3	5.5	
	VDD	3	3.3/5	5.5	
	C1N, C1P, CPUMP,GD	0	5	5.5	
Thermal	Ambient temperature, T_A	–40		125	°C

(1) All voltages are with respect to the potential at the GND pins.

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6.4 Thermal Information

THERMAL METRIC(1)		LP8866-Q1 HTTSOP 38-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	32.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.8	
Ψ_{JT}	Junction-to-top characterization parameter	0.3	
Ψ_{JB}	Junction-to-board characterization parameter	8.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6.5 Electrical Characteristics

Limits apply over the full operation temperature range –40°C ≤T_A ≤ +125°C , unless otherwise speicified. V_{IN} = 12 V, VDD = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Electrical Characteristics						
I_Q	Shutdown mode current, VDD pin	EN = L		0.001	TBD	mA
I_Q	Active mode current, VDD pin	FSW = 303kHz, PWM = H, BOOST-FET IPD25N06S4L-30, Charge Pump Disabled		20	TBD	mA
I_Q	Active mode current, VDD pin	FSW = 2200kHz, PWM = H, BOOST-FET IPD25N06S4L-30, Charge Pump Disabled		40	TBD	mA
I_Q	Active mode current, VDD pin	FSW = 303kHz, PWM = H, BOOST-FET IPD25N06S4L-30, Charge Pump Enabled		25	TBD	mA
I_Q	Active mode current, VDD pin	FSW = 2200kHz, PWM = H, BOOST-FET IPD25N06S4L-30, Charge Pump Enabled		45	TBD	mA
CPUMP and LDO Electrical Characteristics						
V_{CPUMP}	Voltage accuracy	V_{DD} = 3.0 to 3.6V; I_{LOAD} = 1 to 50mA	4.8	5	5.2	V
f_{CP}	CP switching frequency		387	417	447	kHz
V_{CPUMP_UVLO}	VCPUMP UVLO threshold	V_{CPUMP} falling edge	4	4.2	4.4	V
V_{CPUMP_UVLO}	VCPUMP UVLO threshold	V_{CPUMP} rising edge	4.2	4.4	4.6	V
V_{CPUMP_HYS}	VCPUMP UVLO hysteresis		0.1	0.2		V
T_{START_UP}	Charge pump startup time	C_{CPUMP} = 10µF		1000	2000	µs
Protection Electrical Characteristics						
VDD_{UVLO_F}	V_{DD} UVLO threshold	V_{DD} falling	2.7	2.8	2.9	V
VDD_{UVLO_R}	V_{DD} UVLO threshold	V_{DD} rising			3.0	V
VDD_{UVLO_H}	V_{DD} UVLO hysteresis			0.1		V
VIN_{UVLO_TH}	UVLO pin threshold	V_{UVLO} falling	0.763	0.787	0.811	V
I_{UVLO}	UVLO pin bias current	V_{UVLO} = V_{UVLO_TH} + 50mV		–5		µA
VIN_{OVP_TH}	OVP threshold	VSENSE_P rising	40.8	43	45.2	V

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Electrical Characteristics (continued)

Limits apply over the full operation temperature range –40°C ≤T_A ≤ +125°C , unless otherwise speicified. V_{IN} = 12 V, VDD = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_{OVP_HYS}	OVP hysteresis			2.5		V
VIN_{OCP_TH}	Input OCP threshold	R_{ISENSE} = 20mΩ	187	220	253	mV
T_{SD}	Thermal shutdown threshold	Temperature rising	150	165	180	°C
T_{SD}	Thermal shutdown hysteresis			15		°C
$I_{SD\_LEAKAGE}$	SD leakage current	V_{SD} = 48V		1		µA
I_{SD}	SD pull down current	R_{SD} = 20kΩ	250	325	400	µA
V_{FB_OVPL}	FB pin - Boost OVP low threshold			1.423		V
V_{FB_OVPH}	FB pin - Boost OVP high threshold			1.76		V
V_{FB_UVP}	FB pin - Boost OCP threshold			0.886		V
V_{BST_OVPH}	Discharge pin - Boost OVP high threshold		48.5	50	51.5	V
Input PWM Electrical Characteristics						
$I_{PWM\_LEAKAGE}$	PWM leakage current	V_{PWM} = 5V		1		µA
f_{PWM_IN}	PWM input frequency		100		20000	Hz
$t_{PWM\_MIN\_ON}$	PWM input minimum on-time	Direct PWM mode			200	ns
$t_{PWM\_MIN\_ON}$	PWM input minimum on-time	Phase Shift PWM mode, Hybrid mode, Current Dimming mode		200	220	ns
PWM_INRES	PWM input resolution	f_{PWM_IN} = 100 Hz		16		bit
PWM_INRES	PWM input resolution	f_{PWM_IN} = 20 kHz		10		bit
LED Current Sink and LED PWM Electrical Characteristics						
$I_{LEAKAGE}$	Leakage current on OUTx	OUTx = V_{OUT} = 45V, EN= L		0.1	2.5	µA
I_{MAX}	Maximum LED sink current	OUTx		200		mA
V_{ISET}	ISET voltage		1.18	1.21	1.24	V
V_{ISET_UVLO}	ISET pin undervoltage		0.97	1	1.03	V
R_{ISET}	ISET Resistor range	I_{OUT} = 30mA to 200mA	15.6		104	kΩ
I_{LED_LIMIT}	LED current limit when ISET pin short to GND			280		mA
I_{ACC}	LED sink current accuracy	R_{ISET} = 15.6kΩ, I_{OUT} = 200mA, PWM = 100%	-4		4	%
I_{MATCH}	LED sink current matching	R_{ISET} = 15.6kΩ, I_{OUT} = 200mA, PWM = 100%		1	3.5	%
f_{DIM}	LED dimming frequency	PWM_FSET =3.92 kΩ	141	152	163	Hz
f_{DIM}	LED dimming frequency	PWM_FSET =4.75 kΩ	283	305	327	
f_{DIM}	LED dimming frequency	PWM_FSET =5.76 kΩ	567	610	653	
f_{DIM}	LED dimming frequency	PWM_FSET =7.87 kΩ	1135	1221	1307	
f_{DIM}	LED dimming frequency	PWM_FSET =11 kΩ	2270	2441	2612	
f_{DIM}	LED dimming frequency	PWM_FSET =17.8 kΩ	4541	4883	5225	
f_{DIM}	LED dimming frequency	PWM_FSET =42.4 kΩ	9082	9766	10450	
f_{DIM}	LED dimming frequency	PWM_FSET =124 kΩ	18163	19531	20899	
DIM	Dimming ratio	f_{PWM_OUT} = 152Hz		32000:1		
DIM	Dimming ratio	f_{PWM_OUT} = 4.88kHz		1000:1		

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Electrical Characteristics (continued)

Limits apply over the full operation temperature range –40°C ≤T_A ≤ +125°C , unless otherwise speicified. V_{IN} = 12 V, VDD = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HEADROOM}$	LED sink headroom			0.7		V
$V_{HEADROOM\_HYS}$	LED sink headroom hysteresis			0.5		V
$V_{LEDSHORT}$	LED internal short threshold			6		V
$V_{SHORTGND}$	LED short to ground threshold			0.24		V
t_{PWM_OUT}	LED output minimum pulse			200		ns
Boost Converter Electrical Characteristics						
f_{SW}	Switching Frequency	BST_FSET =3.92 kΩ	93	100	107	kHz
f_{SW}	Switching Frequency	BST_FSET =4.75 kΩ	186	200	214	
f_{SW}	Switching Frequency	BST_FSET =5.76 kΩ	281	303	325	
f_{SW}	Switching Frequency	BST_FSET =7.87 kΩ	372	400	428	
f_{SW}	Switching Frequency	BST_FSET =11 kΩ	465	500	535	
f_{SW}	Switching Frequency	BST_FSET =17.8 kΩ	1690	1818	1946	
f_{SW}	Switching Frequency	BST_FSET =42.4 kΩ	1860	2000	2140	
f_{SW}	Switching Frequency	BST_FSET =124 kΩ	2066	2222	2378	
I_{LIM}	External FET current limit	V_{ISNS} threshold, RISNS= 15 to 50 mΩ	180	200	220	mV
I_{SEL_MAX}	IDAC maximum current	V_{DD} = 3.3 V	36.76	38.7	40.64	µA
R_{DS_ONH}	R_{DSON} of high-side FET to gate driver	V_{GD}/(R_{DS_ON} + total resistance to gate input of SW FET) must not be higher than 2.5 A		1.4		Ω
R_{DS_ONL}	R_{DSON} of low-side FET to gate driver	V_{GD}/(R_{DS_ON} + total resistance to gate input of SW FET) must not be higher than 2.5 A		0.75		Ω
t_{STARUP}	Start-up time	Delay from beginning of boost Soft-start to when LED drivers can begin		50		ms
T_{ON}	Minimum switch on-time			120		ns
T_{OFF}	Minimum switch off time			70		ns

6.6 Logic Interface Characteristics

Limits apply over the full operation temperature range –40°C ≤ T_A ≤ +125°C , unless otherwise speicified. V_{IN} = 12 V, VDD = 5 V, V_{EN} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT EN						
VEN_{IL}	EN logic low threshold				0.4	V
VEN_{IH}	EN logic high threshold		1.2			V
R_{ENPD}	EN pin internal pull down resistance			1		MΩ
LOGIC INPUT SDA, SCL, BST_SYNC and PWM						
V_{IL}	Logic low threshold	V_{DD} = 3.3V and 5V			0.4	V
V_{IH}	Logic high threshold	V_{DD} = 3.3V and 5V	1.2			V
LOGIC OUTPUT SDA, INT, FAULT2 and FAULT3						
V_{OL}	Output level low	I = 3mA		0.2	0.4	V
$I_{LEAKAGE}$	Output leakage current	V = 3.3V			1	µA

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6.7 Timing Requirements for I2C Interface

Limits apply over the full operation temperature range –40°C ≤ T_A ≤ +125°C , unless otherwise speicified. V_{IN} = 12 V, VDD = 5 V, V_{EN} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK}	Clock frequency				400	kHz
1	Hold time (repeated) START condition		0.6			µs
2	Clock low time		1.3			µs
3	Clock high time		600			ns
4	Set-up time for a repeated START condition		600			ns
5	Data hold time		50			ns
6	Data setup time		100			ns
7	Rise time of SDA and SCL				300	ns
8	Fall time of SDA and SCL				300	ns
9	Set-up time for STOP condition		600			ns
10	Bus free time between a STOP and a START condition		1.3			µs

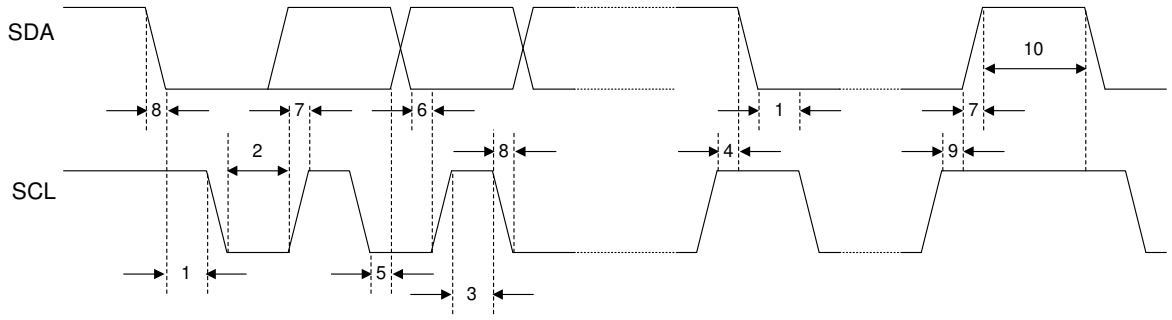

图 1. I2C Timing Diagram

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7 Detailed Description

7.1 Overview

The LP8866-Q1 device is a high-voltage LED driver for automotive infotainment, clusters, HUD and other automotive display LED backlight applications. PWM input is used for brightness control by default. Alternatively, the brightness can also be controlled by I2C Interface.

The boost frequency, LED PWM frequency, and LED string current are configured with external resistors through the BST_FSET, PWM_FSET, and ISET pins. The INT pin is used to report faults to the system. Fault interrupt status can be cleared with the I2C interface, or is cleared on the falling edge of the EN pin.

The LP8866-Q1 supports pure PWM dimming. The six LED current drivers provide up to 200 mA per output and can be tied together to support higher current LEDs. The maximum output current of the LED drivers is set with the ISET resistor and can be optionally scaled by the LEDx_CURRENT[11:0] register bits with I2C interface. The LED output PWM frequency is set with a PWM_FSET resistor. The number of connected LED strings is configured by the LED_SET resistor, and the device automatically selects the corresponding phase shift mode. For example, if the device is set to 4-strings mode, each LED output is phase shifted by 90 degrees with each other(= 360 / 4). Unused outputs, which must be connected to GND, will be disabled and excluded from adaptive voltage and won't generate any LED faults.

A resistor divider connected from V_{OUT} to the FB pin sets the maximum voltage of the boost. For best efficiency, the boost voltage is adapted automatically to the minimum necessary level needed to drive the LED strings by monitoring all the LED output voltages continuously. The switching frequency of the boost regulator can be set between 100 kHz and 2.2 MHz by the BST_FSET resistor. The boost has a start-up feature that reduces the peak current from the power-line during start-up. The LP8866-Q1 can also control a power-line FET to reduce battery leakage when disabled and provide isolation and protection in the event of a fault.

Fault detection features of LP8866-Q1 include:

- Open-string and shorted LED detection
  - LED fault detection prevents system overheating in case of open or short in some of the LED strings
- LED short-to-ground detection
- ISET/BST_FSET/PWM_FSET/LED_SET/MODE resistor out-of-range detection
- Boost overcurrent
- Boost overvoltage
- Device undervoltage protection (VDD UVLO)
  - Threshold sensing from VDD pin
- V_{IN} input overvoltage protection (V_{IN} OVP)
  - Threshold sensing from VSENSE_P pin
- V_{IN} input undervoltage protection (V_{IN} UVLO)
  - Threshold sensing from UVLO pin
- V_{IN} input overcurrent protection (V_{IN} OCP)
  - Threshold sensing across voltage between VSENSE_P pin and VSENSE_N pin
- Thermal shutdown in case of die overtemperature

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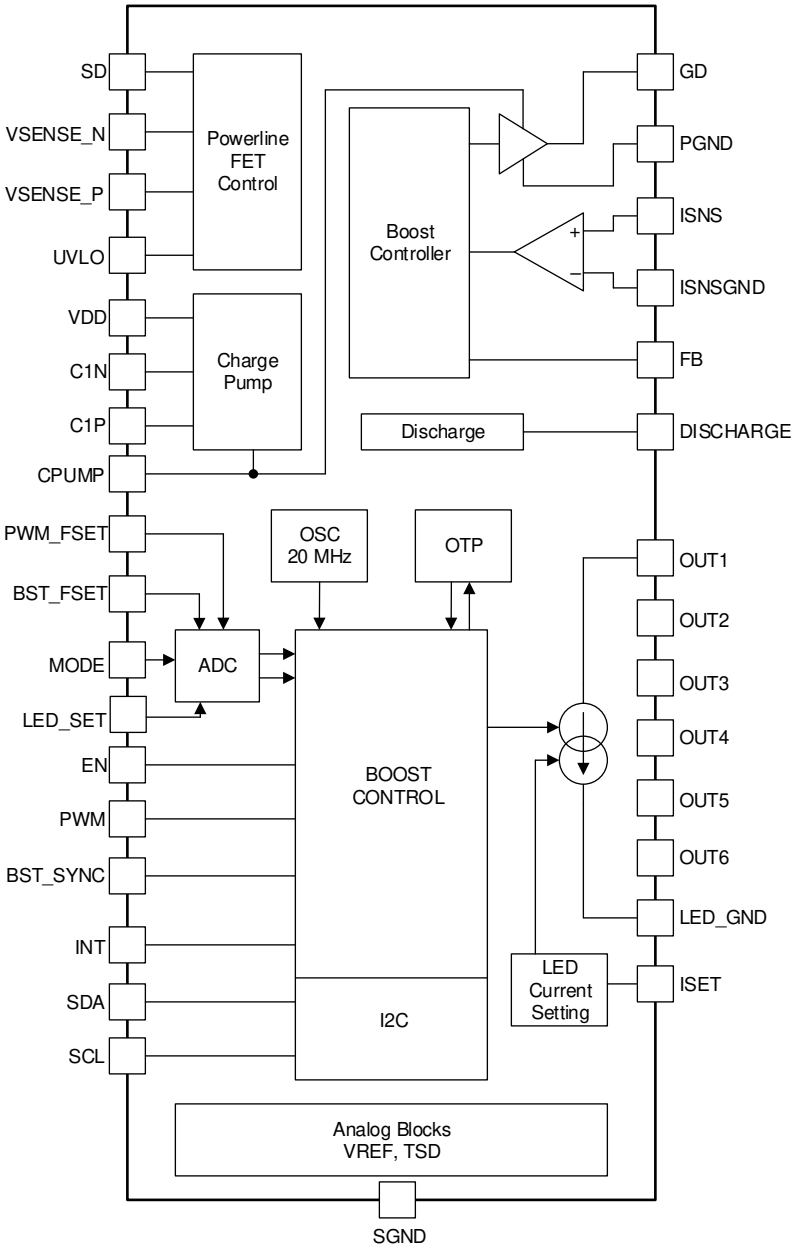
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Interface

Device control interface includes:

- EN is the enable input for the LP8866-Q1 device.
- PWM is the default input to control the brightness of all current sinks by duty cycle.
- INT is an open-drain fault output indicating fault condition detection.
- SDA and SCL are data and clock line for I2C interface to control the brightness of all current sinks and read back the fault conditions for diagnosis.
- FAULT1 is multi-function of INT when I2C interface is disabled. It is an open-drain fault output indicating

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Feature Description (接下页)

supply fault including VIN UVLO and VIN OVP.

- FAULT2 is multi-function of SDA when I2C interface is disabled. It is an open-drain fault output indicating boost fault including VDD UVLO, boost OCP, OVP and TSD.
- FAULT3 multi-function of SCL when I2C interface is disabled. It is an open-drain fault output indicating LED fault including LED open, short and LED short to GND.
- BST_SYNC is used to input an external clock for the boost switching frequency and control the internal boost clock mode.
  - The external clock is auto detected at start-up and, if missing, the internal clock is used.
  - Optionally, the BST_SYNC can be tied to VDD to enable the boost spread spectrum function or tied to GND to disable it.
- ISET pin to set the maximum LED current level per string.

7.3.2 Function Setting

Device parameter setting includes:

- BST_FSET pin is used to set the boost switching frequency through a resistor to signal ground.
- PWM_FSET pin is used to set the LED output PWM dimming frequency through a resistor to signal ground.
- MODE pin is used to set the dimming mode via an external resistor to signal ground.
- LED_SET pin is used to set the LED configuration through a resistor to signal ground.
- ISET pin is used to set the maximum LED current level per string.

7.3.3 Device Supply (VDD)

All internal analog and digital blocks of LP8866-Q1 are biased from external supply from VDD pin. Either a typical 5-V or 3.3-V supply rail is able to supply VDD from previous linear regulator or DC/DC converter with at least 200-mA current capability.

7.3.4 Enable (EN)

The LP8866-Q1 only turns on when the input voltage of EN pin is above the voltage threshold (VEN_{IH}) and turns off when the voltage of EN pin is below the threshold (VEN_{IL}). All analog and digital blocks start operating once the LP8866-Q1 is enabled by asserting EN pin. The I2C interface, V_{IN} UVLO, V_{IN} OVP and SD pin are not active if the EN pin is de-asserted.

7.3.5 Charge Pump

An integrated regulated charge pump can be used to supply the gate drive for the external FET of the boost controller. The charge pump is enabled or disabled by automatically detecting the presence of the external charge pump C_{FLY} capacitor. If VDD is < 4.5 V then use the charge pump to generate a 5-V gate voltage to drive the external boost switching FET. To use the charge pump, a 2.2-µF capacitor is placed between C1N and C1P. If the charge pump is not required, C1N and C1P must be left unconnected and CPUMP pins tied to VDD. A 4.7-µF CPUMP capacitor is used to store energy for the gate driver. The CPUMP capacitor is required to be used in both charge pump enabled and disabled conditions and must be placed as close as possible to the CPUMP pins. 图 2 and 图 3 show required connections for both use cases.

Feature Description (接下页)

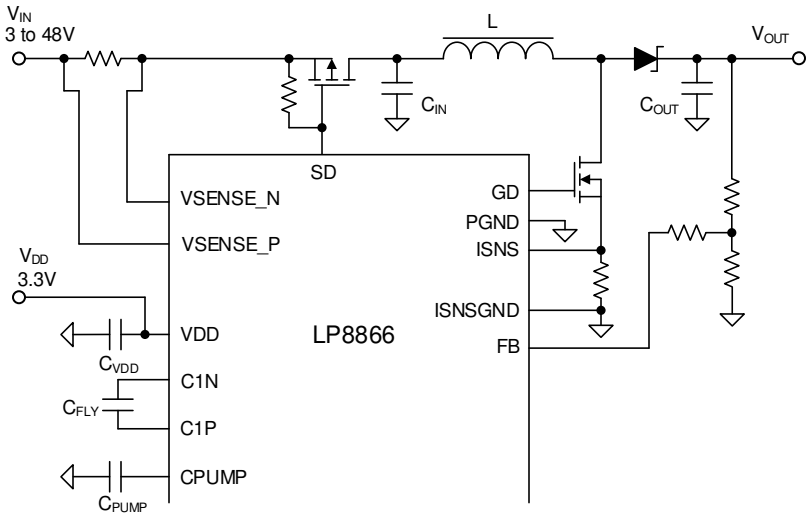

图 2. Charge Pump Enabled Circuit

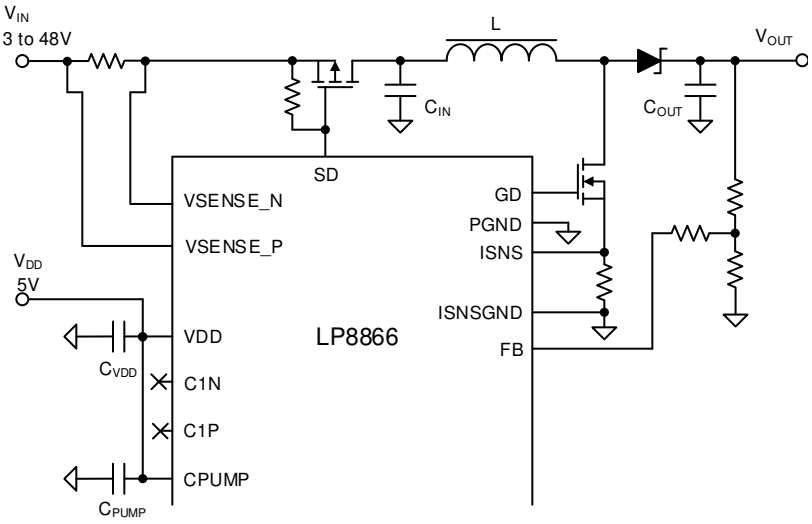

图 3. Charge Pump Disabled Circuit

The CPCAP_STATUS bit shows whether a fly capacitor was detected. The CP_STATUS bit shows status of any charge pump faults and generates an INT signal. The CP_INT_EN bit can be used to prevent the charge-pump fault from causing an interrupt on the INT pin.

7.3.6 Boost Controller

The LP8866-Q1 current-mode-controlled boost DC/DC controller generates the bias voltage for the LEDs. The boost is a current-mode-controlled topology with a cycle by cycle current limit. The boost converter senses the switch current and across the external sense resistor connected between ISNS and ISNSGND. A 20-mΩ sense resistor results in a 10-A cycle by cycle current limit. The sense resistor value could vary from 15 mΩ to 50 mΩ depending on the application. Maximum boost voltage is configured with external FB-pin resistor divider connected between V_{OUT} and FB. The FB-divider equation is described in *Boost Adaptive Voltage Control*.

ADVANCE INFORMATION

Feature Description (接下页)

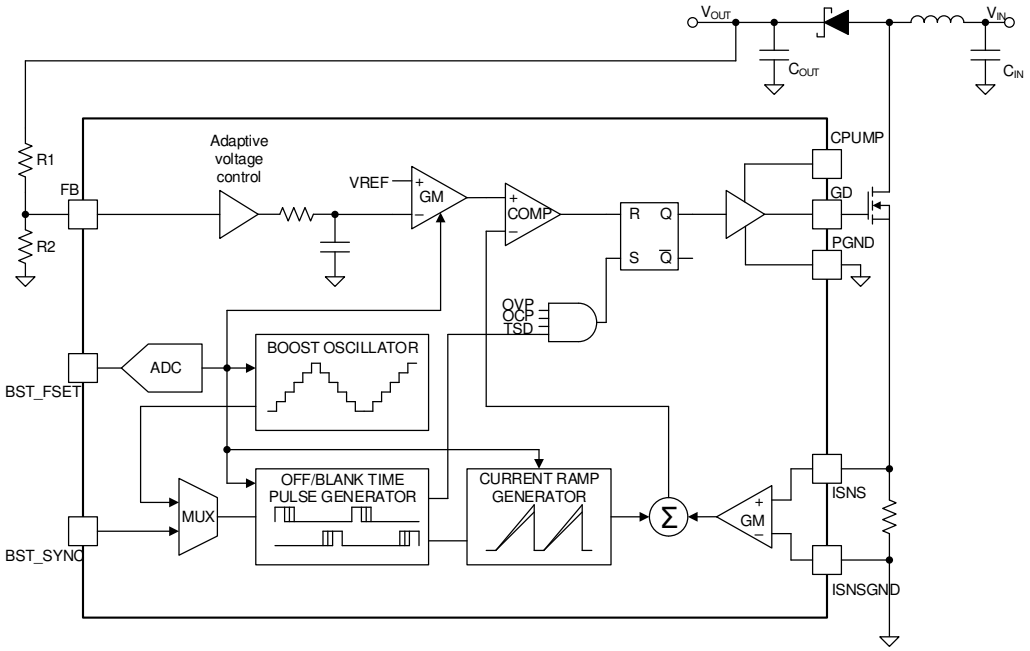

图 4. Boost Controller Block Diagram

The boost switching frequency is adjustable from 100 kHz to 2.2 MHz via an external resistor at BST_FSET (see 表 1). Resistor with 1% accuracy is needed to ensure proper operation.

表 1. Boost Frequency Selection

R_BST_FSET (kΩ)	BOOST FREQUENCY (kHz)
3.92	100
4.75	200
5.76	303
7.87	400
11	500
17.8	1818
42.2	2000
124	2222

7.3.6.1 Boost Adaptive Voltage Control

The LP8866-Q1 boost DC/DC converter generates the bias voltage for the LEDs. During normal operation, boost output voltage is adjusted automatically based on the LED current sink headroom voltages. This is called adaptive boost control. The number of used LED outputs is set by LED_SET pin and only the active LED outputs are monitored to control the adaptive boost voltage. Any LED strings with open or short faults are also removed from the adaptive voltage control loop. The LED driver pin voltages are periodically monitored by the control loop and the boost voltage is raised if any of the LED outputs falls below the $V_{HEADROOM}$ threshold. The boost voltage is lowered until any of the LED outputs touch the $V_{HEADROOM}$ threshold. See 图 5 for how the boost voltage automatically scales based on the OUT approximately 6-pin voltage, $V_{HEADROOM}$ and $V_{HEADROOM\_HYS}$.

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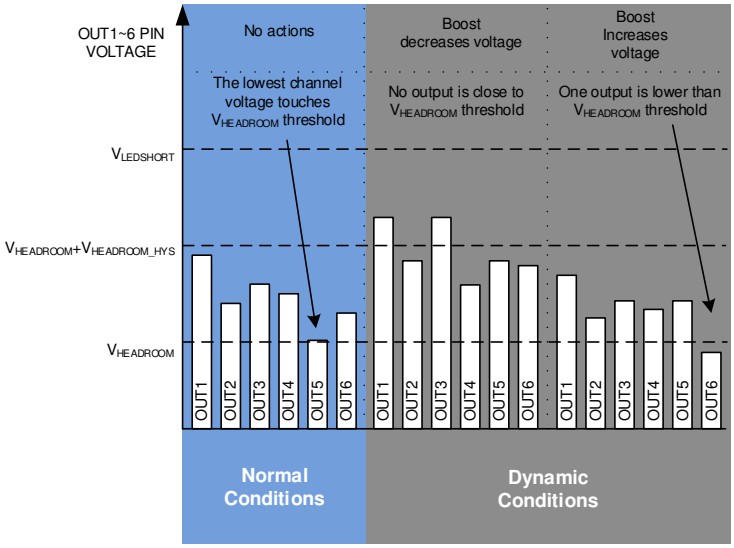

图 5. Adaptive Boost Voltage Control Loop Function

The resistive divider (R_1, R_2) defines both the minimum and maximum adaptive boost voltage levels. The feedback circuit operates the same in boost and SEPIC topologies. Choose maximum boost voltage based on the maximum LED string voltage specification. Before the LED drivers are active, the boost starts up to the initial boost level. The initial boost voltage is approximately in the 88% point of minimum to maximum boost voltage. Once the LED driver channels are active, the boost output voltage is adjusted automatically based on OUT1 approximately 6 pin voltages. The FB pin resistor divider also scales the boost OVP and OCP levels.

ADVANCE INFORMATION

7.3.6.1.1 FB Divider Using Two-Resistor Method

A typical FB-pin circuit uses a two-resistor divider circuit between the boost output voltage and ground.

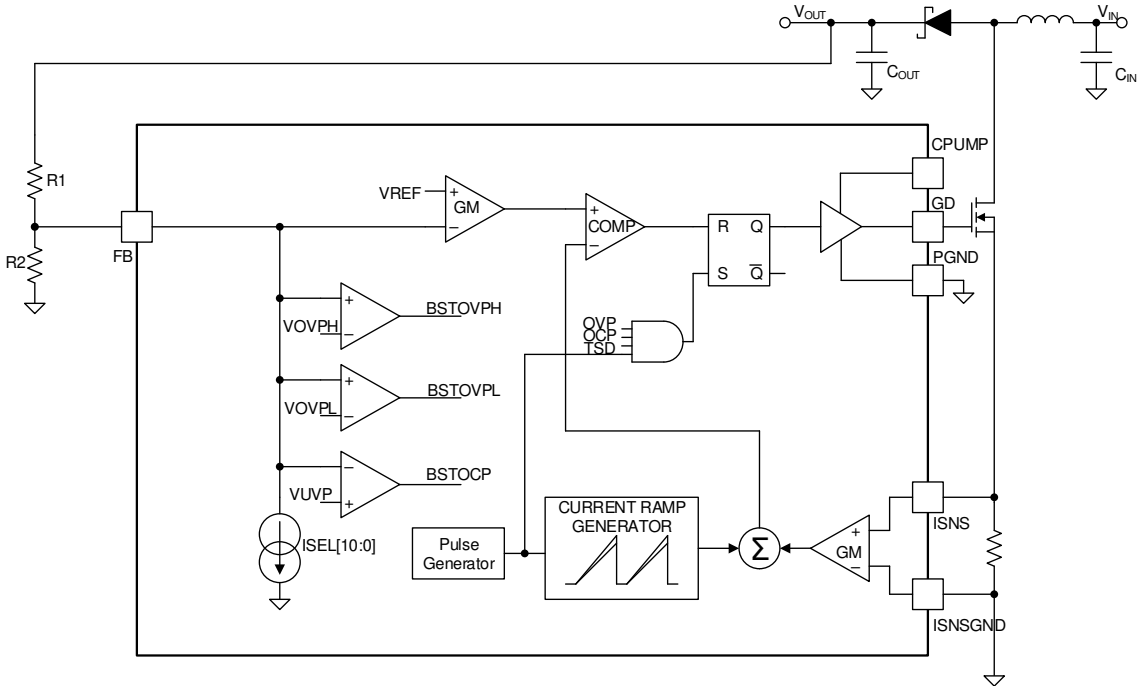

图 6. Two-Resistor FB Divider Circuit

Maximum boost voltage can be calculated with 公式 1. The maximum boost voltage can be reached during OPEN string detection or if all LED strings are left disconnected.

$$V_{BOOST\_MAX} = I_{SEL\_MAX} \times R_1 + \left(\frac{R_1}{R_2} + 1\right) \times V_{REF}$$

where

- V_{REF}= 1.21 V
- I_{SEL_MAX} = 38.7 µA
- R_2 recommended value is 100 kΩ for boost operation and 170 kΩ for SEPIC operation (1)

The minimum boost voltage must be less than the minimum LED string voltage. Minimum boost voltage is calculated with 公式 2:

$$V_{BOOST\_MIN} = \left(\frac{R_1}{R_2} + 1\right) \times V_{REF}$$

where

- V_{REF} = 1.21 V (2)

When the boost OVP_LOW level is reached, the boost controller stops switching the boost FET and the BSTOVPL_STATUS bit is set. The LED drivers are still active during this condition, and the boost resumes normal switching operation once the boost output level falls. The boost OVP low voltage threshold changes dynamically with current boost voltage. It is calculated in 公式 3:

$$V_{BOOST\_OVPL} = V_{BOOST} + \left(\frac{R_1}{R_2} + 1\right) \times (V_{OVPL} - V_{REF})$$

where

- V_{FB_OVPL} = 1.423 V
- V_{REF} = 1.21 V

(3)

When the boost OVP_HIGH level is reached the boost controller enters fault recovery mode, and the BSTOVPH_STATUS bit is set. The boost OVP high-voltage threshold also changes dynamically with current boost voltage and is calculated in 公式 4:

$$V_{BOOST\_OVPH} = V_{BOOST} + \left(\frac{R_1}{R_2} + 1\right) \times (V_{OVPH} - V_{REF})$$

where

- V_{FB_OVPH} = 1.76 V
- V_{REF} = 1.21 V

(4)

When the boost UVP level is reached the boost controller starts a 110-ms OCP counter. The LP8866-Q1 device enters the fault recovery mode and sets the BSTOCP_STATUS bit if the boost voltage does not rise above the UVP threshold before the timer expires. The boost UVP voltage threshold also changes dynamically with current boost voltage and is calculated in 公式 5:

$$V_{BOOST\_UVP} = V_{BOOST} - \left(\frac{R_1}{R_2} + 1\right) \times (V_{REF} - V_{UVP})$$

where

- V_{UVP} = 0.886 V
- V_{REF} = 1.21 V

(5)

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7.3.6.1.2 FB Divider Using Three-Resistor Method

A FB-pin circuit using a three-resistor divider circuit can be used for applications where less than 200-kΩ resistors are required.

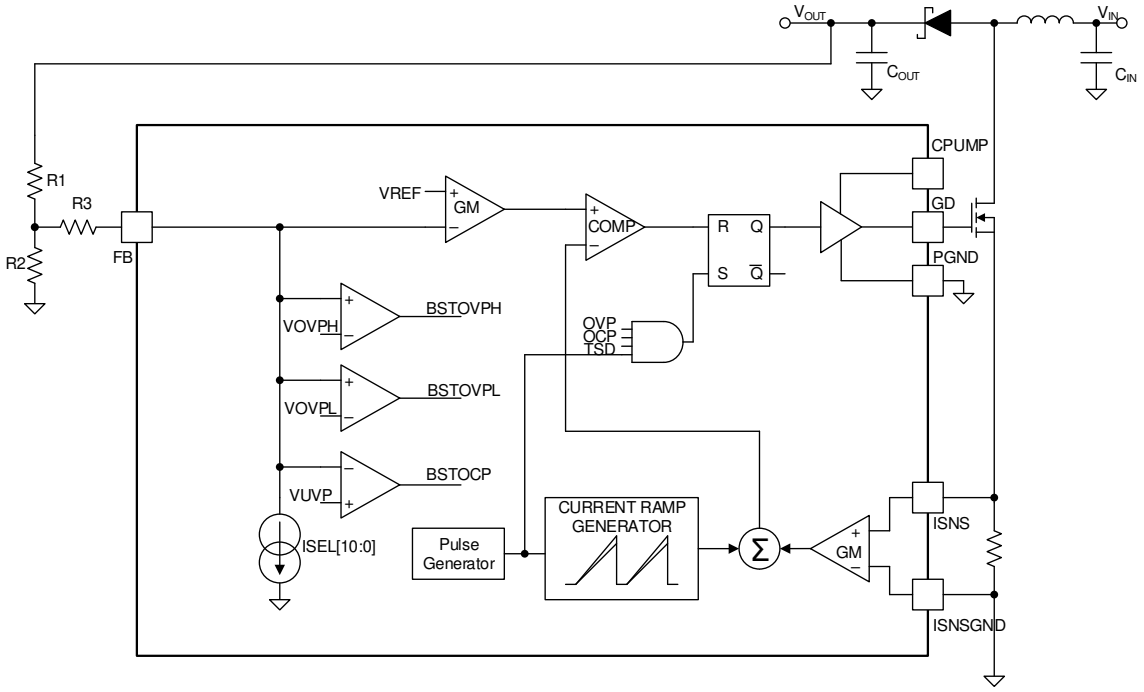

图 7. Three-Resistor FB Divider Circuit

Maximum boost voltage can be calculated with 公式 6. The maximum boost voltage can be reached during OPEN string detection or if all LED strings are left disconnected.

$$V_{BOOST\_MAX} = \left(\frac{R_1 \times R_3}{R_2} + R_1 + R_3 \right) \times I_{SEL\_MAX} + \left(\frac{R_1}{R_2} + 1 \right) \times V_{REF}$$

where

- V_{REF} = 1.21 V
- I_{SEL_MAX} = 38.7 µA
- R_2 recommended value is 6 kΩ for boost operation and 10 kΩ for SEPIC operation
- R_3 recommended value is 27 kΩ for boost operation and 30 kΩ for SEPIC operation (6)

The minimum boost voltage must be less than the minimum LED string voltage. Minimum boost voltage is calculated in 公式 7:

$$V_{BOOST\_MIN} = \left(\frac{R_1}{R_2} + 1 \right) \times V_{REF} \quad (7)$$

When the boost OVP_LOW level is reached the boost controller stops switching the boost FET, and the BSTOVPL_STATUS bit is set. The LED drivers are still active during this condition, and the boost resumes normal switching operation once the boost output level falls. The boost OVP low voltage threshold changes dynamically with current boost voltage. It is calculated in 公式 8:

$$V_{BOOST\_OVPL} = V_{BOOST} + \left(\frac{R_1}{R_2} + 1 \right) \times (V_{OVPL} - V_{REF})$$

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where

- V_{FB_OVPL}= 1.423 V
- V_{REF}= 1.21 V

(8)

When the boost OVP_LOW level is reached the boost controller enters fault recovery mode, and the BSTOVPH_STATUS bit is set. The boost OVP high-voltage threshold also changes dynamically with current boost voltage and is calculated in 公式 9:

$$V_{BOOST\_OVPH} = V_{BOOST} + \left(\frac{R_1}{R_2} + 1\right) \times (V_{OVPH} - V_{REF})$$

where

- V_{FB_OVPH} = 1.76 V
- V_{REF}= 1.21 V

(9)

When the boost UVP level is reached the boost controller starts a 110-ms OCP counter. The LP8866-Q1 device enters the fault recovery mode and sets the BSTOCP_STATUS bit if the boost voltage does not rise above the UVP threshold before the timer expires. The boost UVP voltage threshold also changes dynamically with current boost voltage and is calculated in 公式 10:

$$V_{BOOST\_UVP} = V_{BOOST} - \left(\frac{R_1}{R_2} + 1\right) \times (V_{REF} - V_{UVP})$$

where

- V_{UVP} = 0.886 V
- V_{REF}= 1.21 V

(10)

7.3.6.2 Boost Sync and Spread Spectrum

Spread spectrum function could be enabled when BST_SYNC pin is high and disabled when BST_SYNC pin is low.

If an external CLK signal is on the BST_SYNC pin, the boost controller can be clocked by this signal. If the clock disappears later, the boost continues operation at the frequency defined by RBST_FSET resistor, and the spread spectrum function will be enabled or disabled depending on the final pin level of BST_SYNC.

表 2. Boost Synchronization Mode

BST_SYNC PIN LEVEL	BOOST CLOCK MODE
Low (GND)	Spread spectrum disabled
High (VDDIO)	Spread spectrum enabled
100-kHz to 2222-kHz clock frequency	Spread spectrum disabled, external synchronization mode

If using the external BST_SYNC input, the external frequency must be between 1.2 and 1.5 times higher than the frequency defined by the R_{BST_SET} resistor.

The spread spectrum function helps to reduce EMI noise around the switching frequency and its harmonic frequencies. The internal spread spectrum function modulates the boost frequency ±3% to 6.85% from the central frequency with a 200-Hz to 1.2-kHz modulation frequency. The switching frequency variation is programmable by SPREAD_RANGE register, and the modulation frequency is programmable by SPREAD_MOD_FREQ register. The spread-spectrum function cannot be used when an external synchronization clock is used.

表 3. Spread Spectrum Frequency Range

SPREAD_RANGE (Binary)	SWITCHING FREQUENCY VARIATION
00	±3.3%
01	±4.3%
10 (Default)	±5.3%

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表 3. Spread Spectrum Frequency Range (接下页)

SPREAD_RANGE (Binary)	SWITCHING FREQUENCY VARIATION
11	±7.2%

表 4. Spread Spectrum Modulation Frequency

SPREAD_MOD_FREQ (Binary)	MODULATION FREQUENCY
00 (Default)	200 Hz
01	500 Hz
10	800 Hz
11	1200 Hz

7.3.6.3 Boost Output Discharge

When the EN pin is pulled low, the device stops the boost controller and LED current sinks, turns off the power-line FET, and starts to discharge the boost output. The discharge pin typically sinks 30-mA current. The discharge duration is 400 ms. After 400 ms, the device shuts down. The DISCHARGE pin must be connected with boost output for normal operation.

There is one internal comparator to monitor the voltage of DISCHARGE pin. As soon as the voltage of DISCHARGE pin is higher than V_{BST_OVPH} (typically 50 V), the device enters into fault recovery mode, and BST_OVPH fault is reported. This provide further protection if boost voltage is out of control because of system failure.

7.3.7 LED Current Sinks

7.3.7.1 LED Output Current Setting

The maximum output LED current is set by an external resistor value. For the application only uses external resistor R_{ISET} to set the maximum LED current for each string, the 公式 11 is used to calculate the current setting of all strings:

$$I_{LED} = \frac{1.21V}{R_{ISET}} \times 2580 \tag{11}$$

The LEDx_CURRENT[11:0] registers can also be used to adjust strings current down from this maximum. The default value for LEDx_CURRENT[11:0] registers is the maximum 0xFFF(4095). 公式 12 is used to calculate the current setting of an individual string:

$$I_{LED} = \left(\frac{1.21V}{R_{ISET}} \times 2580 \right) \times \left(\frac{LED\_CURRENT[11:0]}{4095} \right) \tag{12}$$

For high accuracy for LED current, the ILED current is recommended to set in range from 30 mA to 200 mA. So the R_{ISET} value is in the range from 15.6 kΩ to 104 kΩ.

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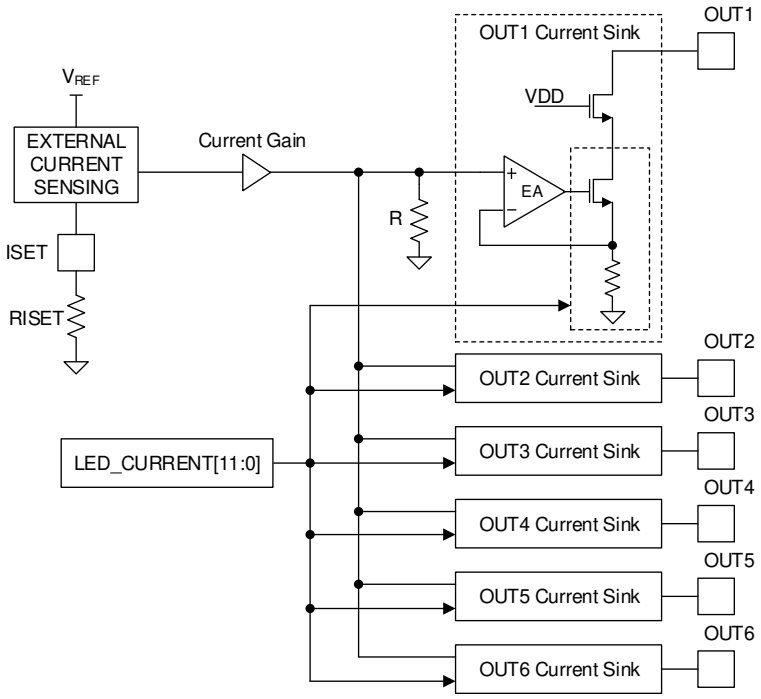

图 8. LED Driver Current Setting Circuit

7.3.7.2 LED Output String Configuration

The six LED driver channels of the LP8866-Q1 device is configured by the LED_SET resistor, which supports applications using one to six LED strings. Resistor with 1% accuracy is needed to ensure proper operation. The driver channels can also be tied together in groups of one, two or three. This allows the LP8866-Q1 device to drive three 400-mA LED strings, two 600-mA LED strings, or one 1200-mA LED string. The LED strings are always appropriately phase shifted for their string configuration. This reduces the ripple seen at the boost output, which allows smaller output capacitors and reduces audible ringing in the capacitors. Phase shift increases the load frequency, which can move potential capacitor noise above the audible band while still keeping PWM frequency low to support a higher dimming ratio.

When the LP8866-Q1 device is firstly powered on, the string configuration is configured by the LED_SET resistor and the phases of each channel are automatically configured. The LED string configuration must not be changed unless the LP8866-Q1 is powered off in shutdown state. The unused LEDx pins should be tied to ground.

表 5. LED Output String Configuration

R_LED_SET (kΩ)	CONFIGURATION	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	AUTOMATIC PHASE SHIFT
3.92	6 Channels	200 mA	200 mA	200 mA	200 mA	200 mA	200 mA	60°
4.75	5 Channels	200 mA	200 mA	200 mA	200 mA	200 mA	(Tied to GND)	72°
5.76	4 Channels	200 mA	200 mA	200 mA	200 mA	(Tied to GND)	(Tied to GND)	90°
7.87	3 Channels	200 mA	200 mA	200 mA	(Tied to GND)	(Tied to GND)	(Tied to GND)	120°
11	2 Channels	200 mA	200 mA	(Tied to GND)	(Tied to GND)	(Tied to GND)	(Tied to GND)	180°
17.8	3 Channels	400 mA		400 mA		400 mA		120°
42.2	2 Channels	600 mA			600 mA			180°
124	1 Channels	1200 mA						None

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7.3.7.3 LED Output PWM Clock Generation

The LED PWM frequency is asynchronous from the input PWM frequency. The LED PWM frequency is generated from the internal 20-MHz oscillator and can be set to eight discrete frequencies from 152 Hz to 19.531 kHz. The PWM dimming resolution is highest when the lowest PWM frequency is used. The PWM_FSET resistor determines the LED PWM frequency based on 表 7. PWM resolution in 表 7 is with PWM dither disabled.

7.3.8 Brightness Control

The LP8866-Q1 supports global brightness control for all LED strings through either duty cycle input on PWM pin or register by I2C bus. An internal 20-MHz clock is used for generating PWM outputs.

7.3.8.1 Brightness Control Signal Path

The BRT_MODE register selects whether the input to the display brightness path is the PWM input pin or DISP_BRT register. PWM input control will be the default setup after power on. The brightness control signal path diagram is shown in 图 9

The display brightness path has sloper function that can be enabled. By default the sloper function is enabled. The sloper and dither function also can be programmable by I2C control. The sloper function is described in Sloper, and the dither function is described in Dither.

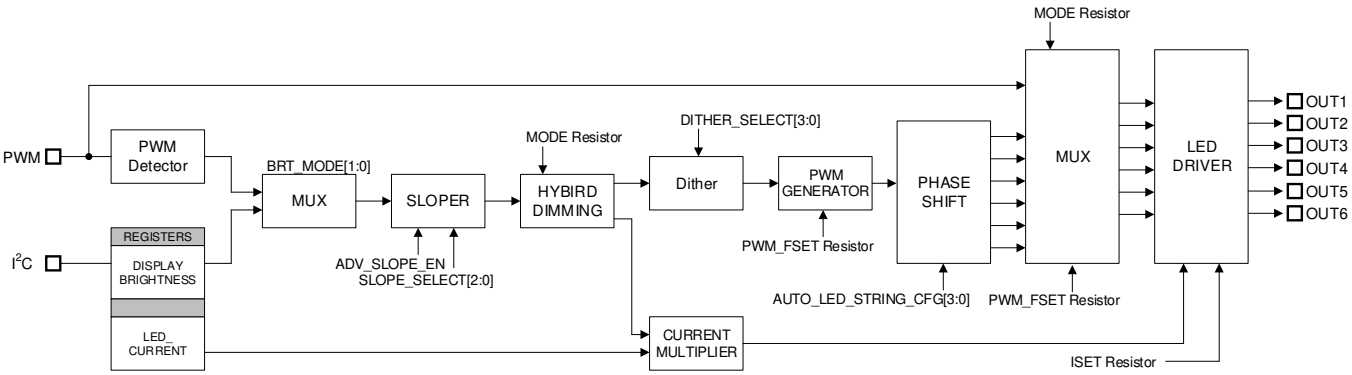

图 9. LP8866-Q1 Brightness Path Diagram

7.3.8.2 Dimming Mode

Dimming mode can be adjusted via an external resistor to MODE pin (see 表 6). Resistor with 1% accuracy is needed to ensure proper operation.

表 6. Dimming Mode Configuration

R_MODE (kΩ)	MODE	I2C
3.92	Phase-shift PWM Mode	Disable
4.75	Hybrid Mode	Disable
5.76	Current Dimming Mode	Disable
7.87	Direct PWM Mode	Disable
11	Phase-shift PWM Mode	Enable
17.8	Hybrid Mode	Enable
42.2	Current Dimming Mode	Enable
124	Direct PWM Mode	Enable

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7.3.8.3 LED Dimming Frequency

The LED dimming frequency is asynchronous from the input PWM frequency for phase-shift PWM mode and hybrid dimming mode. The LED dimming frequency is generated from the internal 20-MHz oscillator and can be set to eight discrete frequencies from 152 Hz to 19.531kHz. The PWM dimming resolution is highest when the lowest PWM frequency is used. The PWM_FSET resistor determines the LED Dimming frequency based on 表 7. Resistor with 1% accuracy is needed to ensure proper operation. PWM resolution in 表 7 is with PWM dither disabled.

表 7. LED PWM Frequency Selection

R_PWM_FSET (kΩ)	LED PWM FREQUENCY (Hz)	PWM DIMMING RESOLUTION (bits)
3.92	152	16
4.75	305	16
5.76	610	15
7.87	1221	14
11	2441	13
17.8	4883	12
42.2	9766	11
124	19531	10

7.3.8.4 Phase-Shift PWM Mode

In Phase-Shift PWM mode, all current feedback channels are turned on and off at LED dimming frequency with a constant delay. However, the number of used channels or channel groups determine the phase delay time between two neighboring channels as shown in 图 10.

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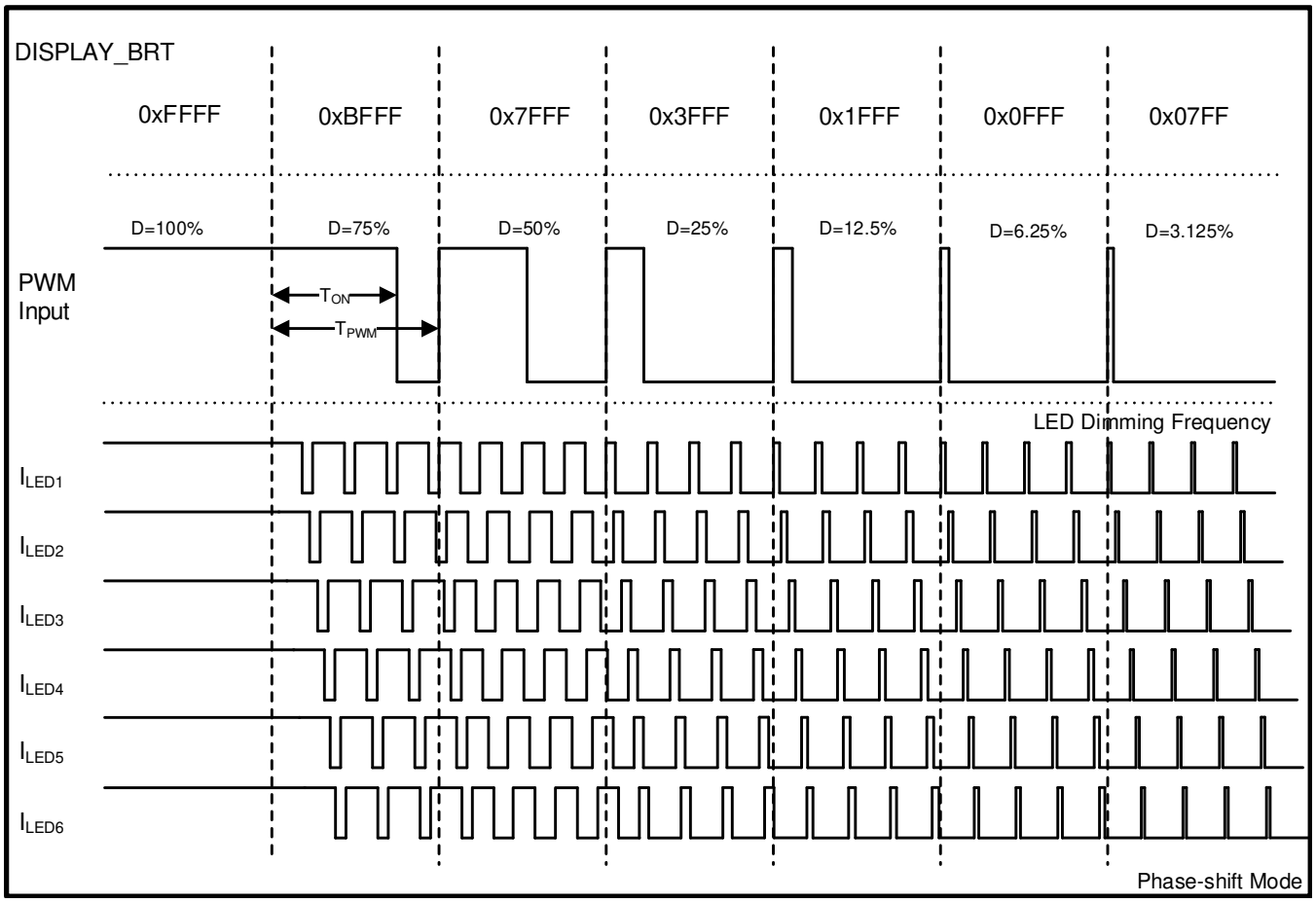

图 10. Phase-shift Dimming Diagram

7.3.8.5 Hybrid Mode

In addition to phase-shift PWM dimming, LP8866-Q1 supports a hybrid-dimming mode. Hybrid dimming combines PWM and current modes for brightness control for the display brightness path. In hybrid mode, PWM dimming is used for low brightness range of brightness, and current dimming is used for high brightness levels as shown in 图 11. Current dimming control enables improved optical efficiency due to increased LED efficiency at lower currents. PWM dimming control at low brightness levels ensures linear and accurate control. Hybrid mode can be selected through resistor value at MODE pin as 表 6. The PWM and current modes transition threshold can be set at 12.5% or at 0% brightness. The latter selection allows for pure current dimming control mode.

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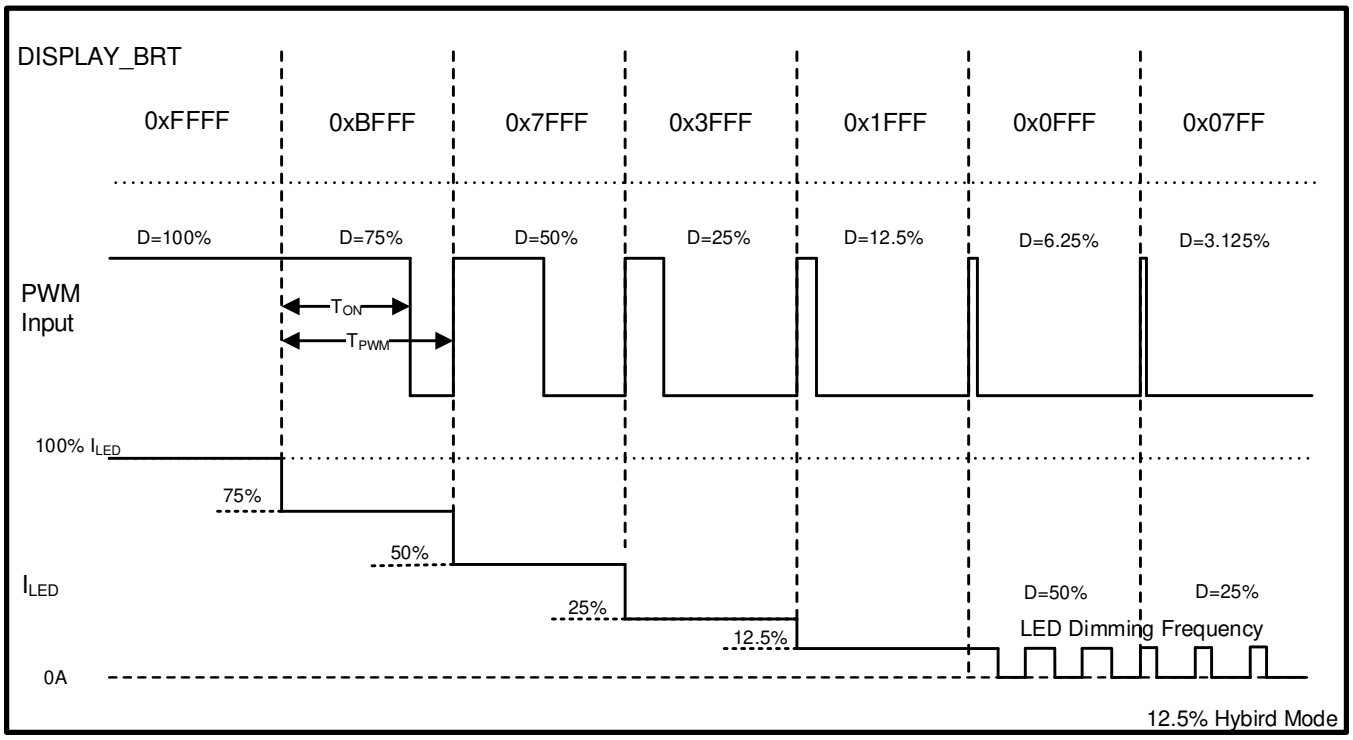

图 11. Hybrid Dimming Diagram

7.3.8.6 Direct PWM Mode

In direct PWM mode, all current feedback channels are turned on and off and are synchronized with the input PWM signal.

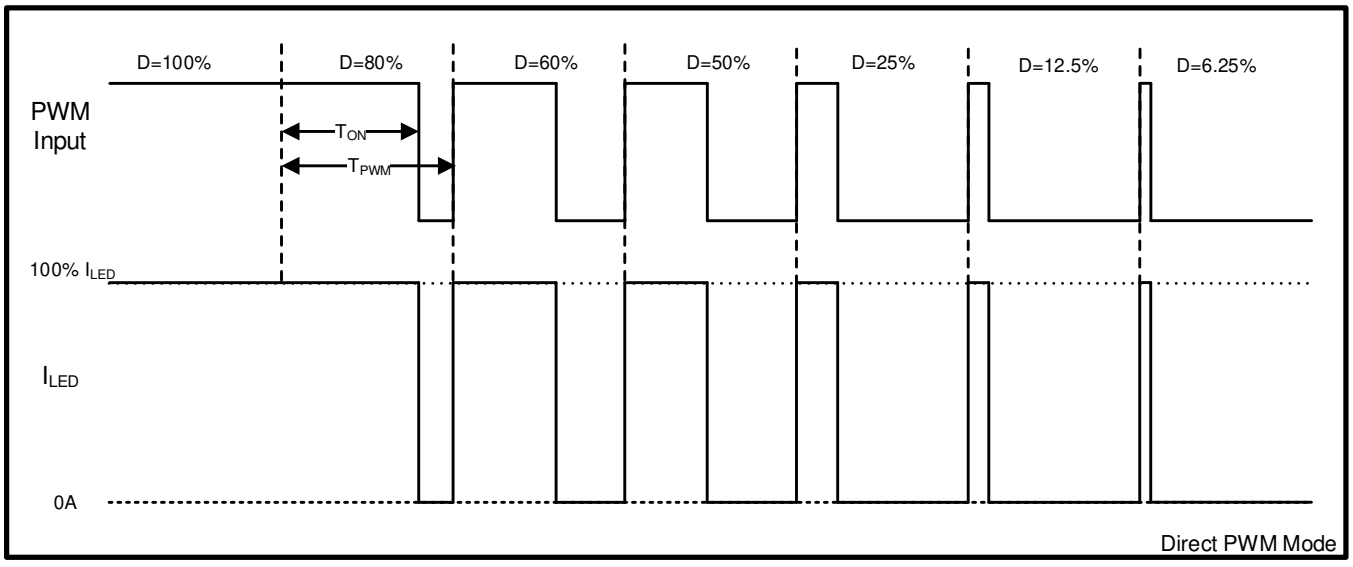

图 12. Direct PWM Dimming Diagram

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7.3.8.7 Sloper

An optional sloper function makes the transition from one brightness value to another optically smooth. By default the advanced sloper is enabled with a 200-ms linear sloper duration. Transition time between two brightness values is programmed with the SLOPE_SELECT[2:0] bits (when 000, sloper is disabled). With advanced sloper enabled the brightness changes are further smoothed to be more pleasing to the human eye. Advanced slope is enabled with ADV_SLOPE_ENABLE register bit.

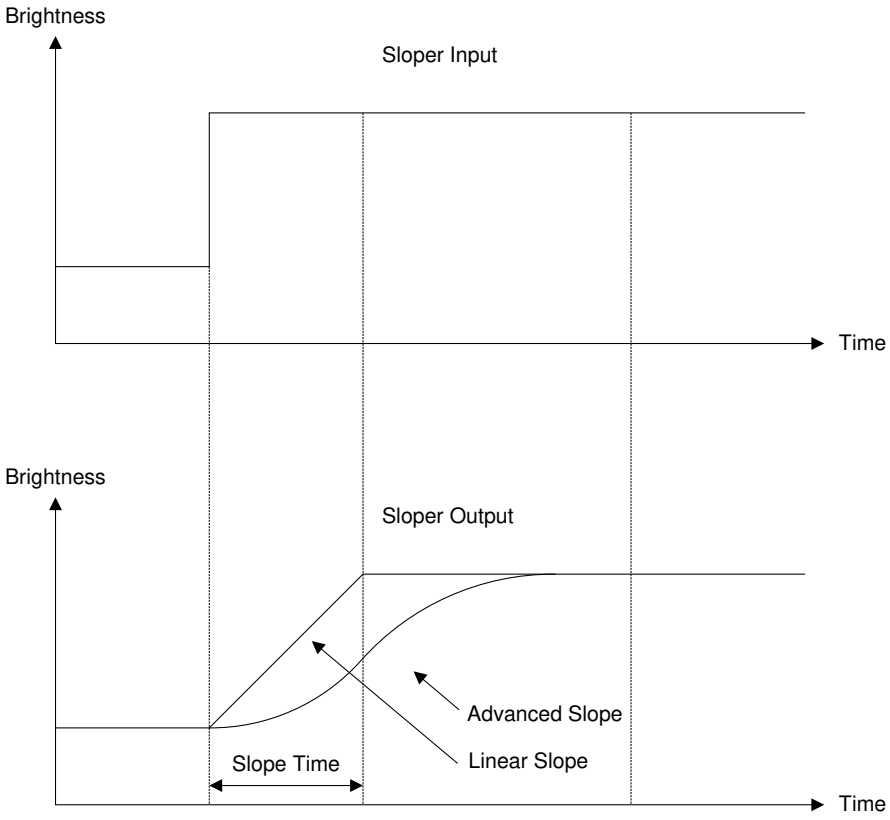

图 13. Brightness Sloper

7.3.8.8 Dither

The number of brightness steps when using LED output PWM dimming is equal to the 20-MHz oscillator frequency divided by the LED PWM frequency (set by PWM FSET resistor). The PWM duty cycle dither is a function the LP8866-Q1 uses to increase the number of brightness dimming steps beyond this oscillator clock limitation. The dither function modulates the LED driver output duty cycle over time to create more possible average brightness levels. The DITHER_SELECT[3:0] register bits control the level of dither, disabled, 1, 2, 3 or 4 bits using the I2C interface. By default the dither is disabled.

When the 1-bit dither is selected, to support higher brightness resolution, the width of every second PWM pulse could be increased by one LSB (one 20-MHz clock period). When the 3-bit dither is selected, within a sequence of 8 PWM periods the number of pulses with increased length varies depending on the dither value: dither value 000 - all 8 pulses at default length; 001 - one of the 8 pulses is longer; 010 - two of the 8 pulses are longer, and so forth, until at 111 seven of the 8 pulses have increased length. 图 14 shows one example of PWM output dither.

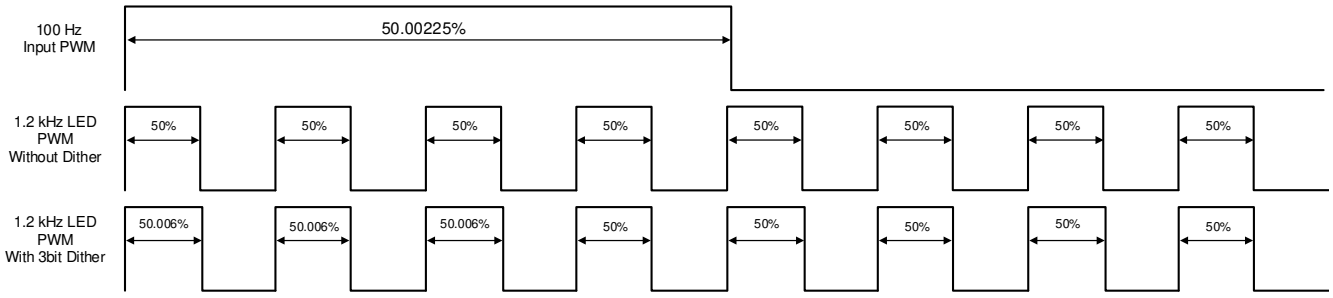

图 14. PWM Dither Example

The dither block also helps in low brightness scenario when LED PWM output pulse is less than the minimum pulse width (200 ns). In such scenario, the dither block will skip some of the PWM pulses to reduce the brightness further, enabling high dimming ratio. The end result is that the LED PWM frequency is reduced as more and more minimum pulses are skipped or dithered out. At the same time, dither block will also guarantee that the minimum LED PWM frequency is not less than 152 Hz to ensure no brightness flickering. 图 15 shows how the dither works in low brightness scenario.

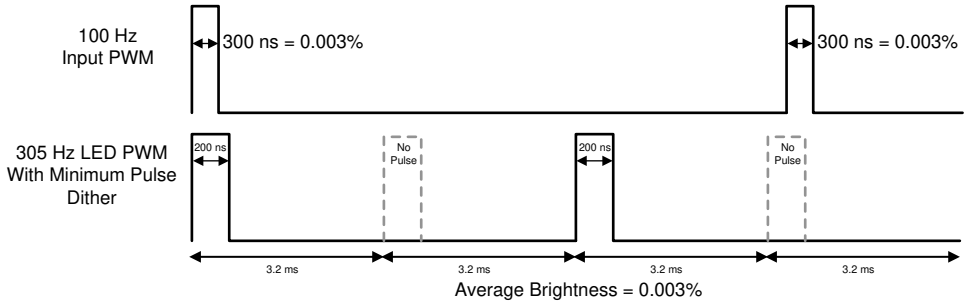

图 15. Minimum Brightness Dither Example

7.3.9 Protection and Fault Detections

The LP8866-Q1 includes fault detections for LED open and short conditions, boost input undervoltage, overvoltage and overcurrent, boost output overvoltage and overcurrent, VDD undervoltage and die overtemperature. Host can monitor the status of the faults in registers SUPPLY_FAULT_STATUS, BOOST_FAULT_STATUS and LED_STATUS.

7.3.9.1 Supply Faults

7.3.9.1.1 V_{IN} Undervoltage Faults (VINUVLO)

The LP8866-Q1 device supports V_{IN} undervoltage and overvoltage protection. The undervoltage threshold is programmable through external resistor divider on UVLO pin. If during operation of the LP8866-Q1 device, the UVLO pin voltage falls below the UVLO falling level (0.787 V typical), the boost, LED outputs, and power-line FET will be turned off, and the device will enter STANDBY mode. The VINUVLO_STATUS bit is also set in the SUPPLY_FAULT_STATUS register, and the INT pin is triggered in I2C enable mode or Fault1 pin is triggered in I2C disable mode. When the UVLO voltage rises above the rising threshold level the LP8866-Q1 exits STANDBY and begins the start-up sequence.

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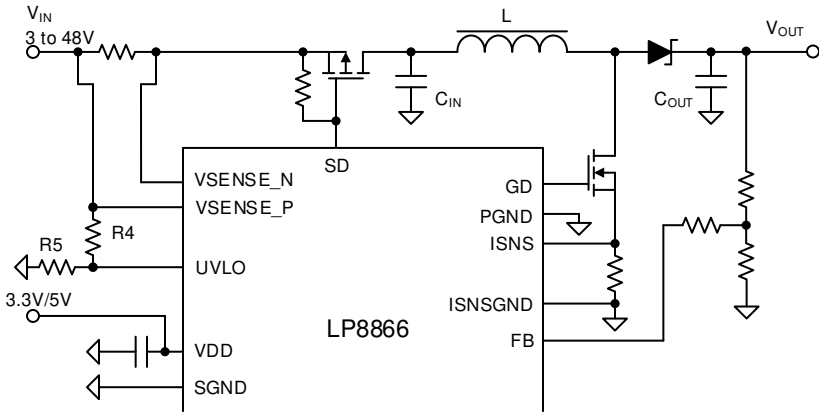

图 16. V_{IN} UVLO Setting Circuit

公式 13 is used to calculate the UVLO threshold for VIN rising edge:

$$VIN_{UVLO\_RISING} = \left(\frac{R_4}{R_5} + 1\right) \times VIN_{UVLO\_TH} \quad (13)$$

where

- VIN_{UVLO_TH} = 0.787 V

The hysteresis of UVLO threshold can be designed and calculated by 公式 14.

$$VIN_{HYST} = R_4 \times I_{UVLO} \quad (14)$$

where

- I_{UVLO} = 5 µA

So the 公式 15 can be used for UVLO threshold for VIN falling edge:

$$VIN_{UVLO\_FALLING} = VIN_{UVLO\_RISING} - VIN_{HYST} \quad (15)$$

The bottom resistors, R_5 of voltage divider is able to be disconnected to the GND through an additional external N-type of FET as 图 17. This design is to minimize the current leakage from VIN in shutdown mode to extend the battery life.

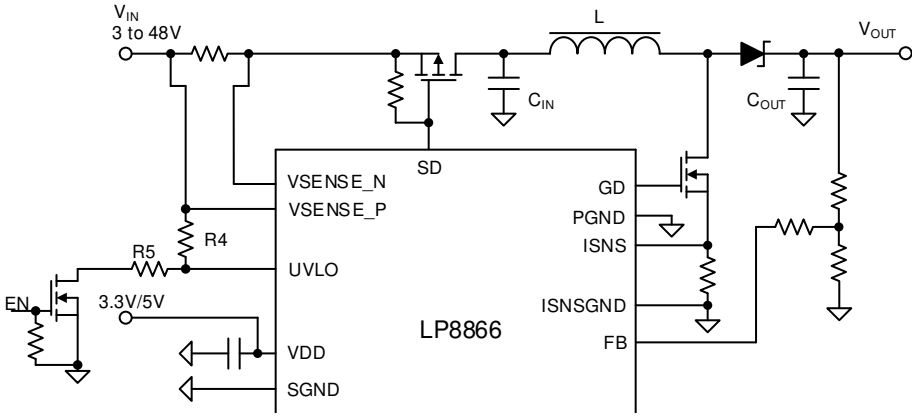

图 17. V_{IN} UVLO Setting Circuit Without Current Leakage Path

7.3.9.1.2 V_{IN} Overvoltage Faults (VINOVP)

The overvoltage threshold for V_{IN} rising edge is internal fixed at typical 43 V. If during LP8866-Q1 operation, VSENSE_P pin voltage rises above the OVP rising threshold, boost, LED outputs, and power-line FET will be turned off, and the device will enter STANDBY mode. The VINOVP_STATUS bit will also be set in the SUPPLY_FAULT_STATUS register, and the INT pin will be triggered. When the VSENSE_P pin voltage falls below the falling threshold level, the LP8866-Q1 exits STANDBY and begins the start-up sequence.

7.3.9.1.3 V_{DD} Undervoltage Faults (VDDUVLO)

If during LP8866-Q1 device operation VDD falls below VDDUVLO falling level, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode. The VDDUVLO_STATUS fault bit will be set in the SUPPLY_FAULT_STATUS register, and the INT pin will be triggered. The LP8866-Q1 recovers automatically to ACTIVE mode when V_{DD} rises above VDDUVLO rising threshold.

7.3.9.1.4 V_{IN} OCP Faults (VINOCP)

If during LP8866-Q1 device operation voltage drop on RISENSE resistor rises above 220 mV, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode and then attempt to restart 100 ms after fault occurs. The VINOCP_STATUS fault bit are set in the SUPPLY_FAULT_STATUS register, and the INT pin is triggered.

7.3.9.1.5 Charge Pump Faults (CPCAP, CP)

If during LP8866-Q1 device operation voltage of CPUMP pin falls below typical 4.2-V, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode and then attempt to restart 100 ms after fault occurs. The CP_STATUS fault bit will beset in the SUPPLY_FAULT_STATUS register, and the INT pin are triggered.

If during LP8866-Q1 device operation the charge pump fly capacitor is disconnected or shorted, charge pump are turned off. In result, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode and then attempt to restart 200 ms after fault occurs. Both CPCAP_STATUS and CP_STATUS fault bits are set in the SUPPLY_FAULT_STATUS register, and the INT pin are triggered.

7.3.9.1.6 Boost Sync Clock Invalid Faults (BSTSYNC)

If LP8866-Q1 is enabled while a valid external SYNC clock is running and BST_SYNC stops or changes to an invalid frequency (< 75kHz), LP8866-Q1 defaults to internal clock frequency selected by BST_FSET resistor and BSTSYNC_STATUS bit will be set. If BST_SYNC input is held high, spread spectrum is enabled. If SYNC input is held low, spread spectrum is disabled.

7.3.9.1.7 CRC Error Faults (CRCERR)

If during LP8866-Q1 device initialization the factory default configuration for registers, options and trim bits are not corrected loaded from memory, LP8866-Q1 keeps operating normally, unless other fault criteria is triggered. The CRCERR_STATUS fault bit are set in the SUPPLY_FAULT_STATUS register and the INT pin are triggered.

7.3.9.2 Boost Faults

7.3.9.2.1 Boost Overvoltage Faults (BSTOVPL, BSTOVPH)

Boost overvoltage is detected if the FB pin voltage exceeds the V_{FB_OVPL} threshold. When boost overvoltage is detected, BSTOVPL_STATUS bit will be set in the BOOST_FAULT_STATUS register. The boost FET stops switching, and the output voltage will be automatically limited. If the BSTOVPL_STATUS bit is continually set (that is, reappears after clearing), it may indicate an issue in the application. Boost overvoltage low is monitored during device normal operation (ACTIVE mode).

A second boost overvoltage high fault is detected if the FB pin voltage exceeds the V_{FB_OVPH} threshold or the DISCHARGE pin voltage exceeds the V_{BST_OVPH}. The LP8866-Q1 device enters the fault recovery state to protect system damage from a high boost voltage. When boost overvoltage is detected, BSTOVPH_STATUS bit is set in the BOOST_FAULT_STATUS register. A fault interrupt is also generated. The device enters STANDBY mode and then attempt to restart after 100 ms. Boost overvoltage high is monitored during device normal operation (ACTIVE mode).

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7.3.9.2.2 Boost Overcurrent Faults (BSTOCP)

Boost overcurrent is detected if the FB pin voltage drops below the V_{UVP} threshold for 110 ms. If the boost overcurrent timer expires before the output voltage recovers, the BSTOCP_STATUS bit is set in the BOOST_FAULT_STATUS register. The fault recovery state is entered, and a fault interrupt is generated. The device will enter STANDBY mode and then attempt to restart after 100 ms. If the BSTOCP_STATUS bit is permanently set, it may indicate an issue in the application. Boost overcurrent is monitored from the boost start, and fault may trigger during boost start-up.

7.3.9.2.3 LEDSET Resistor Missing Faults (LEDSET)

The LEDSET resistor missing or invalid is detected if the resistor is not assembled or not valid value as 表 5 recommended during the initialization. LP8866-Q1 defaults to 6-channel/200mA configuration if LEDSET resistor is missing or invalid. The LEDSET_STATUS fault bit is set in the BOOST_FAULT_STATUS register, and the INT pin is triggered. The LEDSET resistor missing or invalid fault won't be monitored after initialization, so that the LP8866-Q1 is operating in the configuration determined during initialization even though the LEDSET resistor is missing or invalid after initialization.

7.3.9.2.4 MODE Resistor Missing Faults (MODESEL)

The MODE resistor missing or invalid is detected if the resistor is not assembled or not valid value as 表 6 recommended during the initialization. LP8866-Q1 defaults to phase-shift PWM mode with I2C enabled if MODE resistor is missing or invalid. The MODESEL_STATUS fault bit will be set in the BOOST_FAULT_STATUS register, and the INT pin will be triggered. The MODE resistor missing or invalid fault is not monitored after initialization, so that the LP8866-Q1 operates in the mode determined during initialization even though the MODE resistor is missing or invalid after initialization.

7.3.9.2.5 FSET Resistor Missing Faults (FSET)

The FSET resistor missing or invalid for both BOOST_FSET and PWM_FSET is detected if any one of them is not assembled or not a valid value as 表 1 and 表 7 recommended during the initialization. LP8866-Q1 defaults the switching frequency of boost to 400 kHz if BOOST_FSET resistor is missing or invalid, or PWM dimming frequency to 305 Hz if PWM_FSET resistor is missing or invalid. The FSET_STATUS fault bit is set in the BOOST_FAULT_STATUS register, and the INT pin is triggered. The FSET resistor missing or invalid fault is not monitored after initialization, so that the LP8866-Q1 operates at the boost switching frequency and the PWM dimming frequency determined during initialization even though the FSET resistor is missing or invalid after initialization.

7.3.9.2.6 ISET Resistor Out of Range Faults (ISET)

If during device normal operation the ISET pin resistor is shorted to GND, the maximum current for each LED channel can be calculated in 公式 16:

$$I_{LED\_ISET\_FAULT} = \frac{I_{LED\_LIMIT}}{4} \times \left(\frac{LED\_CURRENT[11:0]}{4095} \right) \quad (16)$$

LED_CURRENT[11:0] register will be written to 1/4 of latest programmed data through I2C. The default value of LED_CURRENT[11:0] register is 0xFFF if it's not programmed after device enabling. If ISET pin voltage returns back to above 1.1 V, the LED_CURRENT[11:0] register data is written to latest programmed data through I2C. The ISET_STATUS fault bit will be set in the BOOST_FAULT_STATUS register and the INT pin is triggered.

7.3.9.2.7 Thermal Shutdown Faults (TSD)

If the die temperature of LP8866-Q1 reaches the thermal shutdown threshold T_{SD}, the boost, power-line FET, and LED outputs on LP8866-Q1 shuts down to protect the device from damage. Fault status bit TSD_STATUS bit will be set, and the INT pin will be triggered. The device restarts the power-line FET, the boost, and LED outputs when temperature drops by TSD_HYS amount.

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7.3.9.3 LED Faults

7.3.9.3.1 Open LED Faults (OPEN_LED)

During normal boost operation, boost voltage is raised if any of the used LED outputs falls below the LED_DRV_HEADROOM threshold level. Open LED fault is detected if boost output voltage has reached the maximum and at least one LED output is still below the threshold. The open string is then disconnected from the boost adaptive control loop and its output is disabled. Any LED fault sets the status bit LED_STATUS and an interrupt is generated unless LED interrupt is disabled. The detail of open LED faults can be read from bits OPEN_LED and LEDx_FAULT (x = 1...6, indicating the faulty LED) in LED_FAULT_STATUS register. These bits maintain their value until device power-down while the LED_STATUS bit is cleared by the interrupt clearing procedure. If a new LED fault is detected, LED_STATUS is set and an interrupt generated again.

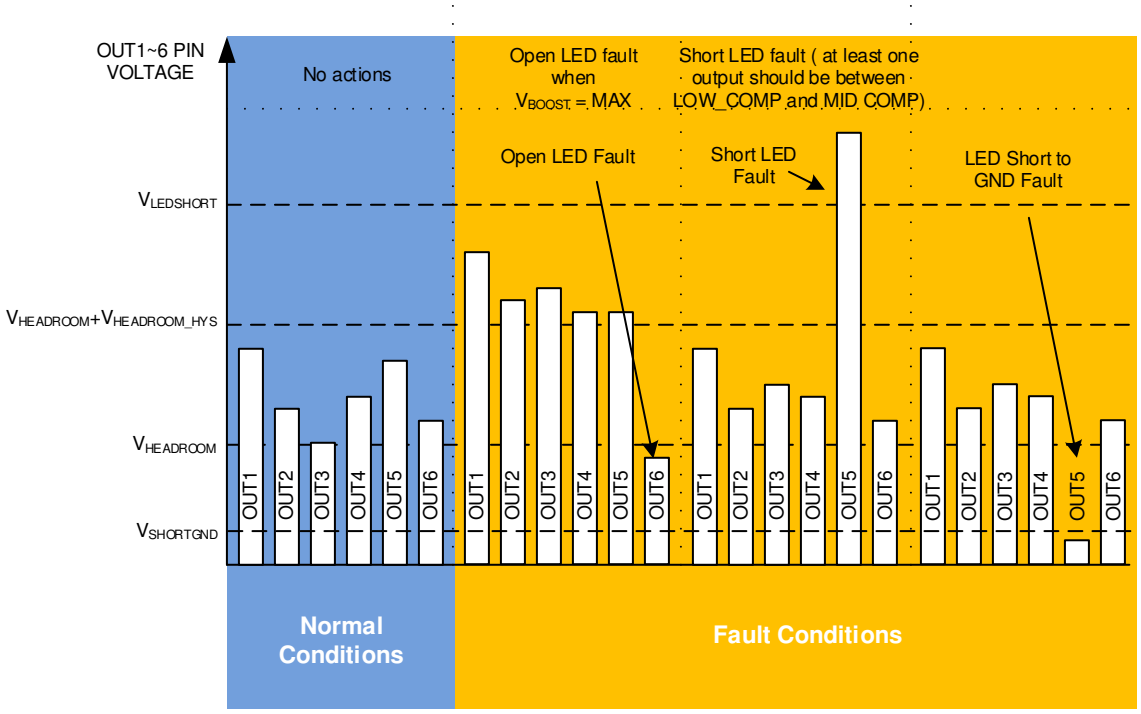

图 18. LED Open and Short Detection Logic

7.3.9.3.2 Short LED Faults (SHORT_LED)

Short LED fault is detected if one or more LED outputs are above the $V_{LEDSHORT}$ typical 6 V and at least one LED output is inside the normal operation window (see 图 18). Shorted string is disconnected from the boost adaptive control loop and the LED PWM output is disabled. LED_STATUS status bit is set and an interrupt generated similarly as in open LED case. Detailed shorted LED fault can be read from bits SHORT_LED and LEDx_FAULT (x = 1...6, indicating the faulty LED) in LED_FAULT_STATUS register.

In HUD application, when output channels are connected as groups and only one or two groups are active, one more special condition will trigger the short LED fault. This is when boost adaptive voltage comes to minimum and one of the LED channels' voltage is still higher than $V_{HEADROOM}$ + $V_{HEADROOM\_HYS}$.

7.3.9.3.3 LED Short to GND Faults (GND_LED)

During power line FET pre-charge state, each active LED output pins outputs a typical 6-mA current for 300-µs period. The LED output pin is recognized as short to GND if its voltage is lower than $V_{HEADROOM}$ in this time period. LED short to GND fault will be reported.

During boost soft start and normal boost operation, if LED output is lower than $V_{SHORTGND}$ for 20 ms, device turns off the corresponding LED output channel and output a typical 6-mA current for 300-µs period again. After this operation, if output voltage is still lower than $V_{HEADROOM}$, LED short to GND fault will be reported.

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If LED short to GND is reported, boost, LED outputs and power-line FET is turned off, the device will enter STANDBY mode. LED_STATUS bit is set and an interrupt generated similarly as in open LED case. LED short to GND fault reason can be read from bits LED_GND and LEDx_FAULT (x = 0...6, indicating the faulty LED) in LED_FAULT_STATUS register. These bits maintain their value until device powers are down while the LED_STATUS bit is cleared by the interrupt clearing procedure.

7.3.9.3.4 Invalid LED String Faults (INVSTRING)

During device initialization, any of un-used LED outputs pins are checked whether connected to GND or not. If they are not connected to GND as expected, the LP8866-Q1 reports invalid string fault and tries to function normally if possible. The INVSTRING_STATUS fault bit is set in the LED_FAULT_STATUS register, and the INT pin is triggered. The LEDSET resistor missing or invalid fault is not detected after initialization, so that the LP8866-Q1 operates in the configuration determined during initialization even though the LEDSET resistor is missing or invalid after initialization.

7.3.9.3.5 I2C timeout Faults

If chip receives I2C command without STOP signal for 500 ms, I2C communication block auto resets and waits for the next command. I2C_ERROR_STATUS fault bit is set in the LED_FAULT_STATUS register, and the INT pin is triggered.

7.3.9.4 Overview of the Fault/Protection Schemes

表 8. Fault/Protection Schemes

FAULT NAME	STATUS BIT	CONDITION	TRIGGER FAULT INTERRUPT	ENTER FAULT RECOVERY	ACTION
V_{IN} undervoltage	VINUVLO_STATUS	UVLO voltage falls below 0.787 V.	Yes	Yes	Device goes to standby and then attempts to restart once the input voltage rises above threshold.
V_{IN} overvoltage	VINOVP_STATUS	V_{IN} voltage rises above 43 V	Yes	Yes	Device goes to standby and waits until input voltage falls below threshold before restarting.
V_{DD} undervoltage	VDDUVLO_STATUS	V_{DD} level falls below VDDUVLO threshold.	Yes	No	Device restarts once VDD level rises above VDDUVLO threshold.
V_{IN} overcurrent	VINOCP_STATUS	Voltage across R_{ISENSE} exceeds 220 mV	Yes	Yes	Device goes to standby and then attempts to restart 100 ms after fault occurs.
Charge pump fault	CP_STATUS	Charge pump voltage level is abnormal.	Yes	Yes	Device goes to standby and then attempts to restart 100 ms after fault occurs.
Charge pump components missing	CPCAP_STATUS	Charge pump is missing components.	Yes	No	Charge pump is disabled. Charge pump fault will be reported. Device tries to keep normal operation
Boost sync clock invalid fault	BSTSYNC_STATUS	Device is enabled while a valid external SYNC clock is running. Then SYNC stops or changes to frequency <75kHz	Yes	No	Defaults to internal clock frequency selected by BST_FSET resistor. If BST_SYNC input is held high then spread spectrum is enabled. If BST_SYNC input is held low then spread spectrum is disabled
CRC error	CRCERR_STATUS	Factory default configuration for registers, options and trim bits are not corrected loaded from memory	Yes	No	Device functions normally, if possible.
Boost OVP low	BSTOVPLOW_STATUS	FB pin voltage rises above V_{FB_OVPL} level	No	No	Boost stops switching until boost voltage level falls. The device remains in normal mode with LED drivers operational.
Boost OVP high	BSTOVPH_STATUS	FB pin voltage rises above V_{FB_OVPH} level or DISCHARGE pin voltage rises above V_{BST_OVPH}	Yes	Yes	Device goes to standby and waits until output voltage falls below threshold before restarting.
Boost overcurrent	BSTOCP_STATUS	FB pin voltages falls below V_{UVP} level for 110 ms	Yes	Yes	Device goes to standby and then attempts to start 100 ms after fault occurs.
LEDSET detection fault	LEDSET_STATUS	LEDSET resistor missing or invalid	Yes	No	Defaults to 6-channel / 200mA configuration
MODE detection fault	MODESEL_STATUS	MODE resistor missing or invalid	Yes	No	Defaults to phase-shift PWM mode, I2C is enabled
FSET detection fault	FSET_STATUS	BST_FSET or PWM_FSET resistor are missing or an invalid value	Yes	No	Device keeps operating at 400kHz switching frequency for boost converter and 305Hz for PWM dimming frequency.
ISET resistor fault	ISET_STATUS	ISET pin voltage is pulled down to below 1V due to ISET pin resistor shorted to GND	Yes	No	LED_CURRENT[11:0] is written to 0x3FF. Total LED current limited to 65mA.

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表 8. Fault/Protection Schemes (接下页)

Thermal shutdown	TSD_STATUS	Junction temperature rises above T_{SD} threshold.	Yes	Yes	Device goes to standby and then attempts to restart once die temperature falls below threshold.
Open LED string	LED_STATUS OPEN_LED	Headroom voltage on one or more channels is below minimum level and boost has adapted to maximum level.	Yes	No	Faulted LED string is disabled and removed from adaptive boost control loop. String is re-enabled next power cycle.
LED internal short	LED_STATUS_SHORT_LED	Headroom voltage on one or more channels is above the SHORTED_LED_THRESHOLD for > 5 ms while the headroom of at least one channel is still below this threshold.	Yes	No	Faulted LED string is disabled and removed from adaptive boost control loop. String is re-enabled next power cycle.
LED short to GND	LED_STATUS_GND_LED	During PL FET SOFT START, voltage of one or more used LED output is below $V_{HEADROOM}$ when small test current is injected. In BOOST_SU and Normal Stage, voltage of one or more used LED output is below $V_{SHORTGND}$.and keeps still when the corresponding channel is off and small test current is injected	Yes	Yes	Device goes to standby and then attempts to restart 100 ms after fault occurs.
Invalid LED string detected	INVSTRING_STATUS	Configured unused LED output is detected not short to GND.	Yes	No	Device functions normally, if possible.
I2C timeout	I2C_ERROR_STATUS	Device receives I2C command without STOP signal for 500 ms	Yes	No	Device functions normally and waits for the next I2C command.

ADVANCE INFORMATION

7.4 Device Functional Modes

7.4.1 State Diagram

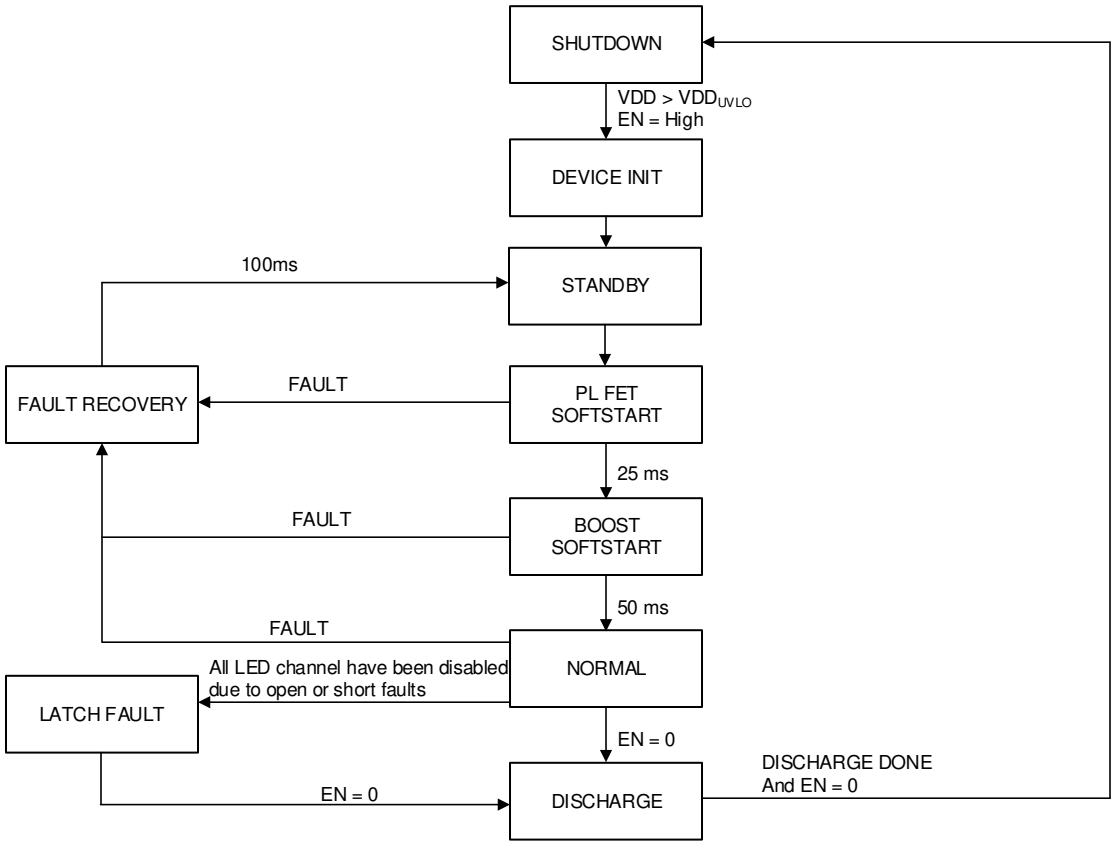

图 19. State Machine Diagram

7.4.2 Shutdown

When EN is pulled low, boost, power-line FET, and LED outputs are turned off, and the device tries to discharge the boost output for 400 ms. After this, the device is totally turned off.

7.4.3 Device Initialization

After POR is released device initialization begins. During this state the LDO is started up, EEPROM default and trim configurations are loaded, LEDSET, MODE, BOOST_FSET and PWM_FSET resistors are detected.

7.4.4 Standby Mode

In standby the Fault/Protection Schemes device can be accessed with I2C to change any configuration registers.

7.4.5 Power-line FET Soft Start

Power-line FET is enabled, and boost input and output capacitors are charged to V_{IN} level. V_{IN} faults for OCP, OVP, and UVP and fault for LED short to GND are enabled.

7.4.6 Boost Start-Up

Boost voltage is ramped to initial boost voltage level with reduced current limit for 50 ms. All boost faults are now enabled.

7.4.7 Normal Mode

LED drivers are enabled when brightness is greater than zero. All LED faults are active.

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Device Functional Modes (接下页)

7.4.8 Fault Recovery

Non-LED faults can trigger fault recover state. LED drivers, boost converter, and power-line FET are disabled for 100 ms, and the device attempts to restart from standby mode if EN is still high and brightness is greater than zero.

7.4.9 Latch Fault

If all LED strings are disabled due to faults then the LP8866-Q1 enters the latch fault mode. This state can be exited only by pulling the EN pin low.

7.4.10 Start-Up Sequence

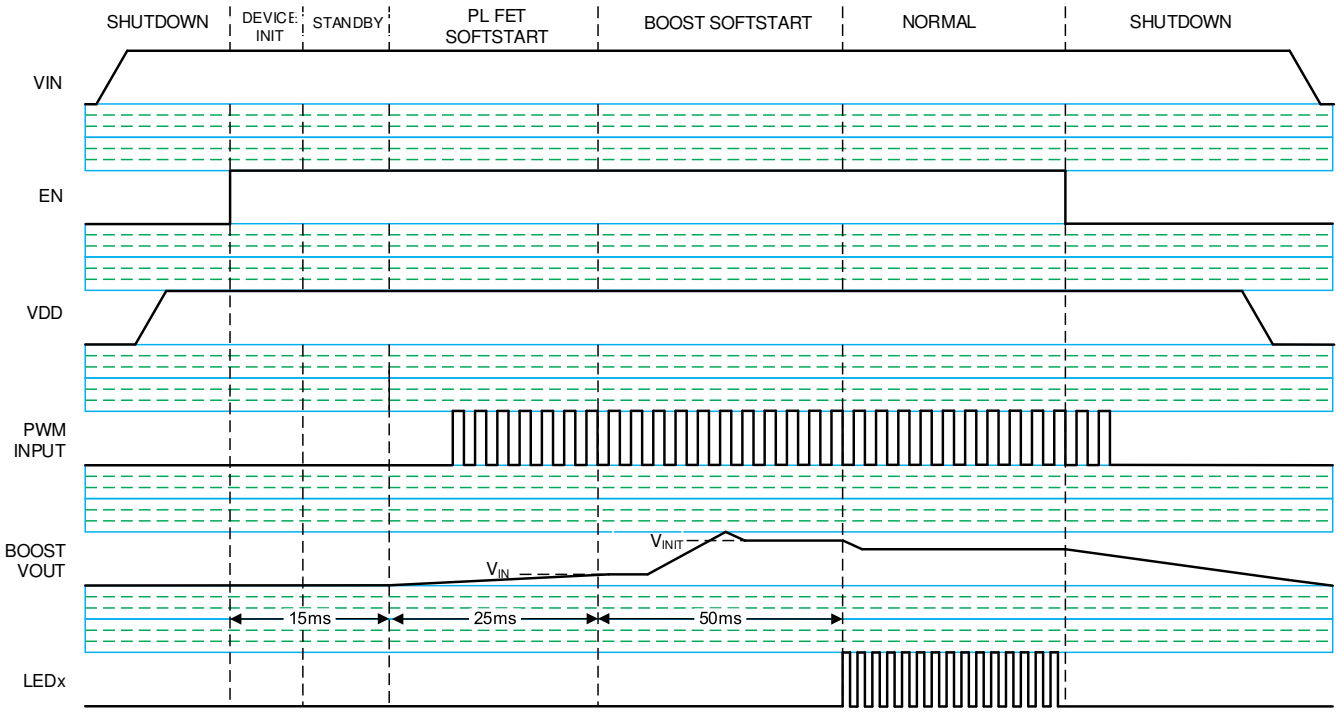

图 20. Start-Up Sequence Diagram

7.5 Programming

7.5.1 I2C-Compatible Interface

The LP8866-Q1 device supports I2C interface to access and change the configuration. The 7-bit base slave address is 0x2A.

Write I2C transactions are made up of 4 bytes. The first byte includes the 7-bit slave address and Write bit. The 7-bit slave address selects the LP8866-Q1 slave device. The second byte is eight bits register address. The last two bytes are the 16-bit register value.

Read I2C transactions are made up of 5 bytes. The first byte includes the 7-bit slave address and Write bit. The 7-bit slave address selects the LP8866-Q1 slave device. The second byte is eight bits register address. The third byte includes the 7-bit slave address and Read bit. The last two bytes are the 16-bit register value returned from the slave.

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Programming (接下页)

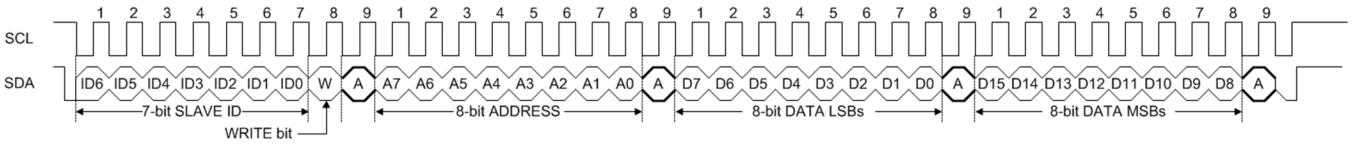

图 21. I2C Write

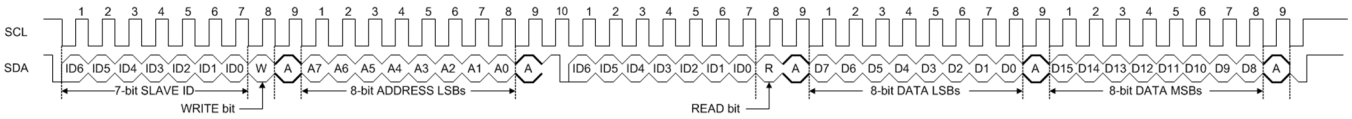

图 22. I2C Read

ADVANCE INFORMATION

Programming (接下页)

7.5.2 Programming Examples

7.5.2.1 General Configuration Registers

The LP8866-Q1 does not require any serial interface configuration. It can be simply controlled with the EN pin and PWM pin. Most of the device configuration is accomplished using external resistor values. If I2C interface is available then extended configuration is possible. The configuration registers can be written from standby state to normal state as shown in 表 9.

表 9. Configuration Registers

REGISTER NAME	FUNCTION
EN_MIN_PWM_LIMIT	Enables 200-ns PWM pulse limit and frequency dither to reach lower minimum brightness levels.
ADV_SLOPE_ENABLE	Enables advance sloper S-shape smoothing function.
DITHER_SELECT	Selects up to 3 bits of PWM dither for added dimming resolution.
SLOPE_SELECT	Selects duration for linear brightness sloper.
BRT_MODE	Selects PWM pin or DISPLAY_BRT register for brightness control.
SPREAD_RANGE	Selects up to 2 bits boost switching frequency spread spectrum range.
SPREAD_MOD_FREQ	Selects up to 2 bits boost switching frequency spread spectrum modulation frequency.
SPREAD_PSEUDO_EN	Enables pseudo random modulation for boost switching spread spectrum frequency

7.5.2.2 Clearing Fault Interrupts

The LP8866-Q1 has an INT pin to alert the host when a fault occurs. If I2C interface is available, the Interrupt Fault Status registers can be read back to learn which fault(s) have been detected. These status bits are located in the SUPPLY_STATUS, BOOST_STATUS and LED_STATUS registers. Each interrupt status has a STATUS bit and a CLEAR bit. To clear a fault interrupt status a 1 must be written to both the STATUS bit and CLEAR bit at the same time.

7.5.2.3 Disabling Fault Interrupts

By default most of the LP8866-Q1 faults trigger the INT pin. Each fault has two INT_EN bits. These bits are located in the SUPPLY_INT_EN, BOOST_INT_EN, and LED_INT_EN registers. If the INT_EN bit is read and returns 2b'10, the INT pin is triggered when that fault occurs. The fault interrupt can be disabled by writing 2b'01 to its INT_EN bits, or it can be enabled by writing 2b'11 to its INT_EN bits. There is also a GLOBAL fault interrupt that can be disabled to prevent any faults from triggering the INT pin.

7.5.2.4 Diagnostic Registers

The LP8866-Q1 contains several diagnostic registers than can be read with the serial interface for debugging or additional device information. 表 10 is a summary of the available registers.

表 10. Diagnostic Registers

REGISTER NAME	FUNCTION
FSM_LIVE_STATUS	Current state of the functional state machine
PWM_INPUT_STATUS	Measured 16-bit duty cycle of the PWM pin input
LED_PWM_STATUS	16-bit LED PWM duty cycle from state machine
LED_CURRENT_STATUS	12-bit LED current DAC value from state machine
VBOOST_STATUS	10-bit value for adaptive boost voltage target — value is linear between VBOOST_MIN and VBOOST_MAX calculations
MODE_SEL_CFG	Dimming mode configuration from MODE detection
LED_STRING_CFG	LED string phase configuration from LEDSET detection
BOOST_FREQ_SEL	Boost switching frequency value from BST_FSET detection
PWM_FREQ_SEL	LED PWM frequency value from PWM_FSET detection

ADVANCE INFORMATION

7.6 Register Maps

7.6.1 FullMap Registers

Table 11 lists the memory-mapped registers for the FullMap registers. All register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

Table 11. FULLMAP Registers

Offset	Acronym	Register Name	Section
00h	BRT_CONTROL	Display Brightness	Go
02h	LED_CURR_CONFIG	LED Current	Go
04h	USER_CONFIG1	User Config 1	Go
06h	USER_CONFIG2	User Config 2	Go
08h	SUPPLY_INT_EN	Supply Interrupt Enable	Go
0Ah	BOOST_INT_EN	Boost Interrupt Enable	Go
0Ch	LED_INT_EN	LED Interrupt Enable	Go
0Eh	SUPPLY_STATUS	Supply Fault Status	Go
10h	BOOST_STATUS	Boost Fault Status	Go
12h	LED_STATUS	LED Fault Status	Go
14h	FSM_DIAGNOSTICS	Device State Diagnostics	Go
16h	PWM_INPUT_DIAGNOSTICS	PWM Input Diagnostics	Go
18h	PWM_OUTPUT_DIAGNOSTICS	PWM Output Diagnostics	Go
1Ah	LED_CURR_DIAGNOSTICS	LED Current Diagnostics	Go
1Ch	ADAPT_BOOST_DIAGNOSTICS	Adaptive Boost Diagnostics	Go
1Eh	AUTO_DETECT_DIAGNOSTICS	Auto Detect Diagnostics	Go

Complex bit access types are encoded to fit into small table cells. Table 12 shows the codes that are used for access types in this section.

Table 12. FullMap Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 BRT_CONTROL Register (Offset = 00h) [reset = 0h]

BRT_CONTROL is shown in Figure 23 and described in Table 13.

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Figure 23. BRT_CONTROL Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISPLAY_BRT															
R/W-0h															

Table 13. BRT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DISPLAY_BRT	R/W	0h	Display Brightness Register

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7.6.1.2 LED_CURR_CONFIG Register (Offset = 02h) [reset = 0FFFh]

LED_CURR_CONFIG is shown in Figure 24 and described in Table 14.

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Figure 24. LED_CURR_CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				LED_CURRENT											
R/W-0h				R/W-FFFh											

Table 14. LED_CURR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	These bits are reserved.
11-0	LED_CURRENT	R/W	FFFh	LED current control for all LED outputs

7.6.1.3 USER_CONFIG1 Register (Offset = 04h) [reset = 8A3h]

USER_CONFIG1 is shown in Figure 25 and described in Table 15.

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Figure 25. GROUPING1 Register

15	14	13	12	11	10	9	8
RESERVED	SPREAD_PSEUDO_EN	SPREAD_MOD_FREQ		SPREAD_RANGE		BRT_MODE	
R/W-0h	R/W-0h	R/W-0h		R/W-2h		R/W-0h	
7	6	5	4	3	2	1	0
SLOPE_SELECT			DITHER_SELECT			ADV_SLOPE_ENABLE	EN_MIN_PWM_LIMIT
R/W-5h			R/W-0h			R/W-1h	R/W-1h

Table 15. USER_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	This bit is reserved.
14	SPREAD_PSEUDO_EN	R/W	0h	0h = Pseudo Random SS disabled 1h = Pseudo Random SS enabled
13-12	SPREAD_MOD_FREQ	R/W	0h	Boost spread spectrum modulation frequency 0h = 200Hz 1h = 500Hz 2h = 800Hz 3h = 1.2kHz
11-10	SPREAD_RANGE	R/W	2h	OSC_BST spread spectrum range 0h = 3.3% 1h = 4.3% 2h = 5.3% 3h = 7.2%
9-8	BRT_MODE	R/W	0h	Select PWM pin or DISPLAY_BRT register for brightness controll 0h = Brightness controlled by PWM input 1h = Reserved 2h = Brightness controlled by DISPLAY_BRT register 3h = Reserved

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Table 15. USER_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	SLOPE_SELECT	R/W	5h	Select duration for linear brightness sloper 0h = Disabled 1h = 1ms 2h = 2ms 3h = 50ms 4h = 100ms 5h = 200ms 6h = 300ms 7h = 500ms Times are for linear slope mode. Advanced sloper will increase durations while adding additional smoothing to brightness transitions. 1 ms and 2 ms sloper times are intended to be used only in linear mode. 50 ms to 500 ms sloper durations may be used with or without advanced sloper function.
4-2	DITHER_SELECT	R/W	0h	Dither mode select 0h = Dither Disabled 1h = 1-bit Dither 2h = 2-bit Dither 3h = 3-bit Dither 4h = 4-bit Dither
1	ADV_SLOPE_ENABLE	R/W	1h	0h = Linear Sloping 1h = Advanced Sloping
0	EN_MIN_PWM_LIMIT	R/W	1h	Allows PWM pulses to be dithered to reduce lower minimum brightness. 0h = Disabled 1h = Enabled

7.6.1.4 USER_CONFIG2 Register (Offset = 06h) [reset = 100h]

USER_CONFIG2 is shown in Figure 26 and described in Table 16.

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Figure 26. USER_CONFIG2 Register

15	14	13	12	11	10	9	8
RESERVED							EN_LED_GND_DETECT
R/W-0h							R/W-1h
7	6	5	4	3	2	1	0
RESERVED		LED6_SHORT_DISABLE	LED5_SHORT_DISABLE	LED4_SHORT_DISABLE	LED3_SHORT_DISABLE	LED2_SHORT_DISABLE	LED1_SHORT_DISABLE
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 16. USER_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	These bits are reserved.
8	EN_LED_GND_DETECT	R/W	1h	Enable LED short to ground detection during Boost_SS and normal stage 0h = Disable 1h = Enable
7-6	RESERVED	R/W	0h	These bits must write 0 for normal operation.

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Table 16. USER_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	LED6_SHORT_DISABLE	R/W	0h	Disable LED string6 internal short fault. 0h = Enable 1h = Disable
4	LED5_SHORT_DISABLE	R/W	0h	Disable LED string5 internal short fault. 0h = Enable 1h = Disable
3	LED4_SHORT_DISABLE	R/W	0h	Disable LED string4 internal short fault. 0h = Enable 1h = Disable
2	LED3_SHORT_DISABLE	R/W	0h	Disable LED string3 internal short fault. 0h = Enable 1h = Disable
1	LED2_SHORT_DISABLE	R/W	0h	Disable LED string2 internal short fault. 0h = Enable 1h = Disable
0	LED1_SHORT_DISABLE	R/W	0h	Disable LED string1 internal short fault. 0h = Enable 1h = Disable

7.6.1.5 SUPPLY_INT_EN Register (Offset = 08h) [reset = 2AAAh]

SUPPLY_INT_EN is shown in Figure 27 and described in Table 17.

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Figure 27. SUPPLY_INT_EN Register

15	14	13	12	11	10	9	8
RESERVED		BSTSYNC_INT_EN		CP_INT_EN		CPCAP_INT_EN	
R/W-0h		R/W-2h		R/W-2h		R/W-2h	
7	6	5	4	3	2	1	0
VINOCP_INT_EN		VDDUVLO_INT_EN		VINOVP_INT_EN		VINUVLO_INT_EN	
R/W-2h		R/W-2h		R/W-2h		R/W-2h	

Table 17. SUPPLY_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	These bits are reserved.
13-12	BSTSYNC_INT_EN	R/W	2h	Missing boost sync interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt

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Table 17. SUPPLY_INT_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	CP_INT_EN	R/W	2h	Charge pump interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
9-8	CPCAP_INT_EN	R/W	2h	Charge pump cap missing interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
7-6	VINOCP_INT_EN	R/W	2h	V_{IN} over-current interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
5-4	VDDUVLO_INT_EN	R/W	2h	V_{DD} under-voltage interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
3-2	VINOVP_INT_EN	R/W	2h	V_{IN} over-voltage interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
1-0	VINUVLO_INT_EN	R/W	2h	V_{IN} under-voltage interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt

7.6.1.6 BOOST_INT_EN Register (Offset = 0Ah) [reset = AAAAh]

BOOST_INT_EN is shown in Figure 28 and described in Table 18.

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Figure 28. BOOST_INT_EN Register

15	14	13	12	11	10	9	8
TSD_INT_EN		ISET_INT_EN		LEDSET_INT_EN		MODE_INT_EN	
R/W-2h		R/W-2h		R/W-2h		R/W-2h	
7	6	5	4	3	2	1	0
FSET_INT_EN		BSTOCP_INT_EN		BSTOVPH_INT_EN		BSTOVPL_INT_EN	
R/W-2h		R/W-2h		R/W-2h		R/W-2h	

Table 18. BOOST_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TSD_INT_EN	R/W	2h	Thermal shutdown interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
13-12	ISET_INT_EN	R/W	2h	ISET resistor short to ground interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
11-10	LEDSET_INT_EN	R/W	2h	Missing LEDSET resistor interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
9-8	MODE_INT_EN	R/W	2h	Missing MODE resistor interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
7-6	FSET_INT_EN	R/W	2h	Missing FSET resistor interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
5-4	BSTOCP_INT_EN	R/W	2h	Boost over-current interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt

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Table 18. BOOST_INT_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	BSTOVPH_INT_EN	R/W	2h	Boost over-voltage high interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
1-0	Reserved	R/W	2h	These bits are reserved.

7.6.1.7 LED_INT_EN Register (Offset = 0Ch) [reset = AAh]

LED_INT_EN is shown in Figure 29 and described in Table 19.

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Figure 29. LED_INT_EN Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
I2C_ERROR_INT_EN		GLOBAL_INT_EN		INVSTRING_INT_EN		VINUVP_INT_EN	
R/W-2h		R/W-2h		R/W-2h		R/W-2h	

Table 19. LED_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	These bits are reserved.
7-6	I2C_ERROR_INT_EN	R/W	2h	I2C time out interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
5-4	GLOBAL_INT_EN	R/W	2h	Global interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt
3-2	INVSTRING_INT_EN	R/W	2h	Invalid LED string configuration interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt

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Table 19. LED_INT_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	LED_INT_EN	R/W	2h	LED open/internal short/short to GND interrupt enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt

7.6.1.8 SUPPLY_STATUS Register (Offset = 0Eh) [reset = 0h]

SUPPLY_STATUS is shown in Figure 30 and described in Table 20.

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Figure 30. SUPPLY_STATUS Register

15	14	13	12	11	10	9	8
CRCERR_STATUS	CRCERR_CLEAR	BSTSYNC_STATUS	BSTSYNC_CLEAR	CP_STATUS	CP_CLEAR	CPCAP_STATUS	CPCAP_CLEAR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VINOCP_STATUS	VINOCP_CLEAR	VDDUVLO_STATUS	VDDUVLO_CLEAR	VINOVP_STATUS	VINOVP_CLEAR	VINUVLO_STATUS	VINUVLO_CLEAR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 20. SUPPLY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CRCERR_STATUS	R/W	0h	CRC error fault status 0h = No fault 1h = Fault
14	CRCERR_CLEAR	R/W	0h	CRC error fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
13	BSTSYNC_STATUS	R/W	0h	Missing boost sync fault status 0h = No fault 1h = Fault
12	BSTSYNC_CLEAR	R/W	0h	Missing boost sync fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
11	CP_STATUS	R/W	0h	Charge pump fault status 0h = No fault 1h = Fault
10	CP_CLEAR	R/W	0h	Charge pump fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
9	CPCAP_STATUS	R/W	0h	Missing charge pump fault status 0h = No fault 1h = Fault
8	CPCAP_CLEAR	R/W	0h	Missing charge pump fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status

Table 20. SUPPLY_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	VINOCP_STATUS	R/W	0h	V_{IN} over-current fault status 0h = No fault 1h = Fault
6	VINOCP_CLEAR	R/W	0h	V_{IN} over-current fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
5	VDDUVLO_STATUS	R/W	0h	V_{DD} under-voltage fault status 0h = No fault 1h = Fault
4	VDDUVLO_CLEAR	R/W	0h	V_{DD} under-voltage fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
3	VINOVP_STATUS	R/W	0h	V_{IN} over-voltage fault status 0h = No fault 1h = Fault
2	VINOVP_CLEAR	R/W	0h	V_{IN} over-voltage fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
1	VINUVLO_STATUS	R/W	0h	V_{IN} under-voltage fault status 0h = No fault 1h = Fault
0	VINUVLO_CLEAR	R/W	0h	V_{IN} under-voltage fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status

7.6.1.9 BOOST_STATUS Register (Offset = 10h) [reset = 0h]

BOOST_STATUS is shown in Figure 31 and described in Table 21.

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Figure 31. BOOST_STATUS Register

15	14	13	12	11	10	9	8
TSD_STATUS	TSD_CLEAR	ISET_STATUS	ISET_CLEAR	LEDSET_STATUS	LEDSET_CLEAR	MODESEL_STATUS	MODESEL_CLEAR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
FSET_STATUS	FSET_CLEAR	BSTOCP_STATUS	BSTOCP_CLEAR	BSTOVPH_STATUS	BSTOVPH_CLEAR	BSTOVPL_STATUS	BSTOVPL_CLEAR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 21. BOOST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TSD_STATUS	R/W	0h	Thermal shutdown fault status 0h = No fault 1h = Fault
14	TSD_CLEAR	R/W	0h	Thermal shutdown fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status

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Table 21. BOOST_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ISET_STATUS	R/W	0h	ISET resistor short to ground fault status 0h = No fault 1h = Fault
12	ISET_CLEAR	R/W	0h	ISET resistor short to ground fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
11	LEDSET_STATUS	R/W	0h	Missing LED resistor fault status 0h = No fault 1h = Fault
10	LEDSET_CLEAR	R/W	0h	Missing LED resistor fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
9	MODESEL_STATUS	R/W	0h	Missing MODE SEL resistor fault status 0h = No fault 1h = Fault
8	MODESEL_CLEAR	R/W	0h	Missing MODE SEL resistor fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
7	FSET_STATUS	R/W	0h	Missing boost FSET resistor fault status 0h = No fault 1h = Fault
6	FSET_CLEAR	R/W	0h	Missing boost FSET resistor fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
5	BSTOCP_STATUS	R/W	0h	Boost over-current fault status 0h = No fault 1h = Fault
4	BSTOCP_CLEAR	R/W	0h	Boost over-current fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
3	BSTOVPH_STATUS	R/W	0h	Boost OVP high fault status 0h = No fault 1h = Fault
2	BSTOVPH_CLEAR	R/W	0h	Boost OVP high fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
1	BSTOVPL_STATUS	R/W	0h	Boost OVP low fault status 0h = No fault 1h = Fault
0	BSTOVPL_CLEAR	R/W	0h	Boost OVP low fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status

7.6.1.10 LED_STATUS Register (Offset = 12h) [reset = 0h]

LED_STATUS is shown in Figure 32 and described in Table 22.

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Figure 32. LED_STATUS Register

15	14	13	12	11	10	9	8
RESERVED	I2C_ERROR_STATUS	I2C_ERROR_CLEAR	INVSTRING_STATUS	INVSTRING_CLEAR	LED_STATUS	LED_CLEAR	GND_LED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SHORT_LED	OPEN_LED	LED6_FAULT	LED5_FAULT	LED4_FAULT	LED3_FAULT	LED2_FAULT	LED1_FAULT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 22. LED_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	This bit is reserved
14	I2C_ERROR_STATUS	R/W	0h	I2C time out fault status 0h = No fault 1h = Fault
13	I2C_ERROR_CLEAR	R/W	0h	I2C time out fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
12	INVSTRING_STATUS	R/W	0h	Invalid string configuration fault status 0h = No fault 1h = Fault
11	INVSTRING_CLEAR	R/W	0h	Invalid string configuration fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
10	LED_STATUS	R/W	0h	LED open/internal short/short to GND fault status 0h = No fault 1h = Fault
9	LED_CLEAR	R/W	0h	LED open/internal short/short to GND fault clear Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status
8	GND_LED	R	0h	LED short to GND fault status 0h = No fault 1h = Fault
7	SHORT_LED	R	0h	LED internal short Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
6	OPEN_LED	R	0h	LED open fault status 0h = No fault 1h = Fault Status is cleared with LED_STATUS bit
5	LED6_FAULT	R	0h	LED 6 Status 0h = No Fault 1h = Fault
4	LED5_FAULT	R	0h	LED 5 Status 0h = No Fault 1h = Fault
3	LED4_FAULT	R	0h	LED 4 Status 0h = No Fault 1h = Fault

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Table 22. LED_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LED3_FAULT	R	0h	LED 3 Status 0h = No Fault 1h = Fault
1	LED2_FAULT	R	0h	LED 2 Status 0h = No Fault 1h = Fault
0	LED1_FAULT	R	0h	LED 1 Status 0h = No Fault 1h = Fault

7.6.1.11 FSM_DIAGNOSTICS Register (Offset = 14h) [reset = 0h]

FSM_DIAGNOSTICS is shown in Figure 33 and described in Table 23.

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Figure 33. FSM_DIAGNOSTICS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			FSM_LIVE_STATUS				
R-0h			R-0h				

Table 23. FSM_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	These bits are reserved
4-0	FSM_LIVE_STATUS	R	0h	Current state of the functional state machine 0h = DISABLED 1h = LDO_STARTUP 2h = OTP_READ 3h = STANDBY 4h-Fh = BOOST_STARTUP 10h = NORMAL 11h = SHUTDOWN 12h = FAULT_RECOVERY 13h = ALL_LED_FAULT

7.6.1.12 PWM_INPUT_DIAGNOSTICS Register (Offset = 16h) [reset = 0h]

PWM_INPUT_DIAGNOSTICS is shown in Figure 34 and described in Table 24.

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Figure 34. PWM_INPUT_DIAGNOSTICS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_INPUT_STATUS															
R-0h															

Table 24. PWM_INPUT_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PWM_INPUT_STATUS	R	0h	16-bit value for detected duty cycle of PWM input signal.

7.6.1.13 6.6.1.13 PWM_OUTPUT_DIAGNOSTICS Register (Offset = 18h) [reset = 0h]

PWM_OUTPUT_DIAGNOSTICS is shown in Figure 35 and described in Table 25.

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Figure 35. PWM_OUTPUT_DIAGNOSTICS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_OUTPUT_STATUS															
R-0h															

Table 25. PWM_OUTPUT_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PWM_OUTPUT_STATUS	R	0h	16-bit value for configured duty cycle of PWM output signal.

7.6.1.14 LED_CURR_DIAGNOSTICS Register (Offset = 1Ah) [reset = 0h]

LED_CURR_DIAGNOSTICS is shown in Figure 36 and described in Table 26.

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Figure 36. LED_CURR_DIAGNOSTICS Register

15	14	13	12	11	10	9	8
RESERVED				LED_CURRENT_STATUS			
R-0h				R-0h			
7	6	5	4	3	2	1	0
LED_CURRENT_STATUS							
R-0h							

Table 26. LED_CURR_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	These bits are reserved.
11-0	LED_CURRENT_STATUS	R	0h	12-bit Current DAC Code that Brightness path is driving to OUT1-6 output.

7.6.1.15 ADAPT_BOOST_DIAGNOSTICS Register (Offset = 1Ch) [reset = 0h]

ADAPT_BOOST_DIAGNOSTICS is shown in Figure 37 and described in Table 27.

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Figure 37. ADAPT_BOOST_DIAGNOSTICS Register

15	14	13	12	11	10	9	8
RESERVED					VBOOST_STATUS		
R-0h					R-0h		
7	6	5	4	3	2	1	0
VBOOST_STATUS							
R-0h							

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Table 27. ADAPT_BOOST_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	These bits are reserved.
10-0	VBOOST_STATUS	R	0h	11-bit Boost Voltage Code that Adaptive Voltage Control Loop sending to Analog Boost Block. In two-resistor method, Boost Output Voltage =((1+R1/R2)*1.21V)+(R1*18.9nA*VBOOST_STATUS)

7.6.1.16 AUTO_DETECT_DIAGNOSTICS Register (Offset = 1Eh) [reset = 0h]

AUTO_DETECT_DIAGNOSTICS is shown in Figure 38 and described in Table 28.

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Figure 38. AUTO_DETECT_DIAGNOSTICS Register

15	14	13	12	11	10	9	8
RESERVED	AUTO_PWM_FREQ_SEL			RESERVED	AUTO_LED_STRING_CFG		
R-0h	R-0h			R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		AUTO_BOOST_FREQ_SEL			MODE_SEL		
R-0h		R-0h			R-0h		

Table 28. AUTO_DETECT_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	This bit is reserved
14-12	AUTO_PWM_FREQ_SEL	R	0h	LED PWM frequency value from PWM_SEL resistor detection 0h = 152Hz 1h = 305Hz 2h = 610Hz 3h = 1221Hz 4h = 2441Hz 5h = 4883Hz 6h = 9766Hz 7h = 19531Hz
11	RESERVED	R	0h	This bit is reserved
10-8	AUTO_LED_STRING_CFG	R	0h	LED string configuration from LED_SET resistor detection 0h = 6 separate strings 1h = 5 separate strings 2h = 4 separate strings 3h = 3 separate strings 4h = 2 separate strings 5h = 6 channel outputs connected in 3 groups to drive 3 strings 6h = 6 channel outputs connected in 2 groups to drive 2strings 7h = 6 channel outputs connected together to drive 1 string
7-6	RESERVED	R	0h	These bits are reserved

Table 28. AUTO_DETECT_DIAGNOSTICS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	AUTO_BOOST_FREQ_SEL	R	0h	Boost switching frequency value from PWM_FSET resistor detection 0h = 100kHz 1h = 200kHz 2h = 303kHz 3h = 400kHz 4h = 500kHz 5h = 1818kHz 6h = 2000kHz 7h = 2222kHz
2-0	MODE_SEL	R	0h	LED dimming MODE value from MODE detection 0h = PWM mode, disable I2C 1h = 12.5% hybrid dimming mode, disable I2C 2h = Constant current mode, disable I2C 3h = Direct PWM, disable I2C 4h = PWM mode, enable I2C 5h = 12.5% hybrid dimming mode, enable I2C 6h = Constant current mode, enable I2C 7h = Direct PWM, enable I2C

ADVANCE INFORMATION

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP8866-Q1 device is designed for automotive applications, and an input voltage V_{IN} is intended to be connected to the vehicle battery. Depending on the input voltage, the device may be used in either boost mode or SEPIC mode. The device is internally powered from the VDD pin, and voltage must be in 2.7-V to 5.5-V range. The device has flexible configurability through external components or by an I2C interface. If the VDD voltage is not high enough to drive an external nMOSFET gate, an internal charge pump must be used to power the gate driver (GD pin).

注

For applications where V_{IN} voltage is below the output voltage, use a boost converter topology. Maximum operating voltage for V_{IN} is 48 V, and the boost converter can achieve output voltage up to 47 V. Conversion ratio of 5.5 (full load) or 10 (half load) must be taken into account. If V_{IN} voltage is expected to be below or above output voltage, a SEPIC converter can be implemented. The SEPIC converter can achieve maximum output voltage up to 24 V, and maximum conversion ratio for SEPIC mode is 5.

8.2 Typical Applications

8.2.1 Full Feature Application for Display Backlight

图 39 shows a full application for the LP8866-Q1 device in a boost topology. It supports 6 LED strings in display mode, each at 100 mA, with an automatic 60° phase shift. Brightness control register is used for LED dimming method through I2C communication. The charge pump is enabled for a 400-kHz boost switching frequency with spread spectrum.

ADVANCE INFORMATION

Typical Applications (接下页)

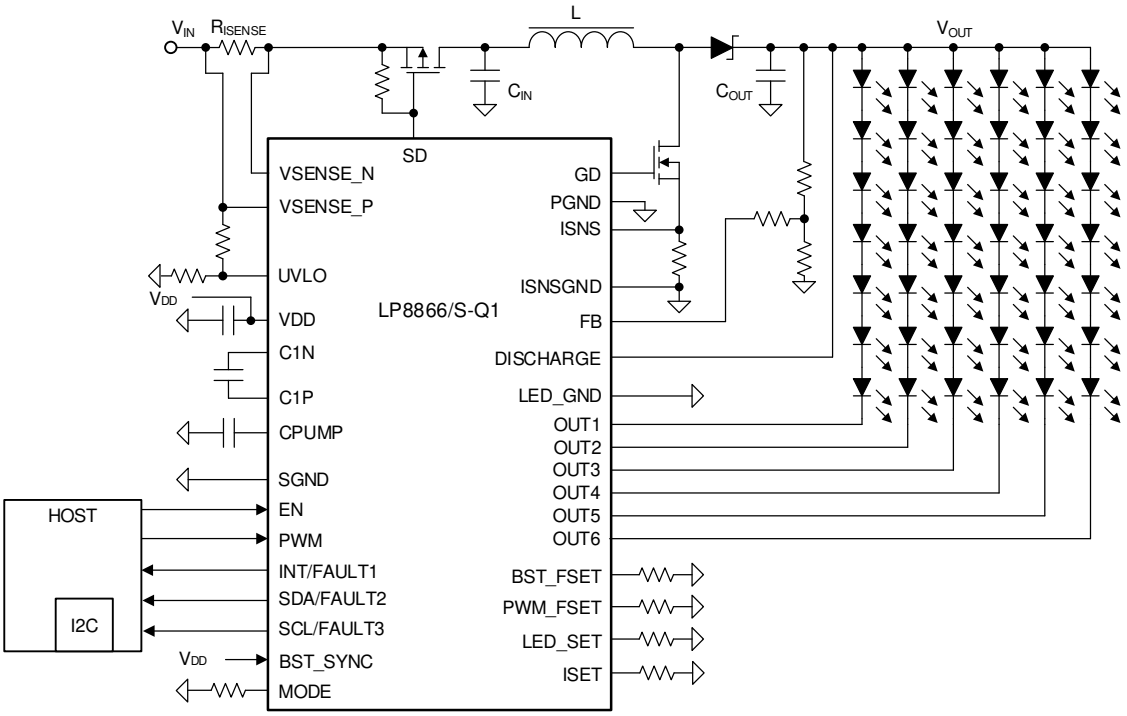

图 39. Full Feature Application for Display Backlight

8.2.1.1 Design Requirements

This typical LED-driver application is designed to meet the parameters listed in 表 29:

表 29. LP8866-Q1 Full-Feature Design Parameters

DESIGN PARAMETER	VALUE
VIN voltage range	3 V to 20V
VDD voltage	3.3 V
LED strings configuration	6 strings, 7 LEDs in series
Charge pump	Enabled
Brightness control	I2C
Output configuration	OUT1 to OUT6 are in phase shift mode (60°)
LED string current	100 mA
Boost frequency	400 kHz
Inductor	22 µH at 12-A saturation current
R_{ISENSE}	20 mΩ
Power-line FET	Enabled
R_{SENSE}	20 mΩ
Input/Output capacitors	C_{IN} and C_{OUT}: 2 × 33-µF electrolytic + 2 × 10-µF ceramic
Spread spectrum	Enabled
Discharge function	Enabled

ADVANCE INFORMATION

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

There are a few things to consider when choosing an inductor: inductance, current rating, and DC resistance (DCR). 表 30 shows recommended inductor values for each operating frequency. The LP8866-Q1 device automatically sets internal boost compensation controls depending on the selected switching frequency.

表 30. Inductance Values for Boost Switching Frequencies

SW FREQUENCY (kHz)	INDUCTANCE (µH)
300	22
400	22
600	15
800	15
1000	10
1250	10
1667	10
2200	10

The current rating of inductor must be at least 25% higher than maximum boost switching current $I_{SW(max)}$, which can be calculated with 公式 17. TI recommends a current rating of 12 A for most applications; use an inductor with low DCR to achieve good efficiency. Efficiency varies with load condition, switching frequency, and components, but 80% can be use as safe estimation. *Power Stage Designer™ Tool of Most Commonly Used Switch-mode Power Supplies* can be used for the boost calculation.

$$I_{SW(max)} = \frac{\Delta I_L}{2} + \frac{I_{OUT(max)}}{1 - D} \quad (17)$$

where

- $\Delta I_L = V_{IN(min)} \times D / f_{SW} \times L$
- $D = 1 - V_{IN(min)} \times \eta / V_{OUT}$
- $I_{SW(max)}$: Maximum switching current
- ΔI_L: Inductor ripple current
- $I_{OUT(max)}$: Maximum output current
- D: Boost duty cycle
- $V_{IN(min)}$: Minimum input voltage
- f_{SW}: Minimum switching frequency of the converter
- L: Inductance
- V_{OUT}: Output voltage
- η: Efficiency of boost converter

8.2.1.2.2 Output Capacitor Selection

Recommended voltage rating for output capacitors is 50% higher than maximum output voltage level — 100-V voltage rating is recommended. Capacitance value determines voltage ripple and boost stability. The DC-bias effect can reduce the effective capacitance significantly, by up to 80%, a consideration for capacitance value selection. Effective capacitance must be at least 50 µF for full load/maximum conversion ratio applications and must be used to achieve good phase and gain margin levels. TI recommends using two 33-µF Al-polymer electrolytic capacitors and two 10-µF ceramic capacitors in parallel to reduce ripple, increase stability, and reduce ESR effect.

8.2.1.2.3 Input Capacitor Selection

Recommended input capacitance is the same as output capacitance although input capacitors are not as critical to boost operation. Input capacitance can be reduced but must ensure enough filtering for input power.

ADVANCE INFORMATION

8.2.1.2.4 Charge Pump Output Capacitor

TI recommends a ceramic capacitor with at least 16-V voltage rating for the output capacitor of the charge pump. A 10-µF capacitor can be used for most applications.

8.2.1.2.5 Charge Pump Flying Capacitor

TI recommends a ceramic capacitor with at least 16-V voltage rating for the flying capacitor of the charge pump. One 2.2-µF capacitor connecting C1P and C1N pins can be used for most applications.

8.2.1.2.6 Output Diode

A Schottky diode must be used for the boost output diode. Current rating must be at least 25% higher than the maximum output current; TI recommends a 12-A current rating for most applications. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. At maximum current, the forward voltage must be as low as possible; less than 0.5 V is recommended. Reverse breakdown voltage of the Schottky diode must be significantly larger than the output voltage, 25% higher voltage rating is recommended. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times cause efficiency and load regulation to suffer.

8.2.1.2.7 Switching FET

Gate-drive voltage for the FET is V_{DD} with charge pump bypassed, or about double V_{DD}, if the charge pump is enabled. Switching FET is a critical component for determining power efficiency of the boost converter. Several aspects need to be considered when selecting switching FET such as voltage and current rating, R_{DSON}, power dissipation, thermal resistance and rise/fall times. An N type MOSFET with at least 25% higher voltage rating than maximum output voltage must be used. Current rating of switching FET should be same or higher than inductor rating. R_{DSON} must be as low as possible, less than 20 mΩ is recommended. Thermal resistance ($R_{\theta JA}$) must also be low to dissipate heat from power loss on switching FET. TI recommends typical rise/fall time values less than 10 ns.

8.2.1.2.8 Boost Sense Resistor

The R_{SENSE} resistor determines the boost overcurrent limit and is sensed every boost switching cycle. A high-power 20-mΩ resistor can be used for sensing the boost SW current and setting maximum current limit at 10 A (typical). R_{SENSE} can be increased to lower this limit and can be calculated with 公式 18, but this should be done carefully because it may also affect stability. In typical condition, boost overcurrent limit is recommended to be set above 4A, therefore R_{SENSE} doesn't exceed 50 mΩ. Power rating can be calculated from the inductor current and sense resistor resistance value.

$$R_{SENSE} = \frac{200\ mV}{I_{BOOST\_OCP}} \quad (18)$$

where

- R_{SENSE}: boost sense resistor (mΩ)
- I_{BOOST_OCP}: boost overcurrent limit

8.2.1.2.9 Power-Line FET

A power line FET can be used to disconnect input power from boost input to protect the LP8866-Q1 device and boost components in case an overcurrent event occurs. A P type MOSFET is used for the power-line FET. Voltage rating must be at least 25% higher than maximum input voltage level. Low R_{DSON} is important to reduce power loss on the FET — less than 20 mΩ is recommended. Current rating for the FET must be at least 25% higher than input peak current. Gate-to-source voltage (V_{GS}) for open transistor must be less than minimum input voltage; use a 20-kΩ resistor between the pFET gate and source.

8.2.1.2.10 Input Current Sense Resistor

A high-power resistor can be used for sensing the boost input current. Overcurrent condition is detected when the voltage across R_{ISENSE} reaches 220 mV. Typical 20 mΩ sense resistor is used to set 11-A input current limit. Sense resistor value can be increased to lower overcurrent limit for application as needed. Power rating can be calculated from the input current and resistance value.

ADVANCE INFORMATION

8.2.1.2.11 Feedback Resistor Divider

Feedback resistors R_{FB1} and R_{FB2} determine the maximum boost output level. Output voltage can be calculated as in 公式 19:

$$V_{OUT\_MAX} = \left(\frac{V_{BG}}{R_{FB2}} + I_{SEL\_MAX} \right) \times R_{FB1} + V_{BG}$$

where

- V_{BG} = 1.21 V
- I_{SEL_MAX} = 38.7 µA
- R_{FB2} = 100 kΩ (recommended for boost mode) (19)

9 Power Supply Recommendations

The LP8866-Q1 is designed to operate from a car battery. The V_{IN} input must be protected from reverse voltage and voltage dump condition over 48 V. The impedance of the input supply rail must be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected with long wires, additional bulk capacitance may be required in addition to normal input capacitor.

The voltage range for V_{DD} is 3 V to 5.5 V. A ceramic capacitor must be placed as close as possible to the VDD pin. The boost gate driver is powered from the CPUMP pins. A ceramic capacitor must be placed as close to the CPUMP pins as possible.

10 Layout

10.1 Layout Guidelines

图 40 shows a layout recommendation for the LP8866-Q1 used to illustrate the principles of good layout. This layout can be adapted to the actual application layout if and where possible. It is important that all boost components are close to each other and to the chip; the high-current traces must be wide enough. VDD must be as noise-free as possible. Place a V_{DD} bypass capacitor near the VDD and GND pins and ground it to a low-noise ground. A charge-pump capacitor, boost input capacitors, and boost output capacitors must be connected to PGND. Place the charge-pump capacitors close to the device. The main points to guide the PCB layout design:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to each other. Input and output capacitor grounds need to be close to each other to minimize current loop size.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High frequency return currents follow the route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the *positive* current route in the ground plane, if the ground plane is intact under the route.
  - For high frequency the copper area capacitance must be taken into account. For example, the copper area for the drain of boost N-MOSFET is a tradeoff between capacitance and the cooling capacity of the components.
- GND plane must be intact under the high-current-boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting must be in the same direction in optimal case.
- Use separate power and noise-free grounds. PGND is used for boost converter return current. Use a low-noise ground for more sensitive signals, like VDD bypass capacitor grounding as well as grounding the GND pins of the LP8866-Q1 device itself.
- Route boost output voltage (V_{OUT}) to LEDs from output capacitors not straight from the diode cathode.
- A small bypass capacitor (TI recommends a 39-pF capacitor) must be placed close to the FB pin and GND to suppress high frequency noise
- VDD line must be separated from the high current supply path to the boost converter to prevent high frequency ripple affecting the chip behavior. A separate 1-µF bypass capacitor is used for the VDD pin, and it is grounded to noise-free ground.
- Capacitor connected to charge pump output CPUMP must have 10-µF capacitance, grounded by the shortest way to boost a switch-current-sensing resistor. This capacitor must be as close as possible to CPUMP pin. This capacitor provides a greater peak current for gate driver and must be used even if the charge pump is disabled. If the charge pump is disabled, the VDD and CPUMP pins must be tied together.
- Input and output capacitors need low-impedance grounding (wide traces with many vias to PGND plane).
- If two or more output capacitors are used, symmetrical layout must be used to get all capacitors working ideally.
- Input/output ceramic capacitors have DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable under certain load conditions. DC bias characteristics should be obtained from the component manufacturer; DC bias is not taken into account on component tolerance. TI recommends X5R/X7R capacitors.

10.2 Layout Example

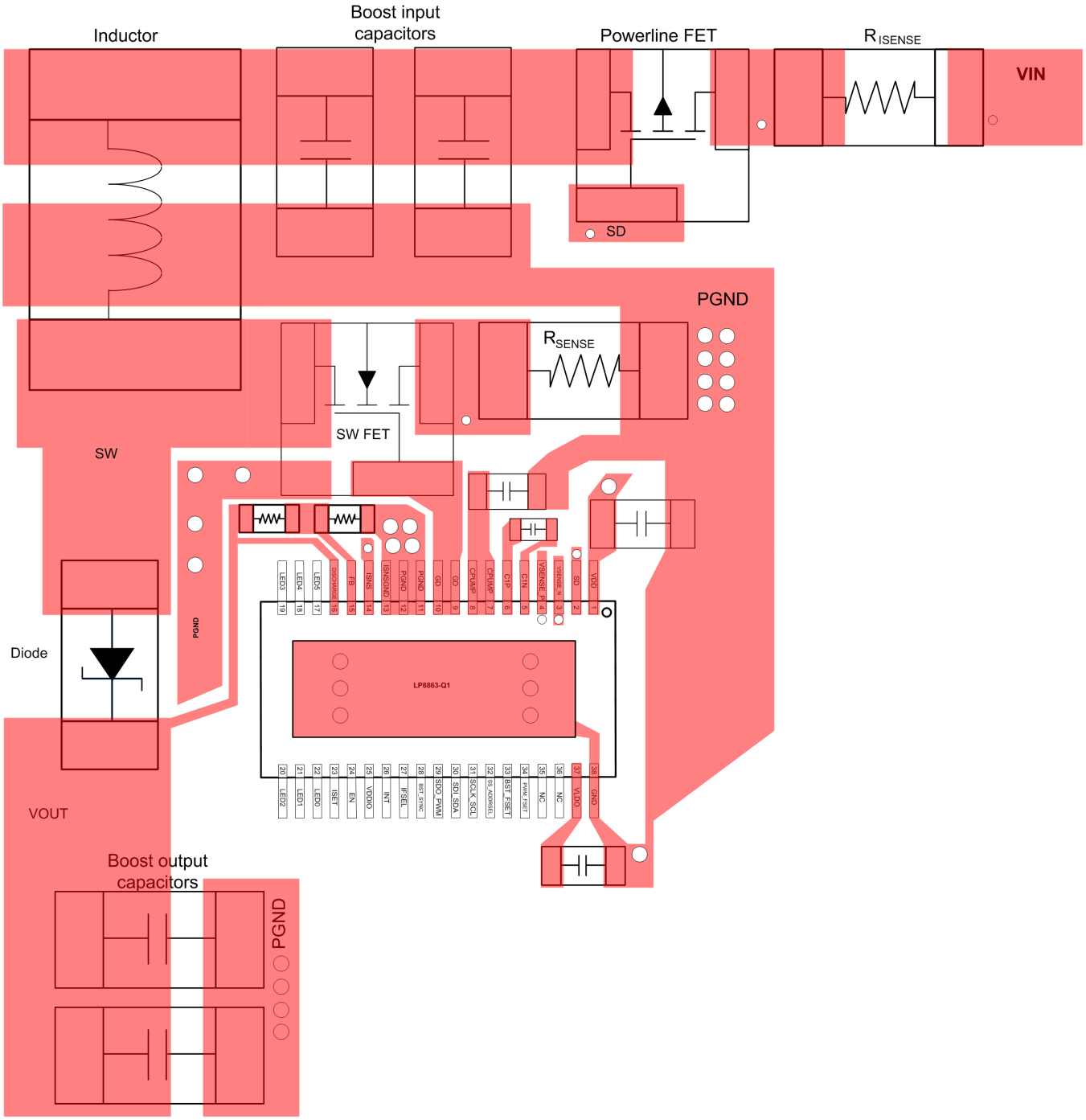

图 40. LP8866-Q1 Layout Guidelines

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
LP8866QDCPRQ1	PREVIEW	HTSSOP	DCP	38	2000	TBD	Call TI	Call TI	–40 to 125	
PLP8866QDCPRQ1	ACTIVE	HTSSOP	DCP	38	2000	TBD	Call TI	Call TI	–40 to 125	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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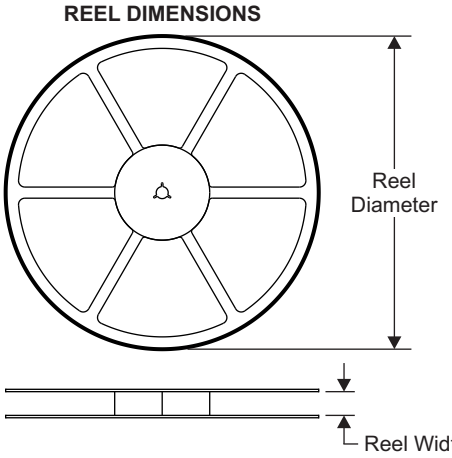
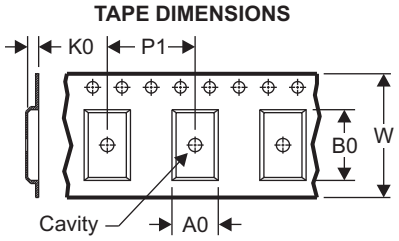
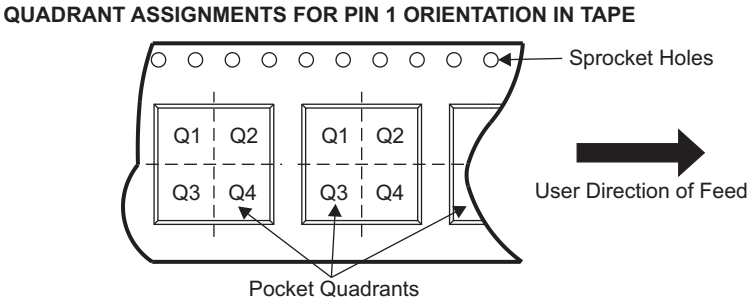
ADVANCE INFORMATION

12.1.2 Tape and Reel Information





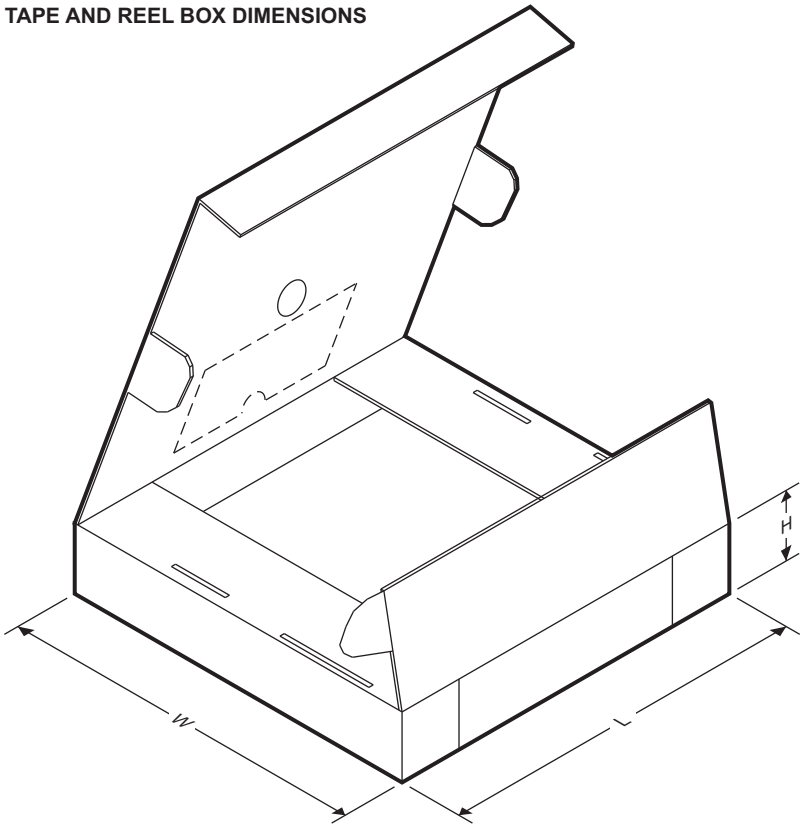
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8866QDCPRQ1	HTSSOP	DCP	38	2000	330	16.4	6.9	10.2	1,8	12.0	16.0	Q1
PLP8866QDCPRQ1	HTSSOP	DCP	38	2000	330	16.4	6.9	10.2	1,8	12.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8866QDCPRQ1	HTSSOP	DCP	38	2000	367.0	367.0	38.0
PLP8866QDCPRQ1	HTSSOP	DCP	38	2000	367.0	367.0	38.0

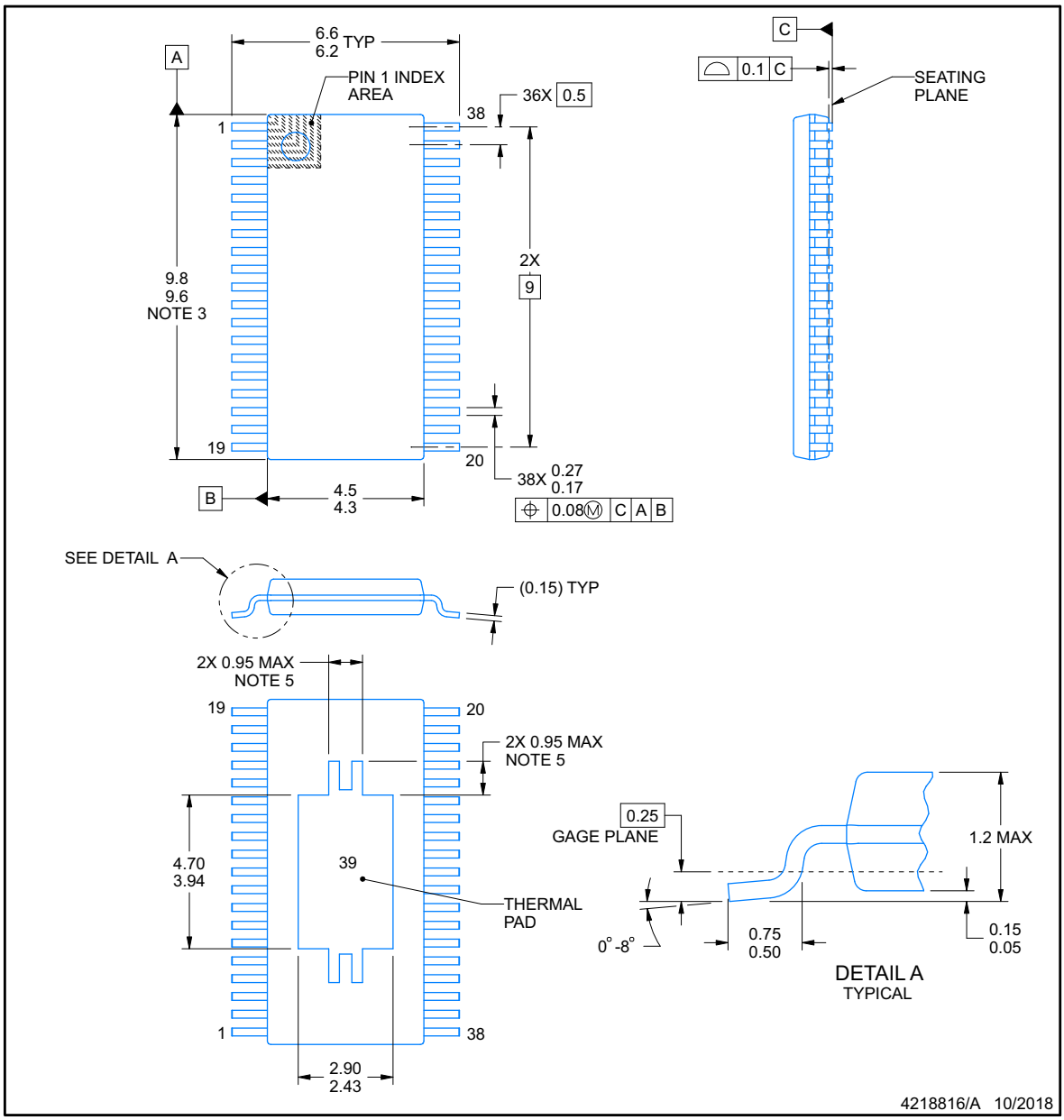
ADVANCE INFORMATION

PACKAGE OUTLINE

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

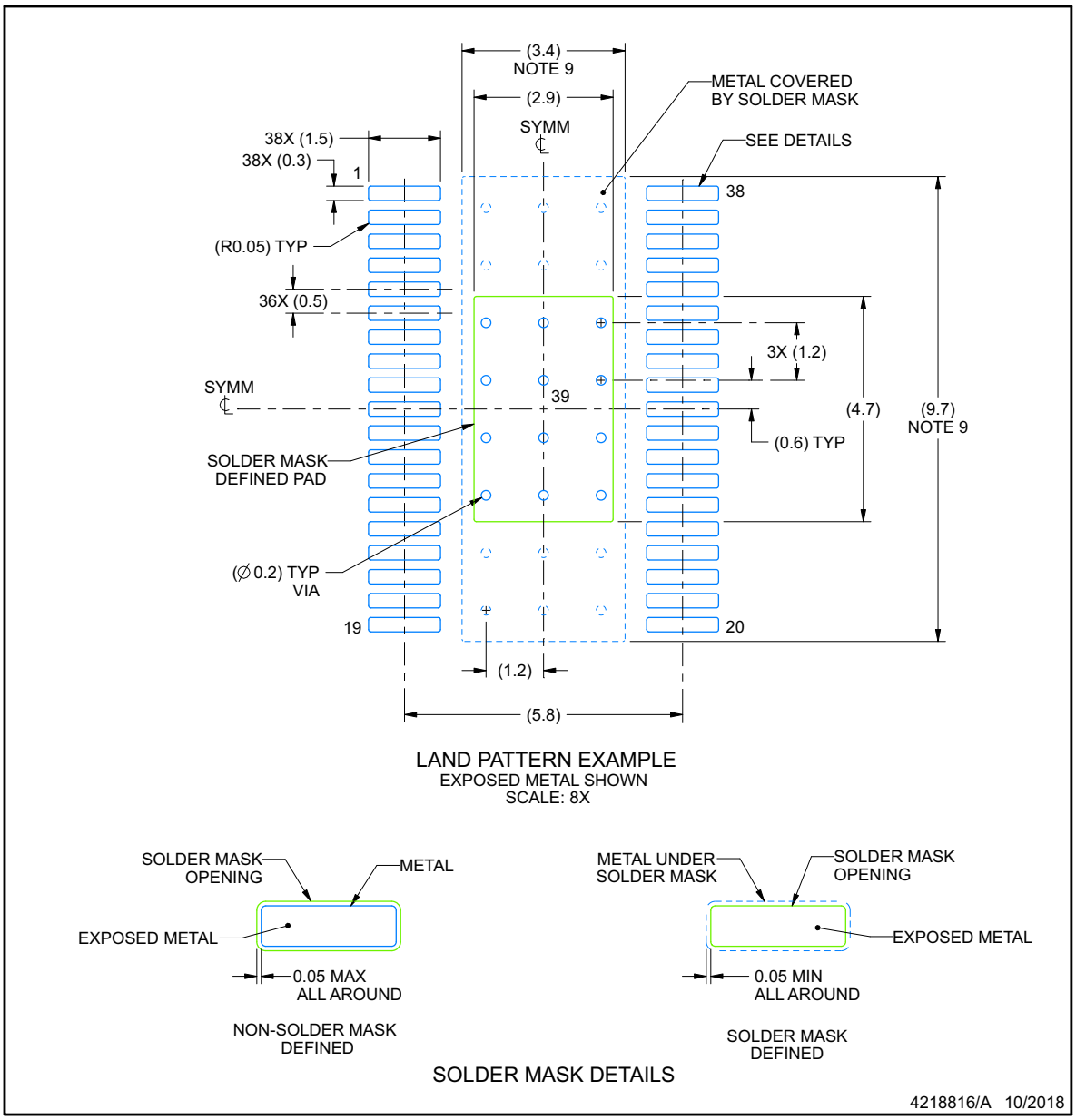
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



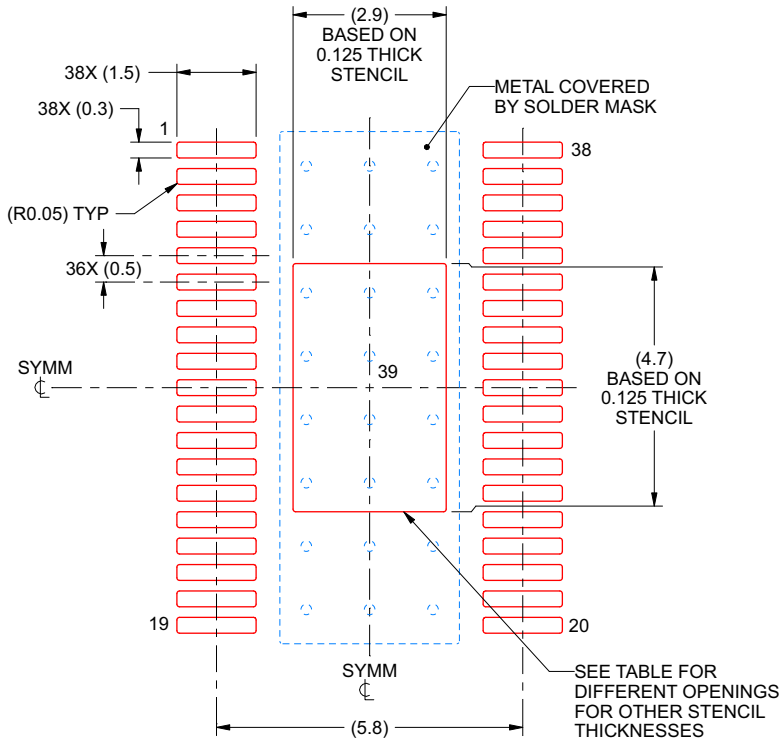
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DCP0038A — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

4218816/A 10/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8866QDCPRQ1	ACTIVE	HTSSOP	DCP	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LP8866Q1	Samples
LP8866QRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8866	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

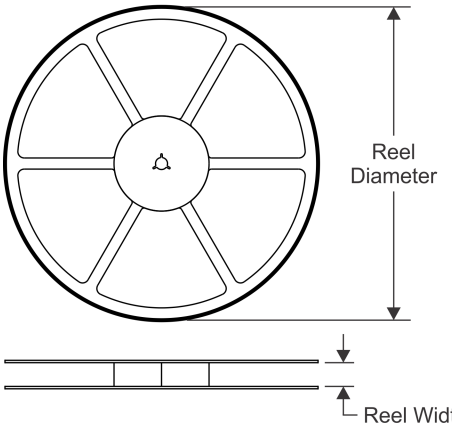
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

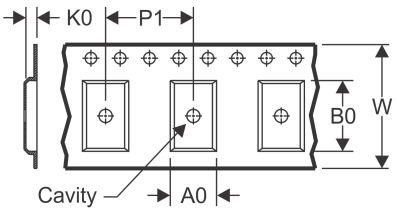
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

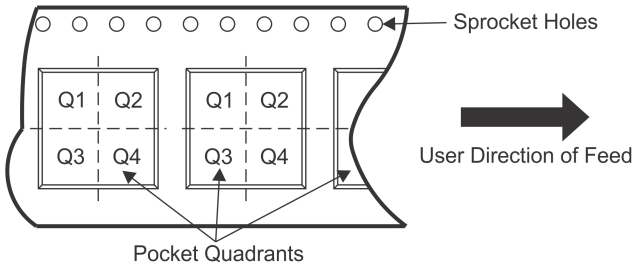


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

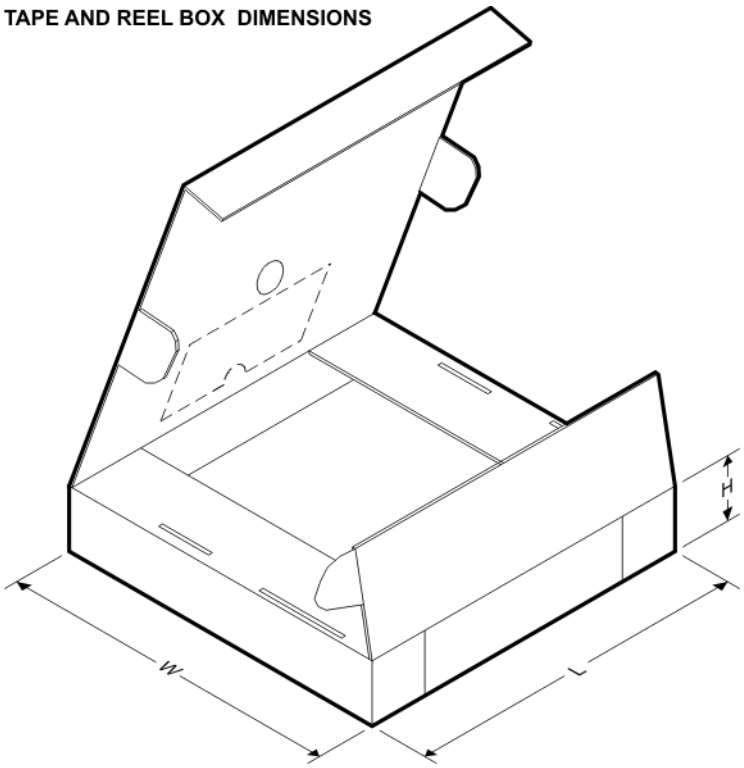
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8866QDCPRQ1	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
LP8866QRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8866QDCPRQ1	HTSSOP	DCP	38	2000	350.0	350.0	43.0
LP8866QRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

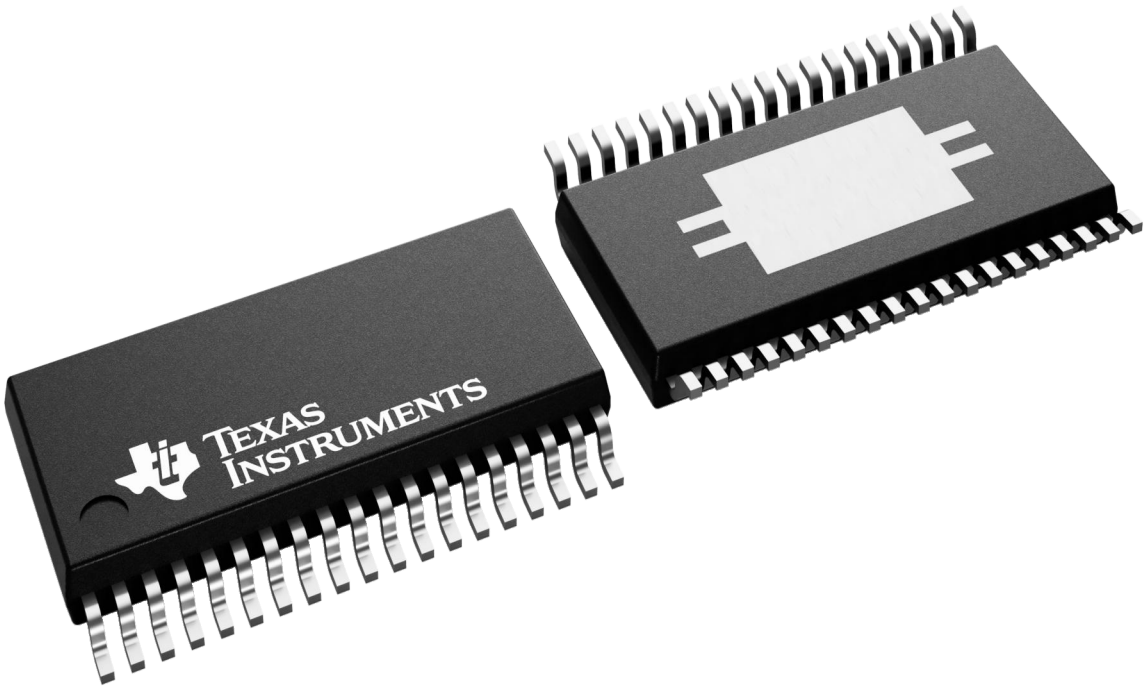
DCP 38

PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

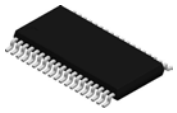
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224560/B

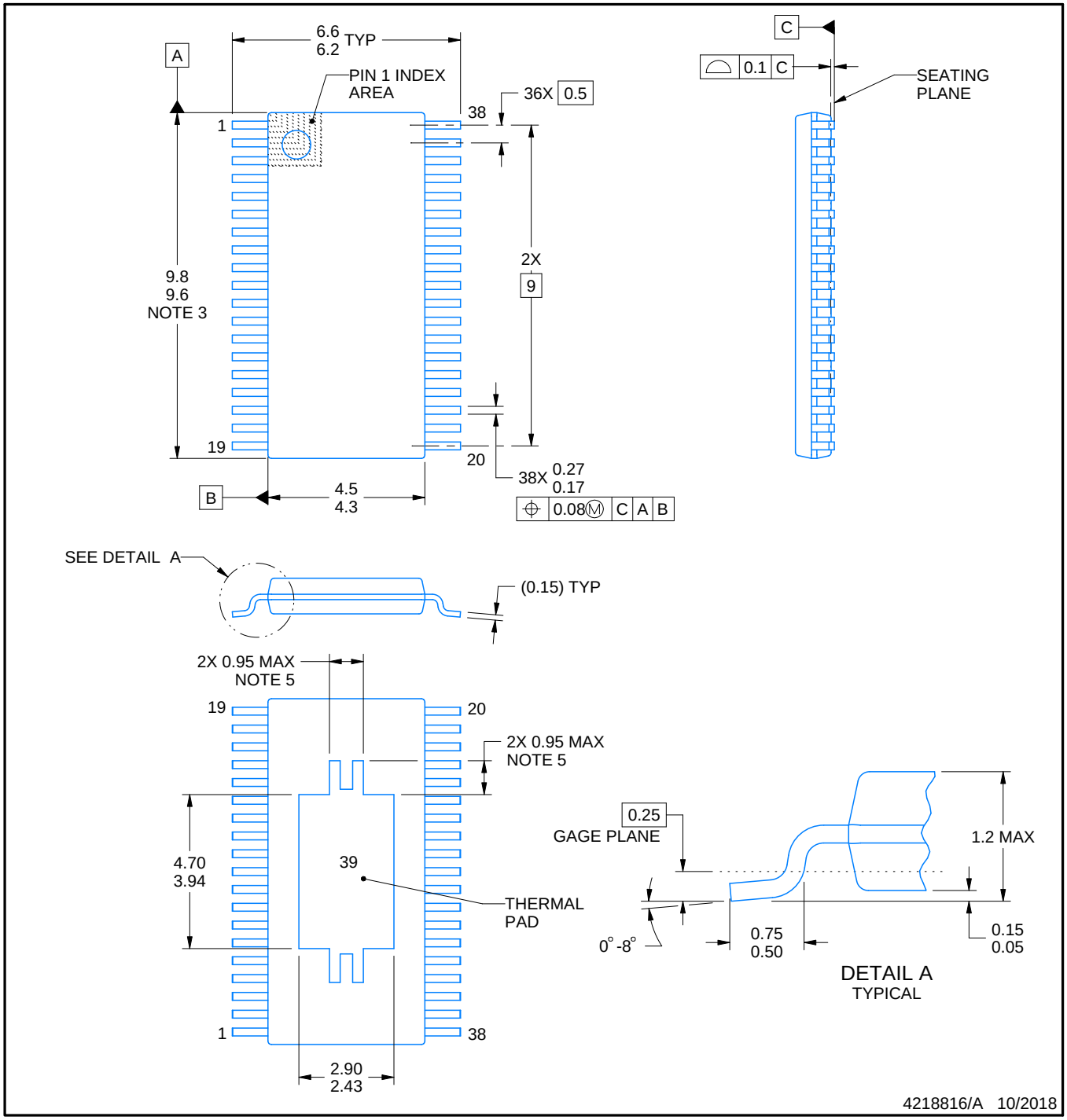
PACKAGE OUTLINE

DCP0038A



PowerPAD™ TSSOP - 1.2 mm max height

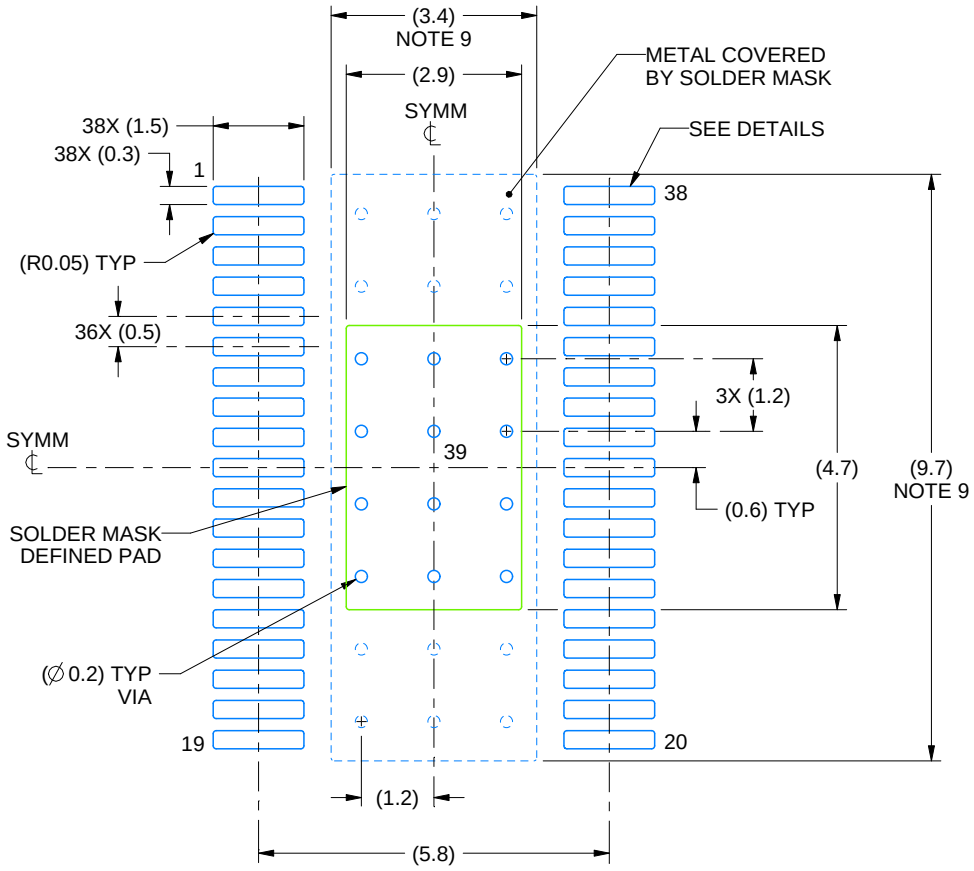
SMALL OUTLINE PACKAGE



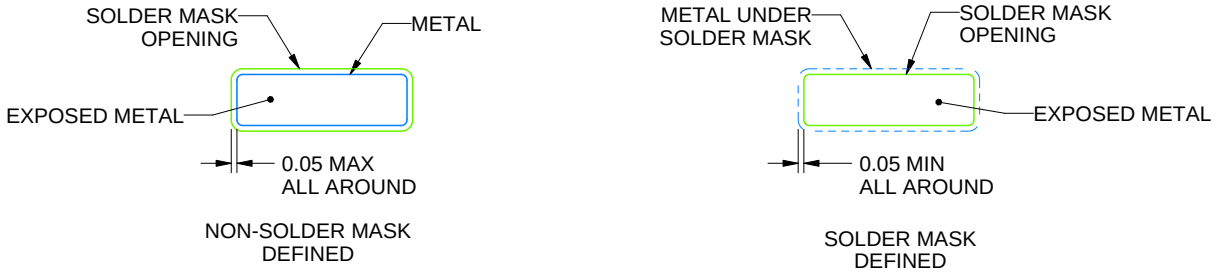
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

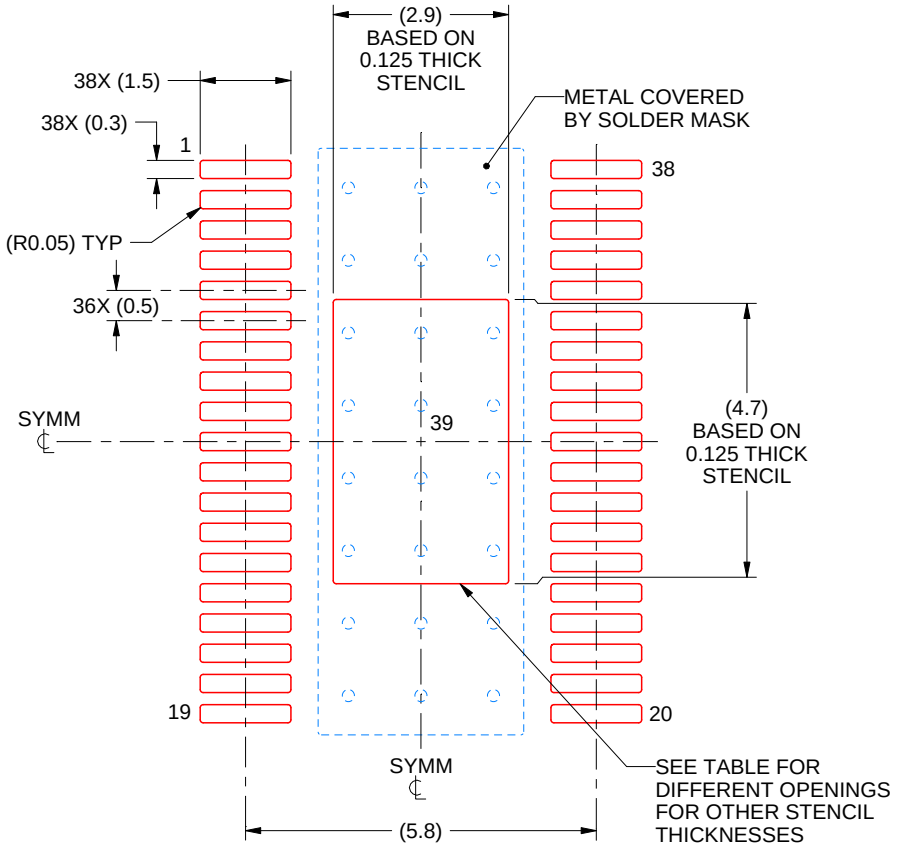


SOLDER MASK DETAILS

4218816/A 10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

4218816/A 10/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

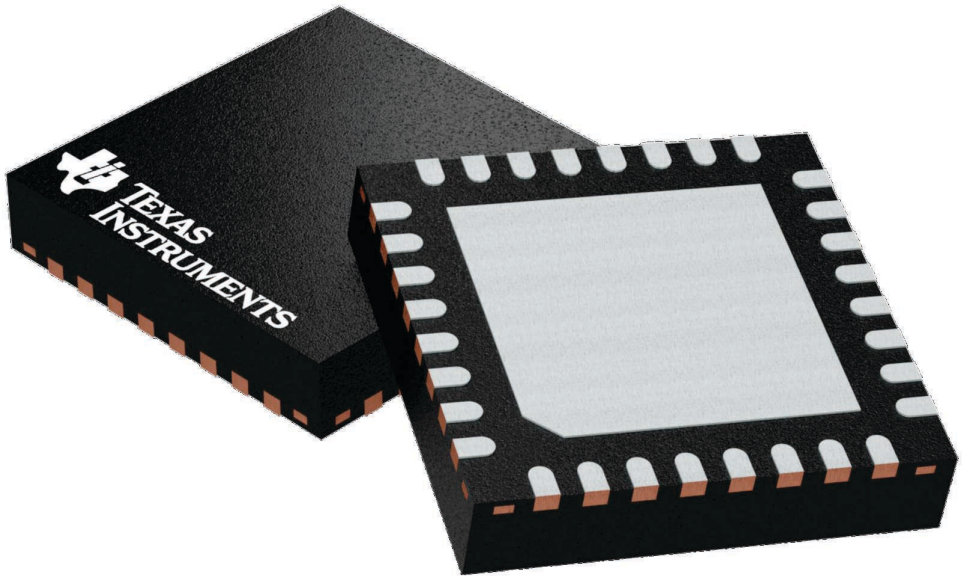
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

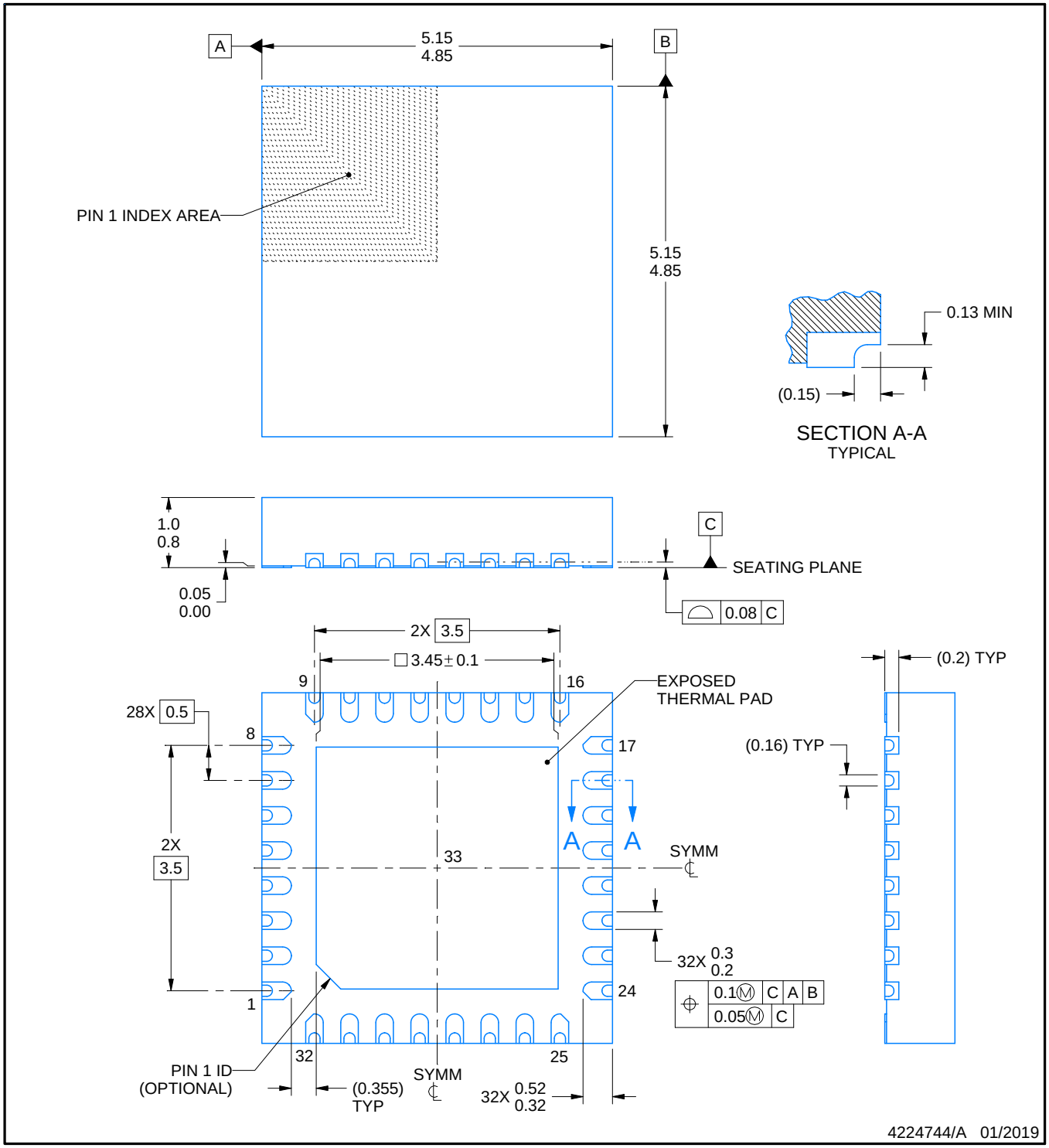
4224745/A

RHB0032T

PACKAGE OUTLINE

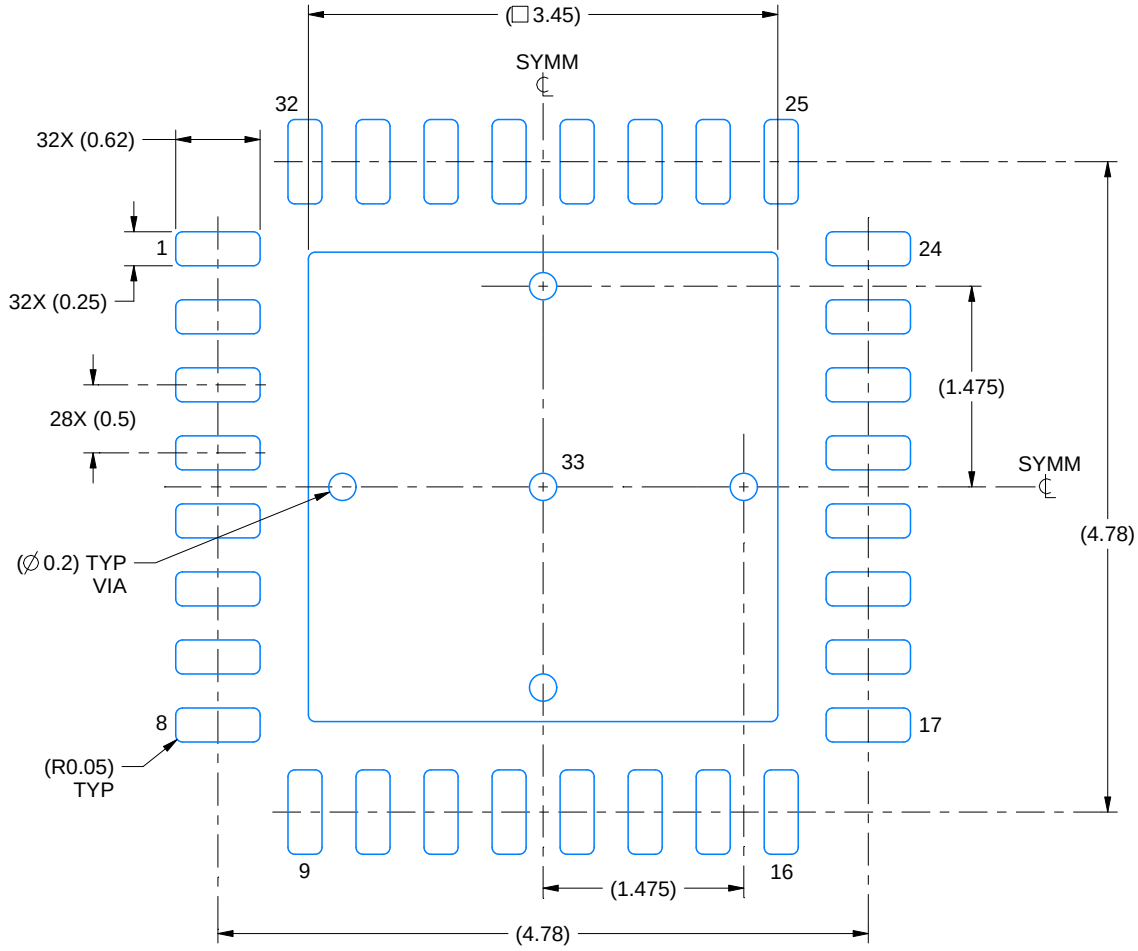
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

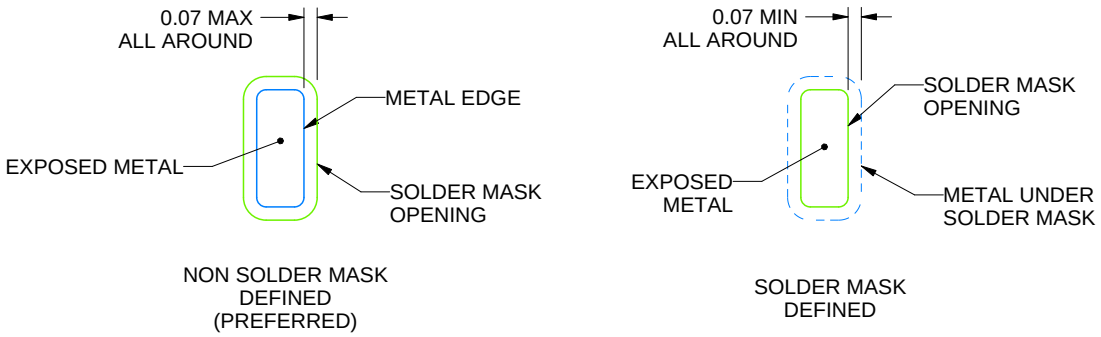
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE:18X

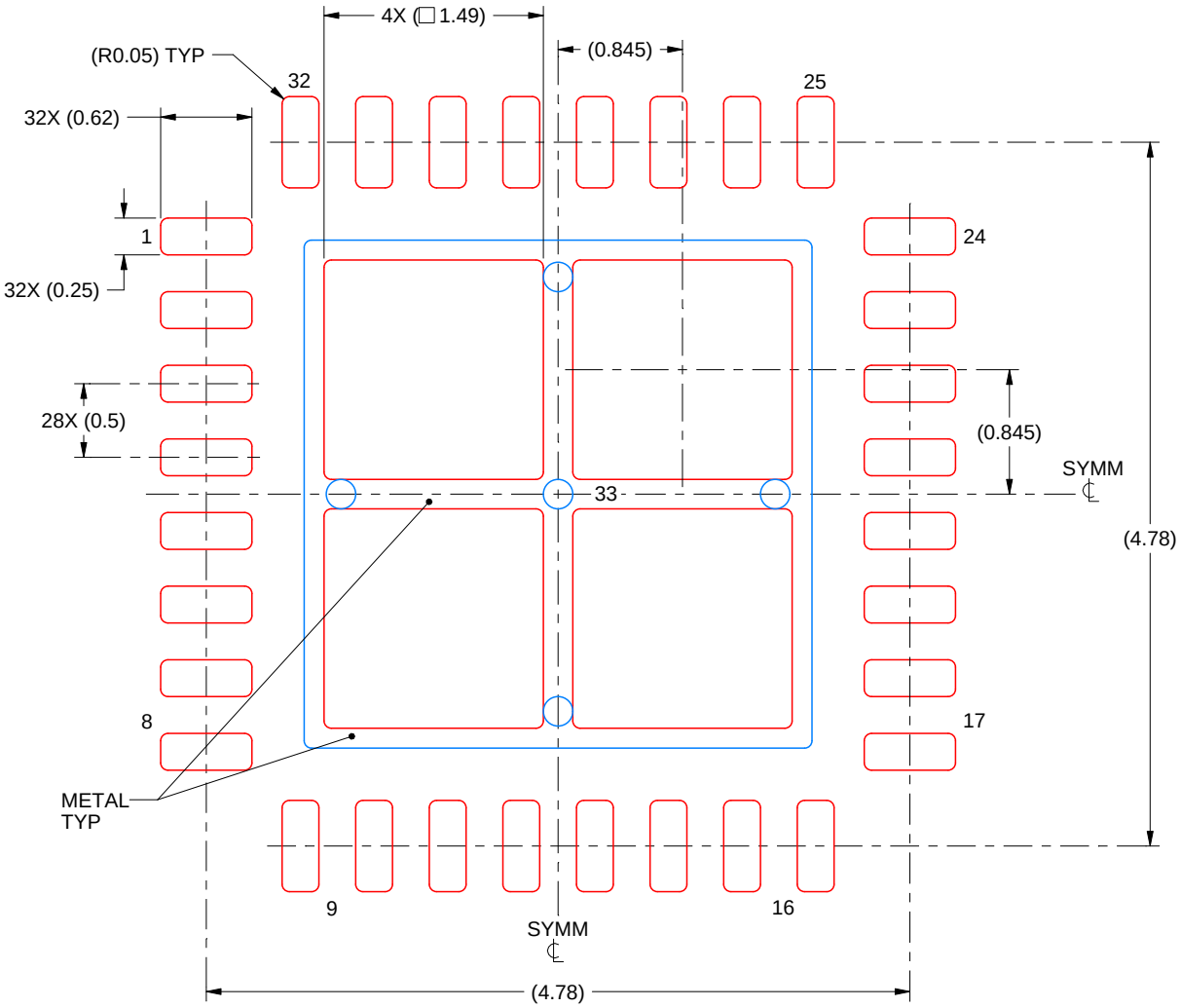


SOLDER MASK DETAILS

4224744/A 01/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4224744/A 01/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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