TLC6C5912 12 通道移位寄存器 LED 驱动器

1 特性

- 3V 至 5.5V 宽 V_{CC} 范围
- 40V 最大额定输出
- 12 路功率双扩散金属氧化物半导体 (DMOS) 晶体管输出：
  50mA 持续电流 (V_{CC} = 5V) 或者
  200mA 脉宽调制 (PWM) 电流（单脉冲持续时间短于 1ms 且平均电流低于 50mA$_r$）
- 热关断保护
- 针对多级的增强型级联
- 所有寄存器由单一输入清零
- 低功耗
- 缓慢开关时间（t 和 t_f），非常有助于减少电磁干扰 (EMI)
- 20 引脚薄型小外形尺寸 (TSSOP)-PW 封装

2 应用

- 电器显示面板
- 电梯显示面板
- PLC 功能指示器
- 七段显示器

3 说明

TLC6C5912 是一款单片、中等电压、低电流功率 12 位移位寄存器，专为负载功率要求相对适中的系统（例如 LED）而设计。

此器件包含一个 12 位串入、并出移位寄存器，此寄存器为一个 12 位 D 类存储寄存器提供数据。移位和存储寄存器之间的数据传输分别在移位寄存器时钟 (SRCK) 和寄存器时钟 (RCK) 的上升边沿上发生。当移位寄存器清零($\overline{CLR}$) 为高电平时，存储寄存器将数据传输到输出缓冲器 。一个$\overline{CLR}$上的低电平将器件中的所有寄存器清零。将输出使能 ($\overline{G}$) 保持为高电平将把输出缓冲器中的所有数据保存为低电平，并且所有漏极输出关闭。保持$\overline{G}$为低电平将使得来自存储寄存器中的数据对于输出缓冲器不可见。

该器件包含一个 12 位串入并出移位寄存器。该寄存器为一个 12 位 D 类存储寄存器提供数据。移位寄存器和存储寄存器各自具备独立时钟。

输出为低侧、漏极开路 DMOS 晶体管输出：额定输出为 40V 及 50mA 持续灌电流或者 200mA PWM 电流（V_{CC} = 5V 时，单脉冲持续时间短于 1ms 且平均电流低于 50mA）。该器件内置热关断保护，在人体模型和 200V 机器模型测试中可提供高达 2000V 的静电放电 (ESD) 保护。

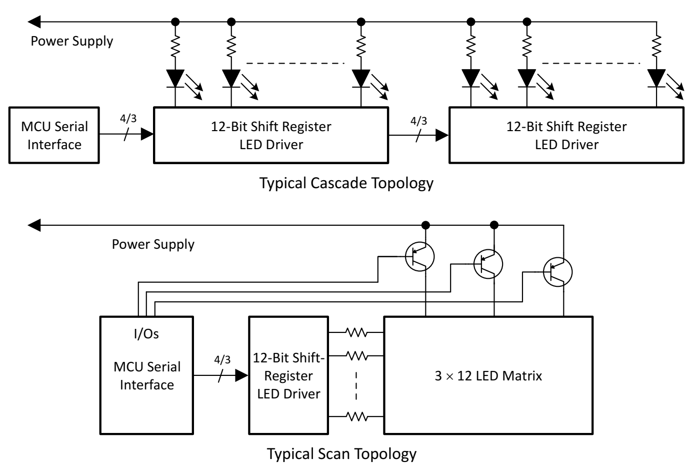
TLC6C5912 的额定工作环境温度范围为 -40°C 至 105°C。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TLC6C5912	薄型小外形尺寸封装 (TSSOP) (20)	6.50mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



目录

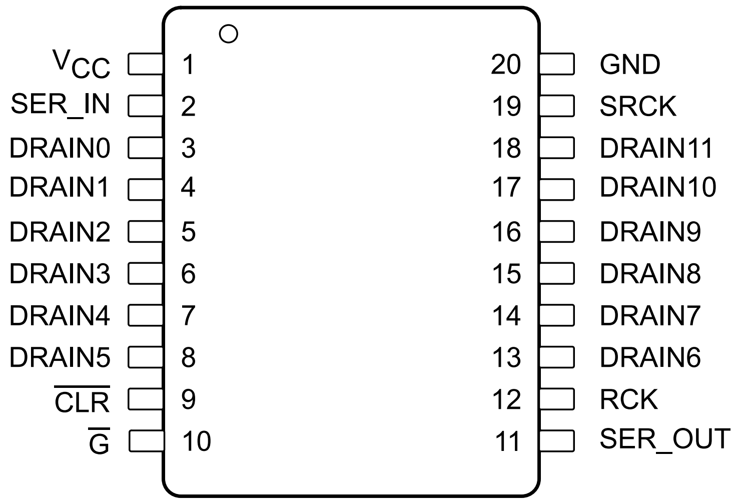
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	注
2016 年 5 月	*	最初发布版本

5 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CLR}$	9	I	**Shift register clear, active-low:** $\overline{CLR}$ is the signal used to clear all the registers. The storage register transfers data to the output buffer when shift register clear $\overline{CLR}$ is high. Driving $\overline{CLR}$ is low clears all the registers in the device.
DRAIN0	3	O	**Open-drain output:** DRAIN0 to DRAIN11 are the LED current-sink channels. These pins connect to the LED cathodes, and they can survive up to 40-V LED supply voltage.
DRAIN1	4	O	
DRAIN2	5	O	
DRAIN3	6	O	
DRAIN4	7	O	
DRAIN5	8	O	
DRAIN6	13	O	
DRAIN7	14	O	
DRAIN8	15	O	
DRAIN9	16	O	
DRAIN10	17	O	
DRAIN11	18	O	
$\overline{G}$	10	I	**Output enable, active-low:** $\overline{G}$ is the LED channel enable and disable input pin. Having $\overline{G}$ low enables all drain channels according to the output-latch register content. When high, all channels are off.
GND	20	—	**Power ground:** GND is the ground reference pin for the device. This pin must connect to the ground plane on the PCB.
RCK	12	I	**Register clock:** RCK is the storage register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK. Data in the storage register appears at the output whenever the output enable $\overline{G}$ input signal is high.
SER IN	2	I	**Serial-data input:** SER IN is the serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SER OUT	11	O	**Serial-data output:** SER OUT is the serial data output of the 12−bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus. By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input at the same rising edge of SRCK.
SRCK	19	I	**Shift-register clock:** SRCK is the serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.
V_{CC}	1	I	**Power supply:** V_{CC} is the power supply pin voltage for the device. TI recommends adding a 0.1 µF ceramic capacitor close to the pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage		8	V
V_I	Logic input-voltage	–0.3	8	V
V_{DS}	Power DMOS drain-to-source voltage		42	V
	Continuous total dissipation	See *Thermal Information*		
	Operating ambient temperature (Top)		105	°C
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage	2.4		V
V_{IL}	Low-level input voltage		0.7	V
t_{su}	Setup time, SER IN high before SRCK↑	15		ns
t_h	Hold time, SER IN high after SRCK↑	15		ns
t_w	Pulse duration	40		ns
T_A	Operating ambient temperature	–40	105	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLC6C5912 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	DRAIN0 to DRAIN11, drain-to-source voltage					40	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 µA	V_{CC} = 5 V	4.9	4.99		V
		I_{OH} = –4 mA		4.5	4.69		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 µA	V_{CC} = 5 V		0.001	0.01	V
		I_{OH} = 4 mA			0.25	0.4	
I_{IH}	High-level input current	V_{CC} = 5 V, V_I = V_{CC}			0.2		µA
I_{IL}	Low-level input current	V_{CC} = 5 V, V_I = 0			–0.2		µA
I_{CC}	Logic supply current	V_{CC} = 5 V, No clock signal	All outputs off		0.1	1	µA
			All outputs on		130	170	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, all outputs on			300		µA
I_{DSX}	Off-state drain current	V_{DS} = 30 V, V_{CC} = 5 V				0.1	µA
		V_{DS} = 30 V, T_C = 125°C, V_{CC} = 5 V			0.15	0.3	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, single channel ON		6	7.4	8.6	Ω
		I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, all channels ON		6.7	8.9	9.6	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, single channel ON		7.9	9.3	11.2	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, all channels ON		8.7	10.6	12.3	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 105°C, single channel ON		9.1	11.2	12.9	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 105°C, all channels ON		10.3	13	14.5	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 105°C, single channel ON		11.6	13.7	16.4	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 105°C, all channels ON		12.8	15.6	18.2	
$T_{SHUTDOWN}$	Thermal shutdown trip point			150	175	200	°C
t_{HYS}	Hysteresis				15		°C

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 48 mA		210		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			75		ns
t_r	Rise time, drain output			250		ns
t_f	Fall time, drain output			200		ns
t_{pd}	Propagation delay time, SRCK↓ to SEROUT	C_L = 30 pF, I_D = 48 mA		35		ns
t_{or}	SEROUT rise time (10% to 90%)	C_L = 30 pF		20		ns
t_{of}	SEROUT fall time (90% to 10%)	C_L = 30 pF		20		ns

Switching Characteristics (continued)

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 20 mA			10	MHz
t_{SRCK_WH}	SRCK pulse duration, high		30			ns
t_{SRCK_WL}	SRCK pulse duration, low		30			ns

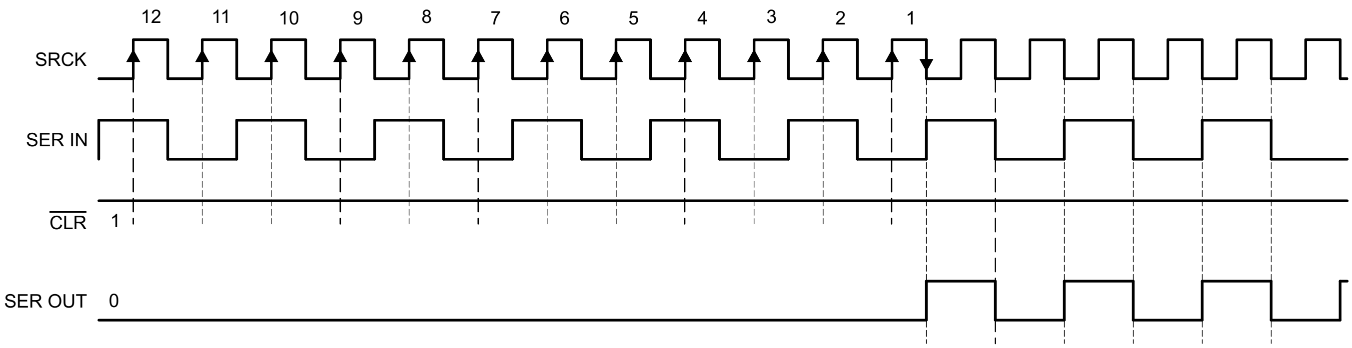


Figure 1. SER IN to SER OUT Waveform

Figure 1 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 2). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

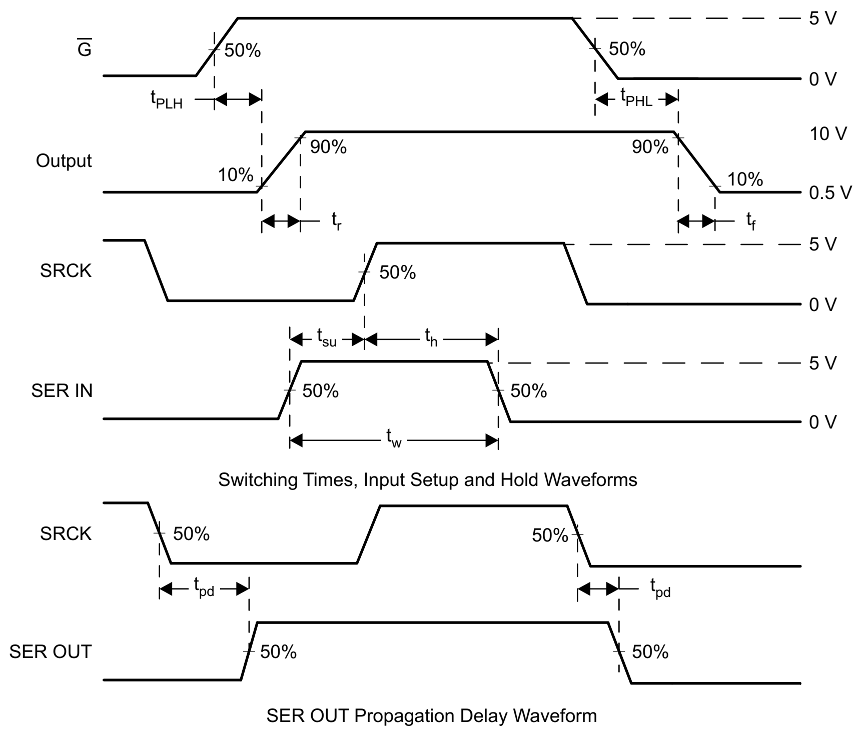


Figure 2. Switching Times and Voltage Waveforms

Figure 2 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 12.

6.7 Typical Characteristics

Conditions for Figure 5 and Figure 6: Single channel on; conditions for Figure 7, Figure 8, and Figure 9: All channels on.

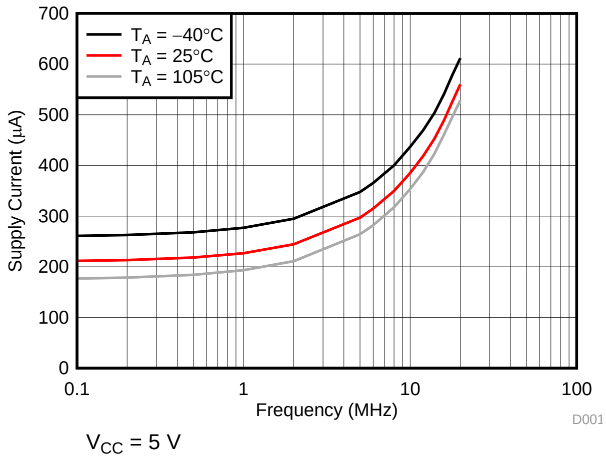


Figure 3. Supply Current vs Frequency

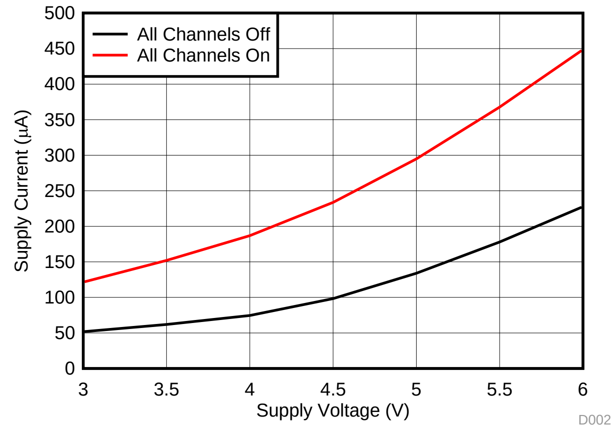


Figure 4. Supply Current vs Supply Voltage

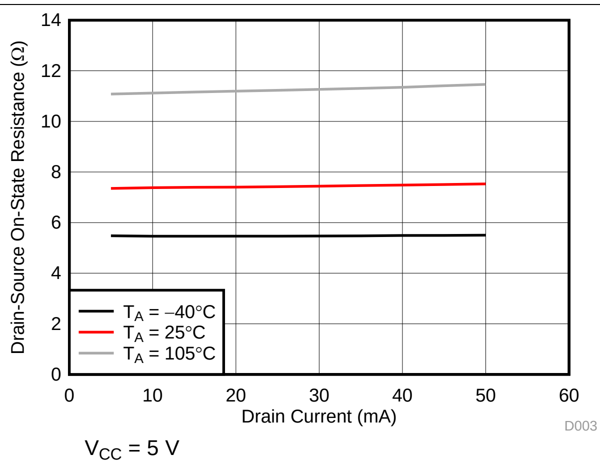


Figure 5. Drain-to-Source On-State Resistance vs Drain Current (Single Channel On)

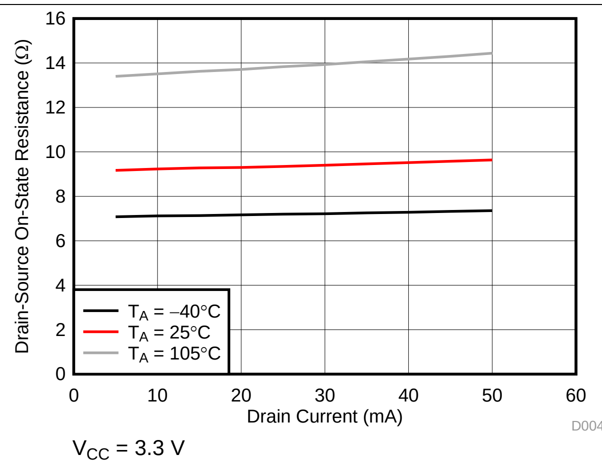


Figure 6. Drain-to-Source On-State Resistance vs Drain Current (Single Channel On)

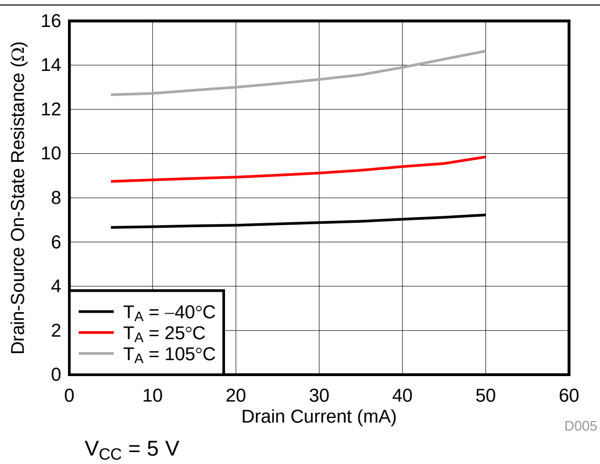


Figure 7. Drain-to-Source On-State Resistance vs Drain Current (All Channels On)

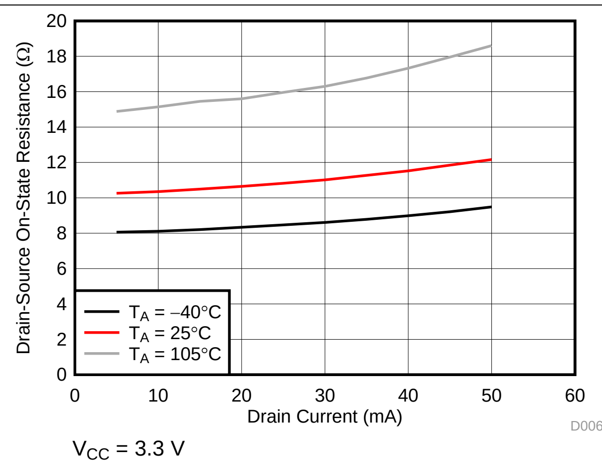
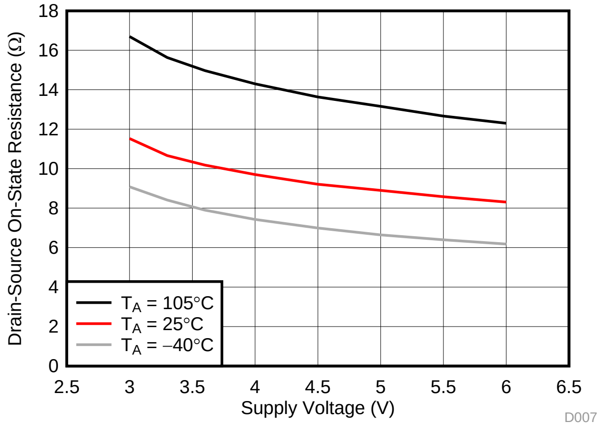


Figure 8. Drain-to-Source On-State Resistance vs Drain Current (All Channels On)

Typical Characteristics (continued)

Conditions for Figure 5 and Figure 6: Single channel on; conditions for Figure 7, Figure 8, and Figure 9: All channels on.



$I_{(ds)}$ = 20 mA

Figure 9. Drain-to-Source On-State Resistance vs Supply Voltage

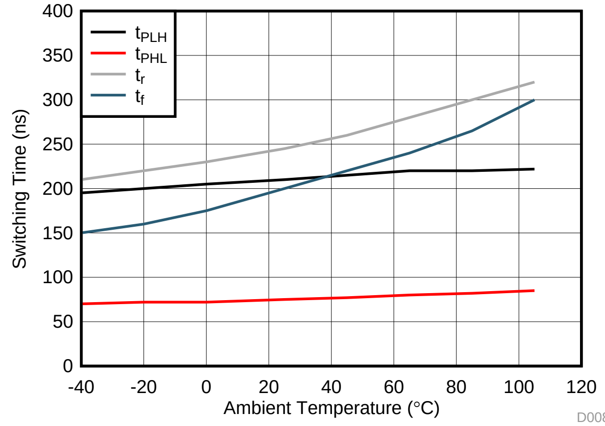
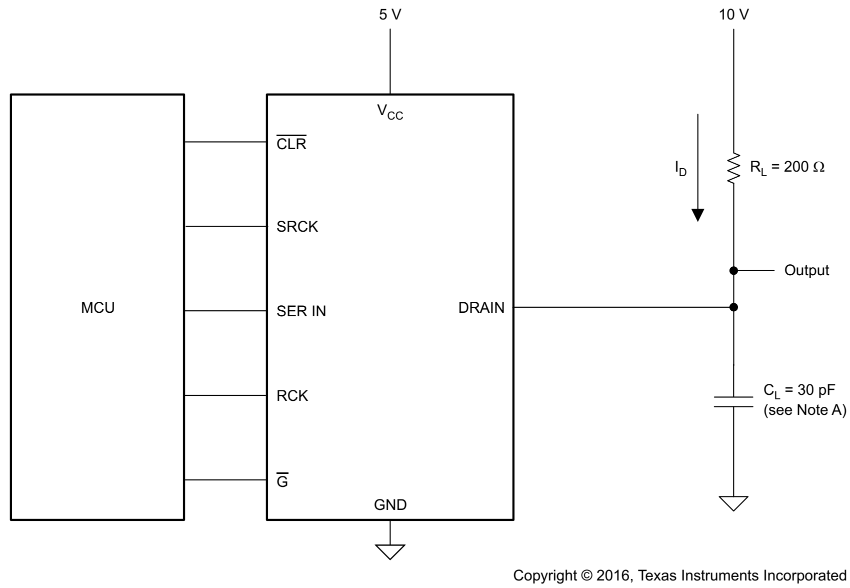


Figure 10. Switching Time vs Ambient Temperature

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

Figure 11. Resistive-Load Test Circuit

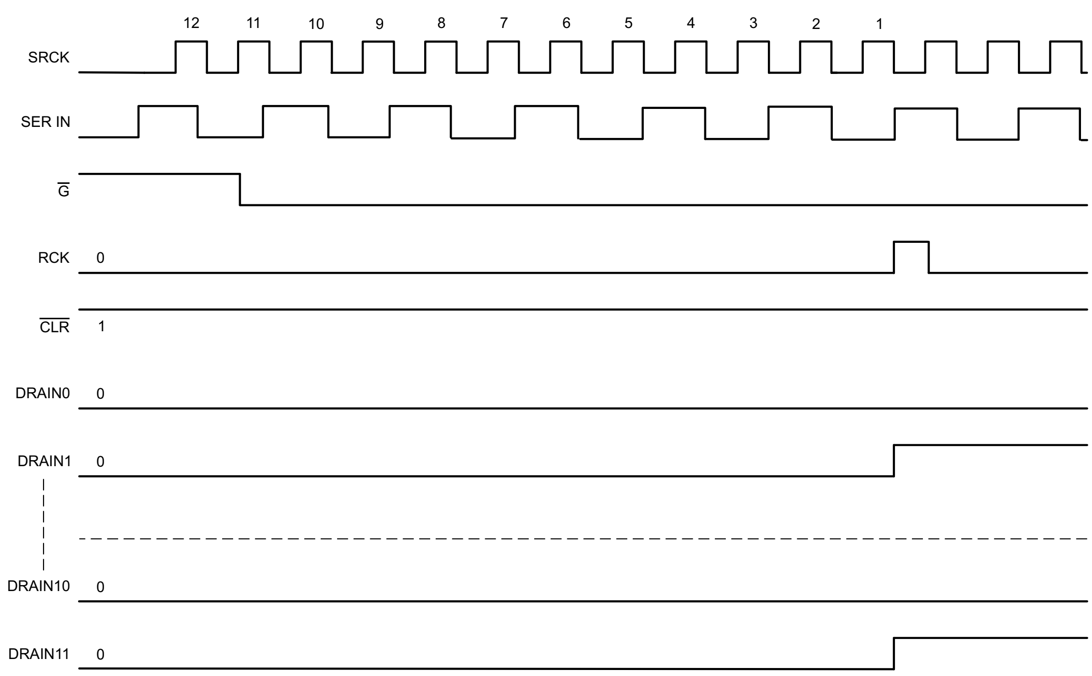


Figure 12. Voltage Waveforms

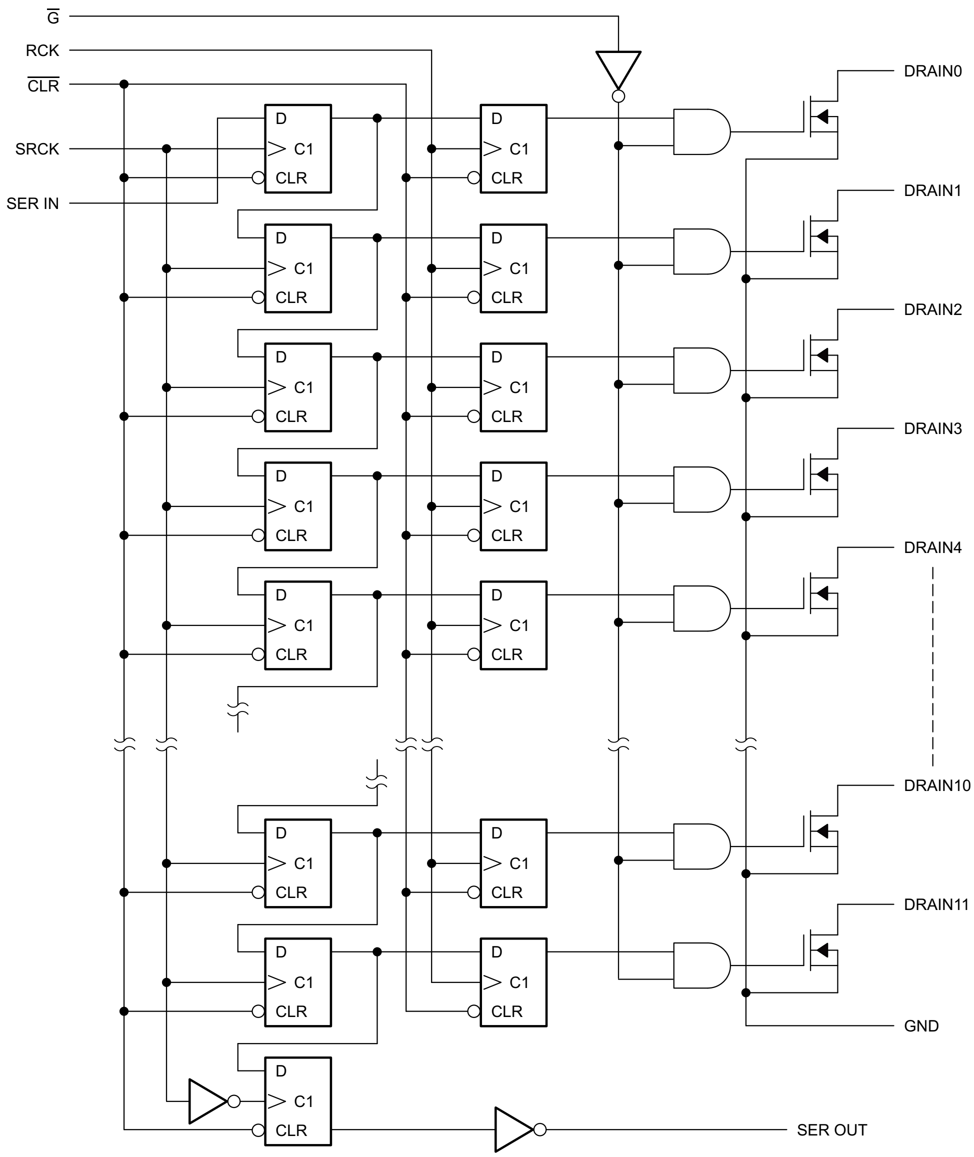
Figure 11 and Figure 12 show the resistive-load test circuit and voltage waveforms. One can see from Figure 12 that with G held low and CLR held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.

8 Detailed Description

8.1 Overview

The TLC6C5912 device is a monolithic, medium-voltage, low current 12-bit shift register designed to drive relatively moderate load power such LEDs. The device contains a 12-bit serial-in, parallel-out shift register that feeds a 12-bit D-type storage register. Thermal shutdown protection is also built-into the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases to less than 160°C (typical), the device begins to operate again.

Feature Description (continued)

8.3.2 Serial-In Interface

The TLC6C598 device contains an 8-bit serial-in, parallel out shift register that feeds an 8-bit D-type storage register. Data transfer through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage transfers data to the output buffer when shift register clear (CLR) is high.

8.3.3 Clear Register

A logic low on $\overline{\text{CLR}}$ clears all registers in the device. TI suggests clearing the device during power up or initialization.

8.3.4 Cascade Through SER OUT

By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid that the second device receives SRCK and data input at the same rising edge of SRCK.

8.3.5 Output Control

Holding the output enable (G) high holds all data in the output buffers low, and all drain outputs are off. Holding G low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sink-current. This pin also be used for global PWM dimming.

8.4 Device Functional Modes

8.4.1 Operation With V_{CC} < 3 V

This device works normally during 3 V ≤ V_{CC} ≤ 5.5 V, when operation voltage is lower than 3 V. The behavior of device cannot be ensured, including communication interface and current capability.

8.4.2 Operation With 5.5 V ≤ V_{CC} ≤ 8 V

The device works normally during this voltage range, but reliability issues may occurs while the device works for a long time in this voltage range.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLC6C5912 device is a serial-in, parallel-out, power logic 8-bit shift register with low-side open-drain DMOS output rating of 40 V and 50-mA continuous sink-current capabilities when V_{CC}= 5 V. The device is designed to drive resistive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The device also provides up to 2000 V of ESD protection when tested using the human body model and 200 V when using the machine model.

9.2 Typical Application

Figure 13 shows a typical cascade application circuit with two TLC6C5912 chips configured to cascade topology. The MCU generates all the input signals.

Typical Application (continued)

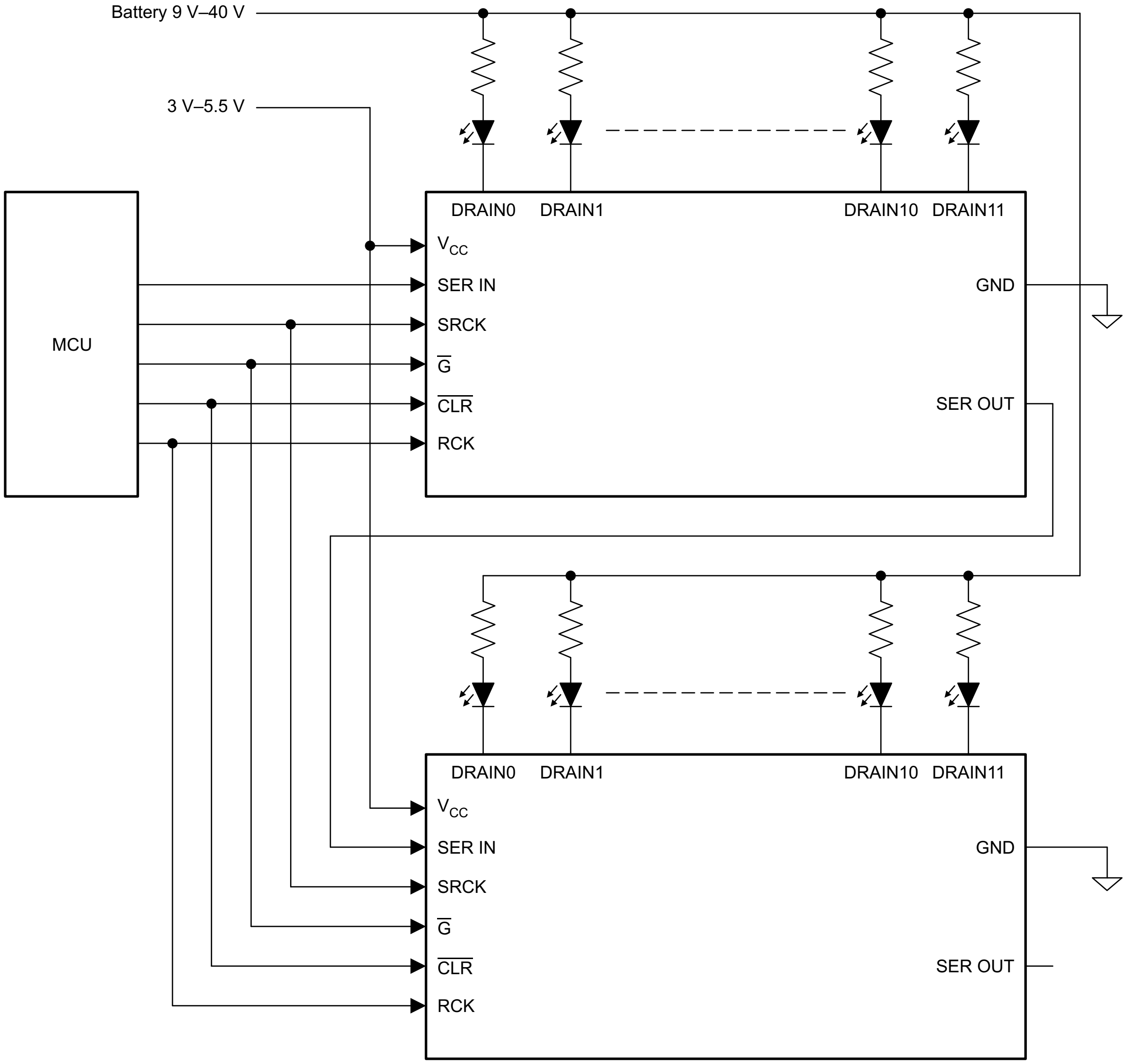


Figure 13. Typical Application Circuit

9.2.1 Design Requirements

Table 1 lists the parameters for this design example.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Vbattery	9 V to 40 V
V_{CC} _ 1	3.3 V
I(D0), I(D1), I(D2), I(D3) , I(D4), I(D5), I(D6), I(D7), I(D8), I(D9), I(D10), I(D11)	30 mA
V_{CC} _ 2	5 V
I(D12), I(D13), I(D14), I(D15) , I(D16), I(D17), I(D18), I(D19), I(D20), I(D21), I(D122), I(D23)	50 mA

9.2.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters:

- Vsupply: LED supply voltage
- VDx: LED forward voltage
- I: LED current

After determining the parameters, calculate the resistor in series with LED using Equation 1.

$$Rx = (Vsupply – VDx) / I \quad (1)$$

9.2.3 Application Curve

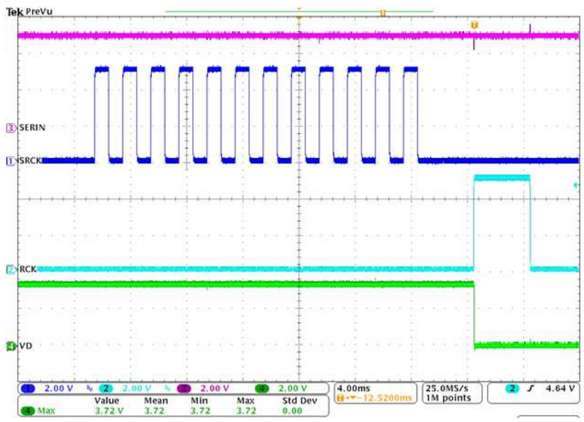


Figure 14. TLC6C5912 Application Waveform

10 Power Supply Recommendations

The TLC6C5912 device is designed to operate from an input voltage supply range from 3 V to 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the V_{CC} pin.

11 Layout

11.1 Layout Guidelines

There are no special layout requirement for the digital signal pins. The only requirement is placing the ceramic bypass capacitors near the corresponding pin.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the cooper on the PCB. Maximizing the copper coverage is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Example

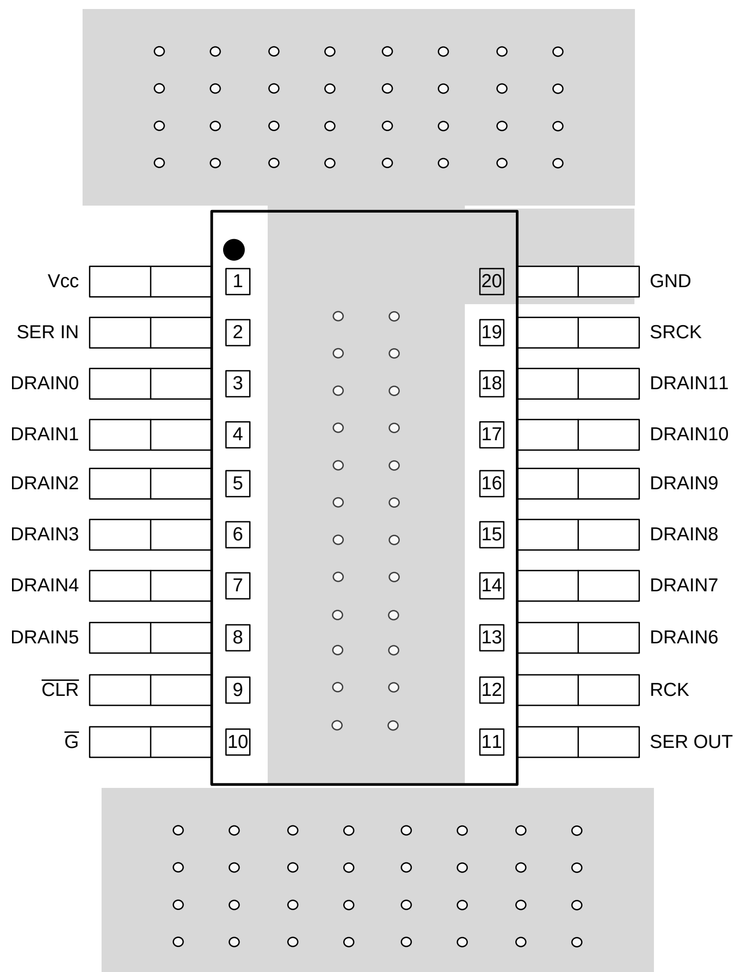


Figure 15. Layout Recommendation

12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

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	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6C5912PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	6C5912I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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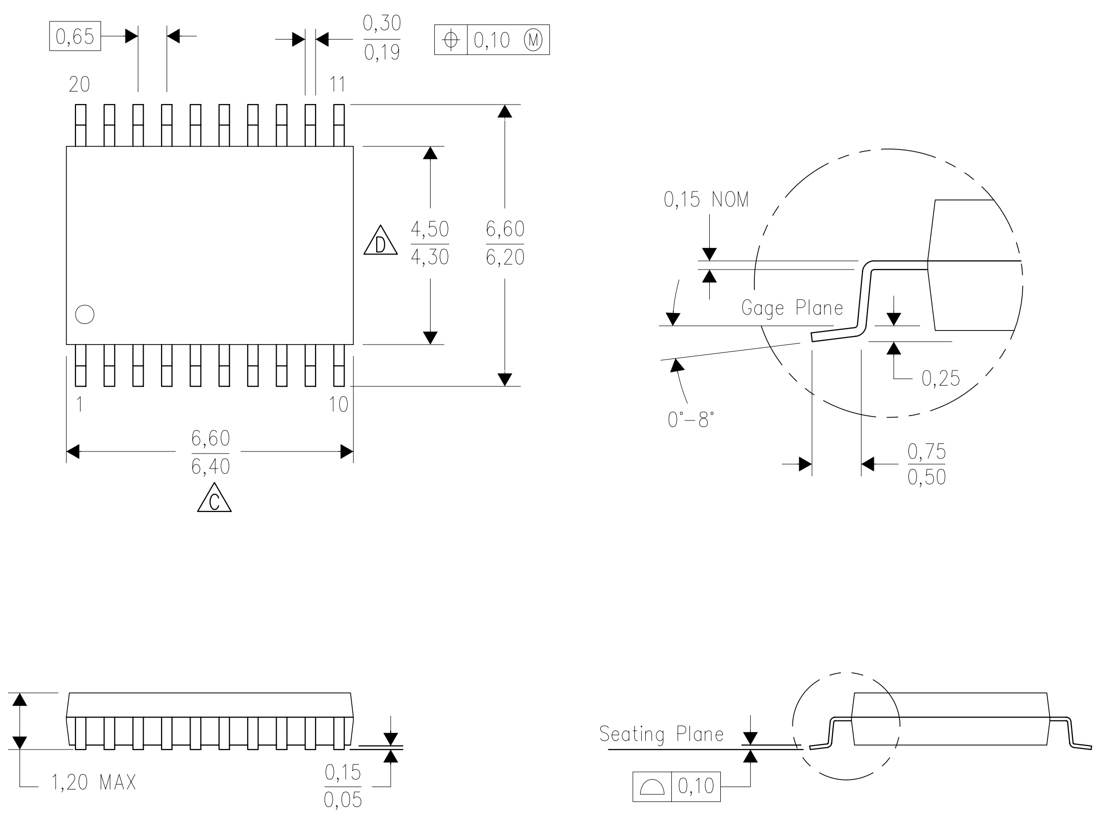
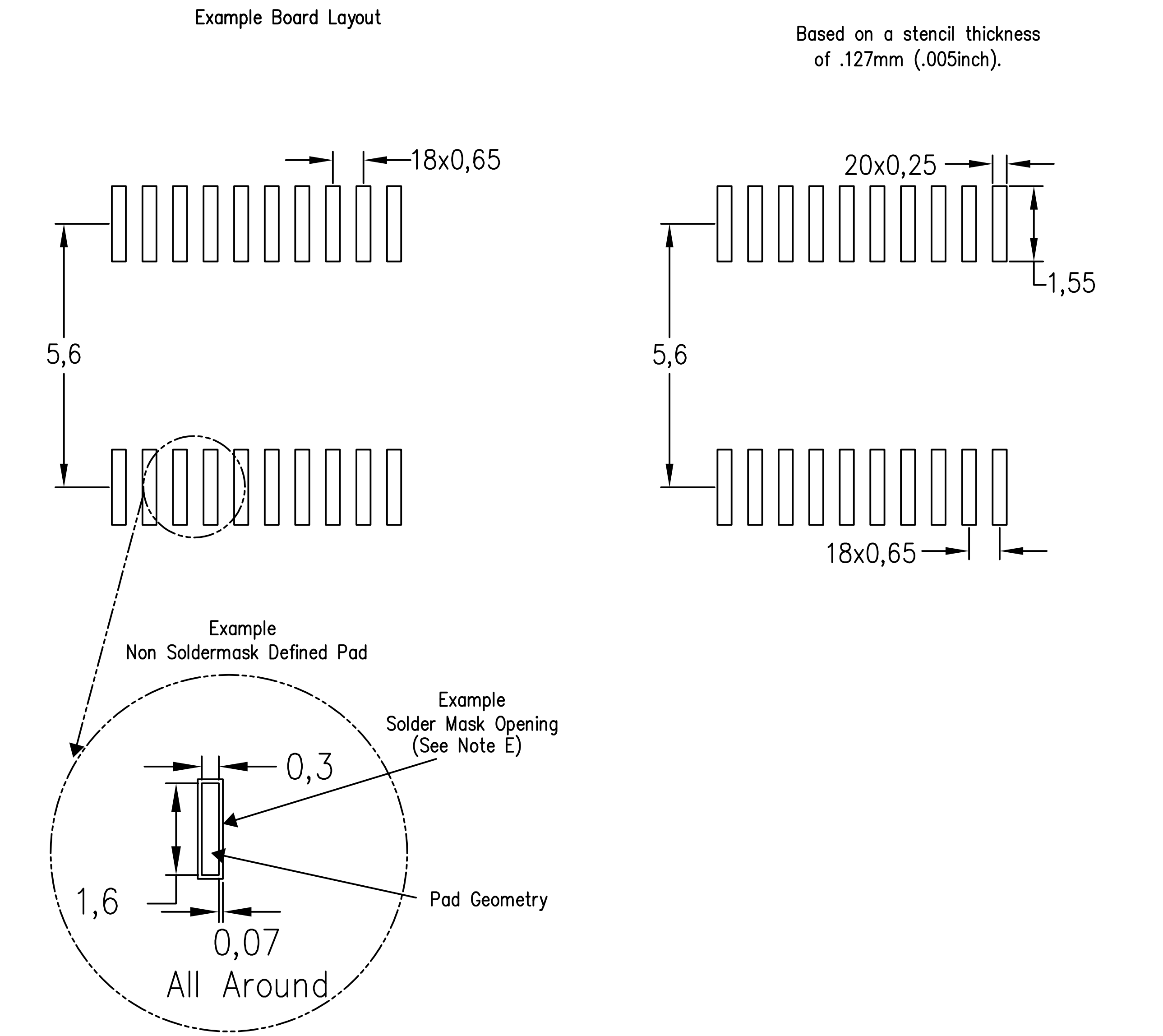
PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



4040064-5/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



4211284-5/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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