TPS7B82-Q1 300mA 高电压超低 I_Q 低压降稳压器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：-40°C ≤ T_A ≤ 125°C
- 工作结温范围：
  –40°C ≤ T_J ≤ 150°C
- 低静态电流 I_Q：
  - 关断模式下 I_Q 为 300nA
  - 轻负载时典型值为 2.7µA
  - 轻负载时最大值为 5µA
- 3V 至 40V 宽 V_{IN} 输入电压范围，瞬态电压高达 45V
- 最大输出电流：300mA
- 输出电压精度为 2%
- 最大压降电压：对于固定 5V 输出版本，200mA 负载电流下为 700mV
- 与低 ESR（0.001Ω 至 5Ω）陶瓷输出稳定电容器（1µF 至 200µF）搭配使用时可保持稳定
- 5V 和 3.3V 固定输出电压
- 热阻 ($R_{\theta JA}$)：63.9°C/W
- 封装：
  - 8 引脚 HVSSOP，$R_{\theta JA}$ = 63.9°C/W
  - 6 引脚 WSON，$R_{\theta JA}$ = 72.8°C/W
  - 5 引脚 TO-252，$R_{\theta JA}$ = 38.8°C/W

2 应用

- 汽车音响主机
- 远程信息处理控制单元
- 前照灯
- 车身控制模块
- 逆变器和电机控制

3 说明

在汽车电池连接 应用中，低静态电流 (I_Q) 对于省电和延长电池寿命而言至关重要。对于始终开启的系统，尤其有必要实现超低 I_Q。

TPS7B82-Q1 是一款旨在在 3V 至 40V（45V 负载突降保护）宽输入电压范围内运行的低压降线性稳压器。TPS7B82-Q1 的工作电压低至 3V，因此可在冷启动以及启动和停止情况下继续工作。该器件在轻负载时的典型静态电流仅为 2.7µA，是用于为待机系统中的微控制器 (MCU) 和 CAN/LIN 收发器供电的最佳解决方案。

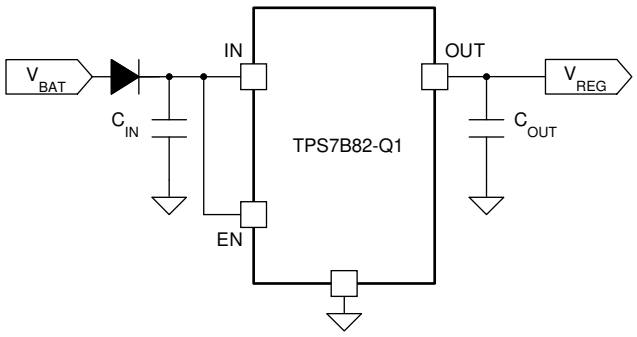
此器件 具有 集成式短路和过流保护。此器件可在 –40°C 至 125°C 的环境温度下运行，且结温范围为 –40°C 至 150°C。此外，此器件采用了热传导封装，即使整个器件散热较多，也能实现持久运行。凭借这些特性，该器件非常适合用作各种汽车应用的 电源。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7B82-Q1	HVSSOP (8)	3.00mm × 3.00mm
	WSON (6)	2.00mm × 2.00mm
	TO-252 (5)	6.10mm × 6.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用原理图



目录

4 修订历史记录

Changes from Revision E (June 2019) to Revision F **Page**

- 已更改 *更改了应用* 部分 ... 1
- 已更改 更改了特定于汽车的*特性* 项目符号 ... 1
- 已更改 将 KVU 封装从“预发布”更改为“生产数据” ... 1
- Added ESD classification levels to *ESD Ratings* table ... 5

Changes from Revision D (October 2018) to Revision E **Page**

- 已添加 向文档添加了 KVU 封装，作为预发布器件 ... 1
- 已更改 将 DRV 状态从“预发布”更改为“生产数据” ... 1
- 已添加 向*封装* 项目符号中添加了 TO-252 子项目符号，并为 HVSSOP 和 WSON 子项目符号添加了 $R_{\theta JA}$ 值 ... 1
- Added KVU to *Pin Configuration and Functions* section ... 4
- Changed *Electrical Characteristics* table ... 6
- Added second column in *Test Conditions* to call out device package differences ... 6

Changes from Revision C (February 2018) to Revision D **Page**

- 已添加 向文档添加了 DRV 封装 ... 1
- 已更改 *将第一个符合 AEC-Q100 标准 子项目符号中的“–40°C 至 125°C”* 更改为*“–40°C ≤ T_A ≤ 125°C”*（位于*特性* 部分） ... 1
- 已更改 更改了*工作结温范围* 项目符号（位于*特性* 部分） ... 1
- 已更改 更改了第一个*低静态电流 I_Q* 子项目符号（位于*特性* 部分） ... 1
- 已删除 删除了*集成故障保护* 项目符号（位于*特性* 部分） ... 1
- 已添加 向*封装* 项目符号中添加了 WSON（位于*特性* 部分） ... 1
- 已更改 通篇将 MSOP 更改为 HVSSOP ... 1
- 已更改 更改了第一个项目符号（位于*应用* 部分） ... 1
- 已添加 添加了*远程信息处理控制单元* 项目符号（位于*应用* 部分） ... 1
- 已更改 更改了*说明* 部分的第二段 ... 1
- Added DRV package to *Pin Configuration and Functions* section ... 4
- Changed maximum specification of second $I_{(Q)}$ parameter row from *5 µA* to *6.5 µA* ... 6

- Added first row and last three rows to $V_{(Dropout)}$ parameter 6
- 已更改 *Input Capacitor* section 12

Changes from Revision B (February 2018) to Revision C **Page**

- 已添加 添加了*特性*：器件结温范围：–40°C 至 150°C 1
- 已更改 将*特性* 从“5V 固定输出电压”更改为“5V 和 3.3V 固定输出电压” 1
- 已添加 添加了*特性*：“热阻 ($R_{\theta JA}$)：63.9°C/W” 1
- 已添加 添加了“为 MCU 和 CAN/LIN 收发器供电”（位于*应用* 列表） 1
- 已更改 更改了*说明* 部分 1
- 已更改 更改了*器件信息* 表 1
- Added PowerPAD to the DGN package description 4
- Changed pins 5 and 6 From: NC To: GND in the *Pin Configuration and Functions* 4
- Deleted Note 3 from V_{OUT} in the *Absolute Maximum Ratings* 5
- 已更改 the VALUE column for Output voltage From: 5 V To: 5 V or 3.3 V in 表 1 12

Changes from Revision A (November 2017) to Revision B **Page**

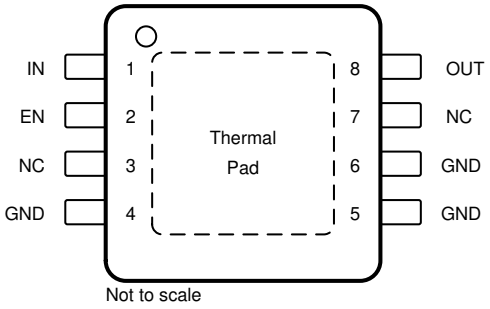
- 已删除 删除了*典型应用原理图* 中电容器 C_{IN} 和 C_{OUT} 的值 1
- Deleted values from capacitors C_{IN} and C_{OUT} in 图 15 12

Changes from Original (September 2017) to Revision A **Page**

- 已删除 删除了*特性* 列表中的 2.5V 和 3.3V 器件选项 1
- Changed V_{EN} to Enable input in the *Absolute Maximum Ratings* 5
- Deleted the blank NOM column from the *Recommended Operating Conditions* table 5
- Deleted requirements for 3.3-V and 2.5-V device versions from the *Electrical Characteristics* table 6
- 已更改 conditions for 图 9 8
- 已删除 3.3-V and 2.5- output voltages from the *Design Requirements* table 12

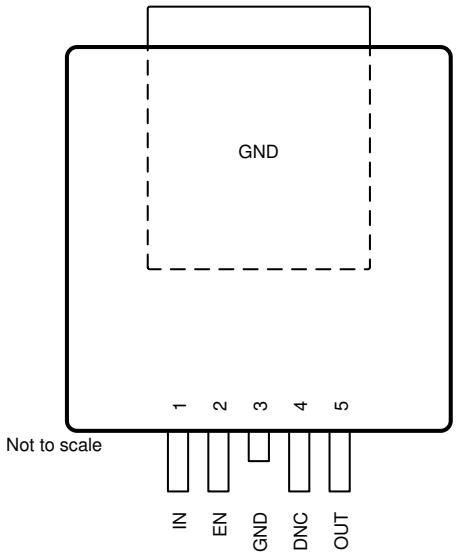
5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP PowerPAD™
Top View



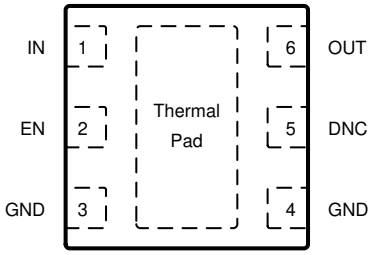
Not to scale

KVU Package
5-Pin TO-252
Top View



Not to scale

DRV Package
6-Pin WSON PowerPAD™
Top View



Not to scale

NC – No internal connection

Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	DGN	DRV	KVU		
DNC	—	5	4	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	2	I	Enable input pin
GND	4, 5, 6	3,4	3, TAB	—	Ground reference
IN	1	1	1	I	Input power-supply pin
NC	3, 7	—	—	—	Not internally connected
OUT	8	6	5	O	Regulated output voltage pin
Thermal pad				—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Unregulated input(3)	–0.3	45	V
V_{EN}	Enable input(3)	–0.3	V_{IN}	V
V_{OUT}	Regulated output	–0.3	7	V
T_J	Junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage, withstand 45 V for 200 ms.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per per AEC Q100-002(1) HBM ESD classification level H2		±2000	V
		Charged-device model (CDM), per per AEC Q100-011 CDM ESD classification level C3B	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	3	40	V
V_{EN}	Enable input voltage	0	V_{IN}	V
C_{OUT}	Output capacitor requirements(1)	1	200	µF
ESR	Output capacitor ESR requirements(2)	0.001	5	Ω
T_A	Ambient temperature range	–40	125	°C
T_J	Junction temperature range	–40	150	°C

(1) The output capacitance range specified in the table is the effective value.
(2) Relevant ESR value at f = 10 kHz.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7B82-Q1			UNIT
		DGN (HVSSOP)	DRV (WSON)	KVU (TO-252)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	31.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	85.8	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	2.7	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.3	37.3	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

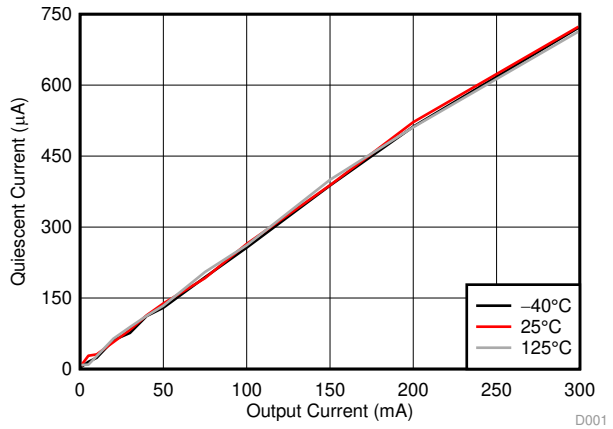
6.5 Electrical Characteristics

V_{IN} = 14-V, 10-µF ceramic output capacitor, T_J = –40ºC to 150ºC, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)								
V_{IN}	Input voltage				$V_{OUT(NOM)}$ + $V_{(Dropout)}$		40	V
$I_{(SD)}$	Shutdown current	EN = 0 V				0.3	1	µA
$I_{(Q)}$	Quiescent current	V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0 mA		DRV and KVU packages		1.9	3.5	µA
				DGN package		1.9	5	
		V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0.2 mA		DRV and KVU packages		2.7	4.5	
				DGN package		2.7	6.5	
$V_{(IN, UVLO)}$	V_{IN} undervoltage detection	Ramp V_{IN} down until the output turns OFF					2.7	V
		Hysteresis				200		mV
ENABLE INPUT (EN)								
V_{IL}	Logic-input low level						0.7	V
V_{IH}	Logic-input high level				2			V
REGULATED OUTPUT (OUT)								
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + $V_{(Dropout)}$ to 40 V, I_{OUT} = 1 mA to 300 mA		DRV and KVU packages	–1.5%		1.5%	
				DGN package	–2%		2%	
$V_{(Line-Reg)}$	Line regulation	V_{IN} = 6 V to 40 V, I_{OUT} = 10 mA					10	mV
$V_{(Load-Reg)}$	Load regulation	V_{IN} = 14 V, I_{OUT} = 1 mA to 300 mA		DRV and KVU packages			10	mV
				DGN package			20	
$V_{(Dropout)}$	Dropout voltage	$V_{OUT(NOM)}$ = 5 V	I_{OUT} = 300 mA	DRV and KVU packages		630	1170	mV
				DGN package			1000	
			I_{OUT} = 200 mA	DRV and KVU packages		420	780	
				DGN package		400	700	
			I_{OUT} = 100 mA	DRV and KVU packages		210	390	
				DGN package		200	350	
		V_{OUT} = 3.3 V	I_{OUT} = 300 mA	DRV and KVU packages		730	1350	
				DGN package			1250	
			I_{OUT} = 200 mA	DRV and KVU packages		475	900	
				DGN package			850	
			I_{OUT} = 100 mA				450	
I_{OUT}	Output current	V_{OUT} in regulation			0		300	mA
$I_{(CL)}$	Output current limit	V_{OUT} short to 90% × V_{OUT}			310	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)}$ = 0.5 V_{PP}, I_{OUT} = 10 mA, frequency = 100 Hz, C_{OUT} = 2.2 µF				60		dB
OPERATING TEMPERATURE RANGE								
$T_{(SD)}$	Junction shutdown temperature					175		ºC
$T_{(HYST)}$	Hysteresis of thermal shutdown					20		ºC

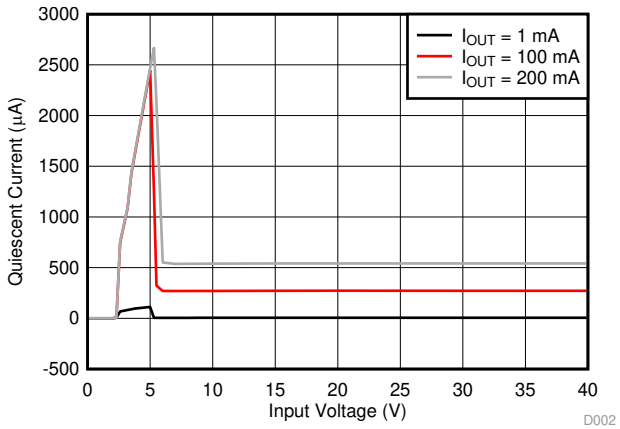
6.6 Typical Characteristics

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40ºC to 150ºC (unless otherwise noted)



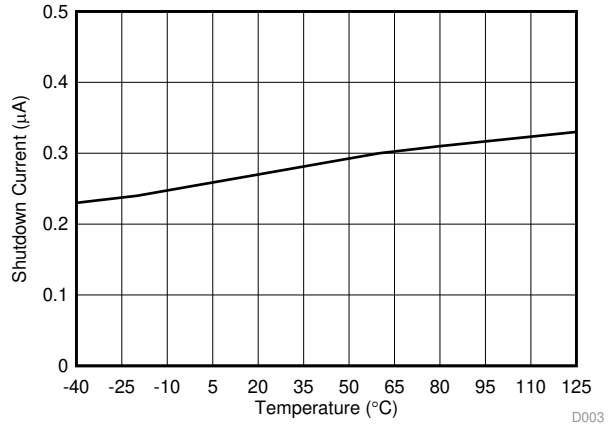
V_{OUT} = 5 V

图 1. Quiescent Current vs Output Current



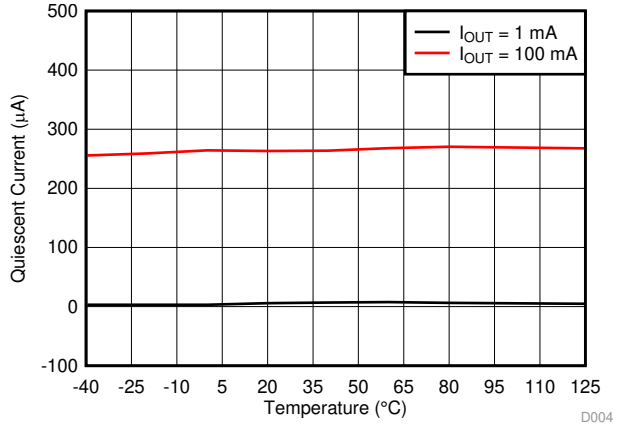
V_{OUT} = 5 V

图 2. Quiescent Current vs Input Voltage



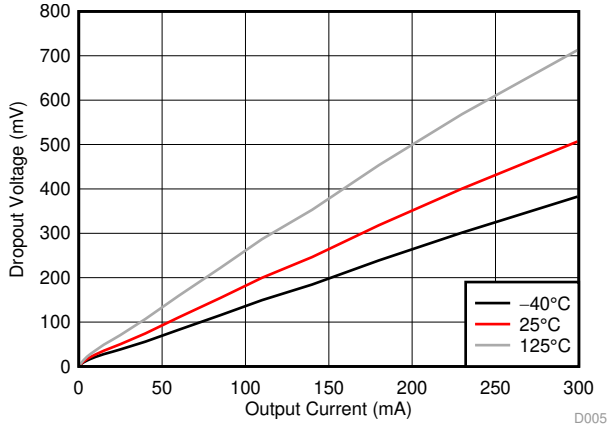
V_{EN} = 0 V

图 3. Shutdown Current vs Ambient Temperature



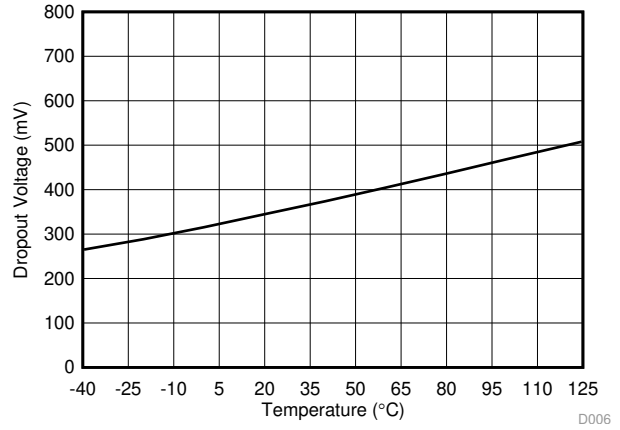
V_{OUT} = 5 V

图 4. Quiescent Current vs Ambient Temperature



V_{IN} = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} – V_{OUT}$

图 5. Dropout Voltage vs Output Current

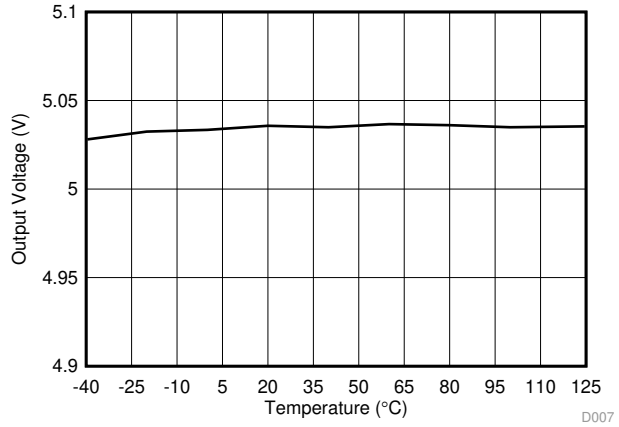


V_{IN} = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} – V_{OUT}$

图 6. Dropout Voltage vs Ambient Temperature

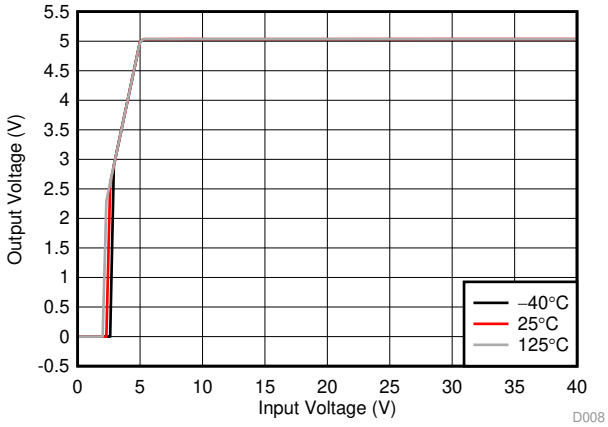
Typical Characteristics (接下页)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40ºC to 150ºC (unless otherwise noted)



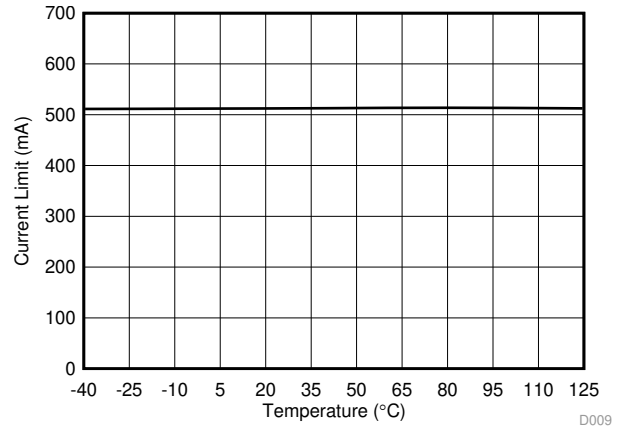
V_{OUT} = 5 V

图 7. Output Voltage vs Ambient Temperature



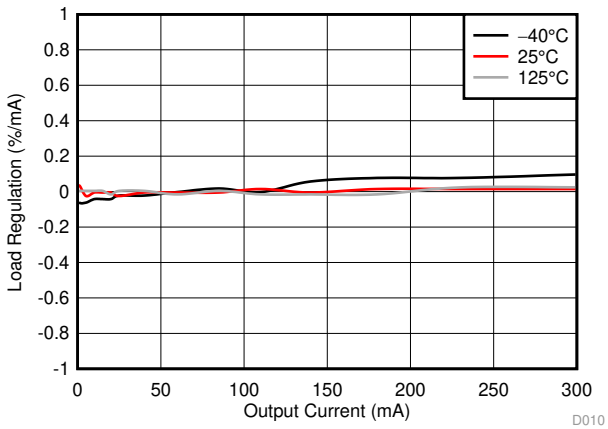
V_{OUT} = 5 V, I_{OUT} = 1 mA

图 8. Output Voltage vs Input Voltage



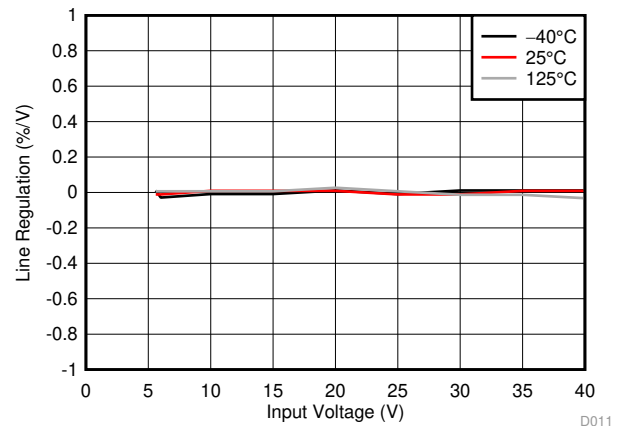
V_{IN} = 14 V, V_{OUT} is shorted to 90% × V_{OUT}

图 9. Output Current Limit vs Ambient Temperature



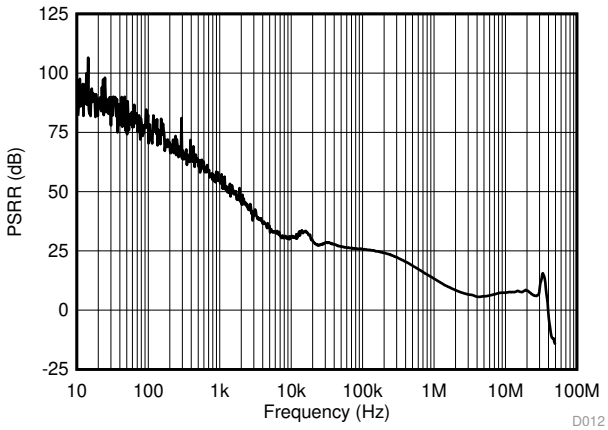
V_{OUT} = 5 V

图 10. Load Regulation



V_{OUT} = 5 V, I_{OUT} = 10 mA

图 11. Line Regulation

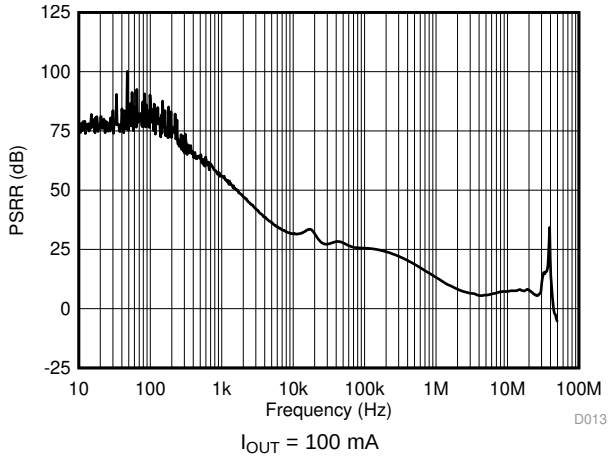


I_{OUT} = 10 mA

图 12. PSRR vs Frequency

Typical Characteristics (接下页)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40ºC to 150ºC (unless otherwise noted)



I_{OUT} = 100 mA

图 13. PSRR vs Frequency

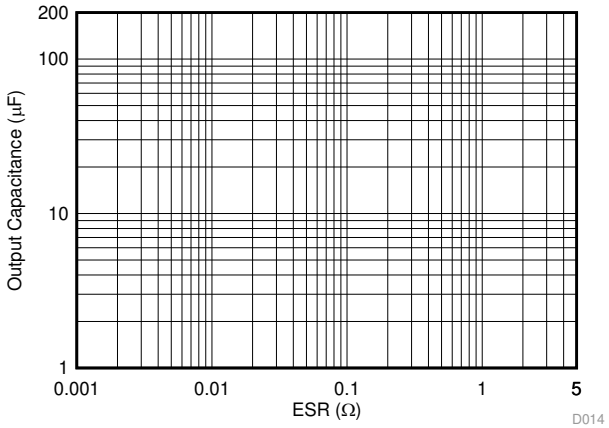


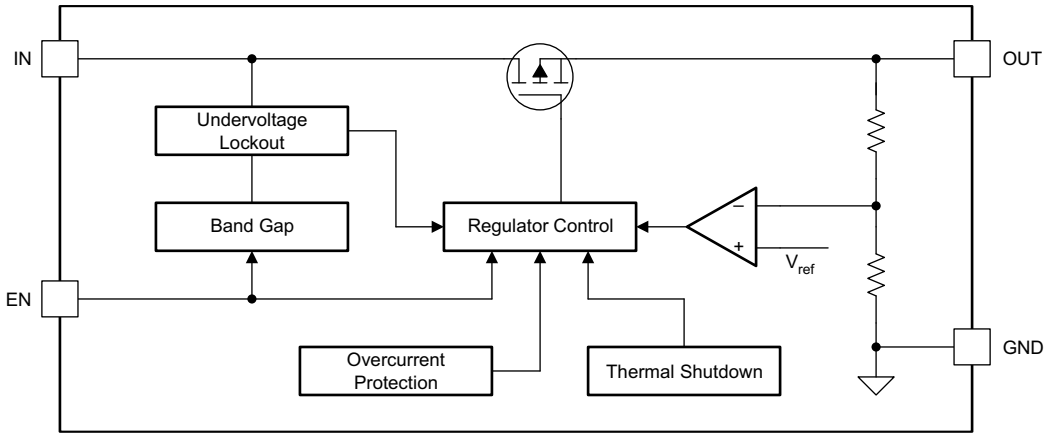
图 14. Output Capacitance vs ESR Stability

7 Detailed Description

7.1 Overview

The TPS7B82-Q1 is a 40-V 300-mA low-dropout linear regulator with ultralow quiescent current. This voltage regulator consumes only 3 µA of quiescent current at light load, and is quite suitable for the automotive always-on application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation ON. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold ($V_{(UVLO)}$). This ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required level.

7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the TSD trip point minus thermal shutdown hysteresis, the output turns on again.

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B82-Q1 is a 300-mA 40-V low-dropout linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

图 15 shows a typical application circuit for the TPS7B82-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

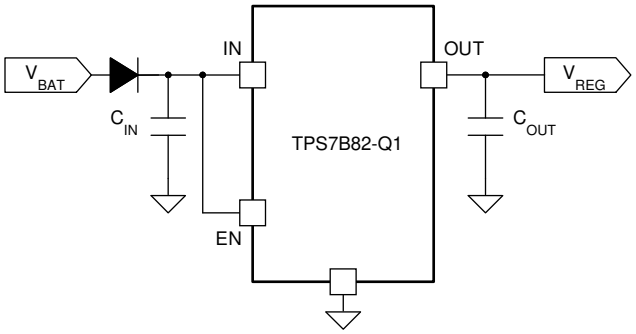


图 15. TPS7B82-Q1 Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 1.

表 1. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	300 mA maximum

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10-µF to 22-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B82-Q1, the device requires an output capacitor with a value in the range from 1 µF to 200 µF and with an ESR range between 0.001 Ω and 5 Ω. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.3 Application Curve

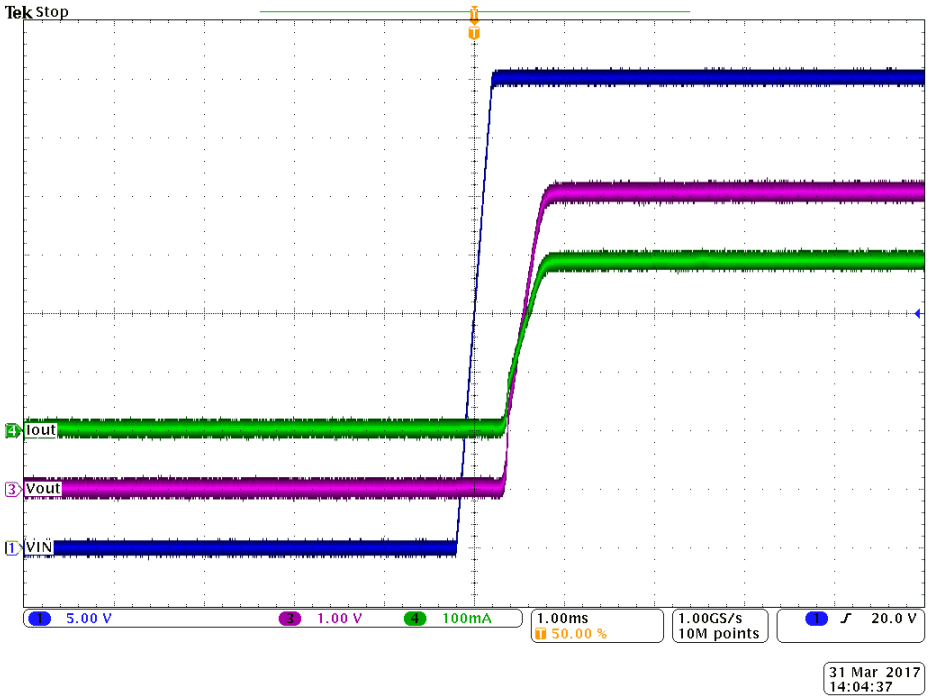


图 16. TPS7B82-Q1 Power-Up Waveform (5 V)

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 3 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B82-Q1, TI recommends adding a capacitor with a value greater than or equal to 10 μF with a 0.1-μF bypass capacitor in parallel at the input.

10 Layout

10.1 Layout Guidelines

For LDO power supplies, especially these high-voltage and large-output-current ones, layout is an important step. If layout is not carefully designed, the regulator could fail to deliver enough output current because of thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, TI recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad. 图 17 shows an example layout.

10.2 Layout Example

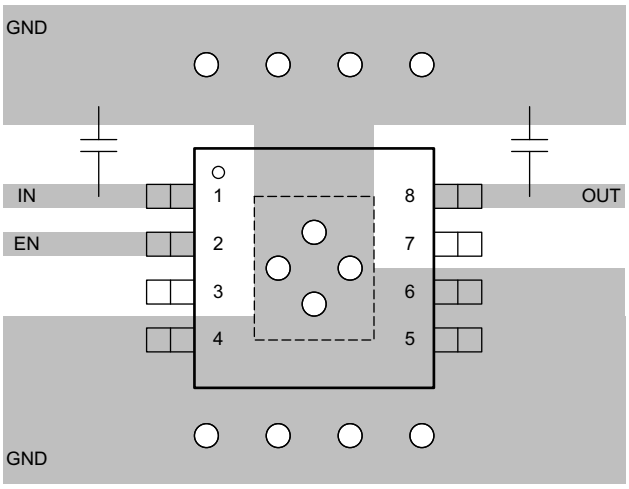


图 17. TPSB82-Q1 Example Layout Diagram

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是适用于指定器件的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7B8233EPWPRQ1	ACTIVE	HTSSOP	PWP	14	2500	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 150		Samples
PTPS7B8250EPWPRQ1	ACTIVE	HTSSOP	PWP	14	2500	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 150		Samples
TPS7B8225QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1QFX	Samples
TPS7B8233QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1GGX	Samples
TPS7B8233QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1ORH	Samples
TPS7B8233QKVURQ1	ACTIVE	TO-252	KVU	5	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	7B8233Q1	Samples
TPS7B8250QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	19TX	Samples
TPS7B8250QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1UFH	Samples
TPS7B8250QKVURQ1	ACTIVE	TO-252	KVU	5	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	7B8250Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

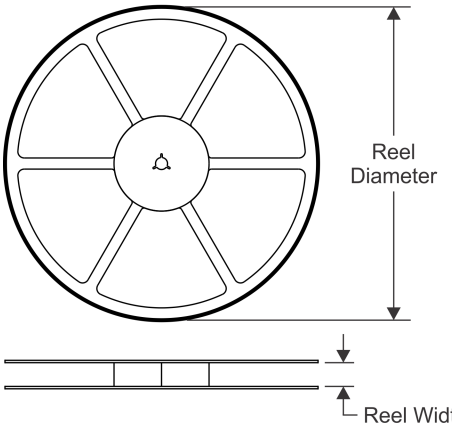
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

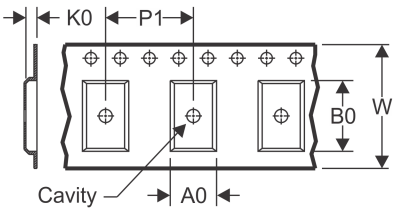
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

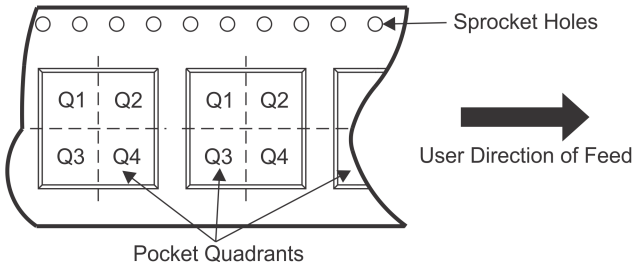


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

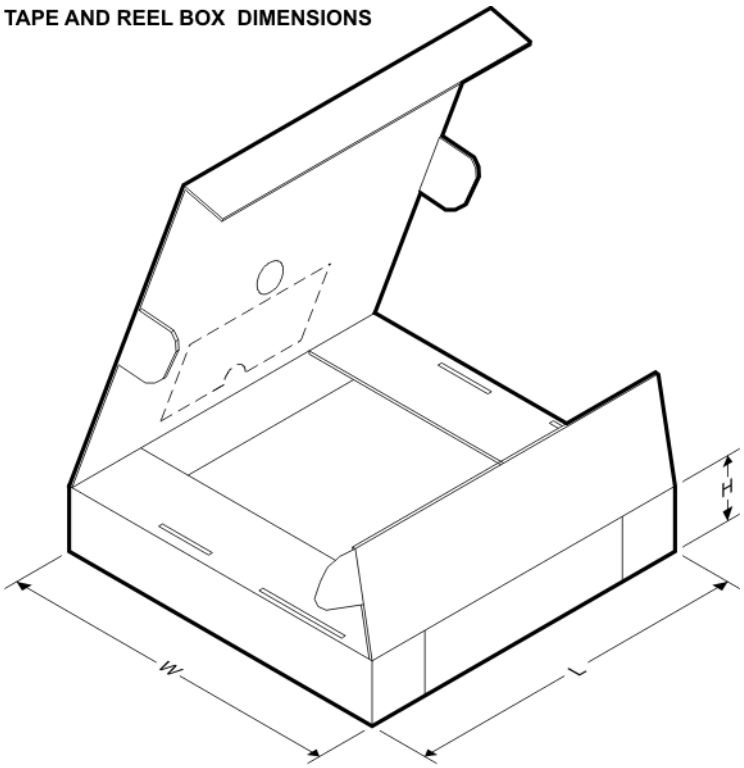
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

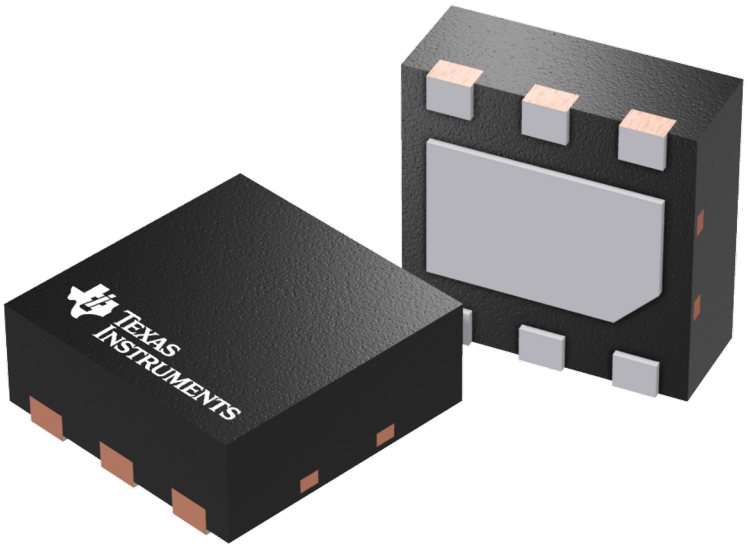


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



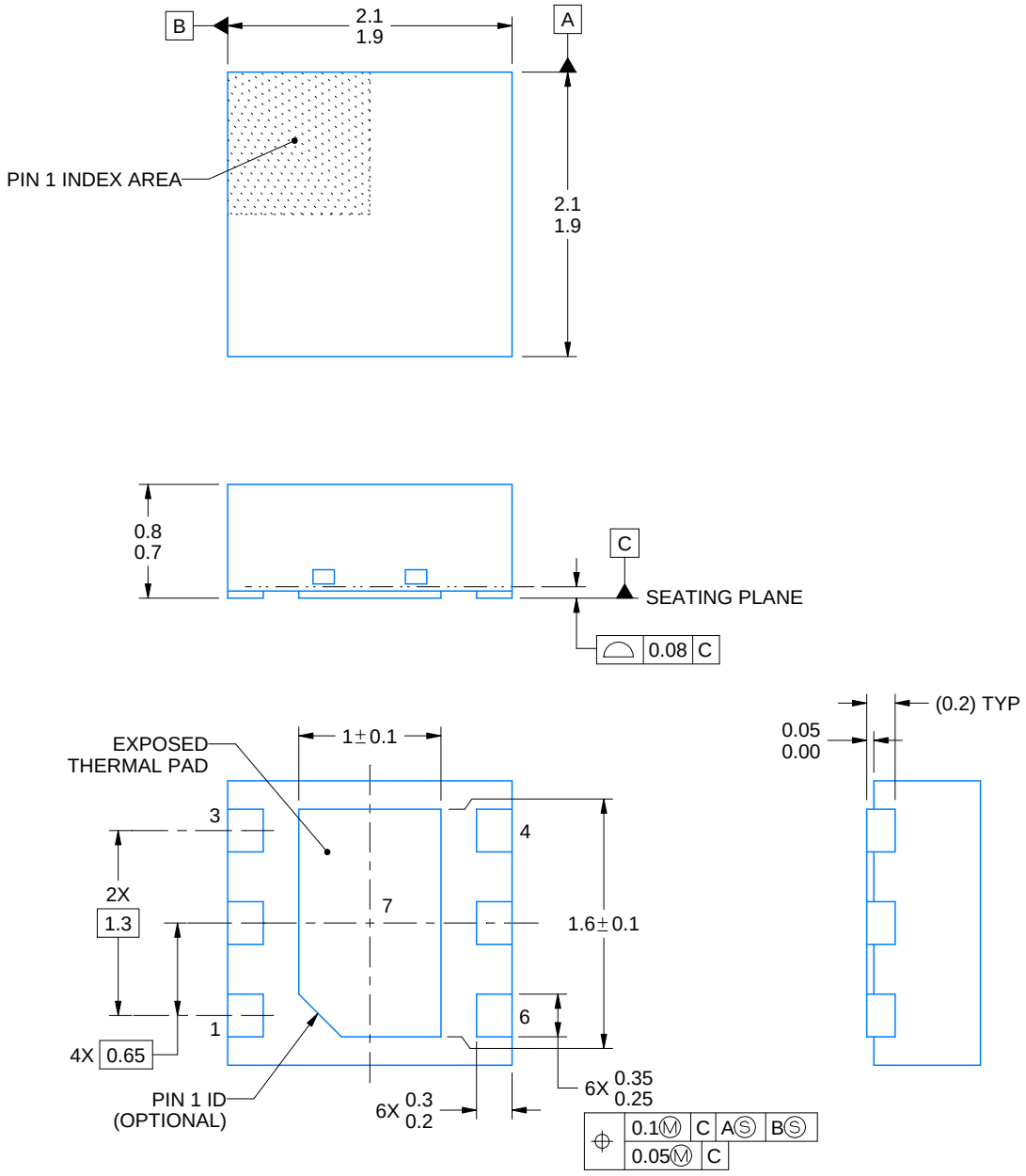
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

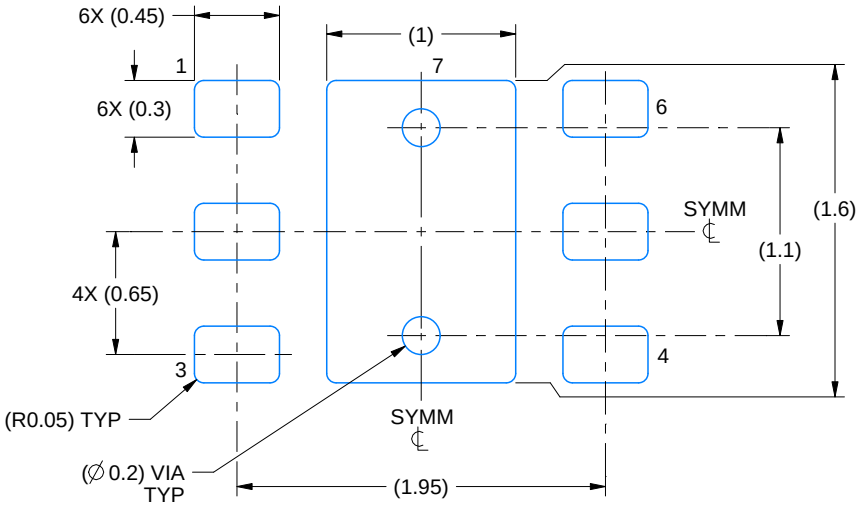
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

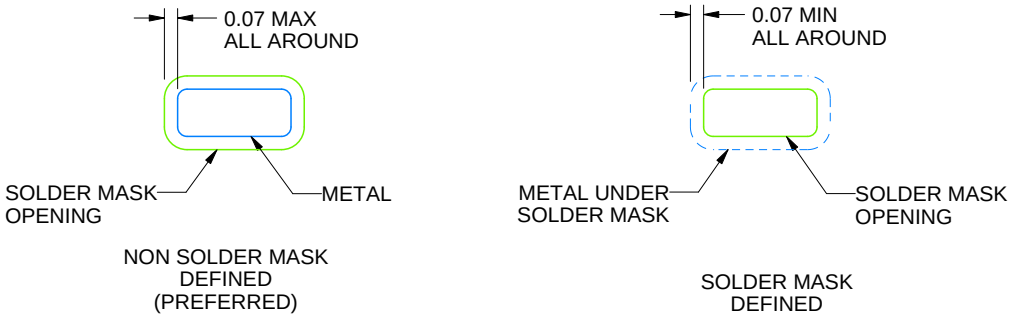


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

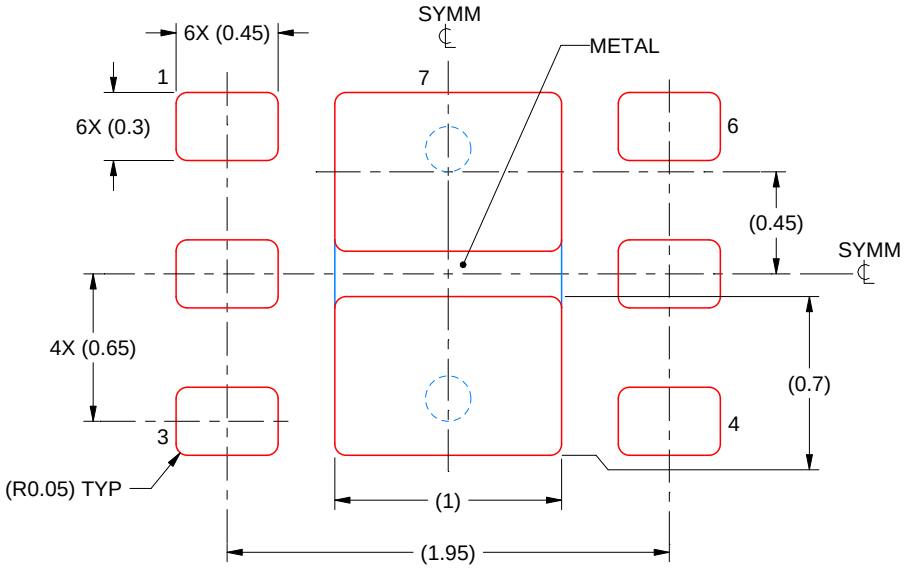
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

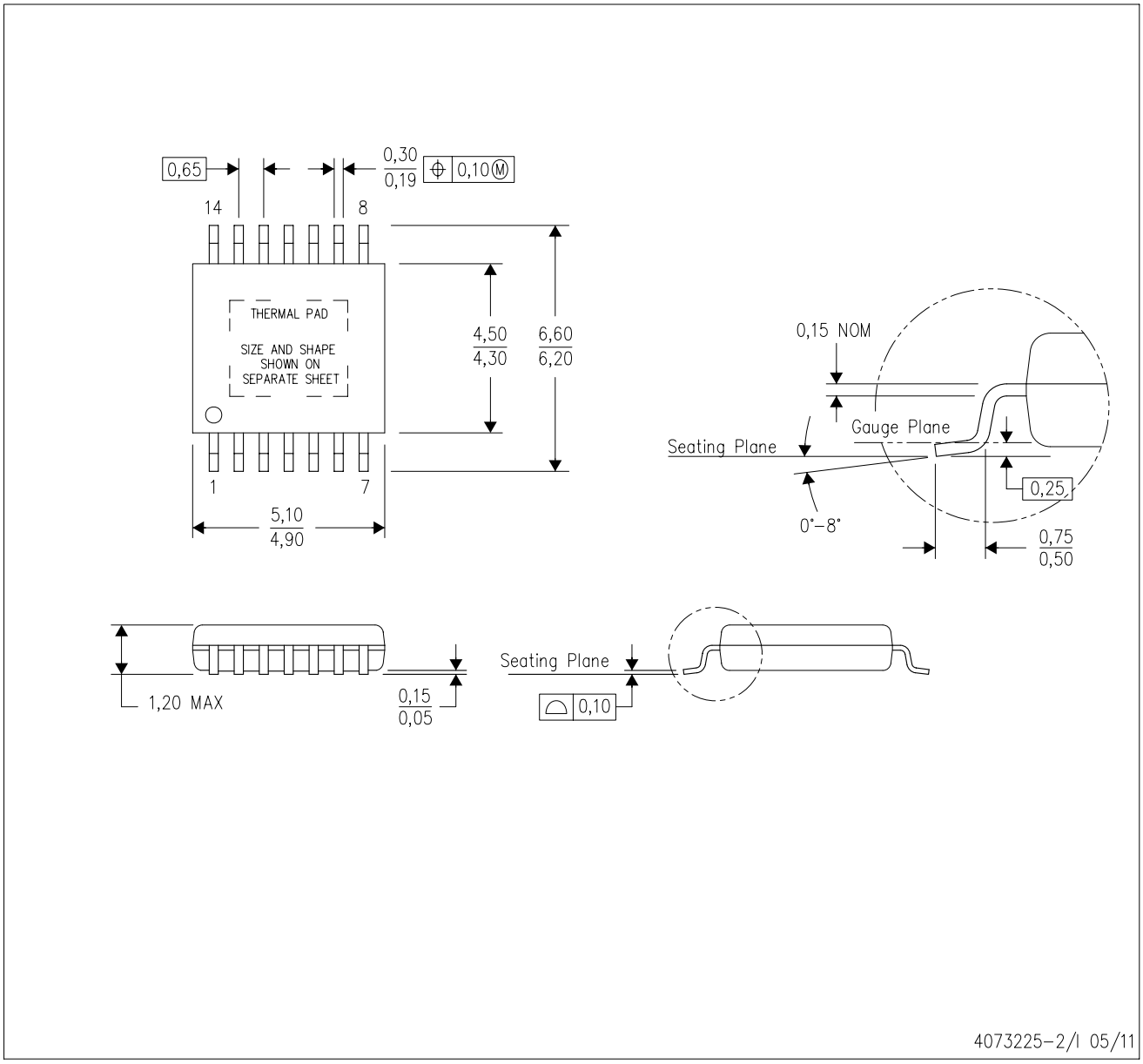
EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

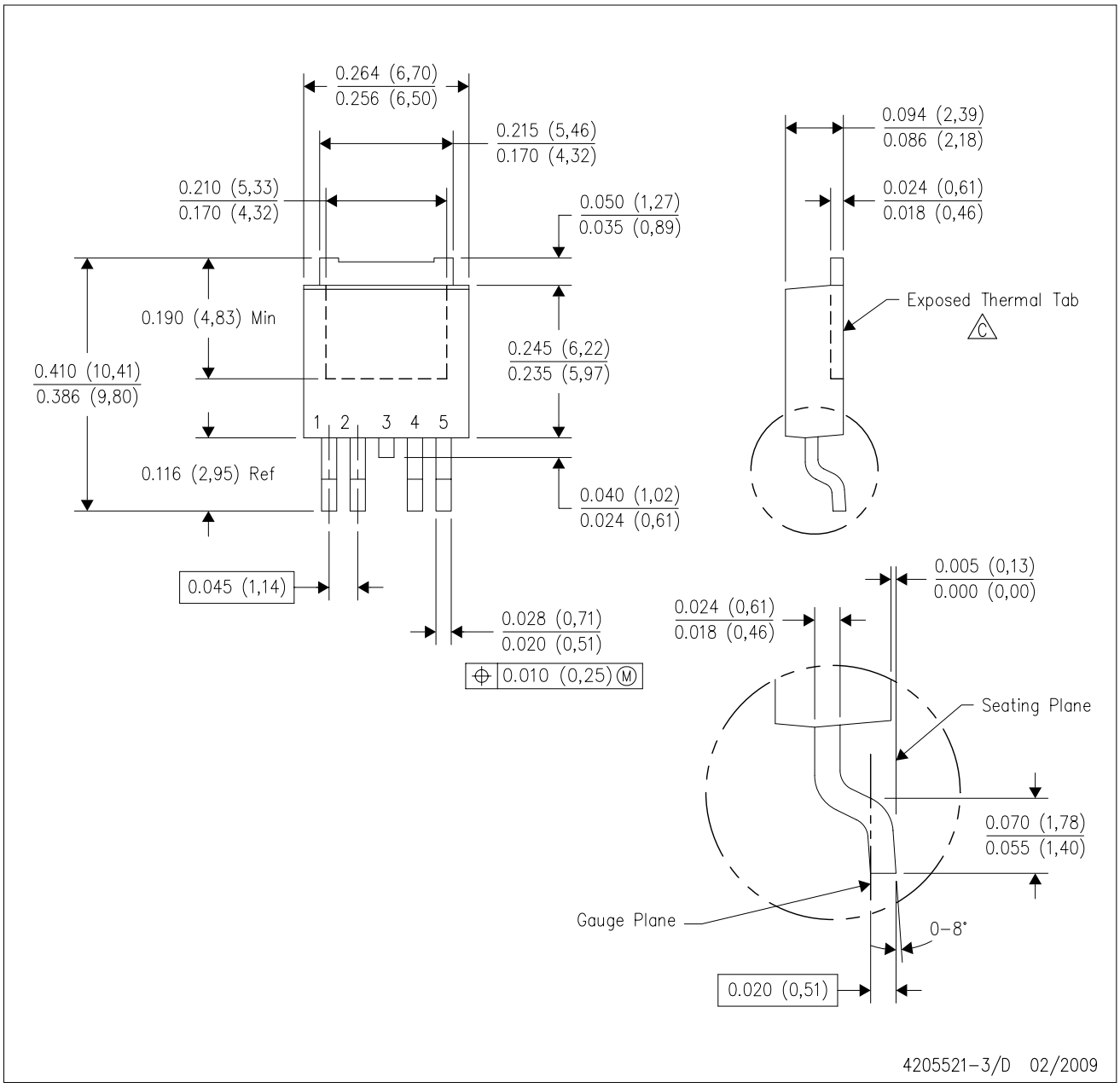
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

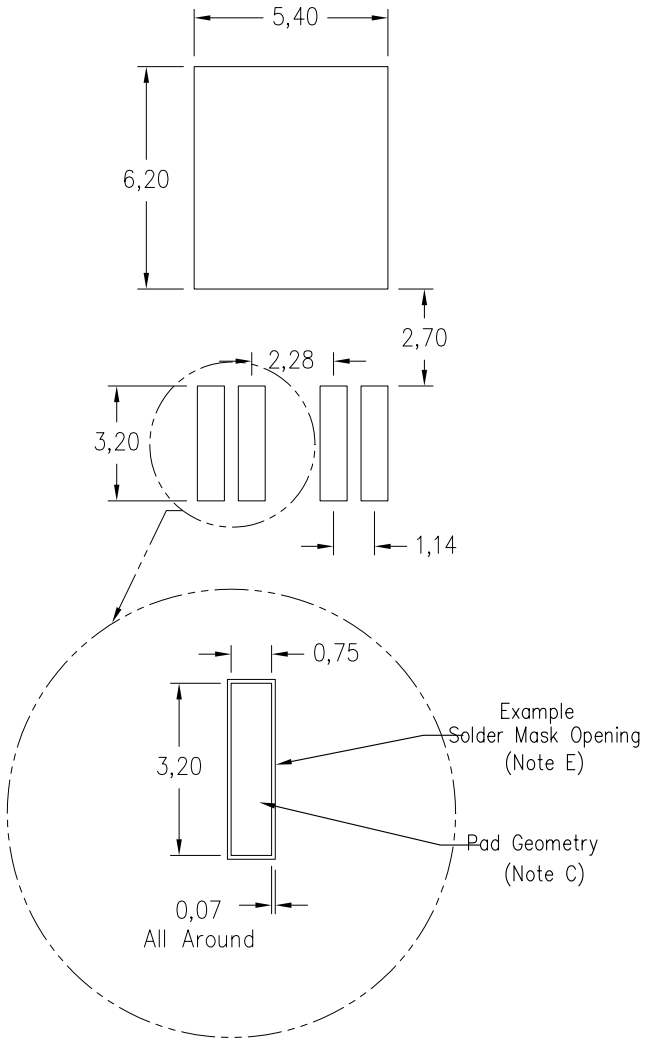
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



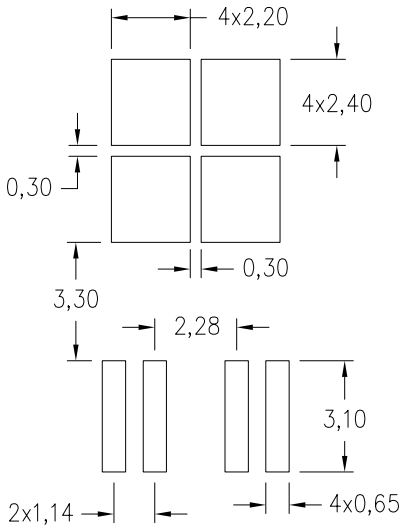
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

GENERIC PACKAGE VIEW

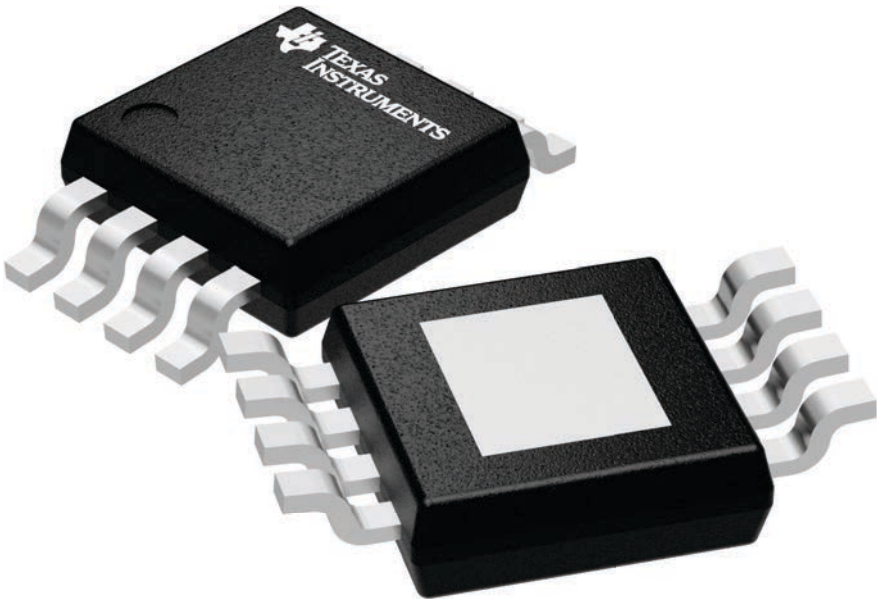
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

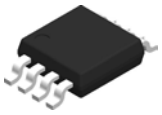
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

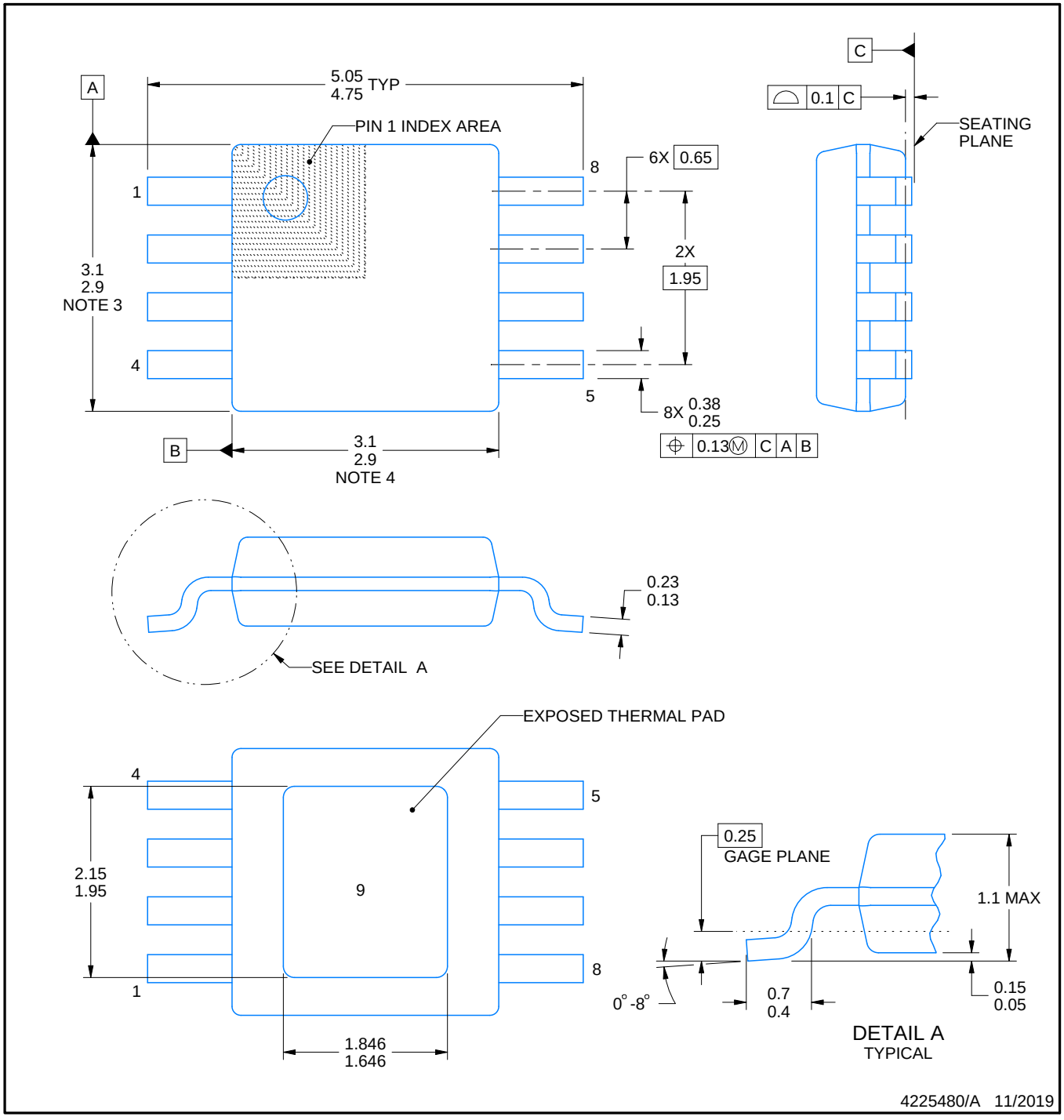
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

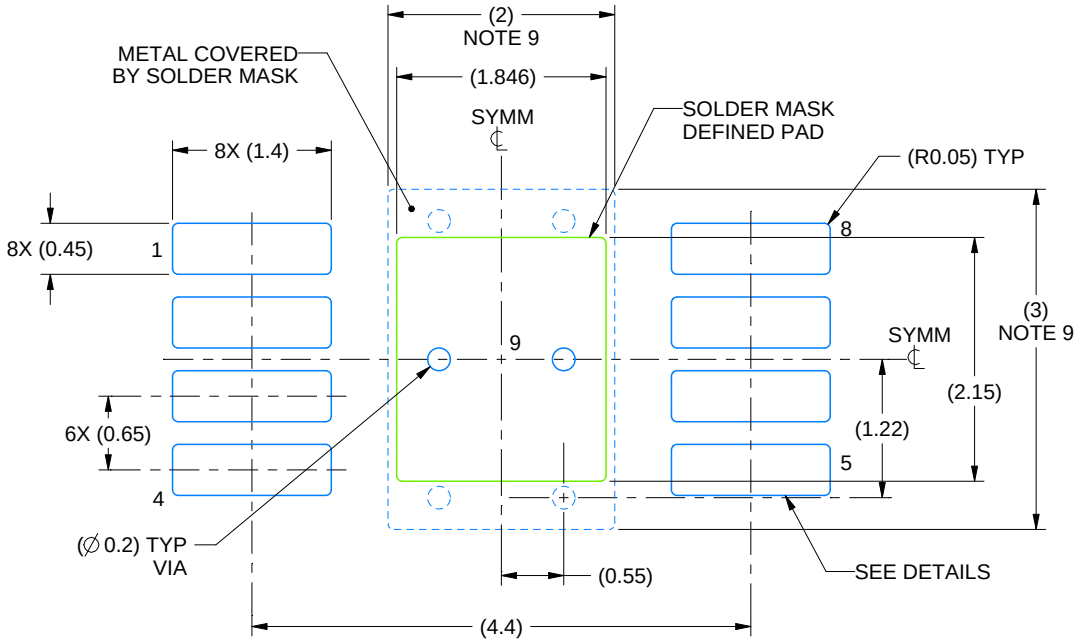
SMALL OUTLINE PACKAGE



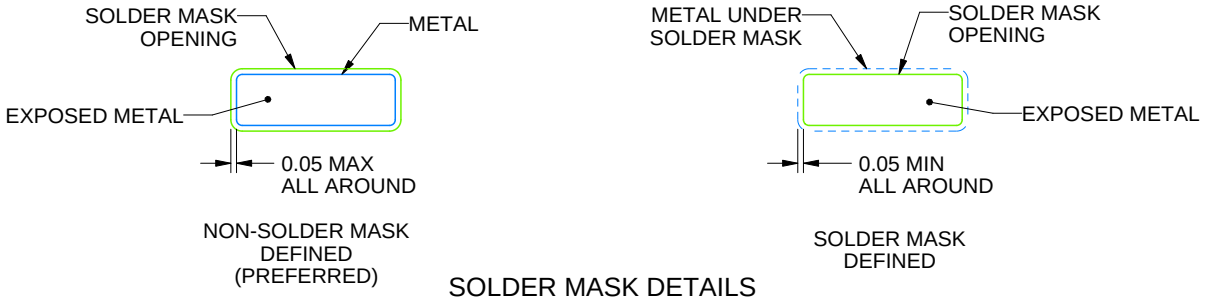
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

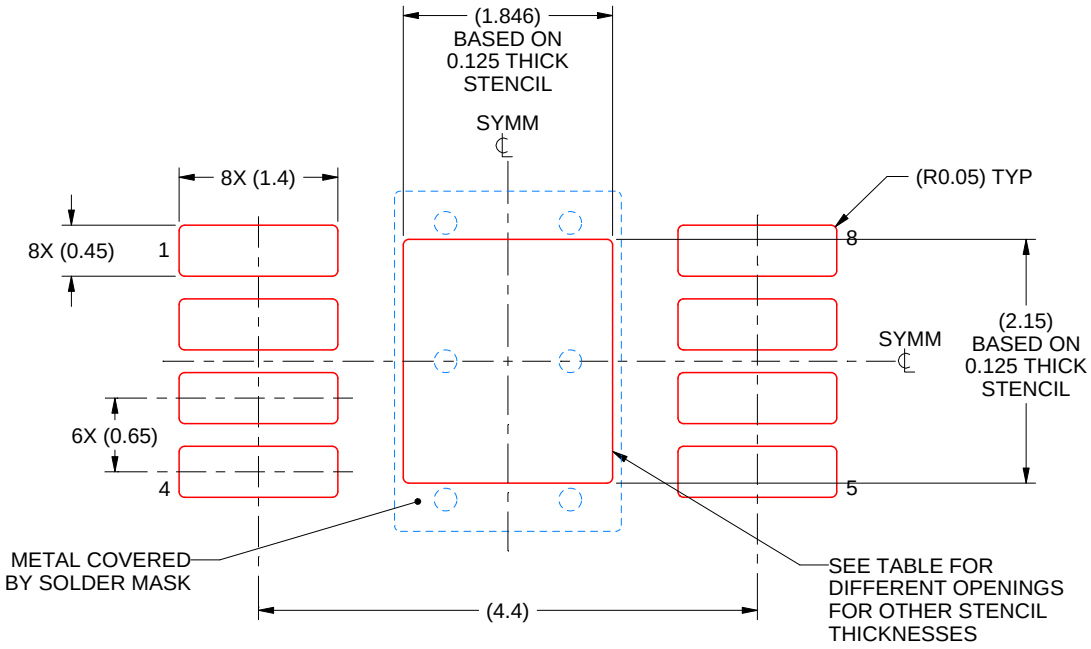


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122