# TPS7A83A 2A 高精度 (0.75%) 低噪声 ($4.4\mu V_{RMS}$) LDO 稳压器

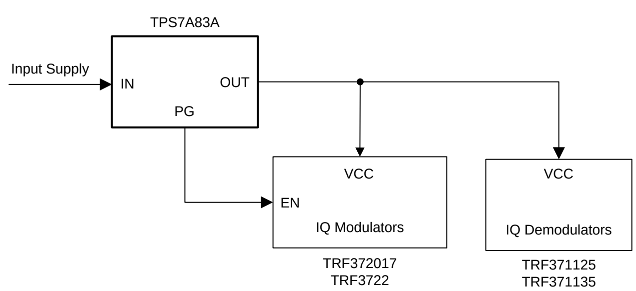
## 1 特性

- 低压差：电流为 2A 时最大值为 200mV
- 线路、负载和温度范围内的偏置精度最大值为 0.75%
- 输出电压噪声：
  – 4.4 $\mu V_{RMS}$（输出为 0.8V）
  – 输出电压为 5.2V 时，噪声为 $7.7\mu V_{RMS}$
- 输入电压范围：
  – 无偏置：1.4V 至 6.5V
  – 有偏置：1.1V 至 6.5V
- ANY-OUT™运行：
  – 输出电压范围：0.8V 至 3.95V
- 可调节运行：
  – 输出电压范围：0.8V 至 5.2V
- 电源纹波抑制：
  – 500kHz 时为 40dB
- 出色的负载瞬态响应
- 可调节软启动浪涌电流控制
- 开漏电源正常 (PG) 输出
- 使用 22µF 或更大的陶瓷输出电容器实现稳定运行
- $\theta_{JC}$ = 3.4°C/W
- 20 引脚 VQFN 封装：
  – 3.5mm × 3.5mm (RGR)
  – 5mm × 5mm (RGW)

## 2 应用

- 数字负载：串行解串器、现场可编程门阵列 (FPGA) 和数字信号处理器 (DSP)
- 仪器仪表、医疗和音频
- 高速模拟电路：
  – 压控振荡器 (VCO)、模数转换器 (ADC)、数模转换器 (DAC) 以及低压差分信令 (LVDS)
- 成像：互补金属氧化物半导体 (CMOS) 传感器和视频专用集成电路 (ASIC)
- 测试和测量

为 **RF** 组件供电




## 3 说明

器件 TPS7A83A 是一款低噪声 ($4.4\mu V_{RMS}$)、低压差线性稳压器 (LDO)，可提供 2A 电流，同时最大压差仅为 200mV。在该器件的输出电压范围中，可进行引脚编程的范围为 0.8V 至 3.95V，可通过外部电阻分压器进行调节的范围为 0.8V 至 5.2V。

TPS7A83A 将低噪声 ($4.4\mu V_{RMS}$)、高 PSRR 和高输出电流能力融为一体，非常适合为高速通信、视频、医疗或测试和测量应用的噪声敏感型组件 供电。TPS7A83A 的优秀性能可抑制电源产生的相位噪声和时钟抖动，因此非常适合为高性能串行器和解串器 (SerDes)、模数转换器 (ADC)、数模转换器 (DAC) 和射频组件供电。该器件的优秀性能和高达 5.2V 的输出能力尤其适合射频放大器使用。

对于需要以低输入和低输出 (LILO) 电压运行的数字负载（例如专用集成电路 (ASIC)、现场可编程门阵列 (FPGA) 和数字信号处理器 (DSP)），TPS7A83A 所具备的极高的精度（在负载和温度范围内可达 0.75%）、遥感功能、出色的瞬态性能和软启动能力可确保实现出色的系统性能。

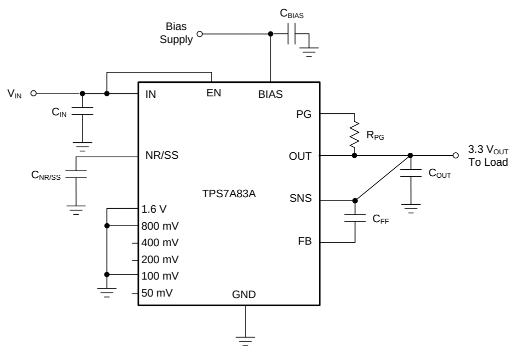
TPS7A83A 的多功能性使其成为许多严苛应用的必选组件。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS7A83A | 超薄四方扁平无引线封装 (VQFN) (20) | 3.50mm x 3.50mm |
| | | 5.00mm × 5.00mm |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路


Bias
Supply
CBIAS
VIN
CIN
IN
EN
BIAS
PG
RPG
NR/SS
OUT
3.3 VOUT
To Load
COUT
CNR/SS
TPS7A83A
SNS
CFF
1.6 V
800 mV
400 mV
FB
200 mV
100 mV
50 mV
GND

目录



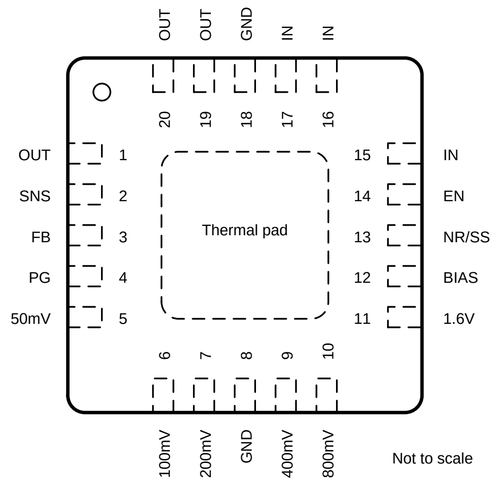
# 4 修订历史记录

**Changes from Original (June 2017) to Revision A** — **Page**

- 已添加 在文档中增加了 RGW 封装 ........ 1
- 已更改 *封装* 特性 项目，添加和区分了 RGW 封装 ........ 1
- 已添加 RGW thermal data to *Thermal Information* table ........ 8

# 5 Pin Configurations and Functions

**RGR, RGW Package**
**3.5-mm × 3.5-mm and 5-mm × 5-mm, 20-Pin VQFN**
**Top View**




## Pin Functions

| PIN | | | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | I/O | |
| 50mV | 5 | I | ANY-OUT voltage setting pins. These pins connect to an internal feedback network. Connect these pins to ground, SNS, or leave floating. Connecting these pins to ground increases the output voltage, whereas connecting these pins to SNS increases the resolution of the ANY-OUT network but decreases the range of the network; multiple pins can be simultaneously connected to GND or SNS to select the desired output voltage. Leave these pins floating (open) when not in use; see the *ANY-OUT Operation* section for additional details. |
| 100mV | 6 | | |
| 200mV | 7 | | |
| 400mV | 9 | | |
| 800mV | 10 | | |
| 1.6V | 11 | | |
| BIAS | 12 | I | BIAS supply voltage. This pin enables the use of low-input voltage, low-output (LILO) voltage conditions (that is, $V_{IN}$ = 1.2 V, $V_{OUT}$ = 1 V) to reduce power dissipation across the die. The use of a BIAS voltage improves dc and ac performance for $V_{IN} \leq 2.2$ V. A 10-µF capacitor or larger must be connected between this pin and ground if the BIAS pin is used. If not used, this pin must be left floating or tied to ground and a capacitor is not needed. |
| EN | 14 | I | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS. |
| FB | 3 | I | Feedback pin connected to the error amplifier. Although not required, TI recommends a 10-nF feed-forward capacitor from FB to OUT (as close to the device as possible) to maximize ac performance. The use of a feed-forward capacitor may disrupt PG (power good) functionality; see the *ANY-OUT Operation* and *Adjustable Operation* sections for more details. |
| GND | 8, 18 | — | Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection. |
| IN | 15-17 | I | Input supply voltage pin. A 10-µF or larger ceramic capacitor (5 µF or greater of capacitance) from IN to ground is recommended to reduce the impedance of the input supply. Place the input capacitor as close as possible to the input; see the *Input and Output Capacitor Requirements* section for more details. |
| NR/SS | 13 | — | Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, TI recommends a 10-nF or larger capacitor to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance; see the *Noise-Reduction and Soft-Start Capacitor* section for more details. |
| OUT | 1, 19, 20 | O | Regulated output pin. A 22-µF or larger ceramic capacitor (10 µF or greater of capacitance) from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load; see the *Input and Output Capacitor Requirements* section for more details. |
| PG | 4 | O | Active-high, power-good pin. An open-drain output indicates when the output voltage reaches $V_{IT(PG)}$ of the target. The use of a feed-forward capacitor can disrupt PG (power-good) functionality; see the *Power-Good (PG) Function* section for more details. |
| SNS | 2 | I | Output voltage sense input pin. This pin connects the internal $R_1$ resistor to the output. Connect this pin to the load side of the output trace only if the ANY-OUT feature is used. If the ANY-OUT feature is not used, leave this pin floating; see the *ANY-OUT Programmable Output Voltage* and *Adjustable Operation* sections for more details. |
| Thermal pad | Pad | — | Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | IN, BIAS, PG, EN | –0.3 | 7.0 | V |
| | IN, BIAS, PG, EN (5% duty cycle, pulse duration = 200 µs) | –0.3 | 7.5 | |
| | SNS, OUT | –0.3 | $V_{IN}$ + 0.3(2) | |
| | NR/SS, FB | –0.3 | 3.6 | |
| | 50mV, 100mV, 200mV, 400mV, 800mV, 1.6V | –0.3 | $V_{OUT}$ + 0.3 | |
| Current | OUT | Internally limited | | A |
| | PG (sink current into device) | | 5 | mA |
| Operating junction temperature, $T_J$ | | –55 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is $V_{IN}$ + 0.3 V or 7.0 V, whichever is smaller.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage range | 1.1 | | 6.5 | V |
| $V_{BIAS}$ | BIAS supply voltage range(1) | 3.0 | | 6.5 | V |
| $V_{OUT}$ | Output voltage range(2) | 0.8 | | 5.2 | V |
| $V_{EN}$ | Enable voltage range | 0 | | $V_{IN}$ | V |
| $I_{OUT}$ | Output current | 0 | | 2 | A |
| $C_{IN}$ | Input capacitor | 10 | 22 | | µF |
| $C_{OUT}$ | Output capacitor | 22 | 22 | | µF |
| $C_{BIAS}$ | BIAS capacitor | 10 (3) | | | µF |
| $R_{PG}$ | Power-good pullup resistance | 10 | | 100 | kΩ |
| $C_{NR/SS}$ | NR/SS capacitor | | 10 | | nF |
| $C_{FF}$ | Feed-forward capacitor | | 10 | | nF |
| $R_1$ | Top resistor value in feedback network for adjustable operation | | 12.1(4) | | kΩ |
| $R_2$ | Bottom resistor value in feedback network for adjustable operation | | | 160(5) | kΩ |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) The BIAS supply is required when the $V_{IN}$ supply is below 1.4 V. Conversely, no BIAS supply is required when the $V_{IN}$ supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for $V_{IN} \leq 2.2$ V.
(2) This output voltage range does not include device accuracy or accuracy of the feedback resistors.
(3) If BIAS is used, a 10-µF capacitor is required. If BIAS is not used, a capacitor on the BIAS pin is not needed.
(4) The 12.1-kΩ resistor is selected to optimize PSRR and noise by matching the internal $R_1$ value.
(5) The upper limit for the $R_2$ resistor is to ensure accuracy by making the current through the feedback network much larger than the leakage current into the feedback node.

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TPS7A83A RGR (VQFN) 20 PINS | TPS7A83A RGW (VQFN) 20 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 43.4 | 33.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 36.8 | 24.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 17.6 | 13.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | 0.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 17.6 | 13 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.4 | 3.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating junction temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V(1), OUT connected to 50 Ω to GND(2), $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted); ypical values are at $T_J$ = 25°C

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage range (3) | | | 1.1 | | 6.5 | V |
| $V_{BIAS}$ | Bias supply voltage range (3) | | $V_{IN}$ = 1.1 V | 3.0 | | 6.5 | V |
| $V_{FB}$ | Feedback voltage | | | | 0.8 | | V |
| $V_{NR/SS}$ | NR/SS pin voltage | | | | 0.8 | | V |
| $V_{UVLO1(IN)}$ | Input supply UVLO with BIAS | | $V_{IN}$ rising with $V_{BIAS}$ = 3.0 V | | 1.02 | 1.085 | V |
| $V_{HYS1(IN)}$ | $V_{UVLO1(IN)}$ hysteresis | | $V_{BIAS}$ = 3.0 V | | 320 | | mV |
| $V_{UVLO2(IN)}$ | Input supply UVLO without BIAS | | $V_{IN}$ rising | | 1.31 | 1.39 | V |
| $V_{HYS2(IN)}$ | $V_{UVLO2(IN)}$ hysteresis | | | | 253 | | mV |
| $V_{UVLO(BIAS)}$ | Bias supply UVLO | | $V_{BIAS}$ rising, $V_{IN}$ = 1.1 V | | 2.83 | 2.9 | V |
| $V_{HYS(BIAS)}$ | $V_{UVLO(BIAS)}$ hysteresis | | $V_{IN}$ = 1.1 V | | 290 | | mV |
| $V_{OUT}$ | Output voltage | Range | Using the ANY-OUT pins | 0.8 – 1.0% | | 3.95 + 1.0% | V |
| | | | Using external resistors (4) | 0.8 – 1.0% | | 5.2 + 1.0% | |
| | | Accuracy (4) (5) | 0.8 V ≤ $V_{OUT}$ ≤ 5.2 V,<br>5 mA ≤ $I_{OUT}$ ≤ 2 A, 1.4 V ≤ $V_{IN}$ ≤ 6.5 V | –1.0% | | 1.0% | |
| | | Accuracy with BIAS | 1.1V ≤ $V_{IN}$ ≤ 2.2 V, 0.8V ≤ $V_{OUT}$ ≤ 1.9 V,<br>5 mA ≤ $I_{OUT}$ ≤ 2 A, 3.0 V ≤ $V_{BIAS}$ ≤ 6.5 V | –0.75% | | 0.75% | |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | | $I_{OUT}$ = 5 mA, 1.4 V ≤ $V_{IN}$ ≤ 6.5 V | | 0.03 | | mV/V |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | | 5 mA ≤ $I_{OUT}$ ≤ 2 A, 3.0 V ≤ $V_{BIAS}$ ≤ 6.5 V,<br>$V_{IN}$ = 1.1 V | | 0.07 | | mV/A |
| | | | 5 mA ≤ $I_{OUT}$ ≤ 2 A | | 0.08 | | |
| | | | 5 mA ≤ $I_{OUT}$ ≤ 2 A, $V_{OUT}$ = 5.2 V | | 0.04 | | |
| $V_{DO}$ | Dropout voltage | | $V_{IN}$ = 1.4 V, $I_{OUT}$ = 2 A, $V_{FB}$ = 0.8 V – 3% | | | 200 | mV |
| | | | $V_{IN}$ = 1.1 V, $V_{BIAS}$ = 5 V,<br>$I_{OUT}$ = 2 A, $V_{FB}$ = 0.8 V – 3% | | | 125 | |
| | | | $V_{IN}$ = 5.3 V, $I_{OUT}$ = 2 A, $V_{FB}$ = 0.8V – 0.3% | | | 200 | mV |
| | | | $V_{IN}$ = 5.5 V, $I_{OUT}$ = 2 A, $V_{FB}$ = 0.8V – 0.3% | | | 300 | |

(1) $V_{OUT(nom)}$ is the calculated $V_{OUT}$ target value from the ANY-OUT in a fixed configuration. In an adjustable configuration, $V_{OUT(nom)}$ is the expected $V_{OUT}$ value set by the external feedback resistors.
(2) This 50-Ω load is disconnected when the test conditions specify an $I_{OUT}$ value.
(3) The BIAS supply is required when the $V_{IN}$ supply is below 1.4 V. Conversely, no BIAS supply is required when the $V_{IN}$ supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for $V_{IN}$ ≤ 2.2 V.
(4) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(5) The device is not tested under conditions where $V_{IN}$ > $V_{OUT}$ + 2.5 V and $I_{OUT}$ = 2 A because the power dissipation is higher than the maximum rating of the package.

## Electrical Characteristics (continued)

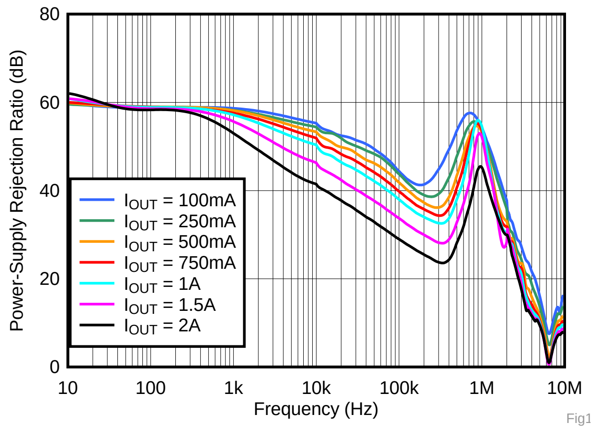
over operating junction temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V(1), OUT connected to 50 Ω to GND(2), $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted); ypical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{LIM}$ | Output current limit | $V_{OUT}$ forced at 0.9 × $V_{OUT(nom)}$,<br>$V_{IN}$ = $V_{OUT(nom)}$ + 0.4 V | | 2.8 | 3.3 | 3.8 | A |
| $I_{SC}$ | Short-circuit current limit | $R_{LOAD}$ = 20 mΩ | | | 1.0 | | A |
| $I_{GND}$ | GND pin current | $V_{IN}$ = 6.5 V, $I_{OUT}$ = 5 mA | | | 2.8 | 4 | mA |
| | | $V_{IN}$ = 1.4 V, $I_{OUT}$ = 2 A | | | 3.7 | 5 | mA |
| | | Shutdown, PG = open, $V_{IN}$ = 6.5 V, $V_{EN}$ = 0.5 V | | | | 25 | µA |
| $I_{EN}$ | EN pin current | $V_{IN}$ = 6.5 V, $V_{EN}$ = 0 V and 6.5 V | | –0.1 | | 0.1 | µA |
| $I_{BIAS}$ | BIAS pin current | $V_{IN}$ = 1.1 V, $V_{BIAS}$ = 6.5 V,<br>$V_{OUT(nom)}$ = 0.8 V, $I_{OUT}$ = 2 A | | | 2.3 | 3.5 | mA |
| $V_{IL(EN)}$ | EN pin low-level input voltage (disable device) | | | 0 | | 0.5 | V |
| $V_{IH(EN)}$ | EN pin high-level input voltage (enable device) | | | 1.1 | | 6.5 | V |
| $V_{IT(PG)}$ | PG pin threshold | For falling $V_{OUT}$ | | 82% × $V_{OUT}$ | 88% × $V_{OUT}$ | 93% × $V_{OUT}$ | V |
| $V_{HYS(PG)}$ | PG pin hysteresis | For rising $V_{OUT}$ | | | 2% × $V_{OUT}$ | | V |
| $V_{OL(PG)}$ | PG pin low-level output voltage | $V_{OUT}$ < $V_{IT(PG)}$, $I_{PG}$ = –1 mA (current into device) | | | | 0.4 | V |
| $I_{lkg(PG)}$ | PG pin leakage current | $V_{OUT}$ > $V_{IT(PG)}$, $V_{PG}$ = 6.5 V | | | | 1 | µA |
| $I_{NR/SS}$ | NR/SS pin charging current | $V_{NR/SS}$ = GND, $V_{IN}$ = 6.5 V | | 4.0 | 6.2 | 9.0 | µA |
| $I_{FB}$ | FB pin leakage current | $V_{IN}$ = 6.5 V | | –100 | | 100 | nA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ – $V_{OUT}$ = 0.4 V,<br>$I_{OUT}$ = 2 A, $C_{NR/SS}$ = 100 nF,<br>$C_{FF}$ = 10 nF,<br>$C_{OUT}$ = 22 µF | f = 10 kHz,<br>$V_{OUT}$ = 0.8 V,<br>$V_{BIAS}$ = 5.0 V | | 42 | | dB |
| | | | f = 500 kHz,<br>$V_{OUT}$ = 0.8 V,<br>$V_{BIAS}$ = 5.0 V | | 39 | | |
| | | | f = 10 kHz,<br>$V_{OUT}$ = 5.0 V | | 40 | | |
| | | | f = 500 kHz,<br>$V_{OUT}$ = 5.0 V | | 25 | | |
| $V_n$ | Output noise voltage | BW = 10 Hz to 100 kHz, $V_{IN}$ = 1.1 V,<br>$V_{OUT}$ = 0.8 V, $V_{BIAS}$ = 5.0 V, $I_{OUT}$ = 2 A,<br>$C_{NR/SS}$ = 100 nF, $C_{FF}$ = 10 nF,<br>$C_{OUT}$ = 22 µF | | | 4.4 | | $µV_{RMS}$ |
| | | BW = 10 Hz to 100 kHz,<br>$V_{OUT}$ = 5.0 V, $I_{OUT}$ = 2 A, $C_{NR/SS}$ = 100 nF,<br>$C_{FF}$ = 10 nF, $C_{OUT}$ = 22 µF | | | 7.7 | | |
| $T_{sd}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | | 160 | | °C |
| | | Reset, temperature decreasing | | | 140 | | |
| $T_J$ | Operating junction temperature | | | –40 | | 125 | °C |

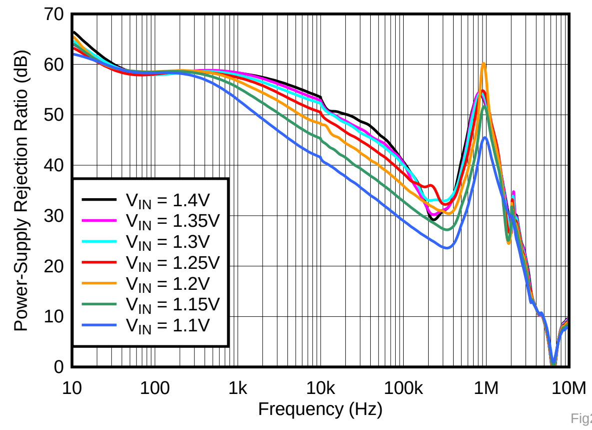
## 6.6 Typical Characteristics

at $T_A$ = 25°C, $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V, $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted)



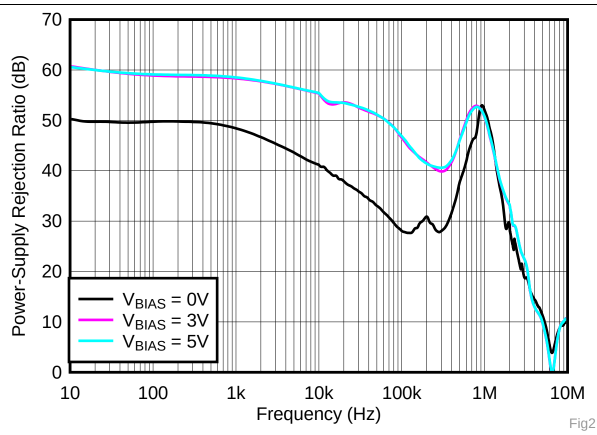

$V_{IN}$ = 1.1 V, $V_{BIAS}$ = 5 V,
$C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF

**图 1. PSRR vs Frequency and $I_{OUT}$**



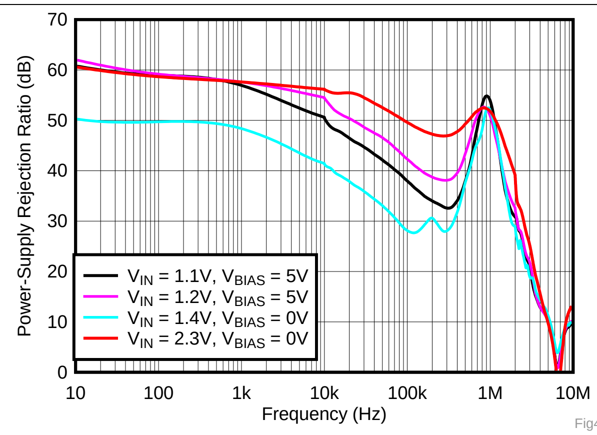

$I_{OUT}$ = 2 A, $V_{BIAS}$ = 5 V,
$C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF

**图 2. PSRR vs Frequency and $V_{IN}$ With BIAS**



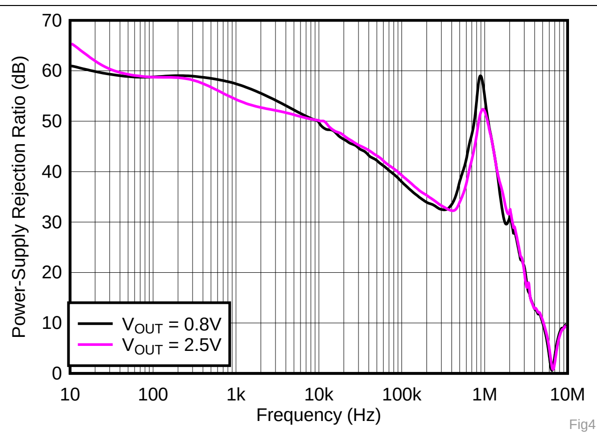

$V_{IN}$ = 1.4 V, $I_{OUT}$ = 1 A,
$C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF

**图 3. PSRR vs Frequency and $V_{BIAS}$**



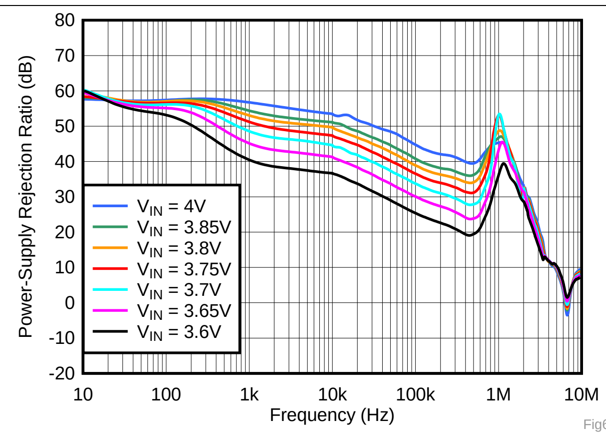

$I_{OUT}$ = 1 A,
$C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF

**图 4. PSRR vs Frequency and $V_{IN}$**




$V_{IN}$ = $V_{OUT}$ + 0.3 V, $V_{BIAS}$ = 5 V, $I_{OUT}$ = 2 A,
$C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF

**图 5. PSRR vs Frequency and $V_{OUT}$ With BIAS**

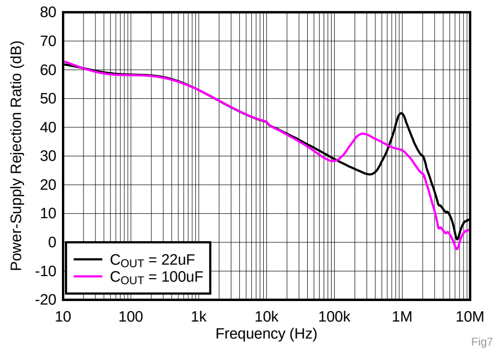



$I_{OUT}$ = 2 A, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF,
$C_{FF}$ = 10 nF

**图 6. PSRR vs Frequency and $V_{IN}$ for $V_{OUT}$ = 3.3 V**

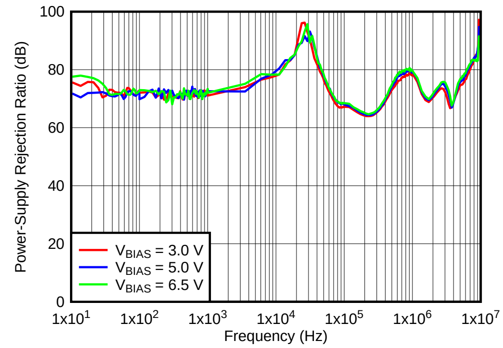
## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V, $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted)



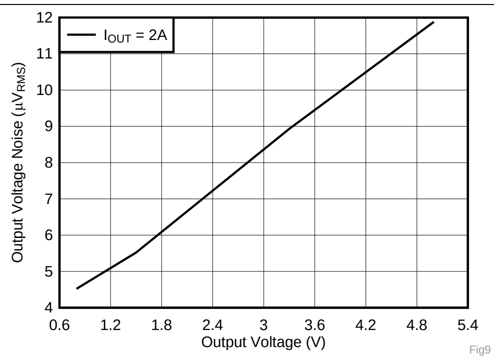

$V_{IN}$ = $V_{OUT}$ + 0.3 V, $V_{OUT}$ = 1 V, $V_{BIAS}$ = 5 V, $I_{OUT}$ = 2 A, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF

**图 7. PSRR vs Frequency and $C_{OUT}$**



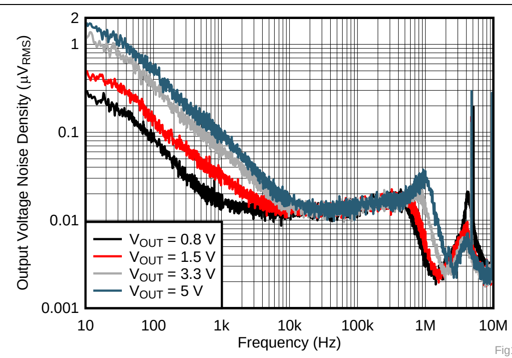

$V_{IN}$ = $V_{OUT}$ + 0.3 V, $V_{OUT}$ = 1 V, $I_{OUT}$ = 2 A, $C_{OUT}$ = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF

**图 8. $V_{BIAS}$ PSRR vs Frequency**



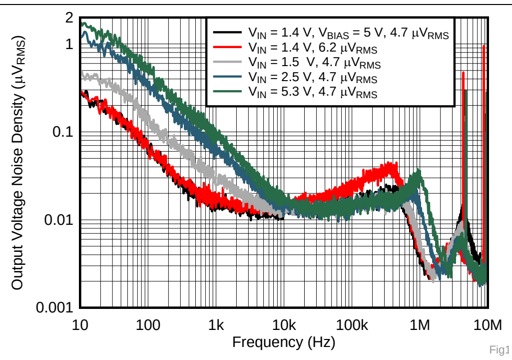

$V_{IN}$ = $V_{OUT}$ + 0.3 V and $V_{BIAS}$ = 5 V for $V_{OUT}$ ≤ 2.2 V, $C_{OUT}$ = 22 µF, $C_{BIAS}$ = 10 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF, RMS noise BW = 10 Hz to 100 kHz

**图 9. Output Voltage Noise vs Output Voltage**



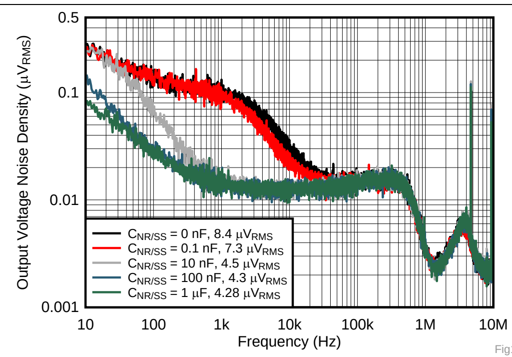

$V_{IN}$ = $V_{OUT}$ + 0.3 V and $V_{BIAS}$ = 5 V for $V_{OUT}$ ≤ 2.2 V, $I_{OUT}$ = 2 A, $C_{OUT}$ = 22 µF, $C_{BIAS}$ = 10 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF, RMS noise BW = 10 Hz to 100 kHz

**图 10. Output Noise vs Frequency and Output Voltage**




$I_{OUT}$ = 2 A, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 10 nF, $C_{FF}$ = 10 nF, RMS noise BW = 10 Hz to 100 kHz

**图 11. Output Noise vs Frequency and Input Voltage**

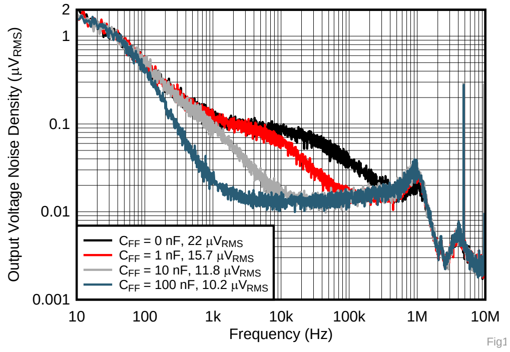



$V_{IN}$ = 1.1V, $V_{OUT}$ = 0.8V, $V_{BIAS}$ = 5 V, $I_{OUT}$ = 2 A, $C_{OUT}$ = 22 µF, $C_{BIAS}$ = 10 µF, $C_{FF}$ = 10 nF, RMS noise BW = 10 Hz to 100 kHz

**图 12. Output Noise vs Frequency and $C_{NR/SS}$**

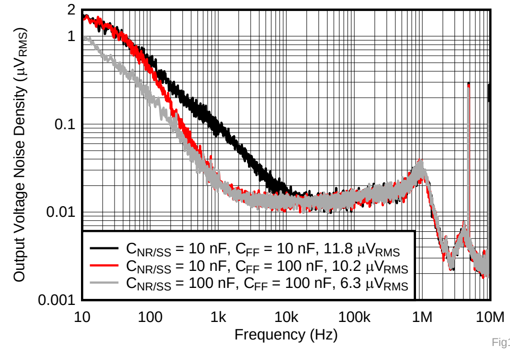
## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V, $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted)



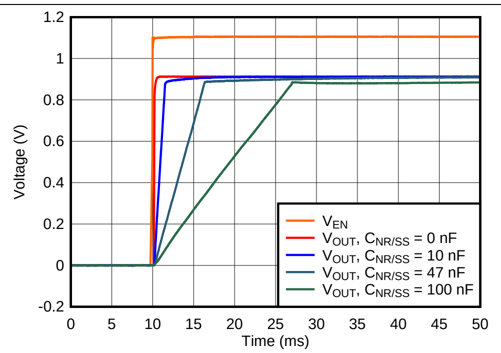

$V_{IN}$ = 5.3V, $V_{OUT}$ = 5V, $V_{BIAS}$ = 5 V, $I_{OUT}$ = 2 A, $C_{OUT}$ = 22 µF, $C_{BIAS}$ = 10 µF, $C_{NR/SS}$ = 10 nF, RMS noise BW = 10 Hz to 100 kHz

**图 13. Output Noise vs Frequency and $C_{FF}$**



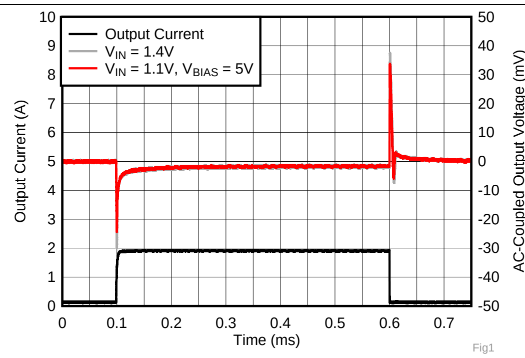

$I_{OUT}$ = 2 A, $C_{OUT}$ = 22 µF, $C_{FF}$ = 10 nF, RMS noise BW = 10 Hz to 100 kHz

**图 14. Output Noise at 5-V Output**



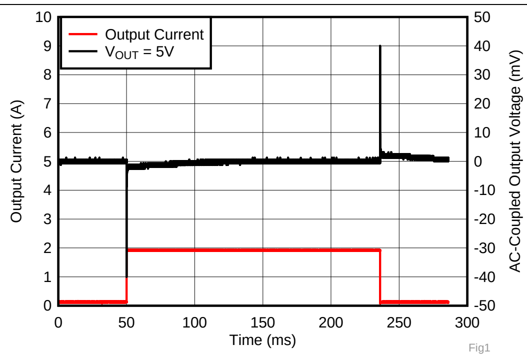

$V_{IN}$ = 1.2 V, $V_{OUT}$ = 0.9 V, $V_{BIAS}$ = 5 V, $I_{OUT}$ = 2 A, $C_{OUT}$ = 22 µF, $C_{BIAS}$ = 10 µF, $C_{FF}$ = 10 nF

**图 15. Start-Up Waveform vs Time and $C_{NR/SS}$**



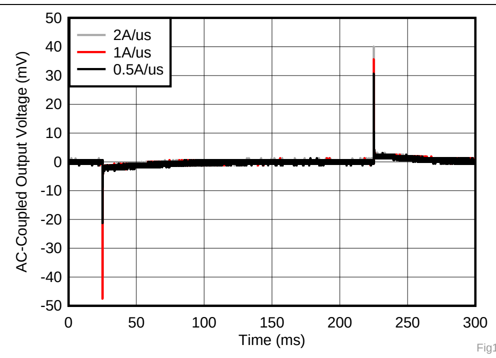

$I_{OUT,\ DC}$ = 100 mA, slew rate = 1 A/µs, $C_{NR/SS}$ = 10 nF, $C_{OUT}$ = 22 µF, $C_{BIAS}$ = 10 µF

**图 16. Load Transient vs Time for $V_{OUT}$ = 0.8 V**




$I_{OUT,\ DC}$ = 100 mA, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = $C_{FF}$ = 10 nF, slew rate = 1 A/µs

**图 17. Load Transient vs Time for $V_{OUT}$ = 5 V**

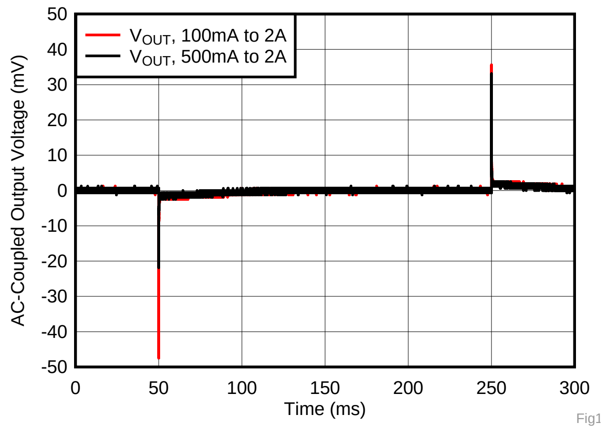



$V_{OUT}$ = 5 V, $I_{OUT,\ DC}$ = 100 mA, $I_{OUT}$ = 100 mA to 2 A, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = $C_{FF}$ = 10 nF

**图 18. Load Transient vs Time and Slew Rate**

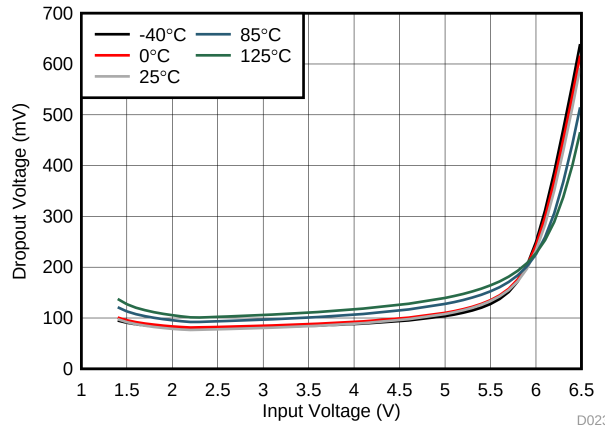
## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V, $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted)



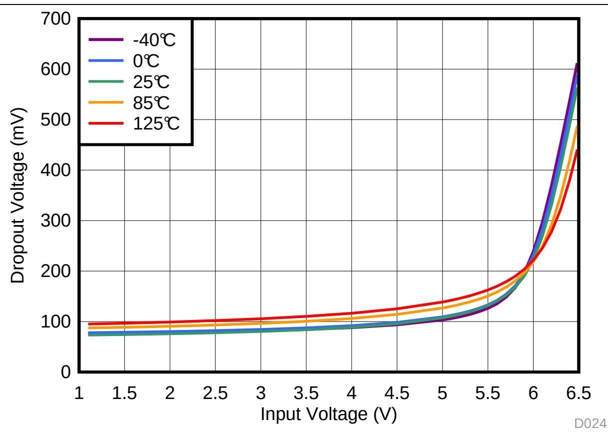

$V_{IN}$ = 5.3 V, $V_{BIAS}$ = 5 V, $C_{OUT}$ = 22 µF, $C_{BIAS}$ = 10 µF, $V_{OUT}$ = 5 V, $C_{NR/SS}$ = $C_{FF}$ = 10 nF, slew rate = 1 A/µs

**图 19. Load Transient vs Time and DC Load**



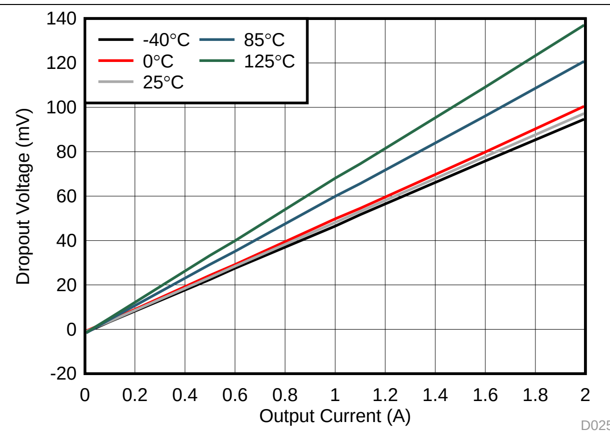

$I_{OUT}$ = 2 A

**图 20. Dropout Voltage vs Input Voltage Without BIAS**



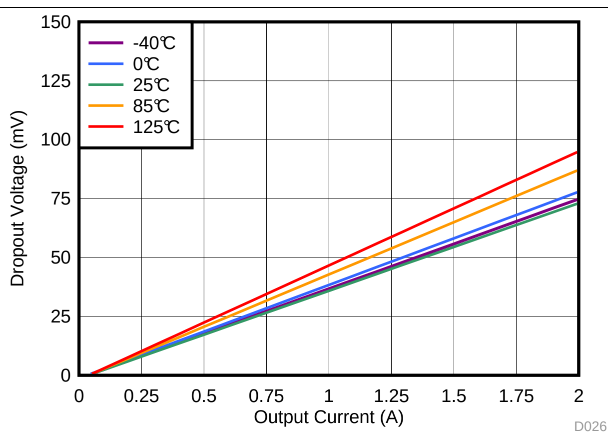

$I_{OUT}$ = 2 A, $V_{BIAS}$ = 6.5 V

**图 21. Dropout Voltage vs Input Voltage With BIAS**



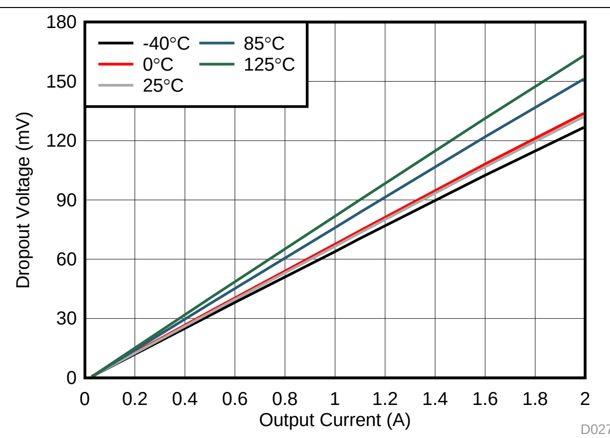

$V_{IN}$ = 1.4 V

**图 22. Dropout Voltage vs Output Current Without BIAS**




$V_{IN}$ = 1.1 V, $V_{BIAS}$ = 3 V

**图 23. Dropout Voltage vs Output Current With BIAS**

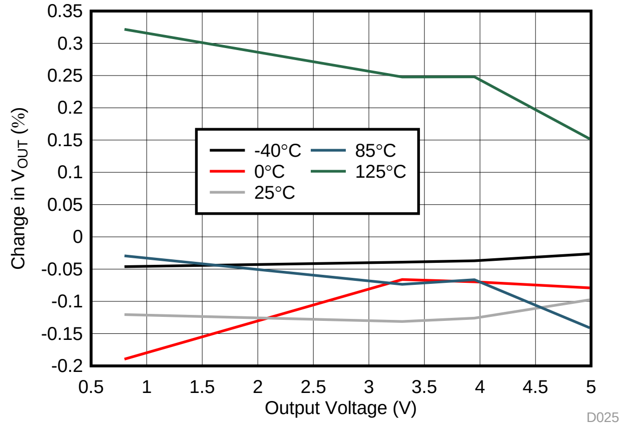



$V_{IN}$ = 5.5 V

**图 24. Dropout Voltage vs Output Current (High $V_{IN}$)**

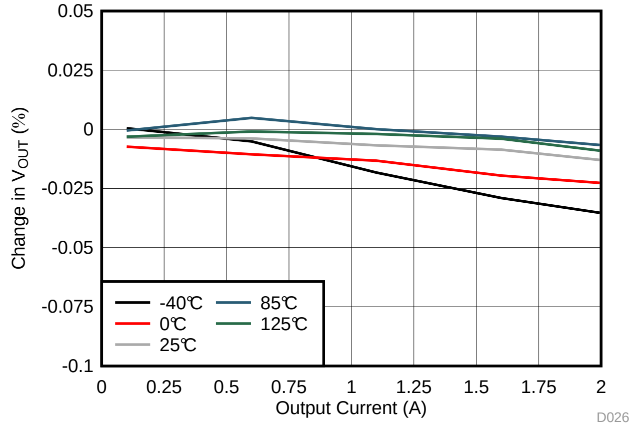
## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V, $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted)



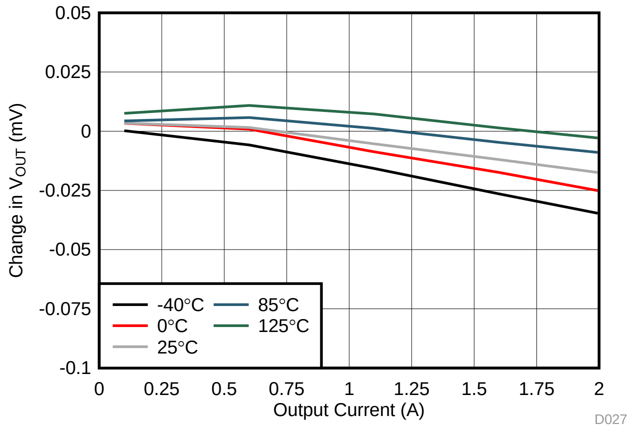

$I_{OUT}$ = 100 mA to 2 A

**图 25. Load Regulation vs Output Voltage**



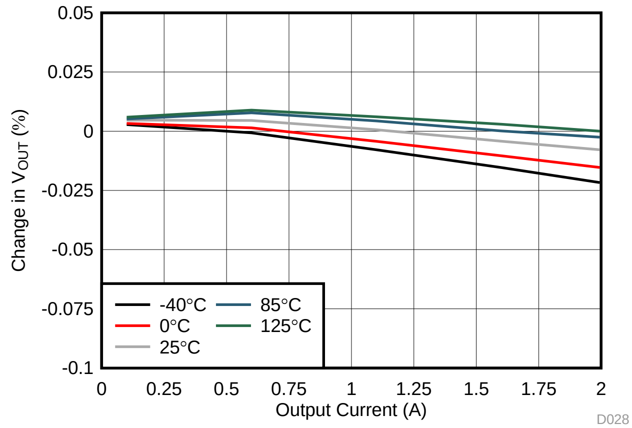

$V_{IN}$ = 1.4 V

**图 26. Load Regulation**



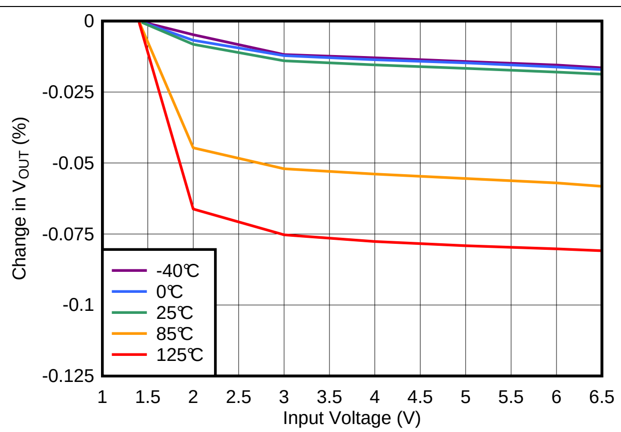

$V_{IN}$ = 3.8 V

**图 27. Load Regulation (3.3-V Output)**



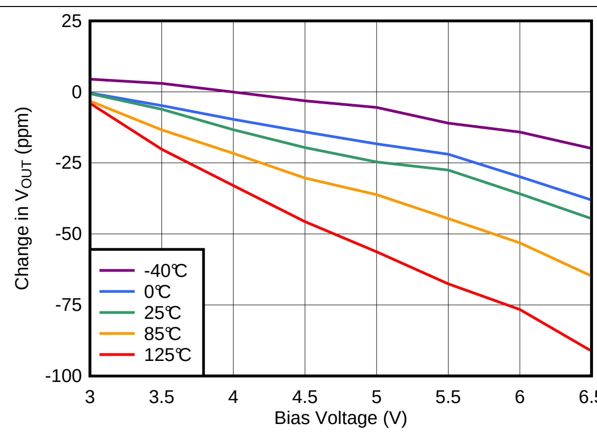

$V_{IN}$ = 5.5 V

**图 28. Load Regulation (5-V Output)**




$V_{OUT}$ = 0.8 V, $I_{OUT}$ = 5 mA

**图 29. Line Regulation**




$V_{OUT}$ = 0.8 V, $V_{IN}$ = 1.1 V, $I_{OUT}$ = 5 mA, $V_{BIAS}$ = 5 V

**图 30. Line Regulation With BIAS**

## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V, $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted)

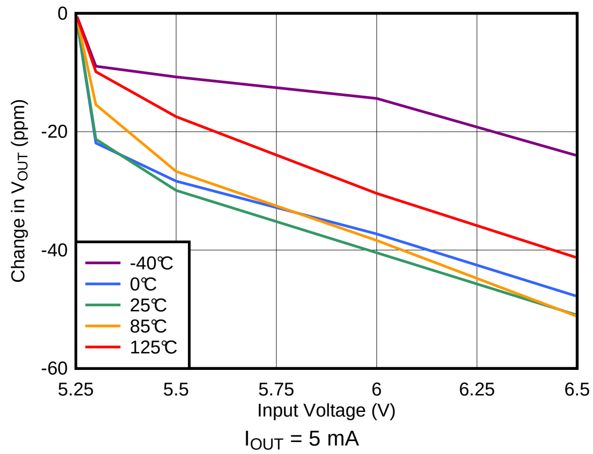



图 31. Line Regulation (5-V Output)

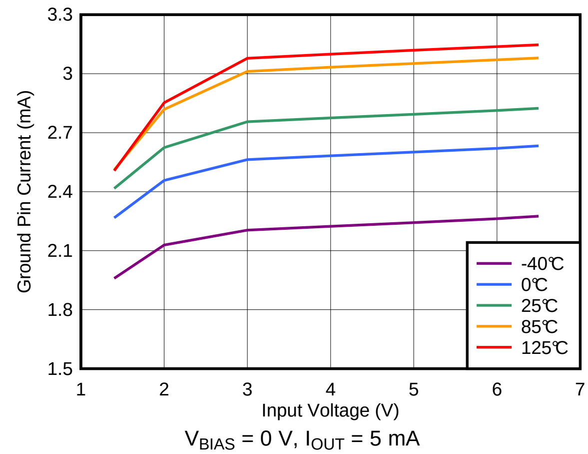



图 32. Ground Pin Current vs Input Voltage

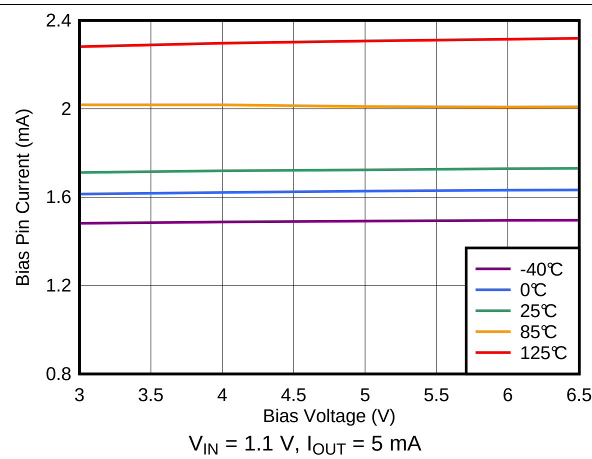



图 33. BIAS Pin Current vs Bias Voltage

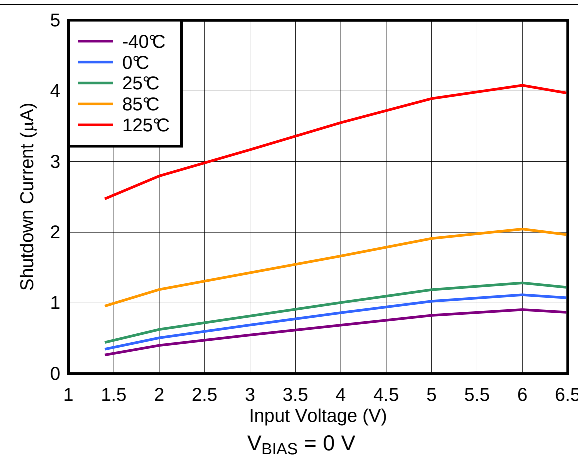



图 34. Shutdown Current vs Input Voltage

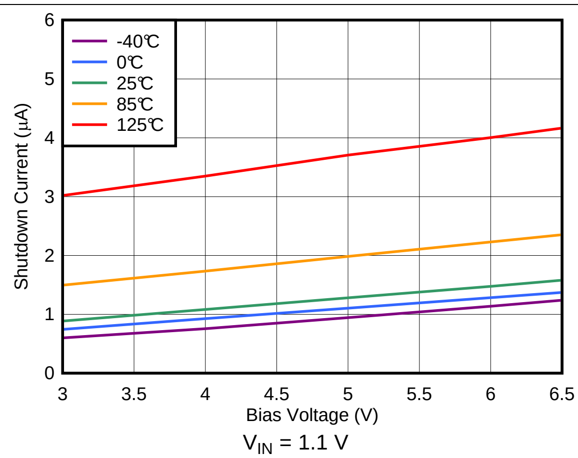



图 35. Shutdown Current vs Bias Voltage

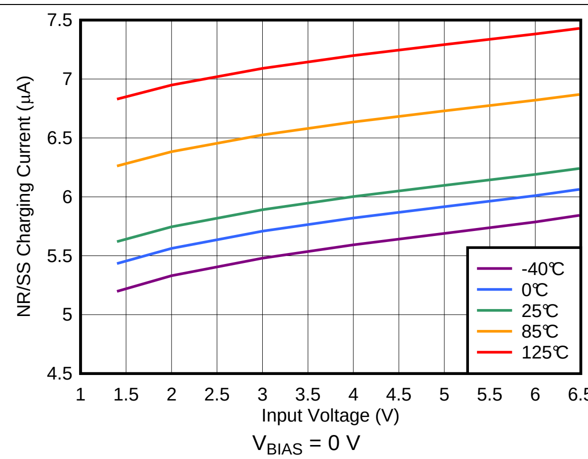



图 36. $I_{NR/SS}$ Current vs Input Voltage

## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_{IN}$ = 1.4 V or $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V (whichever is greater), $V_{BIAS}$ = open, $V_{OUT(nom)}$ = 0.8 V, $V_{EN}$ = 1.1 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 22 µF, $C_{NR/SS}$ = 0 nF, $C_{FF}$ = 0 nF, and PG pin pulled up to $V_{IN}$ with 100 kΩ (unless otherwise noted)

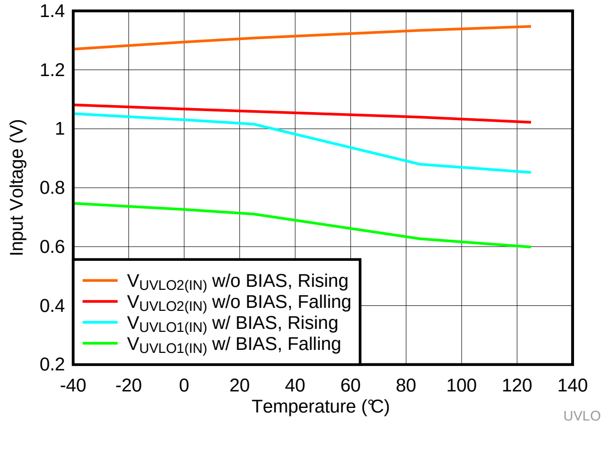



图 37. $V_{IN}$ UVLO vs Temperature

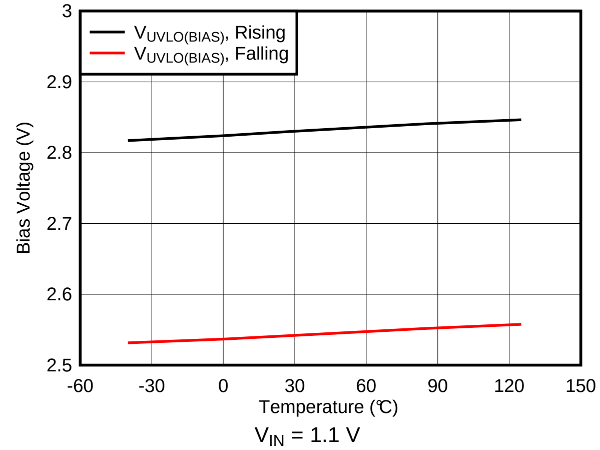



图 38. $V_{BIAS}$ UVLO vs Temperature

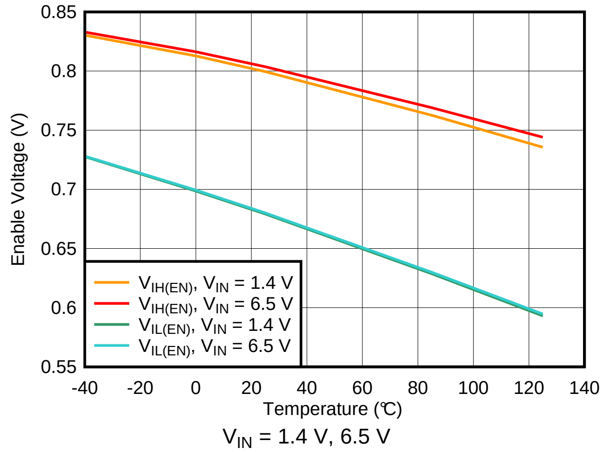



图 39. Enable Threshold vs Temperature

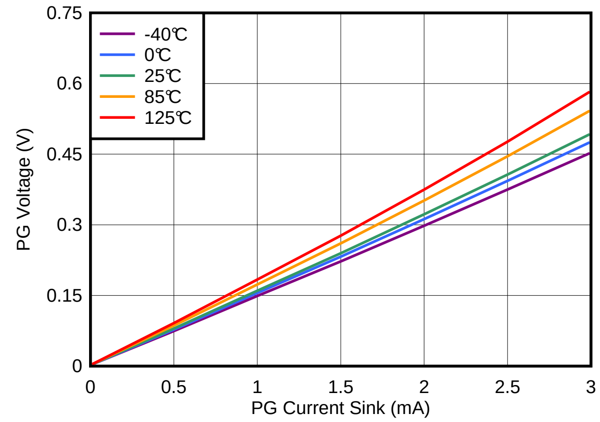



图 40. PG Voltage vs PG Current Sink

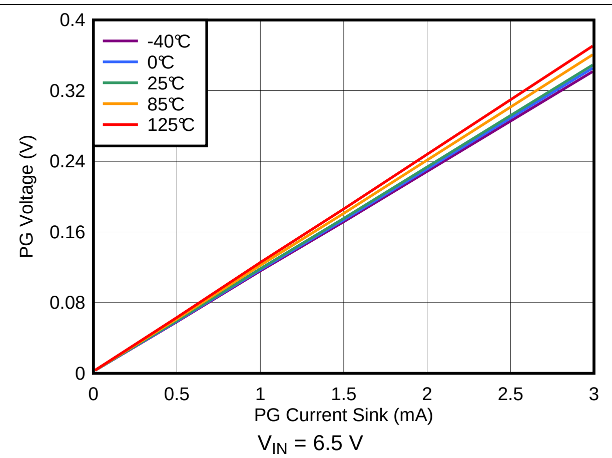



图 41. PG Voltage vs PG Current Sink

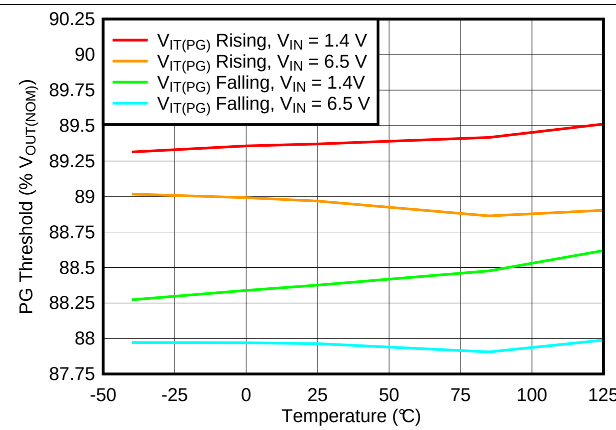



图 42. PG Threshold vs Temperature

# 7 Detailed Description

## 7.1 Overview

The TPS7A83A is a high-current (2 A), low-noise (4.4 $\mu V_{RMS}$), high-accuracy (0.75%), low-dropout linear voltage regulator (LDO). These features make the device a robust solution to solve many challenging problems in generating a clean, accurate power supply.

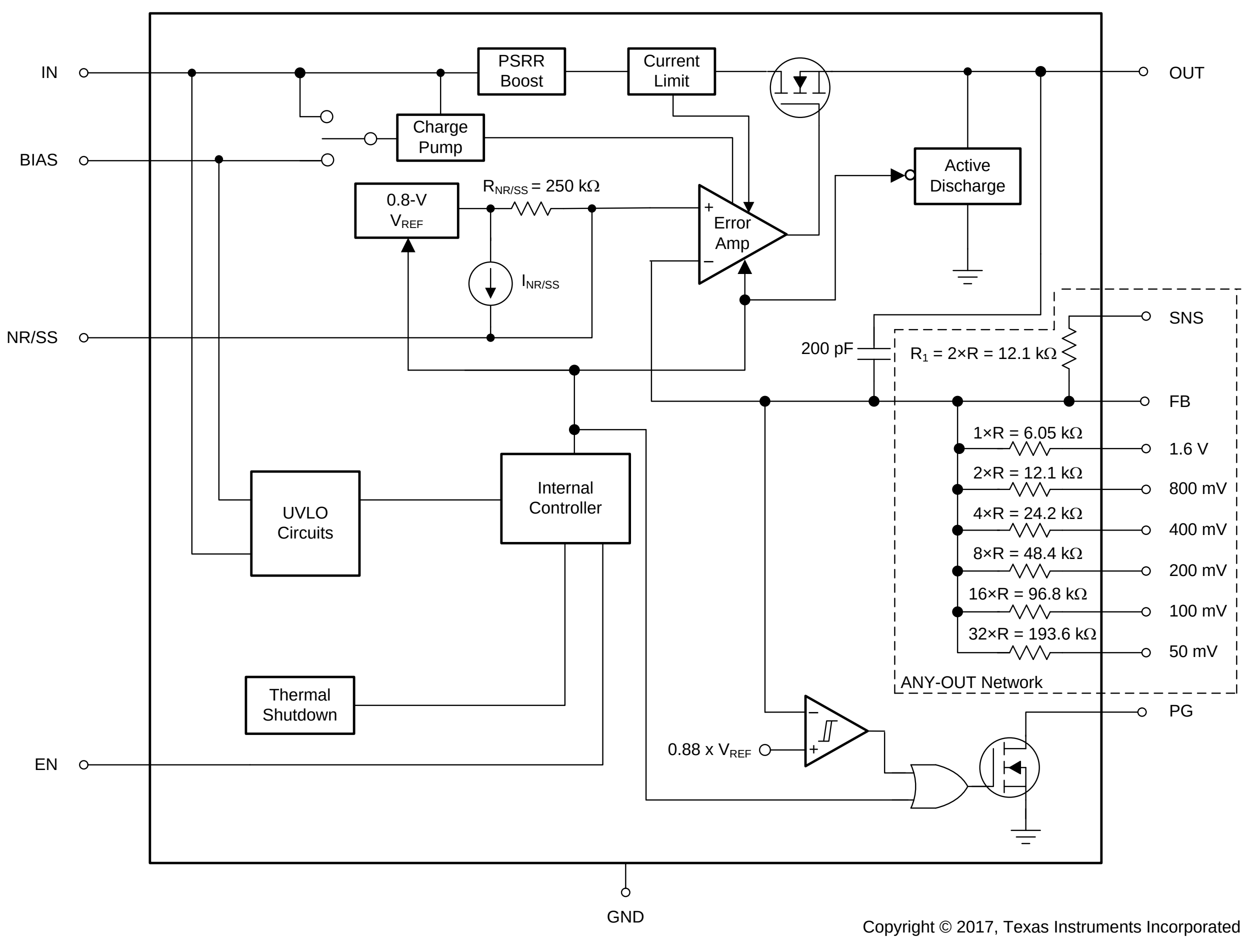
The TPS7A83A has several features that make the device useful in a variety of applications. 表 1 categorizes the functionalities shown in the *Functional Block Diagram* section.

**表 1. Features**

| VOLTAGE REGULATION | SYSTEM START-UP | INTERNAL PROTECTION |
|---|---|---|
| High accuracy | Programmable soft-start | Foldback current limit |
| Low-noise, high-PSRR output | No sequencing requirement between BIAS, IN, and EN | Thermal shutdown |
| Fast transient response | Power-good output | |
| | Start-up with negative bias on OUT | |

Overall, these features make the TPS7A83A the component of choice because of the versatility and ability of the device to generate a supply for most applications.

## 7.2 Functional Block Diagram






NOTE: For the ANY-OUT network, the ratios between the values are highly accurate as a result of matching, but the actual resistance can vary significantly from the numbers listed.

## 7.3 Feature Description

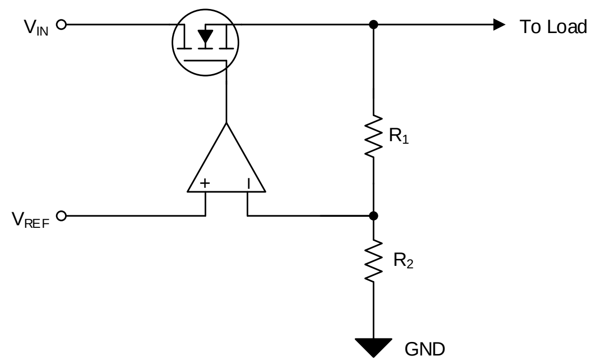
### 7.3.1 Voltage Regulation Features

#### *7.3.1.1 DC Regulation*

As 图 43 shows, an LDO functions as a class-B amplifier in which the input signal is the internal reference voltage ($V_{REF}$). $V_{REF}$ is designed to have a very low bandwidth at the input to the error amplifier through the use of a low-pass filter ($V_{NR/SS}$).

As such, the reference can be considered as a pure dc input signal. The low output impedance of an LDO comes from the combination of the output capacitor and pass element. The pass element also presents a high input impedance to the source voltage when operating as a current source. A positive LDO can only source current because of the class-B architecture.

This device achieves a maximum of 0.75% output voltage accuracy primarily because of the high-precision band-gap voltage ($V_{BG}$) that creates $V_{REF}$. The low dropout voltage ($V_{DO}$) reduces the thermal power dissipation required by the device to regulate the output voltage at a given current level, thereby improving system efficiency. These features combine to make this device a good approximation of an ideal voltage source.




NOTE: $V_{OUT} = V_{REF} \times (1 + R_1 / R_2)$.

**图 43. Simplified Regulation Circuit**

#### *7.3.1.2 AC and Transient Response*

The LDO responds quickly to a transient (large-signal response) on the input supply (line transient) or the output current (load transient) resulting from the LDO high-input impedance and low output-impedance across frequency. This same capability also means that the LDO has a high power-supply rejection ratio (PSRR) and, when coupled with a low internal noise-floor ($e_n$), the LDO approximates an ideal power supply in ac (small-signal) and large-signal conditions.

The choice of external component values optimizes the small- and large-signal response. The NR/SS capacitor ($C_{NR/SS}$) and feed-forward capacitor ($C_{FF}$) easily reduce the device noise floor and improve PSRR; see *Optimizing Noise and PSRR* for more information on optimizing the noise and PSRR performance.

### 7.3.2 System Start-Up Features

In many different applications, the power-supply output must turn on within a specific window of time to either ensure proper operation of the load or to minimize the loading on the input supply or other sequencing requirements. The LDO start-up is well-controlled and user-adjustable, solving the demanding requirements faced by many power-supply design engineers in a simple fashion.

## Feature Description (接下页)

### *7.3.2.1 Programmable Soft-Start (NR/SS)*

Soft-start directly controls the output start-up time and indirectly controls the output current during start-up (in-rush current).

图 44 shows that the external capacitor at the NR/SS pin ($C_{NR/SS}$) sets the output start-up time by setting the rise time of the internal reference ($V_{NR/SS}$).

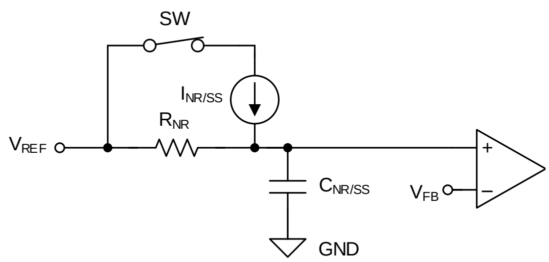



**图 44. Simplified Soft-Start Circuit**

### *7.3.2.2 Internal Sequencing*

Controlling when a single power supply turns on can be difficult in a power distribution network (PDN) because of the high power levels inherent in a PDN, and the variations between all of the supplies. 图 45 and 表 2 show how the LDO turnon and turnoff time are set by the enable circuit (EN) and undervoltage lockout circuits ($UVLO_{1,2(IN)}$ and $UVLO_{BIAS}$).

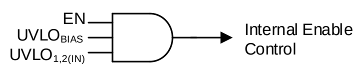



**图 45. Simplified Turnon Control**

**表 2. Internal Sequencing Functionality Table**

| INPUT VOLTAGE | BIAS VOLTAGE | ENABLE STATUS | LDO STATUS | ACTIVE DISCHARGE | POWER GOOD |
|---|---|---|---|---|---|
| $V_{IN} \geq V_{UVLO\_1,2(IN)}$ | $V_{BIAS} \geq V_{UVLO(BIAS)}$ | EN = 1 | On | Off | PG = 1 when $V_{OUT} \geq V_{IT(PG)}$ |
| | | EN = 0 | Off | On | PG = 0 |
| | $V_{BIAS} < V_{UVLO(BIAS)} + V_{HYS(BIAS)}$ | EN = don't care | Off | On (1) | |
| $V_{IN} < V_{UVLO\_1,2(IN)} - V_{HYS1,2(IN)}$ | BIAS = don't care | | Off | | |
| IN = don't care | $V_{BIAS} \geq V_{UVLO(BIAS)}$ | | Off | | |

(1) The active discharge remains on as long as $V_{IN}$ or $V_{BIAS}$ provide enough headroom for the discharge circuit to function.

#### 7.3.2.2.1 Enable (EN)

The enable signal ($V_{EN}$) is an active-high digital control that enables the LDO when the enable voltage is past the rising threshold ($V_{EN} \geq V_{IH(EN)}$) and disables the LDO when the enable voltage is below the falling threshold ($V_{EN} \leq V_{IL(EN)}$). The exact enable threshold is between $V_{IH(EN)}$ and $V_{IL(EN)}$ because EN is a digital control. Connect EN to $V_{IN}$ or $V_{BIAS}$ if enable functionality is not desired.

#### 7.3.2.2.2 Undervoltage Lockout (UVLO) Control

The UVLO circuits respond quickly to glitches on IN or BIAS and attempts to disable the output of the device if either of these rails collapse.

The local input capacitance prevents severe brownouts in most applications; see the *Undervoltage Lockout (UVLO)* section for more details.

#### 7.3.2.2.3 Active Discharge

When either EN or UVLO is low, the device connects a resistor of several hundred ohms from $V_{OUT}$ to GND, discharging the output capacitance.

Do not rely on the active discharge circuit for discharging large output capacitors when the input voltage drops below the targeted output voltage. Current flows from the output to the input (reverse current) when $V_{OUT} > V_{IN}$, which can cause damage to the device (when $V_{OUT} > V_{IN}$ + 0.3 V); see the *Reverse Current* section for more details.

### *7.3.2.3 Power-Good Output (PG)*

The PG signal provides an easy solution to meet demanding sequencing requirements because PG signals when the output nears the nominal value. PG can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUT(nom)}$). 图 46 shows a simplified schematic.

The PG signal is an open-drain digital output that requires a pullup resistor to a voltage source and is active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good.

Using a large feed-forward capacitor ($C_{FF}$) delays the output voltage and, because the PG circuit monitors the FB pin, the PG signal can indicate a false positive. A simple solution to this scenario is to use an external voltage detector device, such as the TPS3890; see the *Feed-Forward Capacitor ($C_{FF}$)* section for more information.

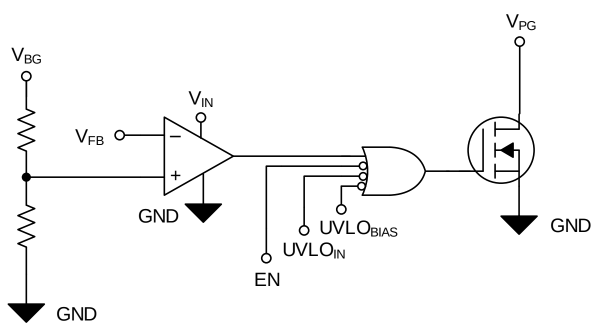



**图 46. Simplified PG Circuit**

## 7.3.3 Internal Protection Features

In many applications, fault events can occur that damage devices in the system. Short circuits and excessive heat are the most common fault events for power supplies. The TPS7A83A implements circuitry to protect the device and its load during these events. Continuously operating in these fault conditions or above a junction temperature of 125°C is not recommended because the long-term reliability of the device is reduced.

### *7.3.3.1 Foldback Current Limit ($I_{CL}$)*

The internal current limit circuit is used to protect the LDO against high load-current faults or shorting events. During a current-limit event, the LDO sources constant current; therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

#### 7.3.3.2 Thermal Protection ($T_{sd}$)

The thermal shutdown circuit protects the LDO against excessive heat in the system, either resulting from current limit or high ambient temperature.

The output of the LDO turns off when the LDO temperature (junction temperature, $T_J$) exceeds the rising thermal shutdown temperature. The output turns on again after $T_J$ decreases below the falling thermal shutdown temperature.

A high power dissipation across the device, combined with a high ambient temperature ($T_A$), can cause $T_J$ to be greater than or equal to $T_{sd}$, triggering the thermal shutdown and causing the output to fall to 0 V. The LDO can cycle on and off when thermal shutdown is reached under these conditions.

Continuously triggering thermal shutdown can degrade long-term reliability.

## 7.4 Device Functional Modes

表 3 provides a quick comparison between the regulation and disabled operation.

**表 3. Device Functional Modes Comparison**

| OPERATING MODE | PARAMETER | | | | |
|---|---|---|---|---|---|
| | $V_{IN}$ | $V_{BIAS}$ | EN | $I_{OUT}$ | $T_J$ |
| Regulation (1) | $V_{IN} > V_{OUT(nom)} + V_{DO}$ | $V_{BIAS} \geq V_{UVLO(BIAS)}$ (2) | $V_{EN} > V_{IH(EN)}$ | $I_{OUT} < I_{CL}$ | $T_J \leq T_{J(maximum)}$ |
| Disabled (3) | $V_{IN} < V_{UVLO\_1,2(IN)}$ | $V_{BIAS} < V_{UVLO(BIAS)}$ | $V_{EN} < V_{IL(EN)}$ | | $T_J > T_{sd}$ |
| Current-limit operation | | | | $I_{OUT} \geq I_{CL}$ | |

(1) All table conditions must be met.
(2) $V_{BIAS}$ is only required for $V_{IN} < 1.4$ V.
(3) The device is disabled when any condition is met.

### 7.4.1 Regulation

The device regulates the output to the nominal output voltage when all the conditions in 表 3 are met.

### 7.4.2 Disabled

When disabled, the pass device is turned off, the internal circuits are shut down, and the output voltage is actively discharged to ground by an internal resistor from the output to ground. See the *Active Discharge* section for additional information.

# 8 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

### 8.1.1 External Component Selection

#### *8.1.1.1 Adjustable Operation*

The TPS7A83A can be used either with the internal ANY-OUT network or by using external resistors. Using the ANY-OUT network allows the TPS7A83A to be programmed from 0.8 V to 3.95 V. For an output voltage range greater than 3.95 V and up to 5.2 V, external resistors must be used. This configuration is referred to as the adjustable configuration of the TPS7A83A throughout this document. 图 47 shows that the output voltage is set by two resistors. 0.75% accuracy can be achieved with an external BIAS for $V_{IN}$ lower than 2.2 V.

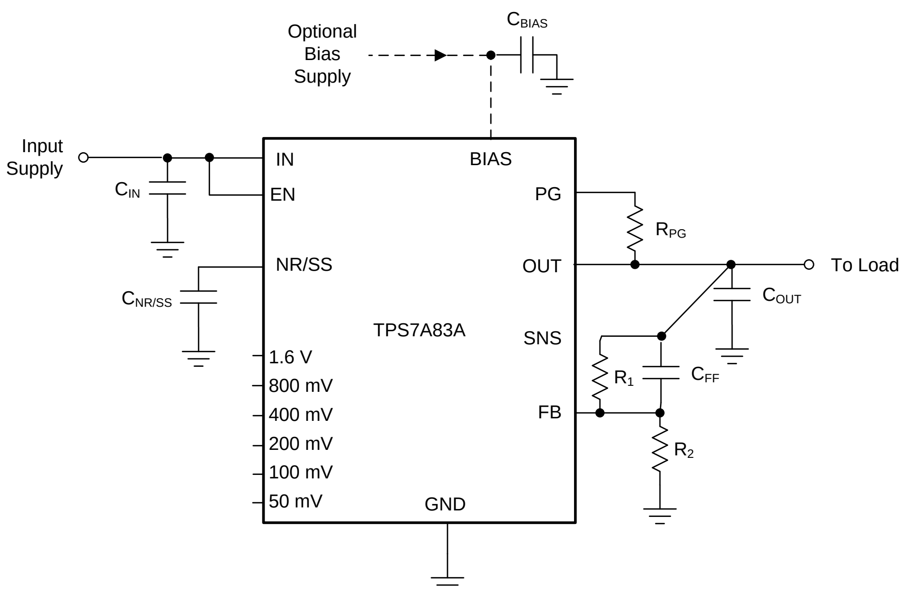



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**图 47. Adjustable Operation**

Use 公式 1 to calculate $R_1$ and $R_2$ for any output voltage range. This resistive network must provide a current equal to or greater than 5 µA for dc accuracy. TI recommends using an $R_1$ of approximately 12 kΩ to optimize the noise and PSRR.

$$V_{OUT} = V_{NR/SS} \times (1 + R_1 / R_2) \quad (1)$$

## Application Information (接下页)

表 4 shows the resistor combinations required to achieve several common rails using standard 1%-tolerance resistors.

**表 4. Recommended Feedback-Resistor Values(1)**

| NOMINAL OUTPUT VOLTAGE (V) | FEEDBACK RESISTOR VALUES | | CALCULATED OUTPUT VOLTAGE (V) |
|---|---|---|---|
| | $R_1$ (kΩ) | $R_2$ (kΩ) | |
| 0.90 | 12.4 | 100 | 0.899 |
| 0.95 | 12.4 | 66.5 | 0.949 |
| 1.00 | 12.4 | 49.9 | 0.999 |
| 1.10 | 12.4 | 33.2 | 1.099 |
| 1.20 | 12.4 | 24.9 | 1.198 |
| 1.50 | 12.4 | 14.3 | 1.494 |
| 1.80 | 12.4 | 10 | 1.798 |
| 1.90 | 12.1 | 8.87 | 1.890 |
| 2.50 | 12.4 | 5.9 | 2.480 |
| 2.85 | 12.1 | 4.75 | 2.838 |
| 3.00 | 12.1 | 4.42 | 2.990 |
| 3.30 | 11.8 | 3.74 | 3.324 |
| 3.60 | 12.1 | 3.48 | 3.582 |
| 4.50 | 11.8 | 2.55 | 4.502 |
| 5.00 | 12.4 | 2.37 | 4.985 |

(1) $R_1$ is connected from OUT to FB; $R_2$ is connected from FB to GND.

#### *8.1.1.2 ANY-OUT Programmable Output Voltage*

The TPS7A83A can use either external resistors or the internally-matched ANY-OUT feedback resistor network to set output voltage. The ANY-OUT resistors are accessible via pin 2 and pins 5 to 11 and are used to program the regulated output voltage. Each pin is can be connected to ground (active) or left open (floating), or connected to SNS. ANY-OUT programming is set by 公式 2 as the sum of the internal reference voltage ($V_{NR/SS}$ = 0.8 V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 50mV (pin 5), 100mV (pin 6), 200mV (pin 7), 400mV (pin 9), 800mV (pin 10), or 1.6V (pin 11). 表 5 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open or floating, the output is thereby programmed to the minimum possible output voltage equal to $V_{FB}$.

$$V_{OUT} = V_{NR/SS} + (\Sigma \text{ ANY-OUT Pins to Ground}) \quad (2)$$

**表 5. ANY-OUT Programmable Output Voltage (RGR package)**

| ANY-OUT PROGRAM PINS (Active Low) | ADDITIVE OUTPUT VOLTAGE LEVEL |
|---|---|
| Pin 5 (50mV) | 50 mV |
| Pin 6 (100mV) | 100 mV |
| Pin 7 (200mV) | 200 mV |
| Pin 9 (400mV) | 400 mV |
| Pin 10 (800mV) | 800 mV |
| Pin 11 (1.6V) | 1.6 V |

表 6 provides a full list of target output voltages and corresponding pin settings when the ANY-OUT pins are only tied to ground or left floating. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.8 V to 3.95 V in 50-mV steps when tying these pins to ground. There are several alternative ways to set the output voltage. The program pins can be driven using external general-purpose input/output pins (GPIOs), manually connected using 0-Ω resistors (or left open), or hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage. As with the adjustable operation, the output voltage is set according to 公式 3 except that $R_1$ and $R_2$ are internally integrated and matched for higher accuracy. Tying any of the ANY-OUT pins to SNS can increase the resolution of the internal feedback network by lowering the value of $R_1$; see the *Increasing ANY-OUT Resolution for LILO Conditions* section for additional information.

$$V_{OUT} = V_{NR/SS} \times (1 + R_1 / R_2) \tag{3}$$

**注**

For output voltages greater than 3.95 V, use a traditional adjustable configuration (see the *Adjustable Operation* section).

### 表 6. User-Configurable Output Voltage Settings

| $V_{OUT(NOM)}$ (V) | 50 mV | 100 mV | 200 mV | 400 mV | 800 mV | 1.6 V | $V_{OUT(NOM)}$ (V) | 50 mV | 100 mV | 200 mV | 400mV | 800mV | 1.6V |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.80 | Open | Open | Open | Open | Open | Open | 2.40 | Open | Open | Open | Open | Open | GND |
| 0.85 | GND | Open | Open | Open | Open | Open | 2.45 | GND | Open | Open | Open | Open | GND |
| 0.90 | Open | GND | Open | Open | Open | Open | 2.50 | Open | GND | Open | Open | Open | GND |
| 0.95 | GND | GND | Open | Open | Open | Open | 2.55 | GND | GND | Open | Open | Open | GND |
| 1.00 | Open | Open | GND | Open | Open | Open | 2.60 | Open | Open | GND | Open | Open | GND |
| 1.05 | GND | Open | GND | Open | Open | Open | 2.65 | GND | Open | GND | Open | Open | GND |
| 1.10 | Open | GND | GND | Open | Open | Open | 2.70 | Open | GND | GND | Open | Open | GND |
| 1.15 | GND | GND | GND | Open | Open | Open | 2.75 | GND | GND | GND | Open | Open | GND |
| 1.20 | Open | Open | Open | GND | Open | Open | 2.80 | Open | Open | Open | GND | Open | GND |
| 1.25 | GND | Open | Open | GND | Open | Open | 2.85 | GND | Open | Open | GND | Open | GND |
| 1.30 | Open | GND | Open | GND | Open | Open | 2.90 | Open | GND | Open | GND | Open | GND |
| 1.35 | GND | GND | Open | GND | Open | Open | 2.95 | GND | GND | Open | GND | Open | GND |
| 1.40 | Open | Open | GND | GND | Open | Open | 3.00 | Open | Open | GND | GND | Open | GND |
| 1.45 | GND | Open | GND | GND | Open | Open | 3.05 | GND | Open | GND | GND | Open | GND |
| 1.50 | Open | GND | GND | GND | Open | Open | 3.10 | Open | GND | GND | GND | Open | GND |
| 1.55 | GND | GND | GND | GND | Open | Open | 3.15 | GND | GND | GND | GND | Open | GND |
| 1.60 | Open | Open | Open | Open | GND | Open | 3.20 | Open | Open | Open | Open | GND | GND |
| 1.65 | GND | Open | Open | Open | GND | Open | 3.25 | GND | Open | Open | Open | GND | GND |
| 1.70 | Open | GND | Open | Open | GND | Open | 3.30 | Open | GND | Open | Open | GND | GND |
| 1.75 | GND | GND | Open | Open | GND | Open | 3.35 | GND | GND | Open | Open | GND | GND |
| 1.80 | Open | Open | GND | Open | GND | Open | 3.40 | Open | Open | GND | Open | GND | GND |
| 1.85 | GND | Open | GND | Open | GND | Open | 3.45 | GND | Open | GND | Open | GND | GND |
| 1.90 | Open | GND | GND | Open | GND | Open | 3.50 | Open | GND | GND | Open | GND | GND |
| 1.95 | GND | GND | GND | Open | GND | Open | 3.55 | GND | GND | GND | Open | GND | GND |
| 2.00 | Open | Open | Open | GND | GND | Open | 3.60 | Open | Open | Open | GND | GND | GND |
| 2.05 | GND | Open | Open | GND | GND | Open | 3.65 | GND | Open | Open | GND | GND | GND |
| 2.10 | Open | GND | Open | GND | GND | Open | 3.70 | Open | GND | Open | GND | GND | GND |
| 2.15 | GND | GND | Open | GND | GND | Open | 3.75 | GND | GND | Open | GND | GND | GND |
| 2.20 | Open | Open | GND | GND | GND | Open | 3.80 | Open | Open | GND | GND | GND | GND |
| 2.25 | GND | Open | GND | GND | GND | Open | 3.85 | GND | Open | GND | GND | GND | GND |
| 2.30 | Open | GND | GND | GND | GND | Open | 3.90 | Open | GND | GND | GND | GND | GND |
| 2.35 | GND | GND | GND | GND | GND | Open | 3.95 | GND | GND | GND | GND | GND | GND |

### 8.1.1.3 ANY-OUT Operation

Considering the use of the ANY-OUT internal network (where the unit resistance of 1R is equal to 6.05 kΩ, see the section) the output voltage is set as shown in 图 48 by grounding the appropriate control pins. When grounded, all control pins add a specific voltage on top of the internal reference voltage ($V_{NR/SS}$ = 0.8 V). Use 公式 4 and 公式 5 to calculate the output voltage. 图 48 and 图 49 show a 0.9-V output voltage, respectively, that provides an example of the circuit usage with and without BIAS voltage.

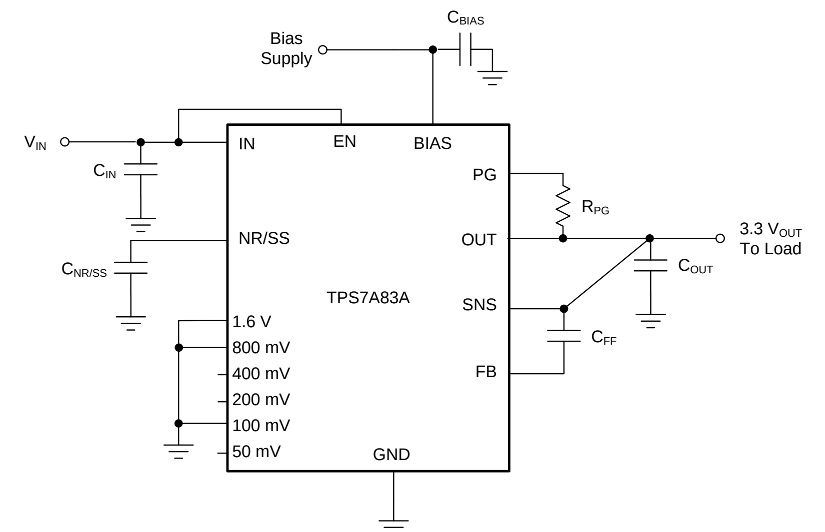


**图 48. ANY-OUT Configuration Circuit (3.3-V Output, No External BIAS)**

$$V_{OUT(nom)} = V_{NR/SS} + 1.6\text{ V} + 0.8\text{ V} + 0.1\text{ V} = 0.8\text{ V} + 1.6\text{ V} + 0.8\text{ V} + 0.1\text{ V} = 3.3\text{ V} \tag{4}$$

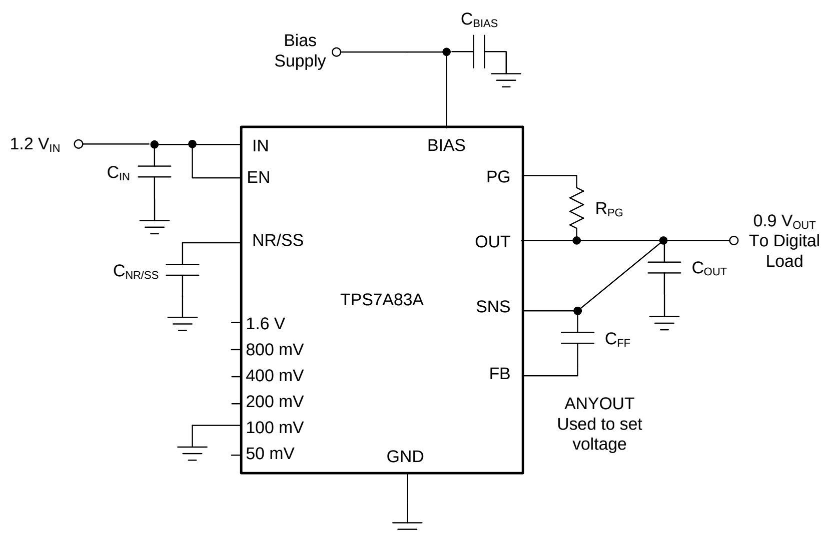


**图 49. ANY-OUT Configuration Circuit (0.9-V Output With BIAS)**

$$V_{OUT(nom)} = V_{NR/SS} + 0.1\text{ V} = 0.8\text{ V} + 0.1\text{ V} = 0.9\text{ V} \tag{5}$$

#### *8.1.1.4 Increasing ANY-OUT Resolution for LILO Conditions*

As with the adjustable operation, the output voltage is set according to 公式 3, except that $R_1$ and $R_2$ are internally integrated and matched for higher accuracy. Tying any of the ANY-OUT pins to SNS can increase the resolution of the internal feedback network by lowering the value of $R_1$. One of the more useful pin combinations is to tie the 800mV pin to SNS, which reduces the resolution by 50% to 25 mV but limits the range. The new ANY-OUT ranges are 0.8 V to 1.175 V and 1.6 V to 1.975 V. 表 7 lists the new additive output voltage levels.

**表 7. ANY-OUT Programmable Output Voltage With 800mV Tied to SNS (RGR Package)**

| ANY-OUT PROGRAM PINS (Active Low) | ADDITIVE OUTPUT VOLTAGE LEVEL |
|---|---|
| Pin 5 (50mV) | 25 mV |
| Pin 6 (100mV) | 50 mV |
| Pin 7 (200mV) | 100 mV |
| Pin 9 (400mV) | 200 mV |
| Pin 11 (1.6V) | 800 mV |

#### *8.1.1.5 Recommended Capacitor Types*

The TPS7A83A is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature; derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high $V_{IN}$ and $V_{OUT}$ conditions (for example, $V_{IN}$ = 5.6 V to $V_{OUT}$ = 5.2 V) the derating can be greater than 50% and must be taken into consideration.

#### *8.1.1.6 Input and Output Capacitor Requirements ($C_{IN}$ and $C_{OUT}$)*

The TPS7A83A is designed and characterized for operation with ceramic capacitors of 22 µF or greater (10 µF or greater of capacitance) at the output and 10 µF or greater (5 µF or greater of capacitance) at the input. Using at least a 22-µF capacitor is highly recommended at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins to minimize trace parasitic. If the trace inductance from the input supply to the TPS7A83A is high, a fast current transient can cause $V_{IN}$ to ring above the absolute maximum voltage rating and damage the device. This situation can be mitigated by additional input capacitors to dampen the ringing and to keep the ringing below the device absolute maximum ratings.

#### *8.1.1.7 Feed-Forward Capacitor ($C_{FF}$)*

Although a feed-forward capacitor ($C_{FF}$) from the FB pin to the OUT pin is not required to achieve stability, a 10-nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance $C_{FF}$ can be used; however, the start-up time is longer, and the PG signal can incorrectly indicate that the output voltage is settled. For a detailed description, see *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*.

#### *8.1.1.8 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)*

The TPS7A83A features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$).The use of an external $C_{NR/SS}$ is highly recommended, especially to minimize in-rush current into the output capacitors. This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak in-rush current during start-up, minimizing start-up transients to the input power bus.

To achieve a monotonic start-up, the TPS7A83A error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage approaches the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference ($V_{NR/SS}$). Use 公式 6 to calculate the soft-start ramp time:

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (6)$$

$I_{NR/SS}$ is provided in the table.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and 公式 7 to calculates the cutoff frequency. The typical value of $R_{NR/SS}$ is 250 kΩ. Increasing the $C_{NR/SS}$ capacitor has a greater affect because the output voltage increases when the noise from the reference is gained up even more at higher output voltages. For low-noise applications, a 10-nF to 1-µF $C_{NR/SS}$ is recommended. When a $C_{NR/SS}$ capacitor gets larger, the capacitor leakage increases, causing a longer than expected start-up time.

$$f_{cutoff} = 1/ (2 \times \pi \times R_{NR/SS} \times C_{NR/SS}) \quad (7)$$

### 8.1.2 Start-Up

#### *8.1.2.1 Soft-Start (NR/SS)*

The output of the device features a user-adjustable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$). This soft-start eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, thus minimizing start-up transients to the input power bus.

The output voltage ($V_{OUT}$) rises proportionally to $V_{NR/SS}$during start-up as the LDO regulates so that the feedback voltage equals the NR/SS voltage ($V_{FB}$ = $V_{NR/SS}$). As such, the time required for $V_{NR/SS}$ to reach its nominal value determines the rise time of $V_{OUT}$ (start-up time).

Not using a noise-reduction capacitor on the NR/SS pin can result in output voltage overshoot of approximately 10%. Using a capacitor on the NR/SS pin minimizes the overshoot.

Values for the soft-start charging currents are provided in the *Specifications* table.

##### 8.1.2.1.1 Inrush Current

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, 公式 8 can estimate this soft-start current:

$$I_{OUT}(t) = \left( \frac{C_{OUT} \times dV_{OUT}(t)}{dt} \right) + \left( \frac{V_{OUT}(t)}{R_{LOAD}} \right)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turnon ramp
- $dV_{OUT}(t)$ / dt is the slope of the $V_{OUT}$ ramp
- $R_{LOAD}$ is the resistive load impedance (8)

### 8.1.2.2 Undervoltage Lockout (UVLO)

The UVLO circuits ensure that the device stays disabled before the input or bias supplies reach the minimum operational voltage range, and ensures that the device properly shuts down when either the input or BIAS supply collapses.

图 50 and 表 8 show one of the UVLO circuits being triggered to various input voltage events, assuming $V_{EN} \geq V_{IH(EN)}$.

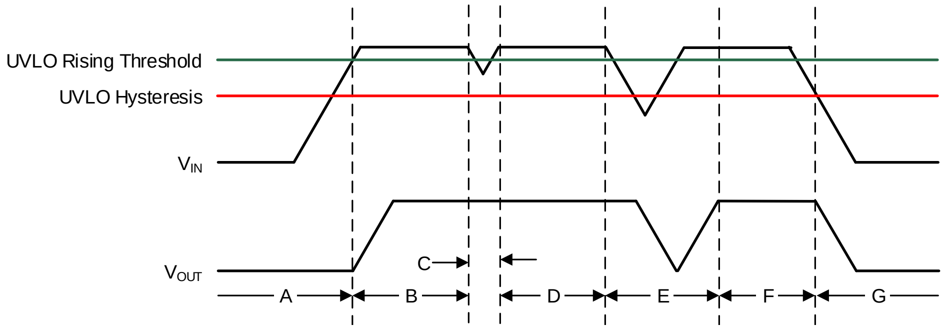


**图 50. Typical UVLO Operation**

**表 8. Typical UVLO Operation Description**

| REGION | EVENT | $V_{OUT}$ STATUS | COMMENT |
|---|---|---|---|
| A | Turnon, $V_{IN} \geq V_{UVLO\_1,2(IN)}$, and $V_{BIAS} \geq V_{UVLO(BIAS)}$ | Off | Start-up |
| B | Regulation | On | Regulates to target $V_{OUT}$ |
| C | Brownout, $V_{IN} \geq V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$ or $V_{BIAS} \geq V_{UVLO(BIAS)} - V_{HYS(BIAS)}$ | On | The output can fall out of regulation but the device is still enabled |
| D | Regulation | On | Regulates to target $V_{OUT}$ |
| E | Brownout, $V_{IN} < V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$ or $V_{BIAS} \geq V_{UVLO(BIAS)} - V_{HYS(BIAS)}$ | Off | The device is disabled and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO fault is removed when either the IN or BIAS UVLO rising threshold is reached by the input or bias voltage and a normal start-up then follows. |
| F | Regulation | On | Regulates to target $V_{OUT}$ |
| G | Turnoff, $V_{IN} < V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$ or $V_{BIAS} < V_{UVLO(BIAS)} - V_{HYS(BIAS)}$ | Off | The output falls because of the load and active discharge circuit |

Similar to many other LDOs with this feature, the UVLO circuits take a few microseconds to fully assert. During this time, a downward line transient below approximately 0.8 V causes the UVLO to assert for a short time; however, the UVLO circuits do not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLO circuits are not given enough time to fully discharge the internal nodes, the outputs are not fully disabled.

The effect of the downward line transient can be mitigated by using a larger input capacitor to increase the fall time of the input supply when operating near the minimum $V_{IN}$.

#### *8.1.2.3 Power-Good (PG) Function*

The PG circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. The PG circuit asserts whenever FB, $V_{IN}$, or EN are below their thresholds. 图 51 and 表 9 describe the PG operation versus the output voltage.

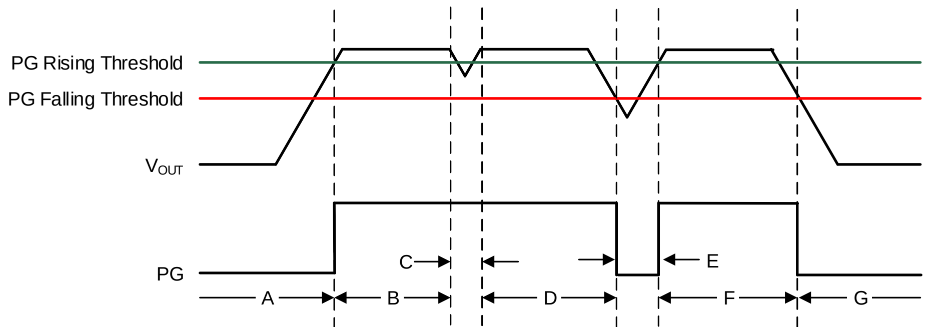


**图 51. Typical PG Operation**

**表 9. Typical PG Operation Description**

| REGION | EVENT | PG STATUS | FB VOLTAGE |
|---|---|---|---|
| A | Turnon | 0 | $V_{FB} < V_{IT(PG)} + V_{HYS(PG)}$ |
| B | Regulation | Hi-Z | $V_{FB} \geq V_{IT(PG)}$ |
| C | Output voltage dip | Hi-Z | |
| D | Regulation | Hi-Z | |
| E | Output voltage dip | 0 | $V_{FB} < V_{IT(PG)}$ |
| F | Regulation | Hi-Z | $V_{FB} \geq V_{IT(PG)}$ |
| G | Turnoff | 0 | $V_{FB} < V_{IT(PG)}$ |

The PG pin is open-drain, and connecting a pullup resistor to an external supply enables others devices to receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices.

To ensure proper operation of the PG circuit, the pullup resistor value must be from 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the PG transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the PG node. If the pullup resistor is outside of this range, then the PG signal may not read a valid digital logic level.

Using a large $C_{FF}$ with a small $C_{NR/SS}$ causes the PG signal to incorrectly indicate that the output voltage has settled during turnon. The $C_{FF}$ time constant must be greater than the soft-start time constant to ensure proper operation of the PG during start-up. For a detailed description, see *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator*.

The state of PG is only valid when the device operates above the minimum supply voltage. During short brownout events and at light loads, PG does not assert because the output voltage (therefore $V_{FB}$) is sustained by the output capacitance.

### 8.1.3 AC and Transient Performance

LDO ac performance includes power-supply rejection ratio, output-current transient response, and output noise. These metrics are primarily a function of open-loop gain, bandwidth, and phase margin that control the closed-loop input and output impedance of the LDO. The output noise is primarily a result of the reference and error amplifier noise.

#### 8.1.3.1 *Power-Supply Rejection Ratio (PSRR)*

PSRR is a measure of how well the LDO control loop rejects signals from $V_{IN}$ to $V_{OUT}$ across the frequency spectrum (usually 10 Hz to 10 MHz). 公式 9 gives the PSRR calculation as a function of frequency for the input signal [$V_{IN}$(f)] and output signal [$V_{OUT}$(f)].

$$PSRR(dB) = 20Log_{10}\left(\frac{V_{IN}(f)}{V_{OUT}(f)}\right) \tag{9}$$

Even though PSRR is a loss in signal amplitude, PSRR is shown as positive values in decibels (dB) for convenience.

图 52 shows a simplified diagram of PSRR versus frequency.

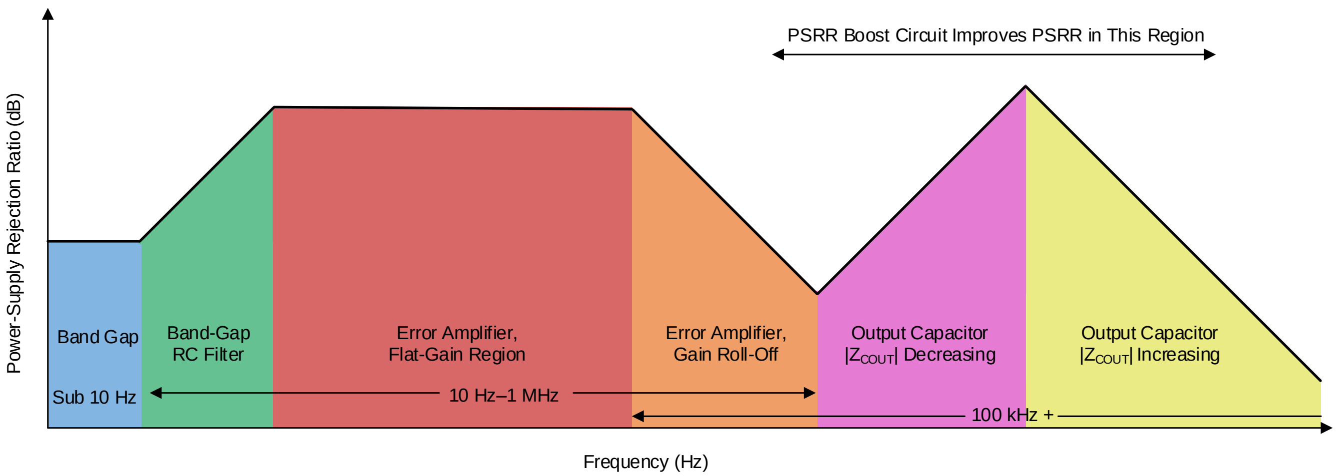


**图 52. Power-Supply Rejection Ratio Diagram**

An LDO is often employed not only as a dc-dc regulator, but also to provide exceptionally clean power-supply voltages that exhibit ultra-low noise and ripple to sensitive system components. This usage is especially true for the TPS7A83A.

The TPS7A83A features an innovative circuit to boost the PSRR from 200 kHz to 1 MHz; see 图 1. To achieve the maximum benefit of this PSRR boost circuit, TI recommends using a capacitor with a minimum impedance in the 100-kHz to 1-MHz band.

#### 8.1.3.2 Output Voltage Noise

The TPS7A83A is designed for system applications where minimizing noise on the power-supply rail is critical to system performance. For example, the TPS7A83A can be used in a phase-locked loop (PLL)-based clocking circuit and can be used for minimum phase noise, or in test and measurement systems where even small power-supply noise fluctuations reduce system dynamic range.

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shot noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker noise, or 1/f noise and dominates at lower frequencies as a function of 1/f). 图 53 shows a simplified output voltage noise density plot versus frequency.

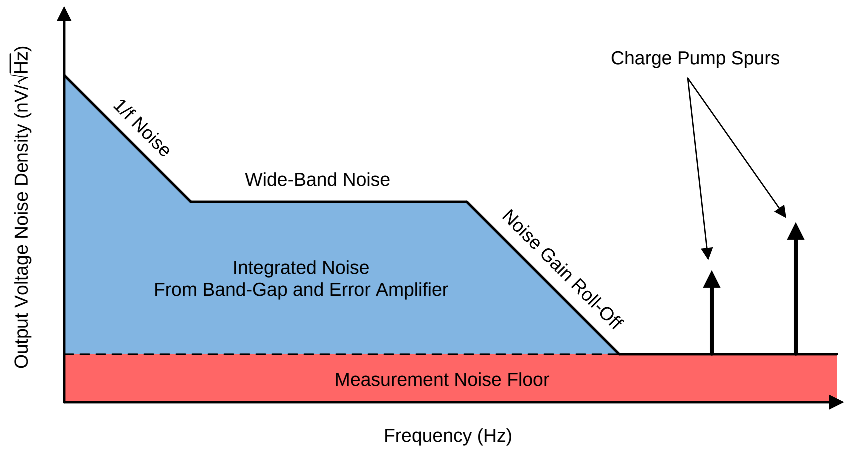


**图 53. Output Voltage Noise Diagram**

For further details, see the *How to Measure LDO Noise* white paper.

#### 8.1.3.3 Optimizing Noise and PSRR

表 10 describes several ways how the ultra-low noise floor and PSRR of the device can be improved.

**表 10. Effect of Various Parameters on AC Performance(1)(2)**

| PARAMETER | NOISE | | | PSRR | | |
|---|---|---|---|---|---|---|
| | LOW-FREQUENCY | MID-FREQUENCY | HIGH-FREQUENCY | LOW-FREQUENCY | MID-FREQUENCY | HIGH-FREQUENCY |
| $C_{NR/SS}$ | +++ | No effect | No effect | +++ | + | No effect |
| $C_{FF}$ | ++ | +++ | + | ++ | +++ | + |
| $C_{OUT}$ | No effect | + | +++ | No effect | + | +++ |
| $V_{IN} – V_{OUT}$ | + | + | + | +++ | +++ | ++ |
| PCB layout | ++ | ++ | + | + | +++ | +++ |

(1) The number of +'s indicates the improvement in noise or PSRR performance by increasing the parameter value.
(2) Shaded cells indicate the easiest improvement to noise or PSRR performance.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby minimizing the output voltage noise floor. The LPF is a single-pole filter, and 公式 10 calculates the cutoff frequency. The typical value of $R_{NR/SS}$ is 250 kΩ. The effect of the $C_{NR/SS}$ capacitor increases when $V_{OUT(nom)}$ increases because the noise from the reference is gained up when the output voltage increases. For low-noise applications, TI recommends a 10-nF to 1-µF $C_{NR/SS}$.

$$f_{cutoff} = 1 / (2 \times \pi \times R_{NR/SS} \times C_{NR/SS}) \quad (10)$$

The feed-forward capacitor reduces output voltage noise by filtering out the mid-band frequency noise. The feed-forward capacitor can be optimized by placing a pole-zero pair near the edge of the loop bandwidth and pushing out the loop bandwidth, thus improving mid-band PSRR.

A larger $C_{OUT}$ or multiple output capacitors reduces high-frequency output voltage noise and PSRR by reducing the high-frequency output impedance of the power supply.

Additionally, a higher input voltage improves the noise and PSRR because greater headroom is provided for the internal circuits. However, a high-power dissipation across the die increases the output noise because of the increase in junction temperature.

Good PCB layout improves the PSRR and noise performance by providing heat sinking at low frequencies and isolating $V_{OUT}$ at high frequencies.

表 11 lists the output voltage noise for the 10-Hz to 100-kHz band at a 5-V output for a variety of conditions with an input voltage of 5.5 V and a load current of 2 A. The 5-V output was chosen as a worst-case nominal operation for output voltage noise.

**表 11. Output Noise Voltage at a 5-V Output**

| OUTPUT VOLTAGE NOISE ($\mu V_{RMS}$) | $C_{NR/SS}$ (nF) | $C_{FF}$ (nF) | $C_{OUT}$ (µF) |
|---|---|---|---|
| 11.7 | 10 | 10 | 22 |
| 7.7 | 100 | 10 | 22 |
| 6 | 100 | 100 | 22 |
| 7.4 | 100 | 10 | 1000 |
| 5.8 | 100 | 100 | 1000 |

#### 8.1.3.3.1 Charge Pump Noise

图 54 shows that the device internal charge pump generates a minimal amount of noise.

Using a BIAS rail minimizes the internal charge-pump noise when the internal voltage is clamped, thereby reducing the overall output noise floor.

The high-frequency components of the output voltage noise density curve are filtered out in most applications by using 10-nF to 100-nF bypass capacitors close to the load. Using a ferrite bead between the LDO output and the load input capacitors forms a pi-filter, further reducing the high-frequency noise contribution.

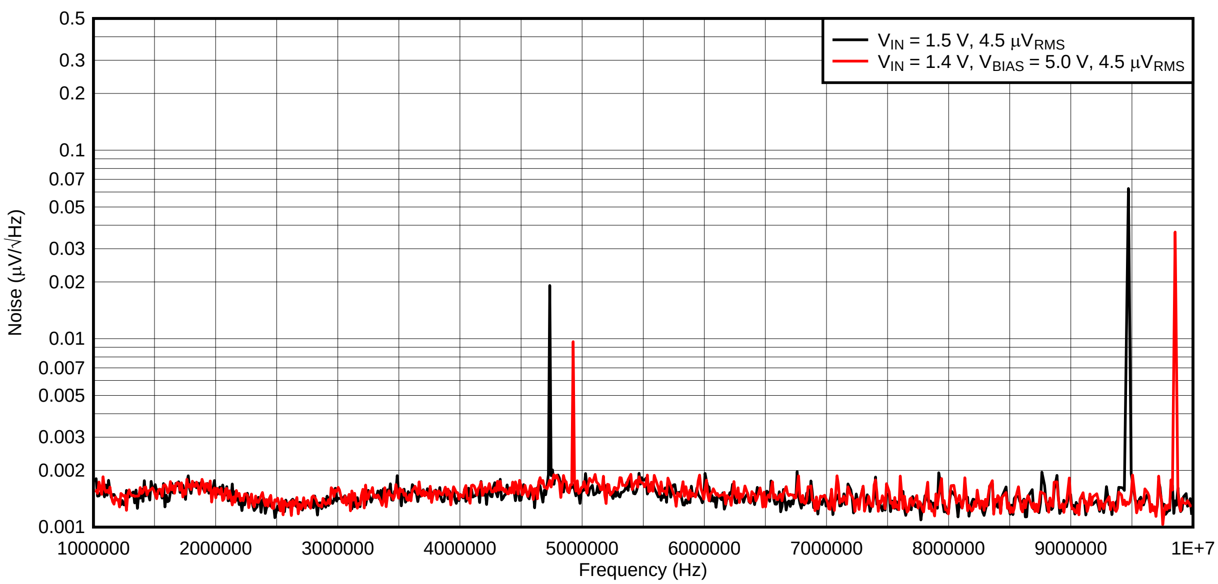


**图 54. Charge Pump Noise**

#### *8.1.3.4 Load Transient Response*

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in 图 55 and described in 表 12 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state.

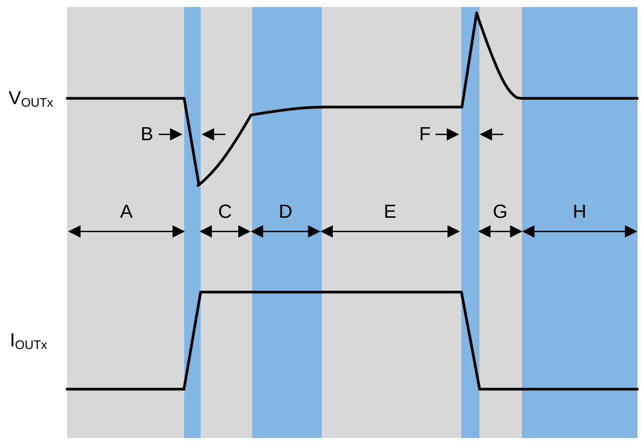


**图 55. Load Transient Waveform**

**表 12. Load Transient Waveform Description**

| REGION | DESCRIPTION | COMMENT |
|---|---|---|
| A | Regulation | Regulation |
| B | Output current ramping | Initial voltage dip is a result of the depletion of the output capacitor charge |
| C | LDO responding to transient | Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation |
| D | Reaching thermal equilibrium | At high load currents the LDO takes some time to heat up. During this time the output voltage changes slightly. |
| E | Regulation | Regulation |
| F | Output current ramping | Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase |
| G | LDO responding to transient | Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor |
| H | Regulation | Regulation |

 

The transient response peaks ($V_{OUT(max)}$ and $V_{OUT(min)}$) are improved by using more output capacitance; however, doing so slows down the recovery time ($W_{rise}$ and $W_{fall}$). 图 56 shows these parameters during a load transient, with a given pulse duration (PW) and current levels ($I_{OUT(LO)}$ and $I_{OUT(HI)}$).

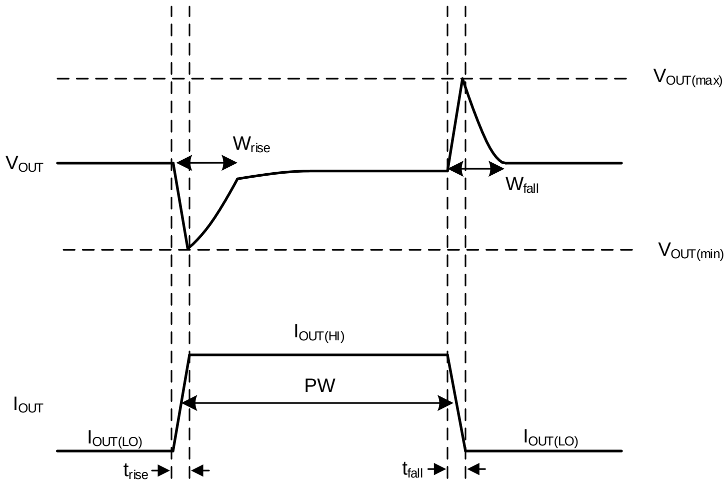


**图 56. Simplified Load Transient Waveform**

### 8.1.4 DC Performance

#### *8.1.4.1 Output Voltage Accuracy ($V_{OUT}$)*

The device features an output voltage accuracy of 0.75% maximum, with BIAS, that includes the errors introduced by the internal reference, load regulation, line regulation, and operating temperature as specified by the table. Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent.

#### *8.1.4.2 Dropout Voltage ($V_{DO}$)*

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} - V_{OUT}$) that is required for regulation. When $V_{IN}$ drops below the required $V_{DO}$ for the given load current, the device functions as a resistive switch and does not regulate output voltage. 图 57 shows that dropout voltage is proportional to the output current because the device is operating as a resistive switch.

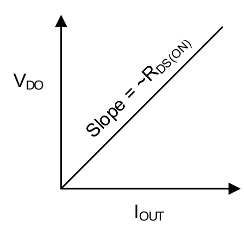


**图 57. Dropout Voltage versus Output Current**

Dropout voltage is affected by the drive strength for the gate of the pass element, which is nonlinear with respect to $V_{IN}$ on this device because of the internal charge pump. Dropout voltage increases exponentially when the input voltage nears its maximum operating voltage.

#### 8.1.4.2.1 Behavior When Transitioning From Dropout Into Regulation

Some applications can have transients that place the LDO into dropout, such as slower ramps on $V_{IN}$ for start-up or load transients. As with many other LDOs, the output can overshoot on recovery from these conditions.

图 58 shows that a ramping input supply can cause an LDO to overshoot on start-up when the slew rate and voltage levels are in the right range. This condition is easily avoided through either the use of an enable signal, or by increasing the soft-start time with $C_{SS/NR}$.

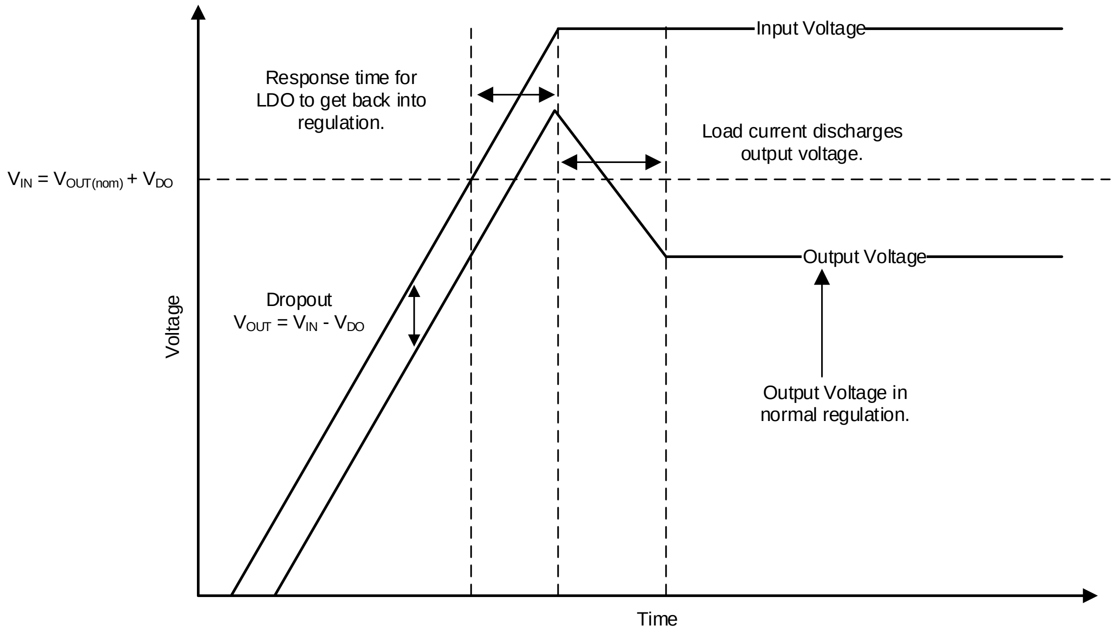


图 58. Start-Up Into Dropout

### 8.1.5 Sequencing Requirements

There is no sequencing requirement between the BIAS, IN, and EN pins in the TPS7A83A.

### 8.1.6 Negatively Biased Output

The TPS7A83A output can be negatively biased to the absolute maximum rating, without affecting start-up condition.

### 8.1.7 Reverse Current

As with most LDOs, this device can be damaged by excessive reverse current.

Reverse current is current that flows through the body diode on the pass element instead of the normal conducting channel. This current flow, at high enough magnitudes, degrades long-term reliability of the device resulting from risks of electro-migration and excess heat being dissipated across the device. If the current flow gets high enough, a latch-up condition can be entered.

Conditions where excessive reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large $C_{OUT}$ and the input supply collapses quickly with little or no load current,
- The output is biased when the input supply is not established, or
- The output is biased above the input supply.

If excessive reverse current flow is expected in the application, then external protection must be used to protect the device. 图 59 shows one approach of protecting the device.

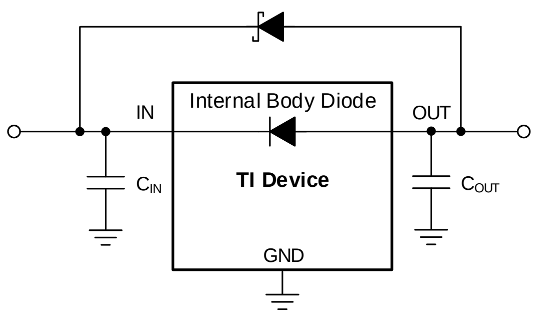


**图 59. Example Circuit for Reverse Current Protection Using a Schottky Diode**

### 8.1.8 Power Dissipation ($P_D$)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 公式 11 to approximate $P_D$:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (11)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature ($T_J$) for the device. According to 公式 12, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB, device package, and the temperature of the ambient air ($T_A$). 公式 13 rewrites 公式 12 for output current.

$$T_J = T_A + R_{\theta JA} \times P_D \quad (12)$$

$$I_{OUT} = (T_J – T_A) / [R_{\theta JA} \times (V_{IN} – V_{OUT})] \quad (13)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the VQFN package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

#### 8.1.8.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are given in the table and are used in accordance with 公式 14.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- $P_D$ is the power dissipated as explained in 公式 11
- $T_T$ is the temperature at the center-top of the device package, and
- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (14)

#### 8.1.8.2 Recommended Area for Continuous Operation (RACO)

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. As shown in 图 60, the recommended area for continuous operation for a linear regulator can be separated into the following parts:

- Limited by dropout: Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN}$ – $V_{OUT}$) at a given output current level; see the *Dropout Voltage ($V_{DO}$)* section for more details.
- Limited by rated output current: The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- Limited by thermals: The shape of the slope is given by 公式 13. The slope is nonlinear because the junction temperature of the LDO is controlled by the power dissipation across the LDO; therefore, when $V_{IN}$ – $V_{OUT}$ increases, the output current must decrease in order to ensure that the rated junction temperature of the device is not exceeded. Exceeding this rating can cause the device to fall out of specifications and reduces long-term reliability.
- Limited by $V_{IN}$ range: The rated input voltage range governs both the minimum and maximum of $V_{IN}$ – $V_{OUT}$.

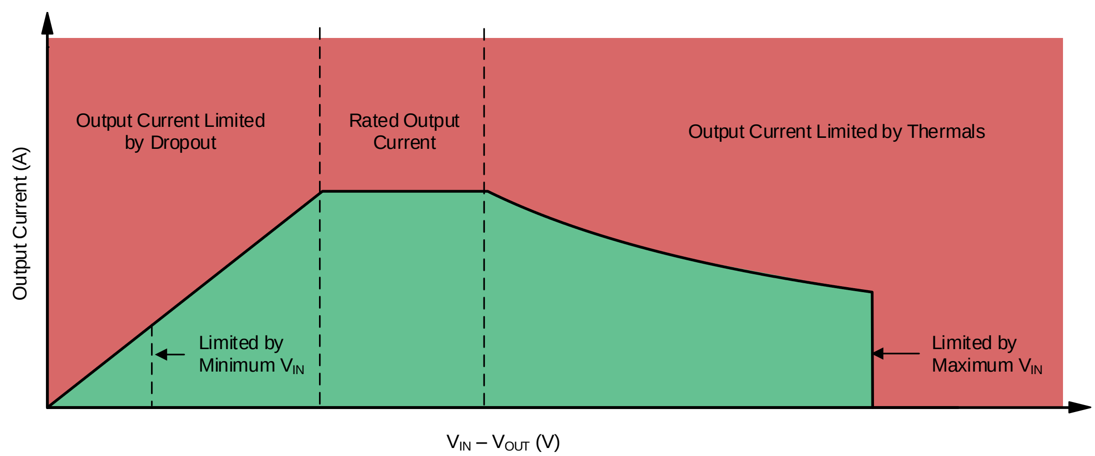


**图 60. Continuous Operation Slope Region Description**

图 61 to 图 66 show the recommended area of operation curves for this device on a JEDEC-standard, high-K board with a $R_{\theta JA}$ = 43.4°C/W, as given in the table.

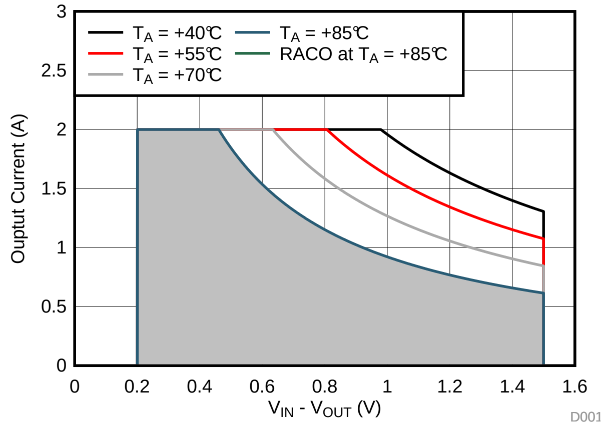


**图 61. Recommended Area for Continuous Operation for $V_{OUT}$ = 0.9 V**

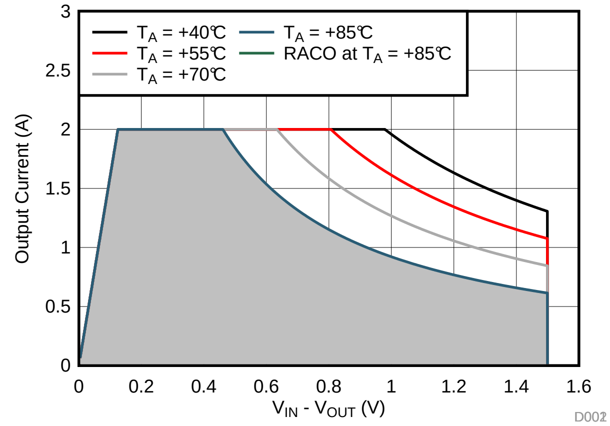


**图 62. Recommended Area for Continuous Operation for $V_{OUT}$ = 1.2 V**

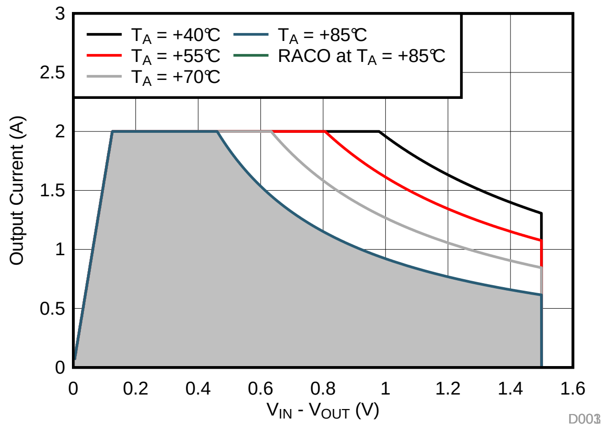


**图 63. Recommended Area for Continuous Operation for $V_{OUT}$ = 1.8 V**

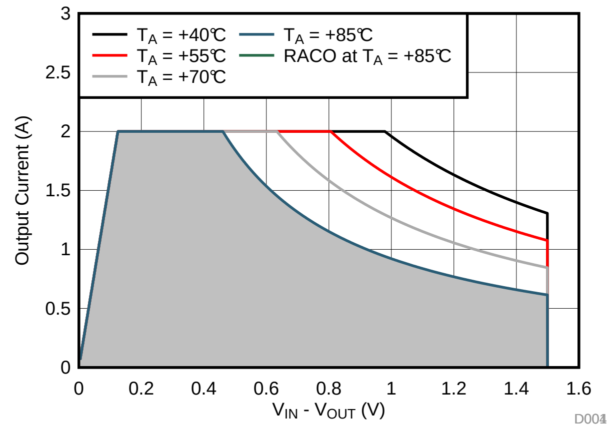


**图 64. Recommended Area for Continuous Operation for $V_{OUT}$ = 2.5 V**

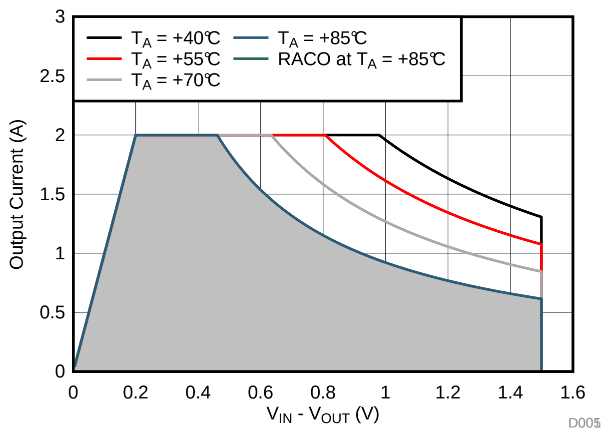


**图 65. Recommended Area for Continuous Operation for $V_{OUT}$ = 3.3 V**

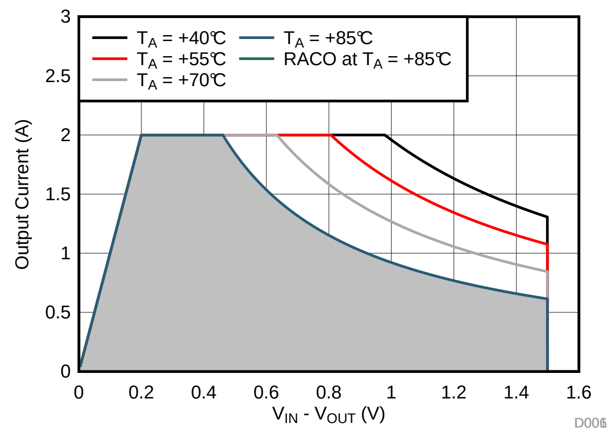


**图 66. Recommended Area for Continuous Operation for $V_{OUT}$ = 5 V**

## 8.2 Typical Application

The TPS7A83A uses the ANY-OUT configuration to regulate a 2-A load requiring good PSRR at high frequency with low-noise at 0.9 V using a 1.2-V input voltage and a 5-V bias supply. 图 67 provides a schematic for this typical application circuit.

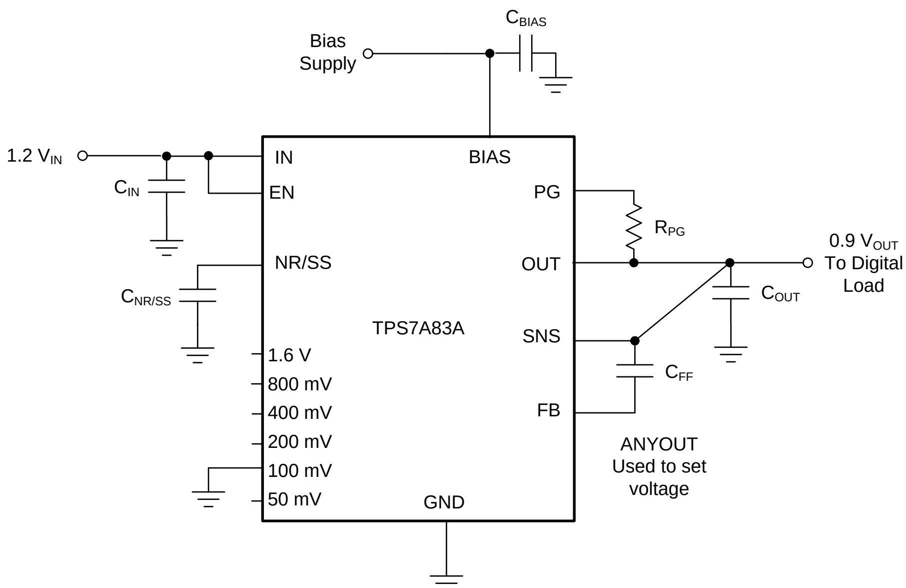




**图 67. TPS7A83A Typical Application: Low-Input, Low-Output (LILO) Voltage Conditions**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 13 as the input parameters.

**表 13. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 1.2 V, ±3%, provided by the dc-dc converter switching at 500 kHz |
| Bias voltage | 5 V, ±5% |
| Output voltage | 0.9 V, ±1% |
| Output current | 2 A (maximum), 100 mA (minimum) |
| RMS noise, 10 Hz to 100 kHz | < 10 $\mu V_{RMS}$ |
| PSRR at 500 kHz | > 40 dB |
| Start-up time | < 25 ms |

### 8.2.2 Detailed Design Procedure

At 2 A, the dropout of the TPS7A83A has 180-mV maximum dropout over temperature, thus a 400-mV headroom is sufficient for operation over both input and output voltage accuracy. The bias rail is provided for better performance for the LILO conditions. As per 表 13, the PSRR is greater than 40 dB in these conditions and noise is less than 10 $\mu V_{RMS}$.

The ANY-OUT internal resistor network is also used for maximum accuracy.

To achieve 0.9 V on the output, the 100mV pin is grounded. 公式 15 describes how the voltage value of 100 mV is added to the 0.8-V internal reference voltage for $V_{OUT(nom)}$ equal to 0.9 V.

$$V_{OUT(nom)} = V_{NR/SS} + 0.1\text{ V} = 0.8\text{ V} + 0.1\text{ V} = 0.9\text{ V} \quad (15)$$

Input and output capacitors are selected in accordance with the *External Component Selection* section. Ceramic capacitors of 10 µF for the input and one 22-µF capacitor for the output are selected.

To satisfy the required start-up time and still maintain low-noise performance, a 100-nF $C_{NR/SS}$ is selected. 公式 16 calculates this value.

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (16)$$

At the 2-A maximum load, the internal power dissipation is 0.6 W and corresponds to a 26.04°C junction temperature rise for the RGR package on a standard JEDEC board. With an 55°C maximum ambient temperature, the junction temperature is at 94.06°C. To further minimize noise, a feed-forward capacitor ($C_{FF}$) of 10 nF is selected.

### 8.2.3 Application Curves

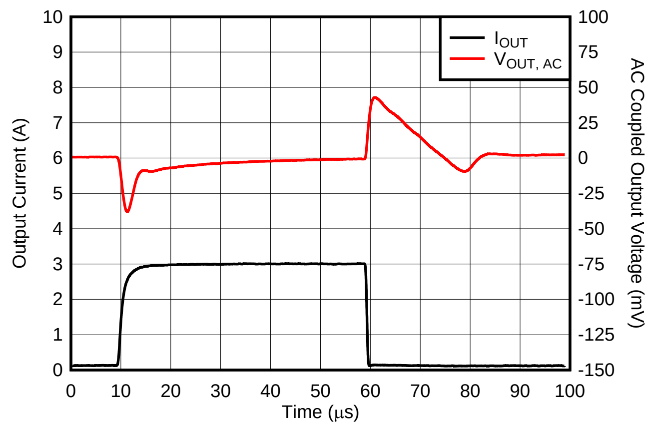


图 68. Output Load Transient Response

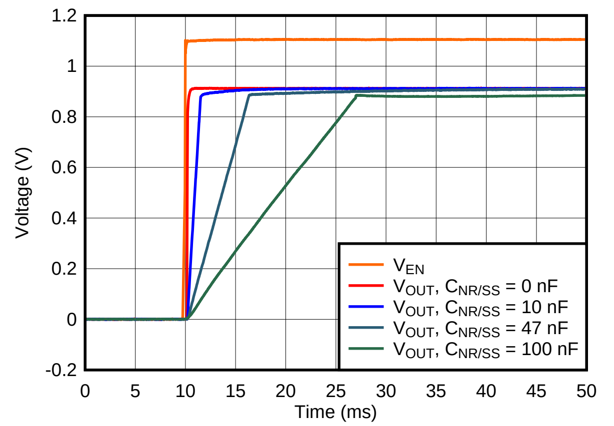


图 69. Output Start-Up Response

## 9 Power Supply Recommendations

The TPS7A83A device is designed to operate from an input voltage supply range from 1.1 V to 6.5 V. If the input supply is less than 1.4 V, then a bias rail of at least 3 V must be used. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR may help improve output noise performance.

## 10 Layout

### 10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. The grounding and layout scheme shown in 图 70 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

TI also recommends a ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

## 10.2 Layout Example

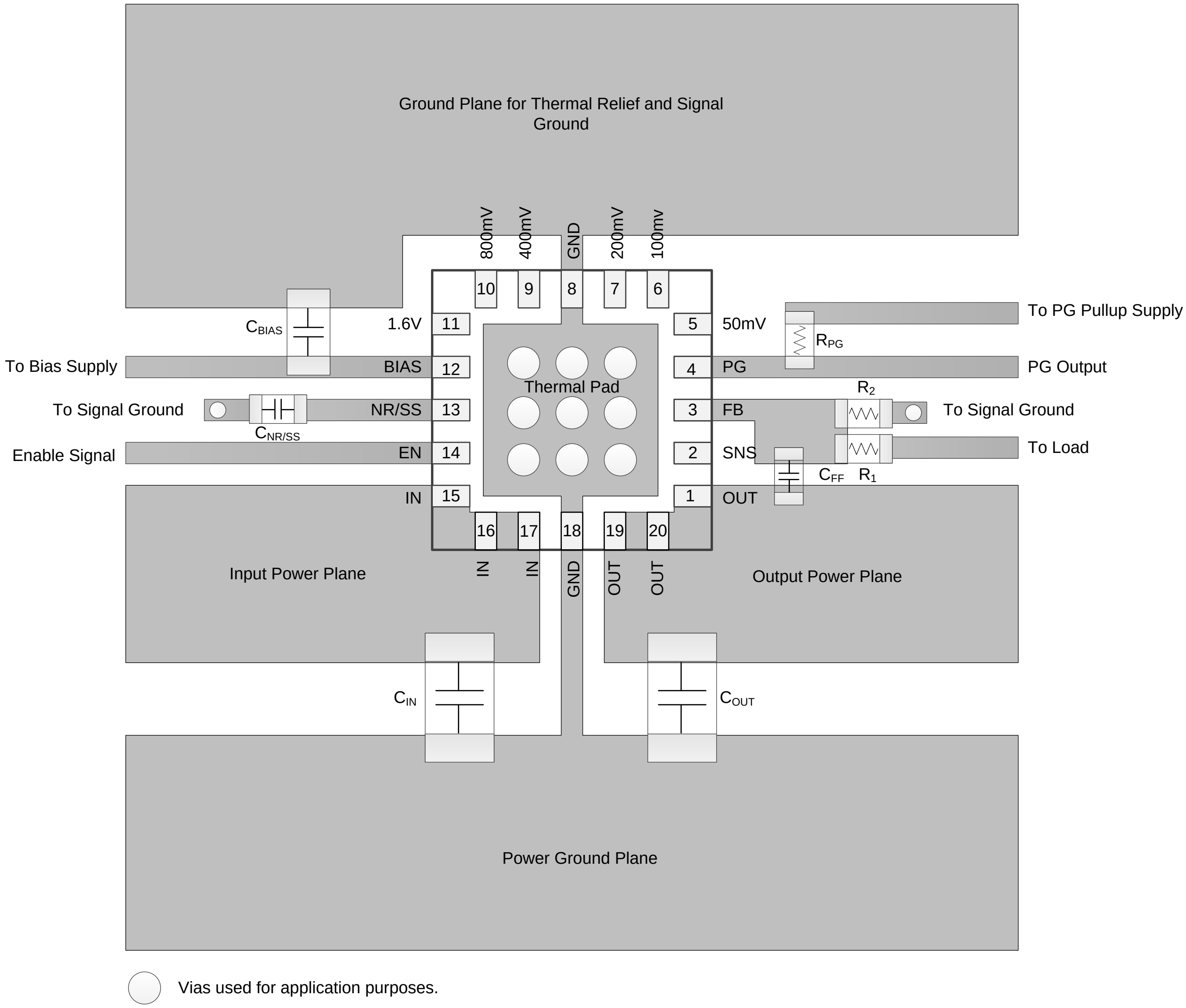


图 70. Example Layout

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 开发支持

#### *11.1.1.1 评估模块*

我们为您提供了评估模块 (EVM)，可以借此来对使用 TPS7A8300 时的电路性能进行初始评估。表 14 显示了此装置的摘要信息。

表 **14.** 设计套件与评估模块

| 名称 | 评估模块 |
|---|---|
| TPS7A8300EVM-579 评估模块 | SBVU021 |

可通过德州仪器 (TI) 网站上的 TPS7A8300 产品文件夹来申请获取该 EVM。

#### *11.1.1.2 Spice 模型*

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以通过仿真模型下的 TPS7A83A 产品文件夹获取 TPS7A83A 器件的 SPICE 模型。

### 11.1.2 器件命名规则

表 **15.** 订购信息[(1)]

| 产品 | 说明 |
|---|---|
| TPS7A8300A YYYZ | YYY 是封装符号<br>Z 是封装数量 |

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者查看 www.ti.com.cn 上的器件产品文件夹。

## 11.2 文档支持

### 11.2.1 相关文档

请参阅如下相关文档：

- *高精度过压和欠压监测*
- *TPS7A8300EVM-579 评估模块*
- *《使用前馈电容器和低压降稳压器的优缺点》*
- *《具有可编程延迟的 TPS3890 低静态电流、1% 精度监控器》*

## 11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

**TI E2E™ 在线社区** ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

## 11.5 商标

ANY-OUT, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A8300ARGRR | ACTIVE | VQFN | RGR | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8300A | Samples |
| TPS7A8300ARGRT | ACTIVE | VQFN | RGR | 20 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8300A | Samples |
| TPS7A8300ARGWR | ACTIVE | VQFN | RGW | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 1F5H | Samples |
| TPS7A8300ARGWT | ACTIVE | VQFN | RGW | 20 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 1F5H | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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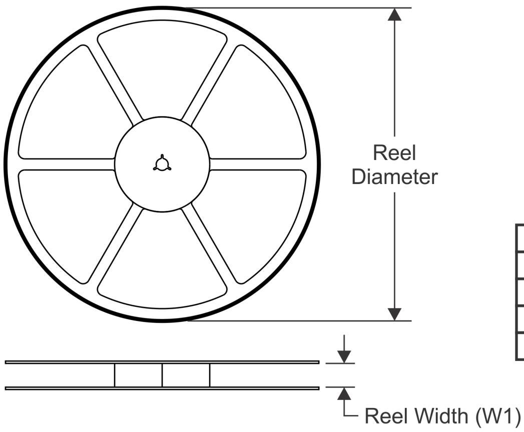
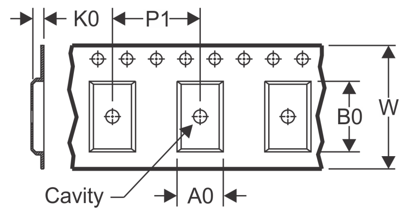
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

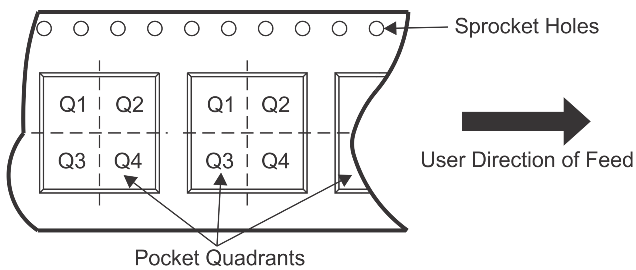



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

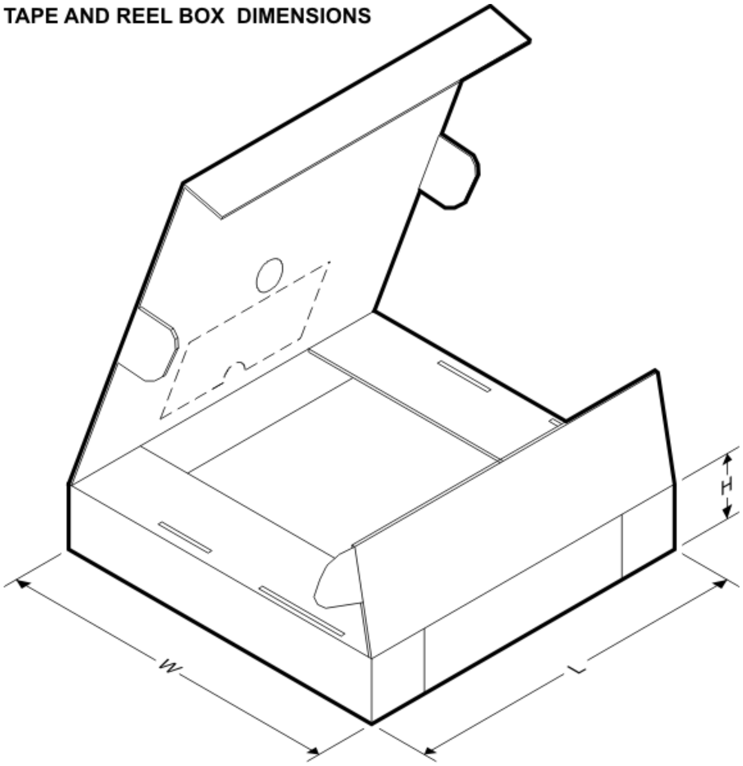
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A8300ARGRR | VQFN | RGR | 20 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS7A8300ARGRT | VQFN | RGR | 20 | 250 | 180.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS7A8300ARGWR | VQFN | RGW | 20 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8300ARGWT | VQFN | RGW | 20 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

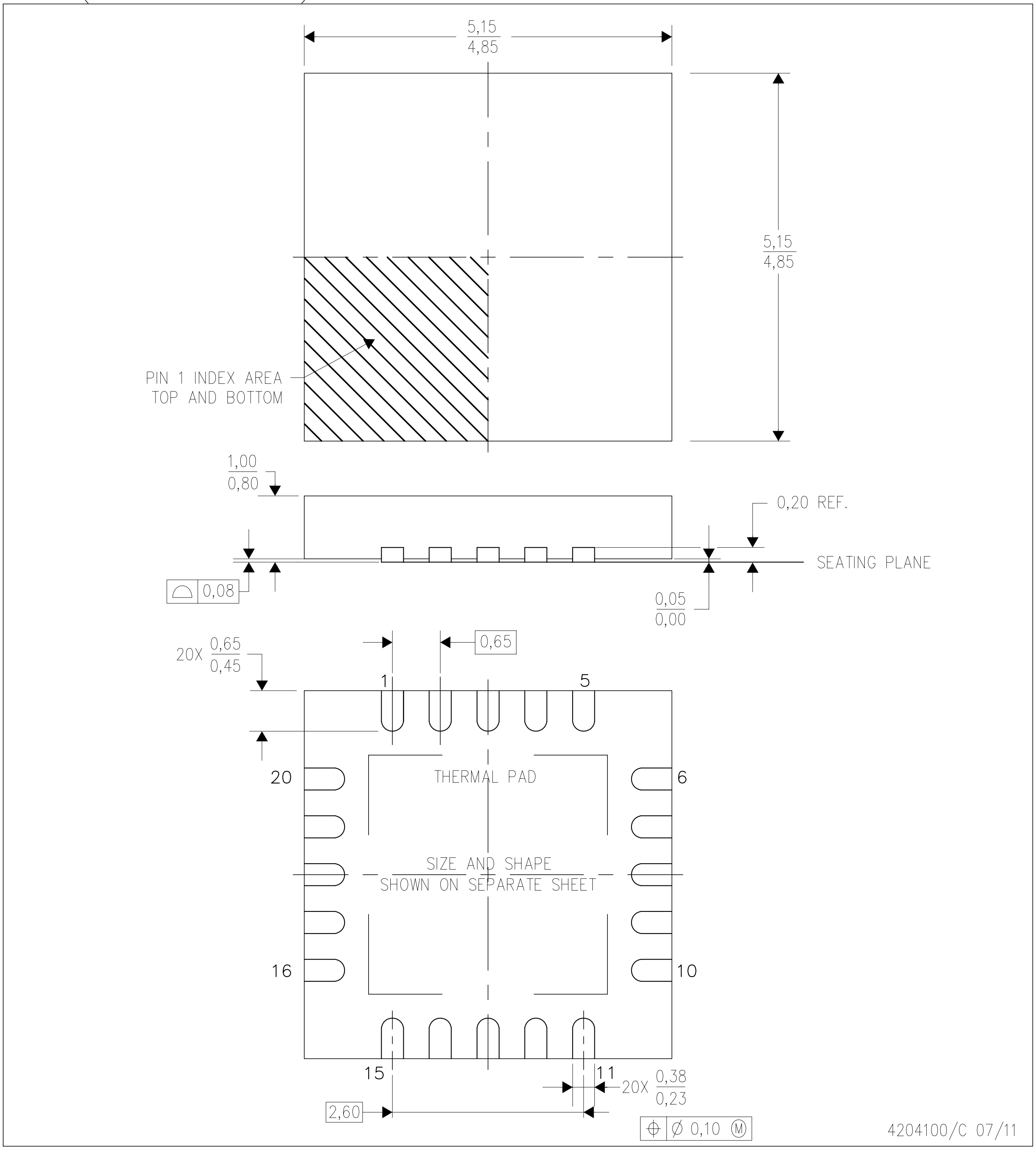
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

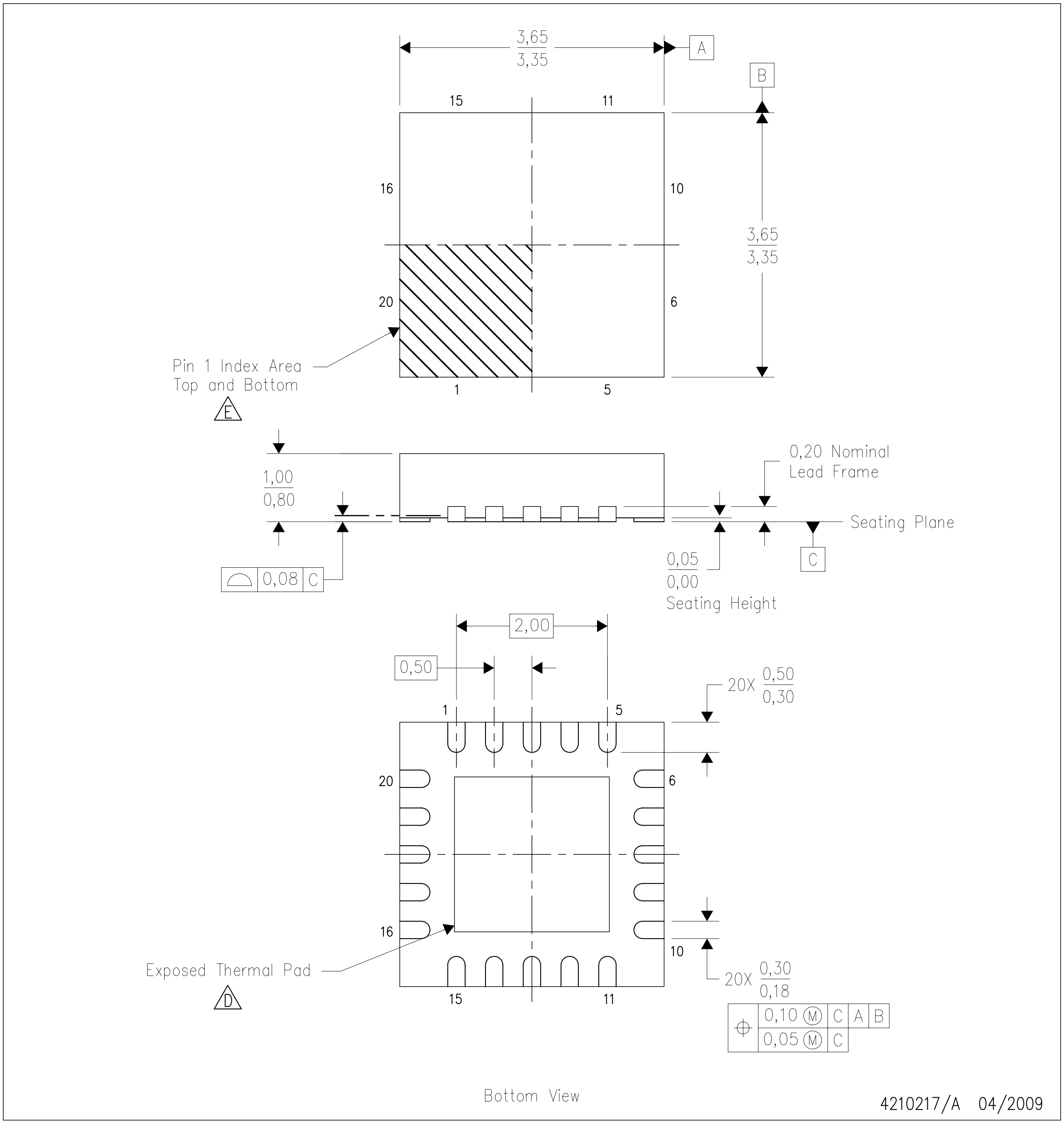
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A8300ARGRR | VQFN | RGR | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS7A8300ARGRT | VQFN | RGR | 20 | 250 | 210.0 | 185.0 | 35.0 |
| TPS7A8300ARGWR | VQFN | RGW | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS7A8300ARGWT | VQFN | RGW | 20 | 250 | 210.0 | 185.0 | 35.0 |

RGW (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flat pack, No-leads (QFN) package configuration
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

RGR (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

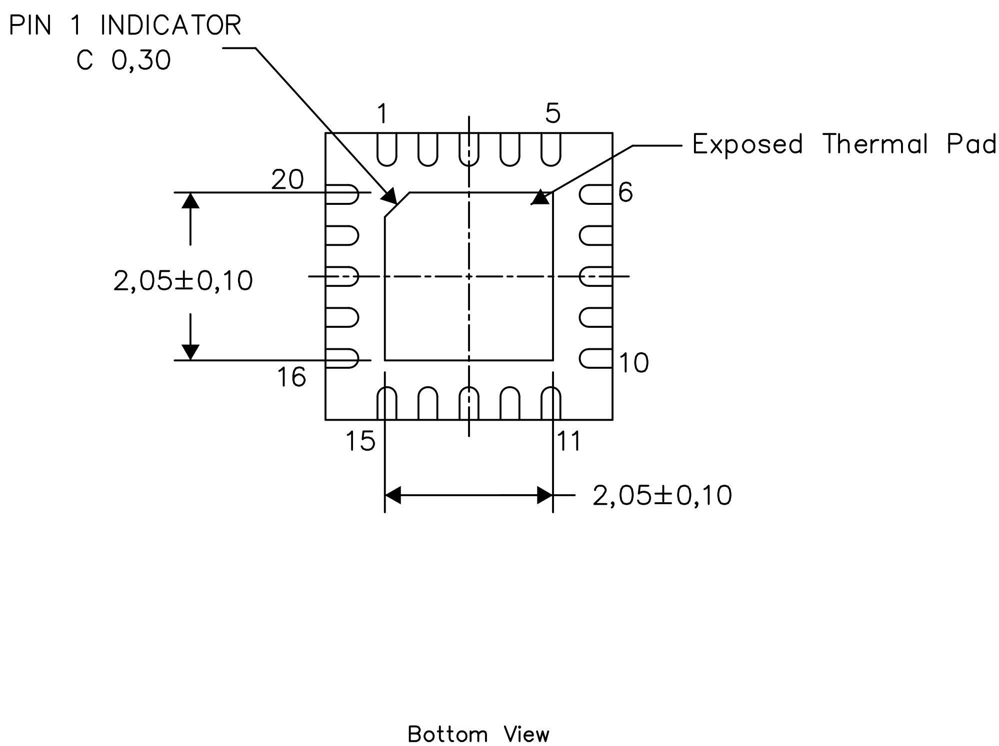
RGR (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

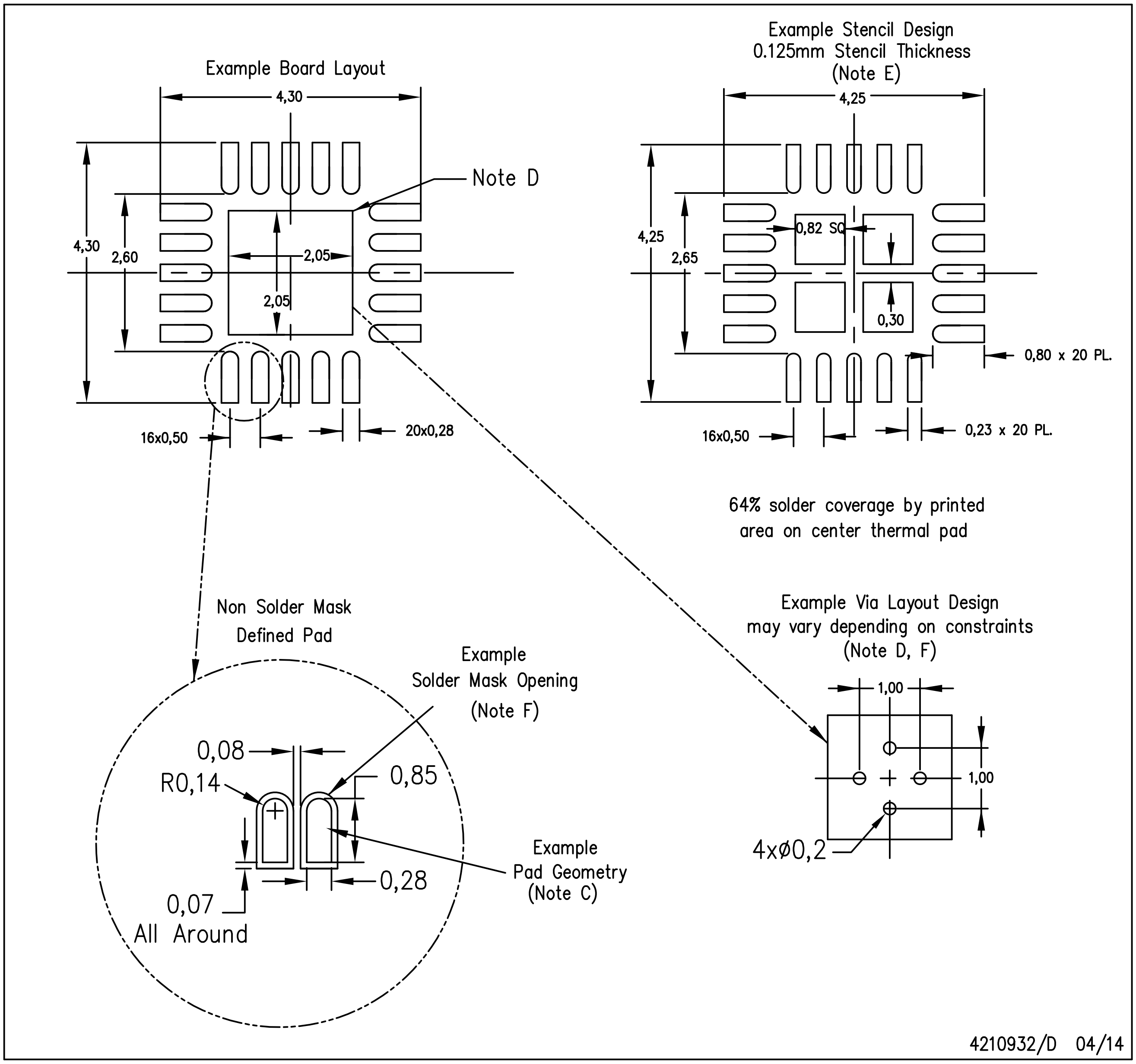



Exposed Thermal Pad Dimensions

4210218/E 04/14

NOTE: All linear dimensions are in millimeters

RGR (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## 重要声明和免责声明



邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122