

TPS7A24 200mA、18V、超低 I_Q 低压降稳压器

1 特性

- 超低 I_Q : 2.0 μ A
- 输入电压: 2.4V 至 18V
- 可用输出电压选项:
 - 固定电压: 1.25V 至 5.5V
 - 可调节电压: 1.24V 至 17.75V
- 在工作温度范围内的精度为 2%
- 低压降: 电流 200mA 时为 250mV (最大值)
- 主动过冲下拉保护
- 热关断保护和过流保护
- 工作结温范围: -40°C 至 $+125^{\circ}\text{C}$
- 与 1 μ F 输出电容器一起工作时保持稳定
- 封装: 5 引脚 SOT-23

2 应用

- 烟雾和热量探测器
- 恒温器
- 运动检测器 (PIR、uWave 等)
- 无线电动工具
- 电器电池组
- 电表
- 水表

3 说明

TPS7A24 低压降 (LDO) 线性稳压器支持 2.4V 至 18V 的输入电压范围, 并具有超低的静态电流 (I_Q)。这些特性能更好地帮助现代电器满足日益严苛的能源要求, 并有助于延长便携式电源解决方案的电池寿命。

TPS7A24 有固定电压和可调节电压两种版本可供选用。固定电压版本无需外部电阻器, 可最大限度减小印刷电路板 (PCB) 尺寸。为获得更大的灵活性或更高的输出电压, 可调节电压版本使用反馈电阻器将输出电压设置为 1.24V 到 17.75V 之间。两种版本都具有 2% 的输出调节精度, 可对微控制器 (MCU) 基准电压进行精密调节。

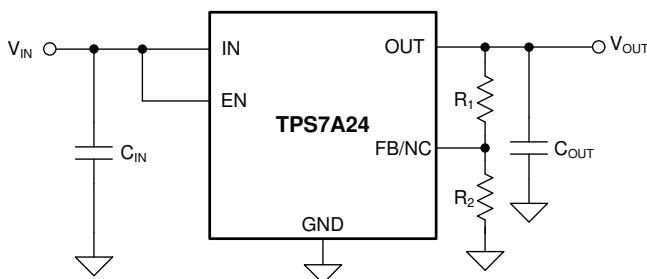
在电流为 200mA 时, TPS7A24 LDO 的最大压降小于 250mV, 因此它比标准线性稳压器的工作效率更高。此最大压降使得在 3.55V 输入电压 (V_{IN}) 至 3.3V 输出电压 (V_{OUT}) 范围内的效率达到了 92.8%。

器件信息⁽¹⁾

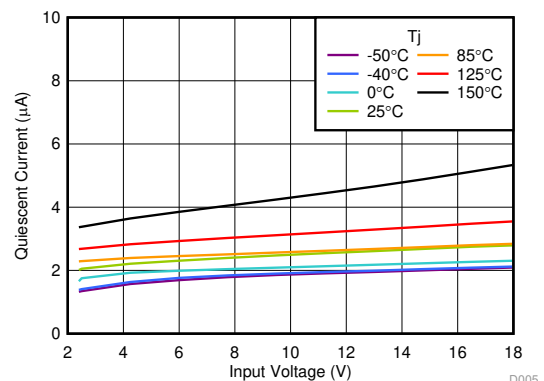
器件型号	封装	封装尺寸 (标称值)
TPS7A24	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的封装选项附录。

典型应用电路



静态电流与输入电压
($V_{OUT} = 1.24\text{V}$, $I_{OUT} = 0\text{A}$)



D005



目录

1	特性	1	7.4	Device Functional Modes.....	12
2	应用	1	8	Application and Implementation	13
3	说明	1	8.1	Application Information.....	13
4	修订历史记录	2	8.2	Typical Application	16
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	18
6	Specifications	4	10	Layout	18
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	18
6.2	ESD Ratings.....	4	10.2	Layout Examples.....	18
6.3	Recommended Operating Conditions.....	4	11	器件和文档支持	19
6.4	Thermal Information	4	11.1	器件支持	19
6.5	Electrical Characteristics.....	5	11.2	接收文档更新通知	19
6.6	Typical Characteristics	6	11.3	社区资源	19
7	Detailed Description	9	11.4	商标	19
7.1	Overview	9	11.5	静电放电警告	19
7.2	Functional Block Diagrams	9	11.6	Glossary	19
7.3	Feature Description.....	10	12	机械、封装和可订购信息	19

4 修订历史记录

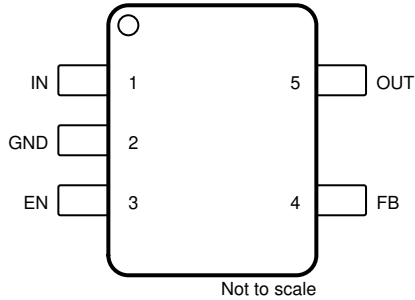
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2019) to Revision B	Page
• Changed maximum shutdown current to 650nA from 600nA	5

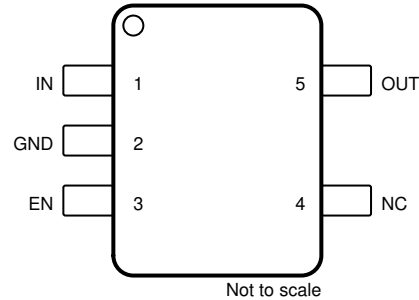
Changes from Original (August 2019) to Revision A	Page
• 已更改 将文档状态从预告信息更改为生产数据	1

5 Pin Configuration and Functions

TPS7A24: DBV Package (Adjustable)
5-Pin SOT-23
Top View



TPS7A24: DBV Package (Fixed)
5-Pin SOT-23
Top View



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DBV (Adjustable)	DBV (Fixed)		
EN	3	3	Input	Enable pin. Drive EN greater than $V_{EN(HI)}$ to enable the regulator. Drive EN less than $V_{EN(LOW)}$ to put the regulator into low-current shutdown. Do not float this pin. If not used, connect EN to IN.
FB	4	—	Input	Feedback pin. Input to the control-loop error amplifier. This pin is used to set the output voltage of the device with the use of external resistors. For adjustable-voltage version devices only.
GND	2	2	—	Ground pin.
IN	1	1	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger capacitor from IN to ground as listed in the Recommended Operating Conditions table. Place the input capacitor as close to the IN and GND pins of the device as possible.
NC	—	4	—	No internal connection. For fixed-voltage version devices only. This pin can be floated but the device has better thermal performance with this pin tied to GND.
OUT	5	5	Output	Output pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor from OUT to ground. Follow the recommended capacitor value as listed in the Recommended Operating Conditions table. Place the output capacitor as close to the OUT and GND pins of the device as possible.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	V _{IN}	−0.3	20	V
	V _{OUT}	−0.3	V _{IN} + 0.3 ⁽³⁾	
	V _{FB}	−0.3	5.5	
	V _{EN}	−0.3	20	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T _J	−50	150	°C
	Storage, T _{stg}	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages with respect to GND.
- (3) V_{IN} + 0.3 V or 20 V (whichever is smaller).

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	2.4		18	V
V _{OUT}	Output voltage (adjustable version)	1.24		18 - V _{DO}	V
V _{OUT}	Output voltage (fixed version)	1.25		5.5	V
I _{OUT}	Output current	0		200	mA
V _{EN}	Enable voltage	0		18	V
C _{IN} ⁽¹⁾	Input capacitor		1		μF
C _{OUT} ⁽¹⁾	Output capacitor	1	2.2	100	μF
T _J	Operating junction temperature	−40		125	°C

- (1) All capacitor values are assumed to derate to 50% of the nominal capacitor value.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A24	UNIT
		DBV (SOT23-5)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	167.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	86.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	38.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	14.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	38.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

specified at $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or $V_{IN} = 2.4\text{ V}$ (whichever is greater), FB tied to OUT, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 2\text{ V}$, and $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$ ceramic (unless otherwise noted); typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage accuracy	Adjustable version, $V_{OUT} = V_{FB}$	1.22	1.24	1.26	V
		Fixed output versions	–2		2	%
V_{FB}	Feedback voltage	Adjustable version only		1.24		V
$\Delta V_{OUT(\Delta V_{IN})}$	Line regulation ⁽¹⁾	$(V_{OUT(nom)} + 0.5\text{ V or } 2.4\text{ V}) \leq V_{IN} \leq 18\text{ V}$	–0.25		0.25	%
$\Delta V_{OUT(\Delta I_{OUT})}$	Load regulation	$1\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$	–1		1	%
I_{GND}	Ground pin current	$I_{OUT} = 0\text{ mA}$		2	4.5	μA
		$I_{OUT} = 1\text{ mA}$		15		
$I_{SHUTDOWN}$	Shutdown current	$V_{EN} \leq 0.4\text{ V}$, $V_{IN} = 2.4\text{ V}$, $I_{OUT} = 0\text{ mA}$		325	650	nA
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$	250	410	620	mA
I_{FB}	FB pin current			10		nA
V_{DO}	Dropout voltage ⁽²⁾	$I_{OUT} = 100\text{ mA}$		110	160	mV
		$I_{OUT} = 200\text{ mA}$		160	250	
PSRR	Power-supply rejection ratio	$f = 10\text{ Hz}$		75		dB
		$f = 100\text{ Hz}$		70		
		$f = 1\text{ kHz}$		62		
V_n	Output noise voltage	$\text{BW} = 10\text{ Hz to } 100\text{ kHz}$, $V_{OUT} = 1.24\text{ V}$		300		μV_{RMS}
$V_{UVLO(\text{RISING})}$	UVLO threshold rising	V_{IN} rising	1.95	2.15	2.35	V
$V_{UVLO(\text{HYS})}$	UVLO hysteresis			70		mV
$V_{UVLO(\text{FALLING})}$	UVLO threshold falling	V_{IN} falling	1.85	2.09	2.25	V
$V_{EN(\text{HI})}$	Enable pin high-level input voltage	Device enabled	0.9			V
$V_{EN(\text{LOW})}$	Enable pin low-level input voltage	Device disabled			0.4	V
I_{EN}	EN pin current	$V_{EN} = 18\text{ V}$		10		nA
$T_{SD(\text{shutdown})}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		$^{\circ}\text{C}$
$T_{SD(\text{reset})}$	Thermal shutdown reset temperature	Reset, temperature decreasing		145		$^{\circ}\text{C}$

(1) $V_{OUT(nom)} + 0.5\text{ V}$ or 2.4 V (whichever is greater).

(2) V_{DO} is measured with $V_{IN} = 0.97 \times V_{OUT(nom)}$ for fixed output voltage versions. V_{DO} is not measured for fixed output voltage versions when $V_{OUT} \leq 2.5\text{ V}$. For the adjustable output device, V_{DO} is measured with $V_{FB} = 0.97 \times V_{FB(nom)}$.

6.6 Typical Characteristics

at operating temperature $T_J = 25^\circ\text{C}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 0.9\text{ V}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(typ)} + 0.8\text{ V}$ or 2.4 V (whichever is greater), unless otherwise noted; typical values are at $T_J = 25^\circ\text{C}$

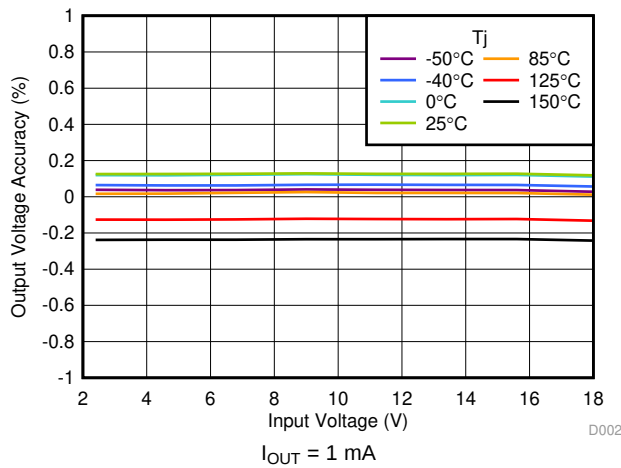


图 1. Line Regulation vs V_{IN}

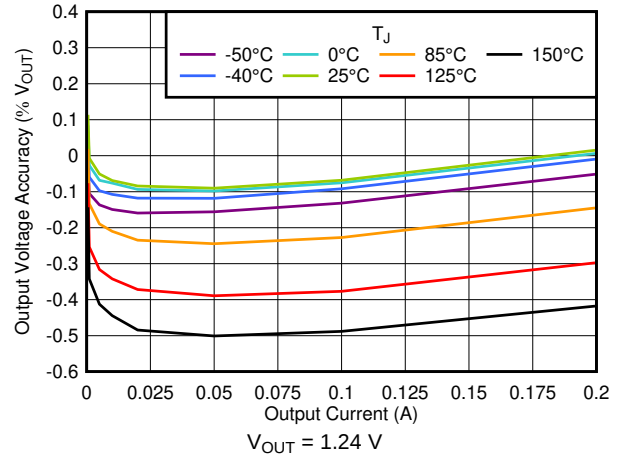


图 2. Load Regulation vs I_{OUT}

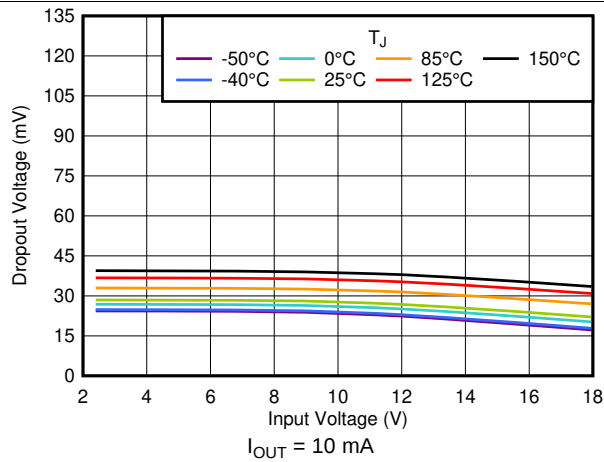


图 3. Dropout Voltage vs V_{IN}

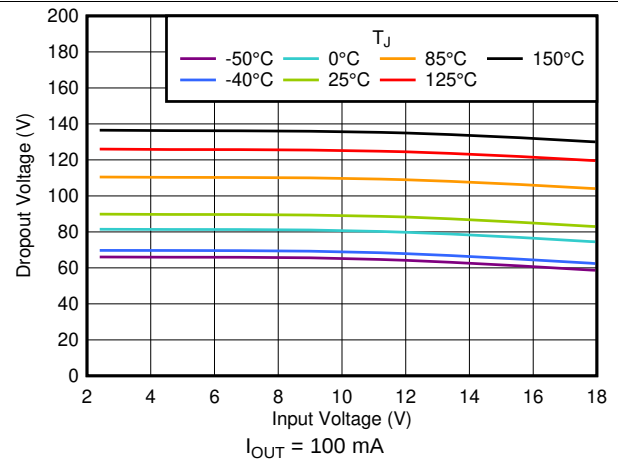


图 4. Dropout Voltage vs V_{IN}

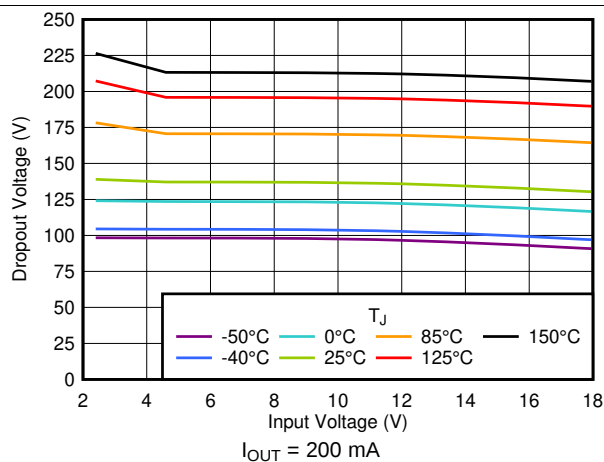


图 5. Dropout Voltage vs V_{IN}

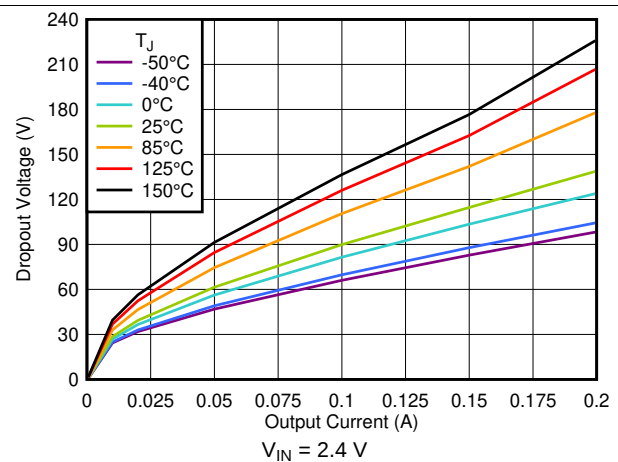


图 6. Dropout Voltage vs I_{OUT}

Typical Characteristics (接下页)

at operating temperature $T_J = 25^\circ\text{C}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 0.9\text{ V}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(\text{typ})} + 0.8\text{ V}$ or 2.4 V (whichever is greater), unless otherwise noted; typical values are at $T_J = 25^\circ\text{C}$

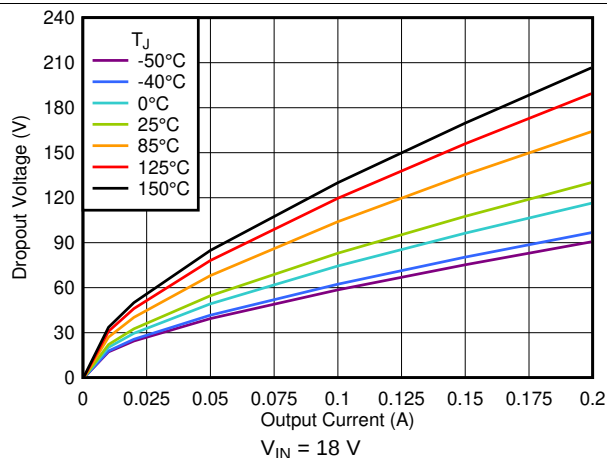


图 7. Dropout Voltage vs I_{OUT}

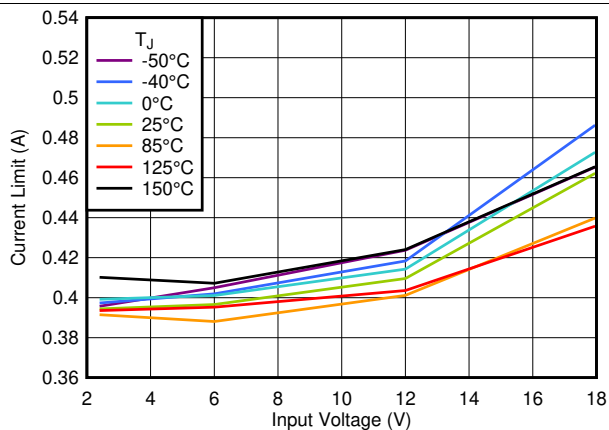


图 8. Current Limit vs V_{IN}

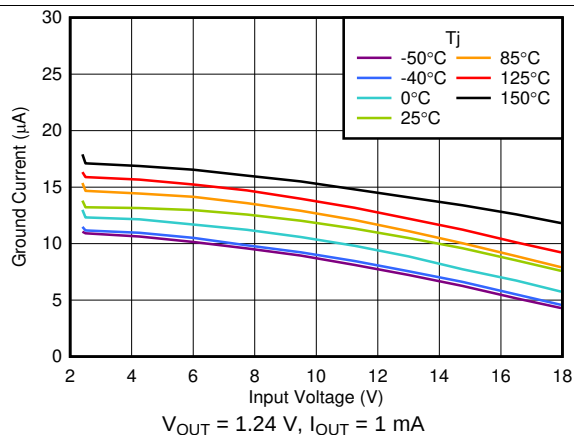


图 9. I_{GND} vs V_{IN}

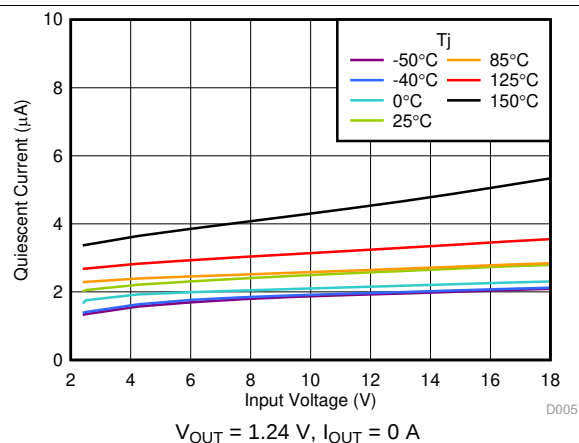


图 10. I_Q vs V_{IN}

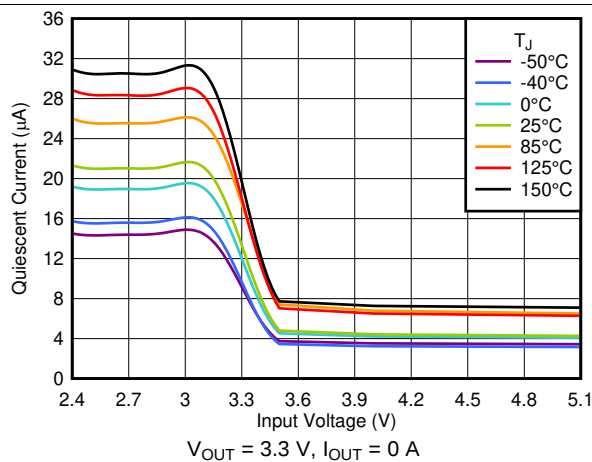


图 11. I_Q vs V_{IN}

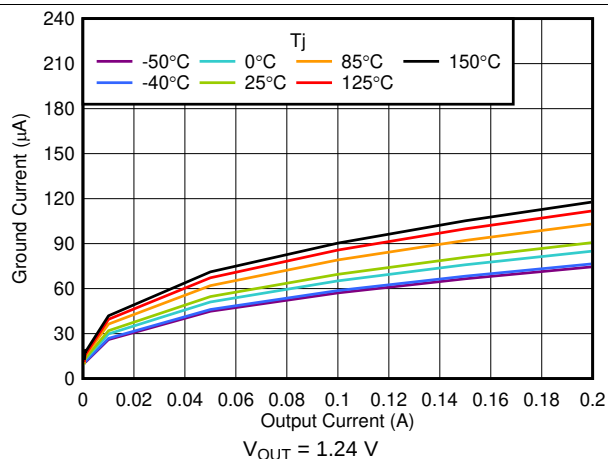


图 12. I_{GND} vs I_{OUT}

Typical Characteristics (接下页)

at operating temperature $T_J = 25^\circ\text{C}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 0.9\text{ V}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(\text{typ})} + 0.8\text{ V}$ or 2.4 V (whichever is greater), unless otherwise noted; typical values are at $T_J = 25^\circ\text{C}$

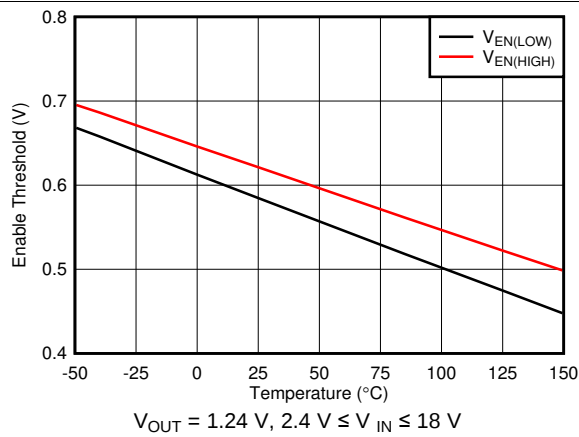


图 13. V_{EN} vs Temperature

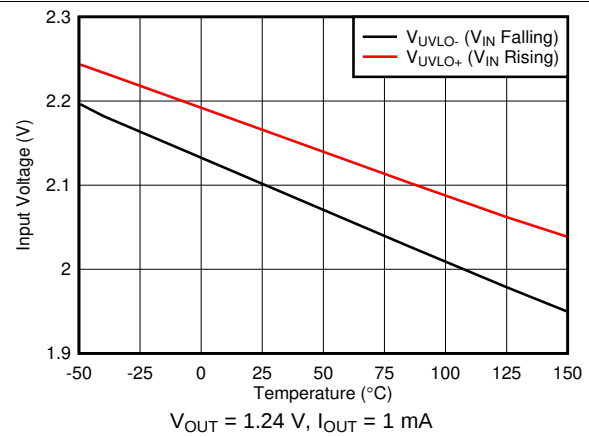


图 14. UVLO Thresholds vs Temperature

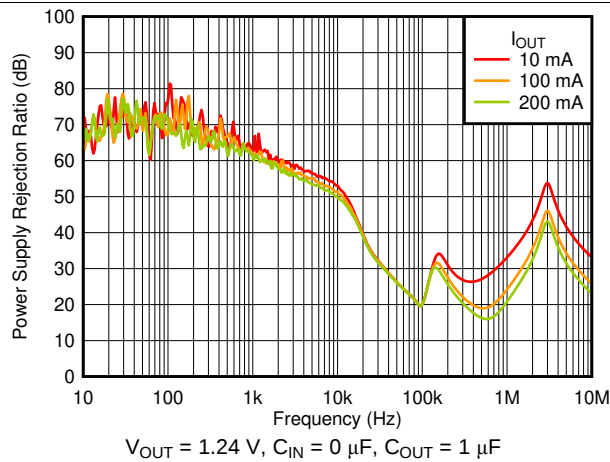


图 15. PSRR vs Frequency and I_{OUT}

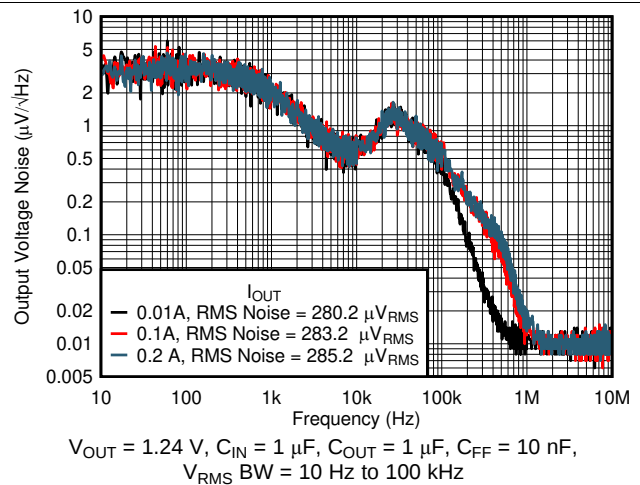


图 16. Output Noise (V_n) vs Frequency and I_{OUT}

7 Detailed Description

7.1 Overview

The TPS7A24 is an 18-V, low quiescent current, low-dropout (LDO) linear regulator. The low I_Q performance makes the TPS7A24 an excellent choice for battery-powered or line-power applications that are expected to meet increasingly stringent standby-power standards. The fixed-output versions have the advantage of providing better accuracy with fewer external components, whereas the adjustable version has the flexibility for a far wider output voltage range.

The 2% accuracy over temperature makes this device an excellent choice for meeting a wide range of microcontroller power requirements.

For increased reliability, the TPS7A24 also incorporates overcurrent, overshoot pulldown, and thermal shutdown protection. The operating junction temperature is -40°C to $+125^{\circ}\text{C}$, and adds margin for applications concerned with higher working ambient temperatures.

7.2 Functional Block Diagrams

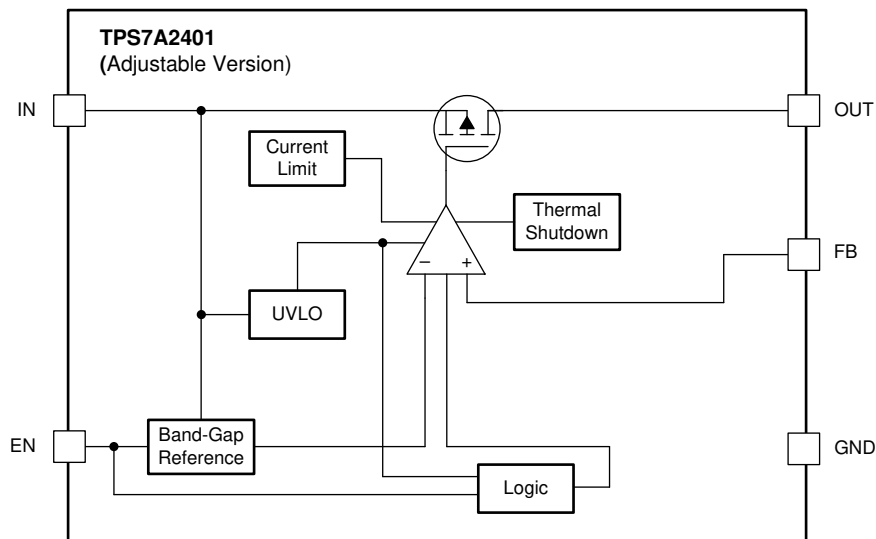


图 17. Adjustable Version Block Diagram

Functional Block Diagrams (continued)

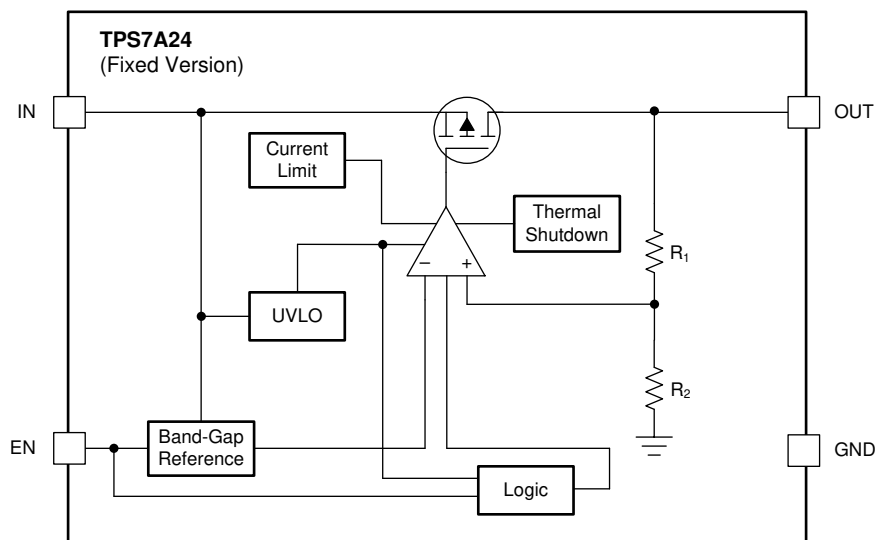


图 18. Fixed Version Block Diagram

7.3 Feature Description

7.3.1 Output Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

7.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use [Equation 1](#) to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

7.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brickwall scheme. In a high-load current fault, the brickwall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application report](#).

Feature Description (continued)

Figure 19 shows a diagram of the current limit.

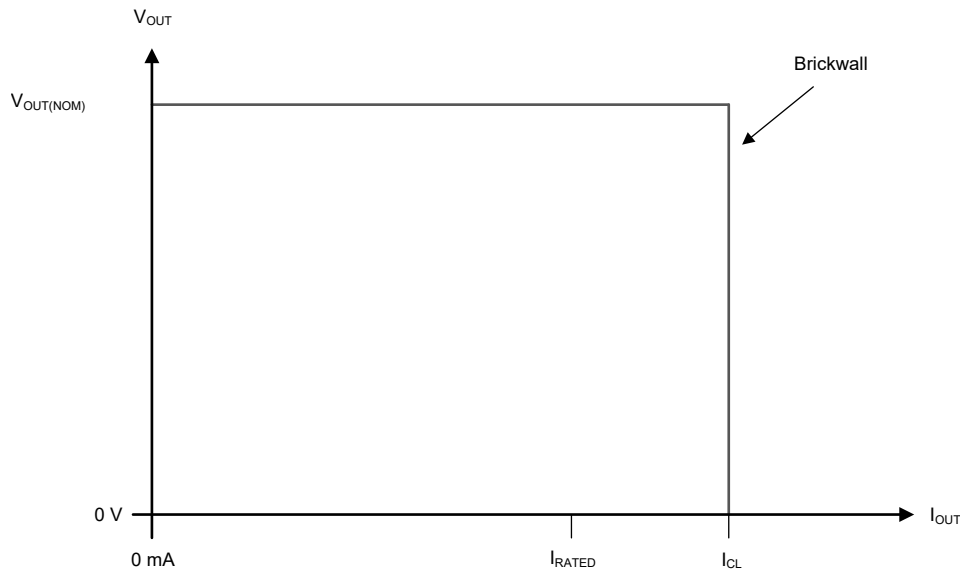


Figure 19. Current Limit

7.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

When the thermal limit is triggered with load currents near the value of the current limit, the output may oscillate prior to the output switching off.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.6 Active Overshoot Pulldown Circuitry

This device has pulldown circuitry connected to V_{OUT} . This circuitry is a 100- μ A current sink, in series with a 5.5-k Ω resistor, controlled by V_{EN} . When V_{EN} is below $V_{EN(LOW)}$, the pulldown circuitry is disabled and the LDO output is in high-impedance mode.

If the output voltage is more than 2% above nominal voltage when $V_{EN} \geq V_{EN(LOW)}$, the pulldown circuitry turns on and the output is pulled down until the output voltage is within 2% from the nominal voltage. This feature helps reduce overshoot during the transient response.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shutdown.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2 , according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

8.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω . A higher value capacitor may be necessary if large, fast load transient or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

The effective output capacitance value is recommended to not exceed 50 μ F.

8.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

Application Information (continued)

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 20 shows one approach for protecting the device.

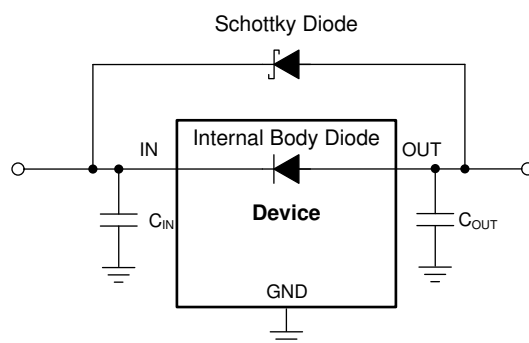


Figure 20. Example Circuit for Reverse Current Protection Using a Schottky Diode

图 21 shows another, more commonly used, approach in high input voltage applications.

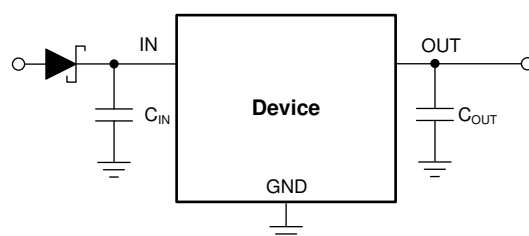


图 21. Reverse Current Prevention Using a Diode Before the LDO

8.1.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the startup time increases. For a detailed description of C_{FF} tradeoffs, see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator](#) application report.

8.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 4 calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

NOTE

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

Application Information (continued)

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to [Equation 5](#), power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (Ψ_{JT}) and junction-to-board characterization parameter (Ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J). As described in , use the junction-to-top characterization parameter (Ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. As described in , use the junction-to-board characterization parameter (Ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D$$

where

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

Application Information (continued)

8.1.8 Special Consideration for Line Transients

During a line transient, the response of this LDO to a very large or fast input voltage change can cause a brief shutdown lasting up to a few hundred microseconds from the voltage transition. This shutdown can be avoided by reducing the voltage step size, increasing the transition time, or a combination of both. 图 22 provides a boundary to follow to avoid this behavior. If necessary, reduce slew rate and the voltage step size to stay below the curve.

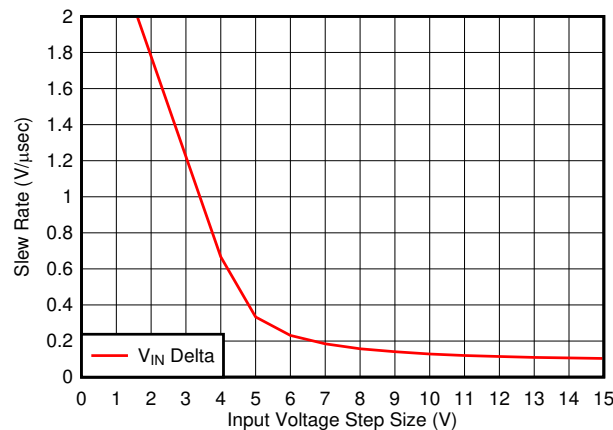


图 22. Recommended Input Voltage Step and Slew Rate in a Line Transient

8.2 Typical Application

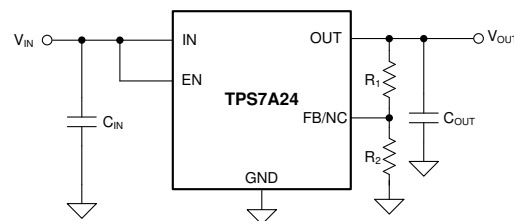


图 23. Generating a 3.3-V Rail From a Multicell Power Bank

8.2.1 Design Requirements

表 2 summarizes the design requirements for 图 23.

表 2. Design Parameters

PARAMETER	DESIGN VALUES
V_{IN}	5.3 V
V_{OUT}	3.3 V $\pm 2\%$
$I_{(IN)}$ (no load)	$< 5 \mu A$
I_{OUT} (max)	200 mA
T_A	57.88°C (max)

8.2.2 Detailed Design Procedure

Select a 3.3-V output, fixed or adjustable device to generate the 3.3-V rail. The fixed-version LDO has internal feedback divider resistors, and thus has lower quiescent current. The adjustable-version LDO requires external feedback divider resistors, and is described in the [Selecting Feedback Divider Resistors](#) section.

8.2.2.1 Transient Response

As with any regulator, increasing the output capacitor value reduces over- and undershoot magnitude, but increases transient response duration.

8.2.2.2 Selecting Feedback Divider Resistors

For this design example, V_{OUT} is set to 5 V. The following equations set the output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (8)$$

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (9)$$

For improved output accuracy, use [Equation 9](#) and $I_{FB(TYP)} = 10$ nA as listed in the [Electrical Characteristics](#) table to calculate the upper limit for series feedback resistance, $R_1 + R_2 \leq 5$ M Ω .

The control-loop error amplifier drives the FB pin to the same voltage as the internal reference ($V_{FB} = 1.24$ V as listed in the [Electrical Characteristics](#) table). Use [Equation 8](#) to determine the ratio of $R_1 / R_2 = 1.66$. Use this ratio and solve [Equation 9](#) for R_2 . Now calculate the upper limit for $R_2 \leq 1.24$ M Ω . Select a standard value resistor of $R_2 = 1.18$ M Ω .

Reference [Equation 8](#) and solve for R_1 :

$$R_1 = (V_{OUT} / V_{FB} - 1) \times R_2 \quad (10)$$

From [公式 10](#), $R_1 = 1.96$ M Ω can be determined. From [Equation 8](#), select $V_{OUT} = 3.299$ V.

8.2.2.3 Thermal Dissipation

Junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use [公式 11](#) to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A), as [公式 12](#) shows, to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (11)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (12)$$

[公式 13](#) calculates the maximum ambient temperature. [公式 14](#) calculates the maximum ambient temperature for typical design applications.

$$T_{A(MAX)} = T_{J(MAX)} - (R_{\theta JA} \times P_D) \quad (13)$$

$$T_{A(MAX)} = 125^\circ\text{C} - [167.8^\circ\text{C/W} \times (5.3\text{ V} - 3.3\text{ V}) \times 0.2\text{ A}] = 57.88^\circ\text{C} \quad (14)$$

8.2.3 Application Curve

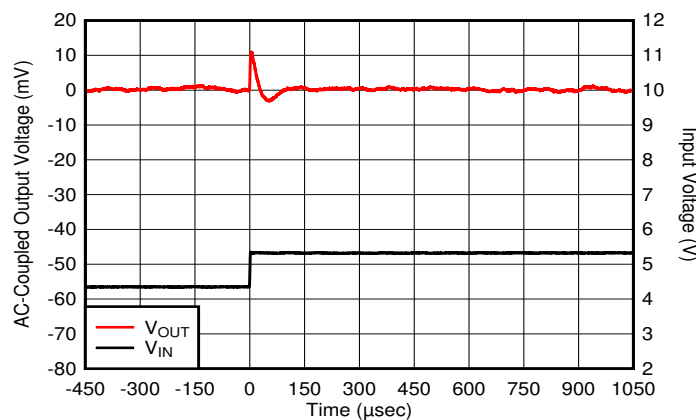


图 24. Line Transient (4.3 V to 5.3 V)

9 Power Supply Recommendations

The device is designed to operate with an input supply range of 2.4 V to 18 V. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance. Connect a low output impedance power supply to the input pin of the TPS7A24. In order to optimize regulation, refer to the [Feature Description](#) section for more information on operation modes and performance features.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device pins as possible
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device to distribute heat

10.2 Layout Examples

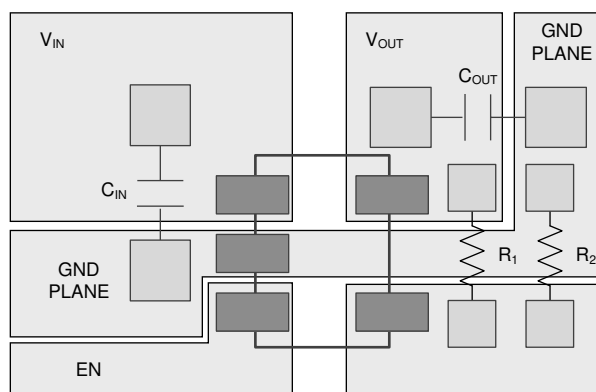
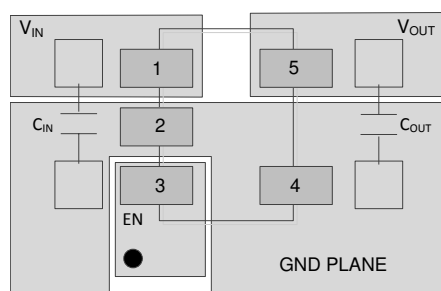


图 25. Adjustable Version Layout Example



● Represents via used for application specific connections

图 26. Fixed Version Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

表 3. 器件命名规则⁽¹⁾

产品	V _{OUT}
TPS7A24xx(x)yyyz	xx(x) 是标称输出电压。对于分辨率为 100mV 的输出电压，订购编号使用两位数字；对于分辨率为 50mV 的输出电压，则使用三位数字（例如，28 = 2.8V；125 = 1.25V）。01 表示可调节输出版本。 yyy 为封装标识符。 z 为封装数量。R 表示大数量卷带

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹，此文件夹位于www.ti.com.cn内。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A2401DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1XFF	Samples
TPS7A24125DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1XTF	Samples
TPS7A2418DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1XLF	Samples
TPS7A2425DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1XKF	Samples
TPS7A2430DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1XJF	Samples
TPS7A2433DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1XHF	Samples
TPS7A2436DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1XIF	Samples
TPS7A2450DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1XGF	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2401DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2401DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A24125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A24125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2418DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2418DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2425DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2425DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2430DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2430DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2433DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2433DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2436DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2436DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2450DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2450DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A2401DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2401DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A24125DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A24125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2418DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2418DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2425DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2425DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2430DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2430DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2433DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2433DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2436DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2436DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2450DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2450DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

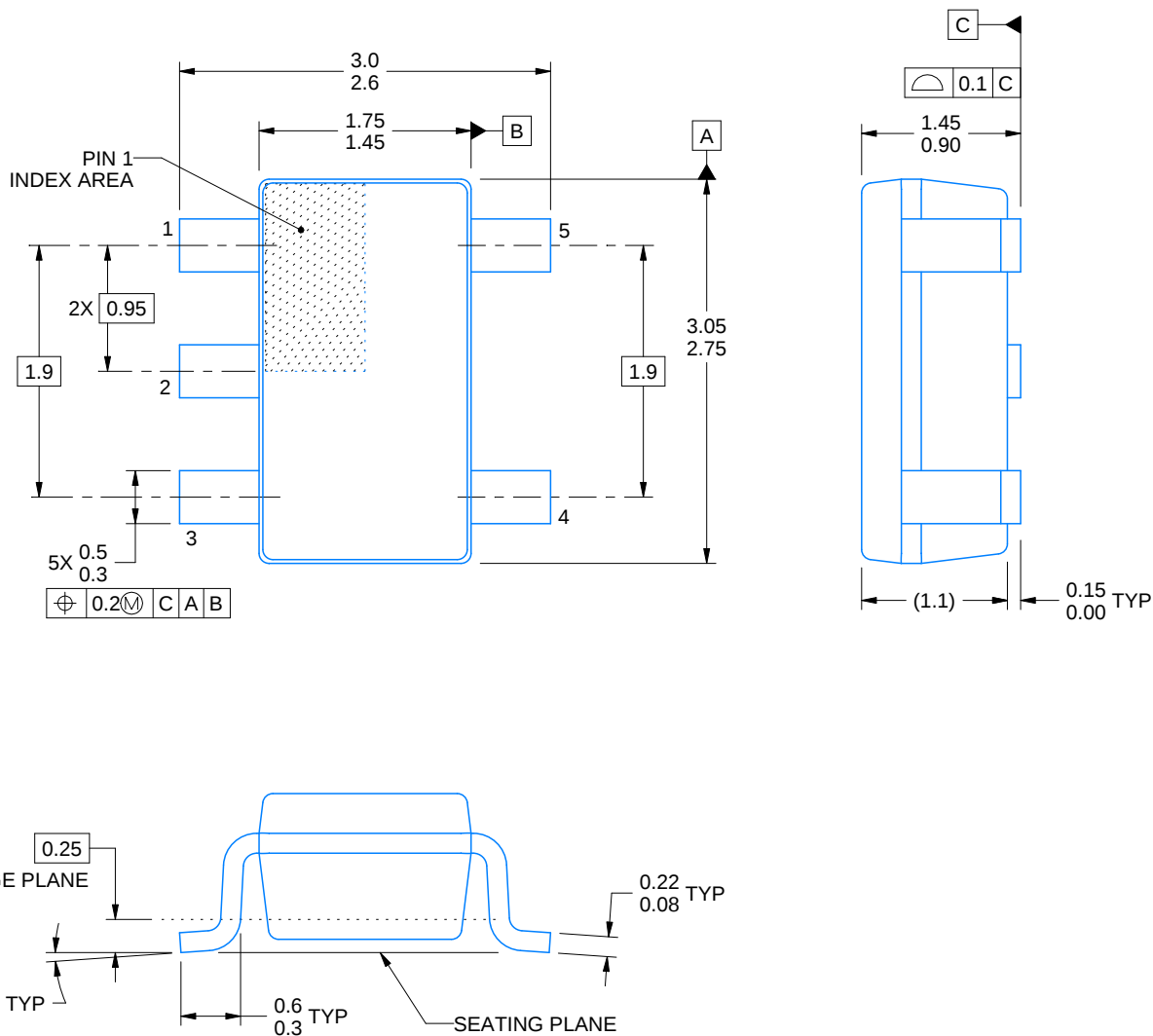


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

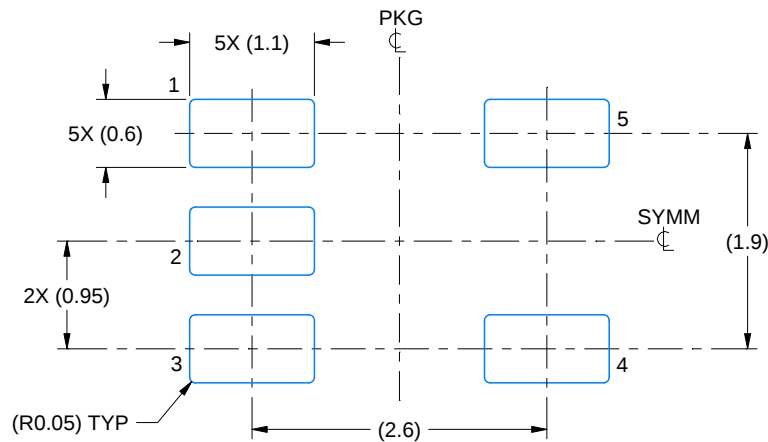
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

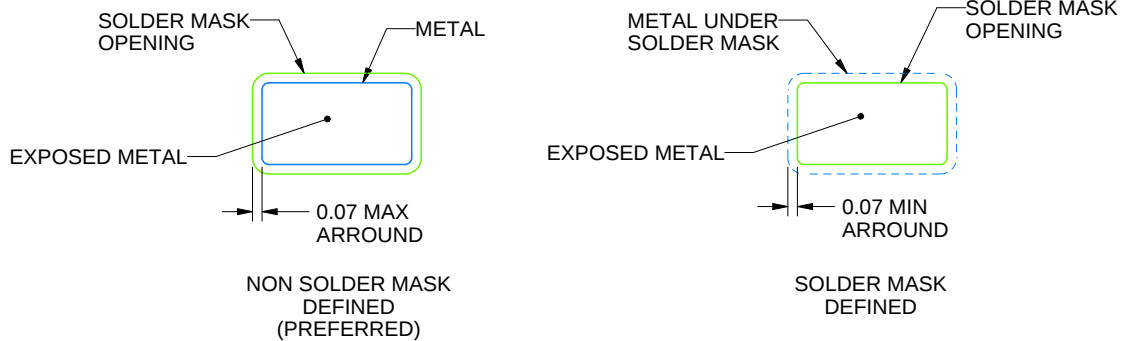
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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