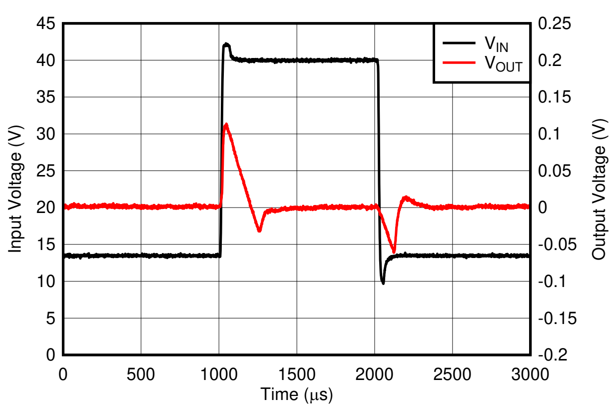
TPS7B88-Q1 500mA、40V、低压降稳压器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
  - 结温：–40°C 至 +150°C，T_J
- 输入电压范围：3V 至 40V（最大 42V）
- 输出电压范围：3.3V 和 5V（固定）
- 最大输出电流：500mA
- 输出电压精度：±1.15%（最大值）
- 低压降：
  - 450mA 时为 525mV（最大值）
- 低静态电流：
  - 轻负载时典型值为 17μA
- 出色的线路瞬态响应：
  - 冷启动时出现 ±2% V_{OUT} 偏差
  - ±2% V_{OUT} 偏差（V_{IN} 压摆率 1V/μs）
- 与 2.2μF 或更高的电容器搭配使用时可保持稳定
- 3 引脚 TO-252 封装：($R_{\theta JA}$)：30°C/W

2 应用

- 可重新配置仪表组
- 车身控制模块 (BCM)
- 常开型电池连接应用：
  - 汽车网关
  - 远程免钥匙进入 (RKE)



线路瞬态响应（V_{IN} 压摆率 3V/μs）

3 说明

TPS7B88-Q1 是一款低压降线性稳压器，专用于连接汽车应用中的电池。该器件的输入电压范围高达 40V，因此可承受汽车系统可能发生的瞬变（如负载突降）。此器件在轻负载下的静态电流仅为 17μA，是为备用系统中微控制器 (MCU) 和控制器局域网 (CAN) 收发器等常开型器件供电的出色解决方案。

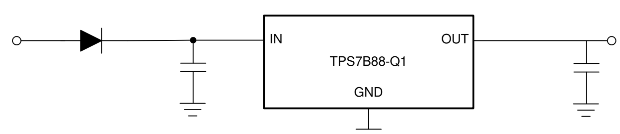
该器件具有先进的瞬态响应，因此输出端可对负载或线路变化（例如，在冷启动条件下）作出迅速响应。此外，该器件架构新颖，可在从电压跌落恢复过程中最大限度降低输出过冲幅度。正常运行时，该器件可在整个线路、负载和温度范围内维持 ±1.15% 的直流精度。

该器件采用导热封装，可将热量高效传导到电路板上。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7B88-Q1	TO-252 (3)	6.60mm × 6.10mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



输出等于基准电压

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
January 2021	*	Initial Release

5 Pin Configuration and Functions

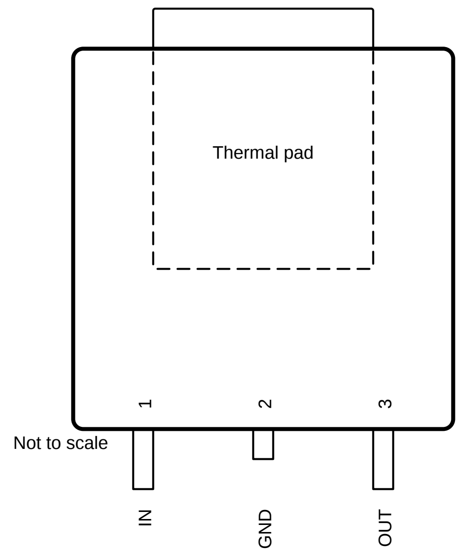


图 5-1. KVU Package, 3-Pin TO-252, Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	KVU		
GND	2	G	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
IN	1	P	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input Capacitor* section. Place the input capacitor as close to the input of the device as possible
OUT	3	O	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Output Capacitor* section. Place the output capacitor as close to output of the device as possible. If using a high ESR capacitor, decouple the output with a 100-nF ceramic capacitor.
Thermal pad	Pad	—	Connect the thermal pad to a large area GND plane for improved thermal performance.

(1) I = input; O = output; P = power; G = ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{IN}	Unregulated input	–0.3	42	V
V_{OUT}	Regulated output	–0.3	V_{IN} + 0.3 V[(2)]	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. Theseare stress ratings only and functional operation of the device at these or any other conditionsbeyond those indicated under *recommended operating conditions* isnot implied. Exposure to absolute-maximum-rated conditions for extended periods may affect devicereliability.
(2) The absolute maximum rating is VIN + 0.3 V or 20 V, whichever is smaller

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	3		40	V
V_{OUT}	Output voltage	1.2		18	V
I_{OUT}	Output current	0		500	mA
C_{OUT}	Output capacitor[(2)]	2.2		220	µF
ESR	Output capacitor ESR requirements	0.001		2	Ω
C_{IN}	Input capacitor[(1)]	0.1	1		µF
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance is 500 nF.
(2) Effective output capacitance of 1 µF minimum required for stability.

6.4 Thermal Information

THERMAL METRIC[(1)] [(2)]		TPS7B88-Q1 KVU 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) The thermal data is based on the JEDEC standard high K profile,JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered tothe thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics,see the Semiconductor and IC PackageThermal Metrics application report.

6.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF typical values are at T_J = 25°C

PARAMETER		Test Conditions	MIN	TYP	MAX	UNIT
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 100 µA to 450 mA, T_J = 25ºC(1)	–0.85		0.85	%
		V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 100 µA to 500 mA, T_J = 25ºC(1)	–0.85		0.85	
		V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 100 µA to 450 mA(1)	–1.15		1.15	
		V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 100 µA to 500 mA(1)	–1.15		1.15	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	V_{IN} = V_{OUT} + 1 V, I_{OUT} = 100 µA to 450 mA , V_{OUT} ⩾ 3.3 V			0.425	%
		V_{IN} = V_{OUT} + 1 V, I_{OUT} = 100 µA to 500 mA , V_{OUT} ⩾ 3.3 V			0.45	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 100 µA			0.2	%
ΔV_{OUT}	Load transient response settling time	t_R = t_F = 1 µs; C_{OUT} = 10 µF, V_{OUT} ⩾ 3.3V			100	µs
ΔV_{OUT}	Load transient response overshoot, undershoot(2)	t_R = t_F = 1 µs; C_{OUT} = 10 µF; I_{OUT} = 150 mA to 350 mA	–2%			$\%V_{OUT}$
		t_R = t_F = 1 µs; C_{OUT} = 10 µF; I_{OUT} = 350 mA to 150 mA			10%	
		t_R = t_F = 1 µs; C_{OUT} = 10 µF; I_{OUT} = 0 mA to 500 mA	–10%			
I_Q	Quiescent current	V_{IN} = V_{OUT} + 1 V to 40V, I_{OUT} = 0 mA, T_J = 25ºC(3)		17	21	µA
		V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 0 mA(3)			26	
		I_{OUT} = 500 µA			35	
V_{DO}	Dropout voltage fixed output voltages (KVU Package)	I_{OUT} ⩽ 1 mA, V_{OUT} ⩾ 3.3 V, V_{IN} = $V_{OUT(NOM)}$ x 0.95			46	mV
		I_{OUT} = 315 mA, V_{OUT} ⩾ 3.3 V, V_{IN} = $V_{OUT(NOM)}$		275	400	
		I_{OUT} = 450 mA, V_{OUT} ⩾ 3.3 V, V_{IN} = $V_{OUT(NOM)}$		360	525	
		I_{OUT} = 500 mA, V_{OUT} ⩾ 3.3 V, V_{IN} = $V_{OUT(NOM)}$		390	575	
$V_{UVLO(RISING)}$	Rising input supply UVLO	V_{IN} rising	2.6	2.7	2.82	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO	V_{IN} falling	2.38	2.5	2.6	V
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ hysteresis			230		mV
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 1 V, V_{OUT} short to 90% x $V_{OUT(NOM)}$	540		780	mA
PSRR	Power supply rejection ratio	V_{IN} - V_{OUT} = 1 V, frequency = 1 kHz, I_{OUT} = 450 mA		70		dB
T_J	Junction temperature		–40		150	°C
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			20		°C

(1) Power dissipation is limited to 2 W for device production testing purposes. The power dissipation can be higher during normal operation. See the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150℃.
(2) Specified by design.
(3) For the adjustable output this is tested in unity gain and resistor current is not included.

6.6 Typical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 μA, C_{OUT} = 2.2 μF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 μF (unless otherwise noted)

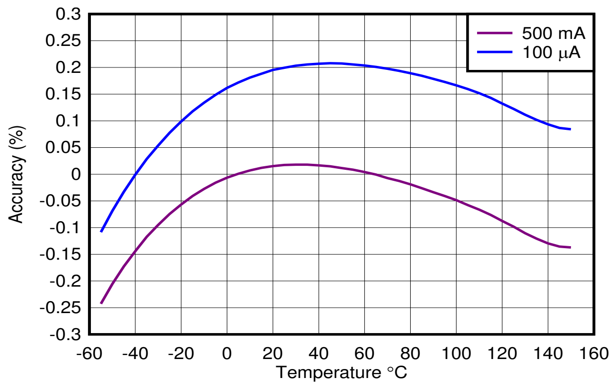
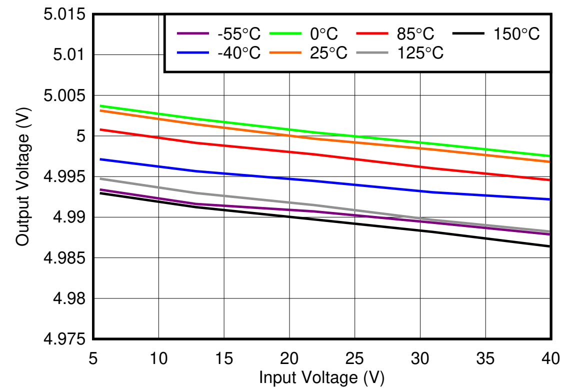
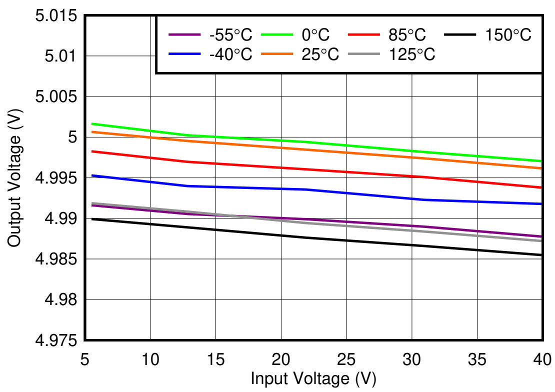


图 6-1. Accuracy vs Temperature



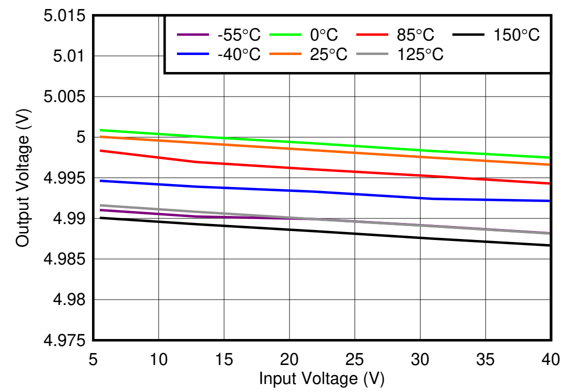
V_{OUT} = 5 V, I_{OUT} = 150 mA

图 6-2. Line Regulation vs V_{IN}



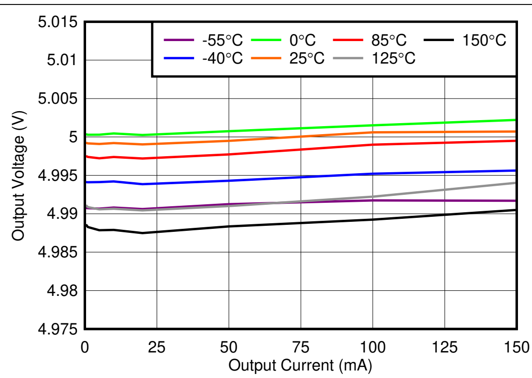
V_{OUT} = 5 V, I_{OUT} = 5 mA

图 6-3. Line Regulation vs V_{IN}



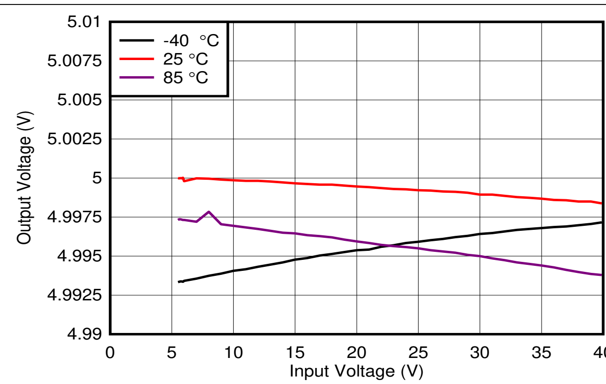
V_{OUT} = 5 V, I_{OUT} = 1 mA

图 6-4. Line Regulation vs V_{IN}



V_{OUT} = 5 V

图 6-5. Load Regulation vs I_{OUT}

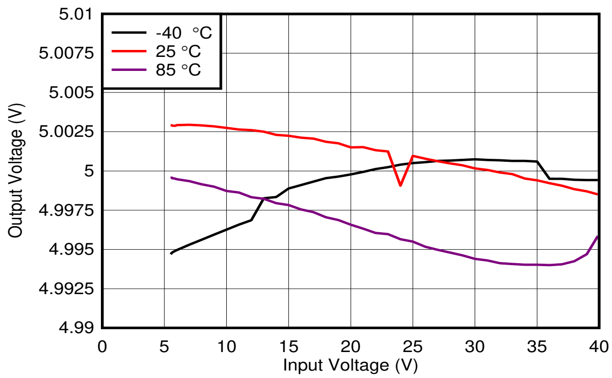


C_{OUT} = 10 μF, V_{OUT} = 5 V

图 6-6. Line Regulation at 50 mA

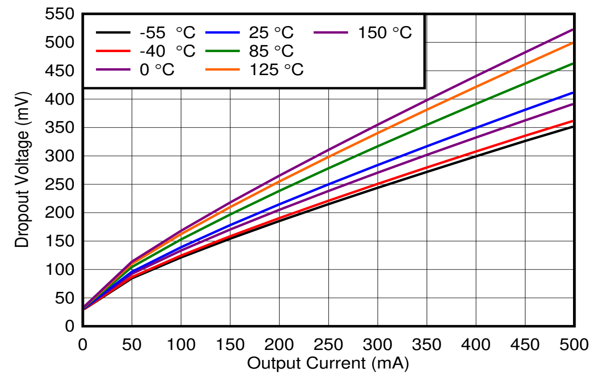
6.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 μA, C_{OUT} = 2.2 μF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 μF (unless otherwise noted)



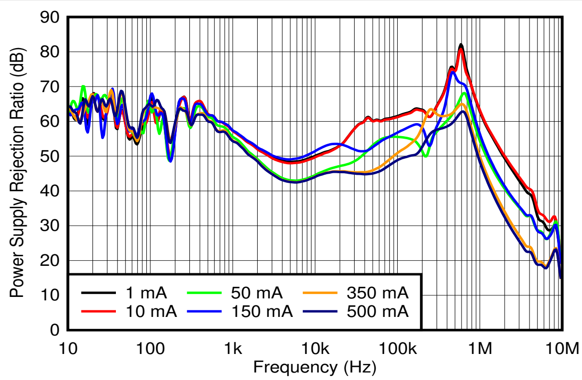
C_{OUT} = 10 μF, V_{OUT} = 5 V

图 6-7. Line Regulation at 100 mA



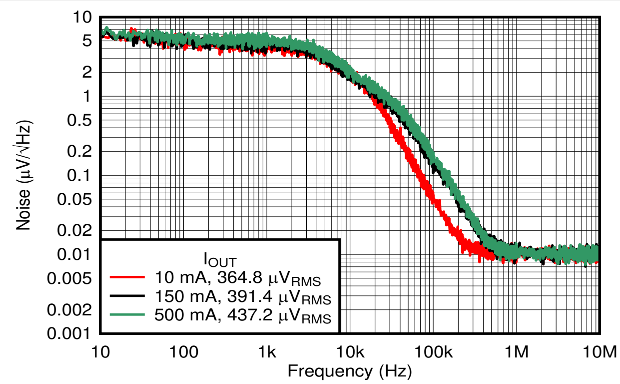
V_{IN} = 3 V

图 6-8. Dropout Voltage (V_{DO}) vs I_{OUT}



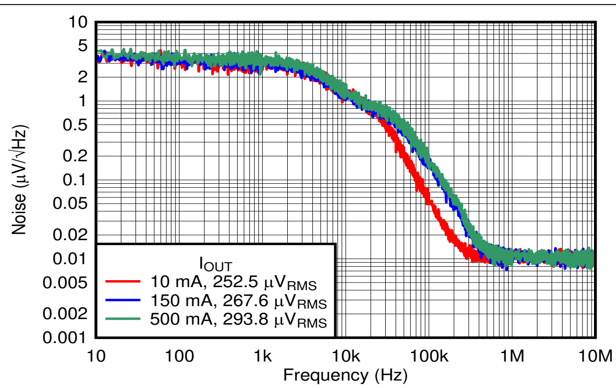
C_{OUT} = 10 μF (X7R 50 V), V_{OUT} = 5 V

图 6-9. PSRR vs Frequency and I_{OUT}



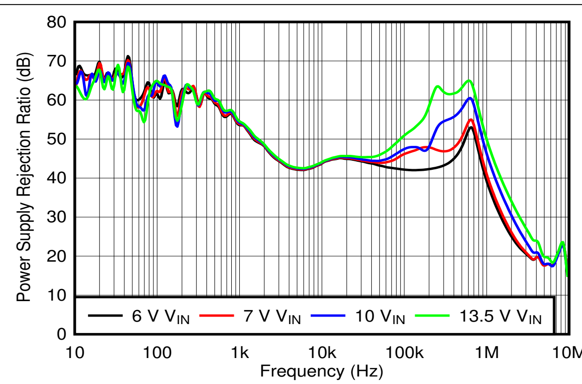
C_{OUT} = 10 μF (X7R 50 V), V_{OUT} = 5 V

图 6-10. Noise vs Frequency



C_{OUT} = 10 μF (X7R 50 V), V_{OUT} = 3.3 V

图 6-11. Noise vs Frequency

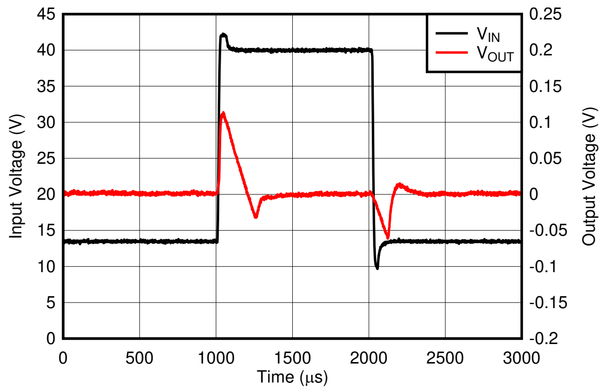


C_{OUT} = 10 μF (X7R 50 V), I_{OUT} = 500 mA, V_{OUT} = 5 V

图 6-12. PSRR vs Frequency and V_{IN}

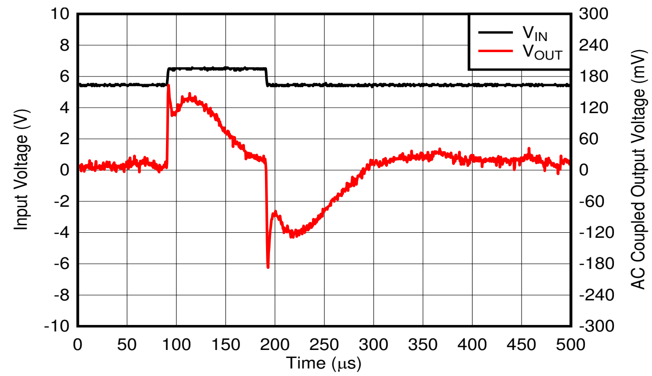
6.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF (unless otherwise noted)



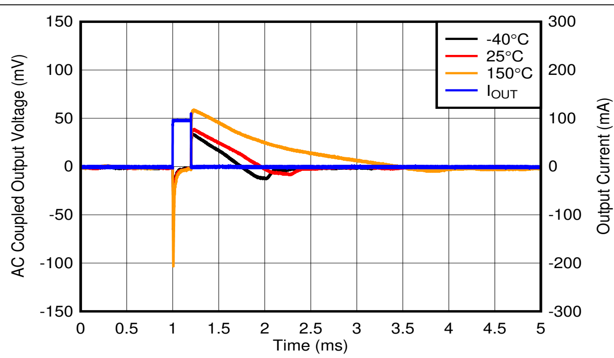
V_{OUT} = 5 V, I_{OUT} = 1 mA, V_{IN} = 13.5 V to 45 V, slew rate = 2.7 V/µs

图 6-13. Line Transients



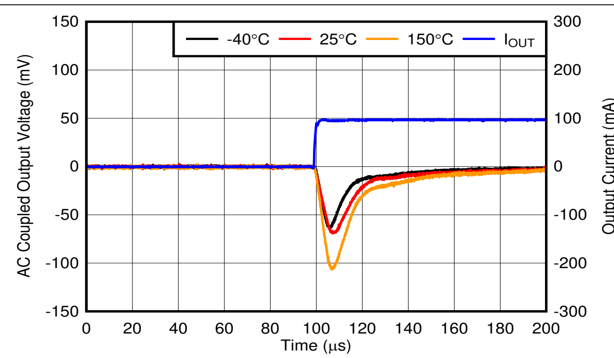
V_{OUT} = 5 V, I_{OUT} = 100 mA, V_{IN} = 5.5 V to 6.5 V, rise time = 1 µs

图 6-14. Line Transients



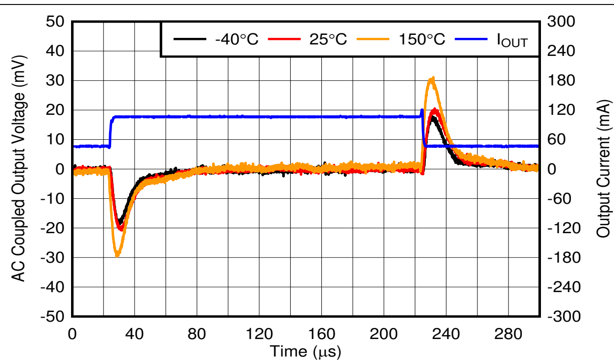
V_{OUT} = 5 V, I_{OUT} = 0 mA to 100 mA, slew rate = 1 A/µs, C_{OUT} = 10 µF

图 6-15. Load Transient, No Load to 100 mA



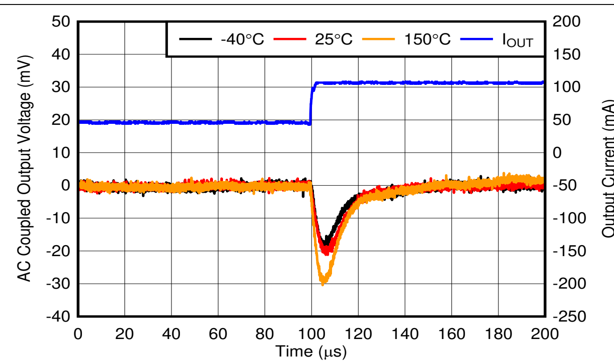
V_{OUT} = 5 V, I_{OUT} = 0 mA to 100 mA, slew rate = 1 A/µs, C_{OUT} = 10 µF

图 6-16. Load Transient, No Load to 100-mA Rising Edge



V_{OUT} = 5 V, I_{OUT} = 45 mA to 105 mA, slew rate = 0.1 A/µs, C_{OUT} = 10 µF

图 6-17. Load Transient, 45 mA to 105 mA

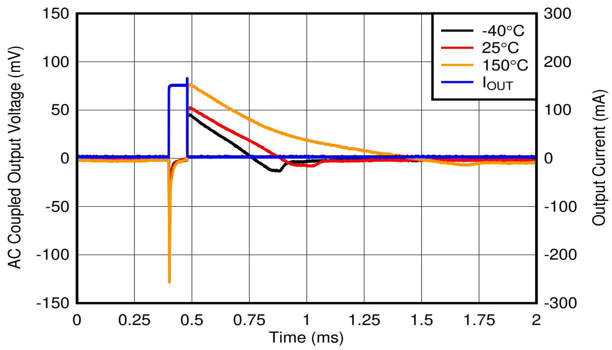


V_{OUT} = 5 V, I_{OUT} = 45 mA to 105 mA, slew rate = 0.1 A/µs, C_{OUT} = 10 µF

图 6-18. Load Transient, 45-mA to 105-mA Rising Edge

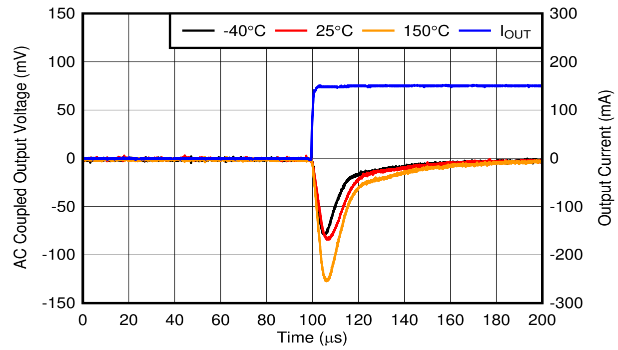
6.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF (unless otherwise noted)



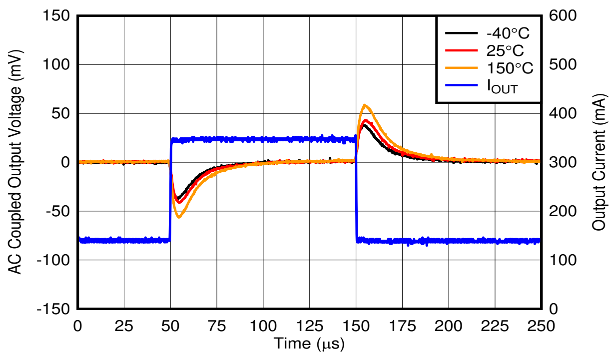
V_{OUT} = 5 V, I_{OUT} = 0 mA to 150 mA, slew rate = 1 A/µs, C_{OUT} = 10 µF

图 6-19. Load Transient, No Load to 150-mA



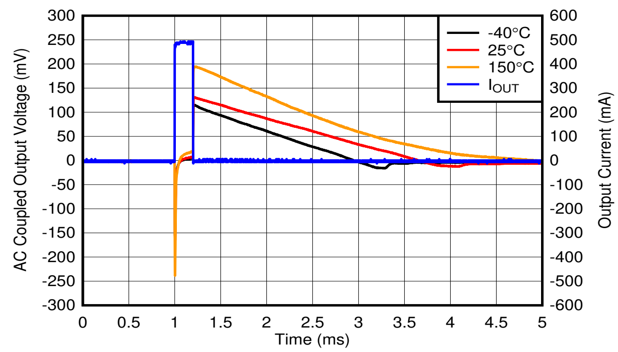
V_{OUT} = 5 V, I_{OUT} = 0 mA to 150 mA, slew rate = 1 A/µs, C_{OUT} = 10 µF

图 6-20. Load Transient, No Load to 150-mA Rising Edge



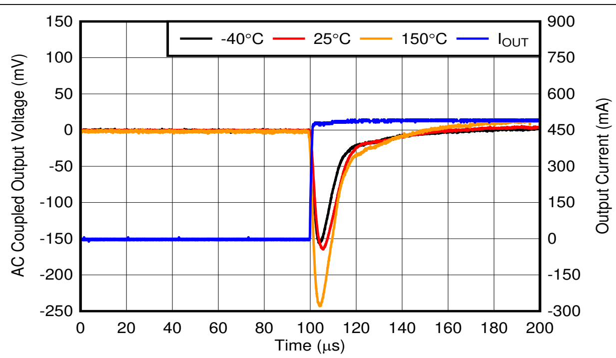
V_{OUT} = 5 V, I_{OUT} = 150 mA to 350 mA, slew rate = 0.1 A/µs, C_{OUT} = 10 µF

图 6-21. Load Transient, 150-mA to 350-mA



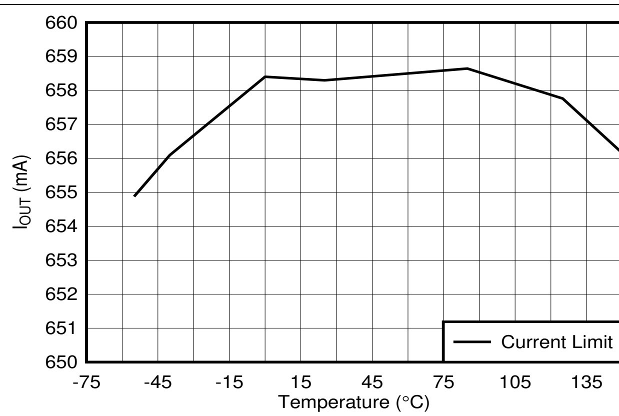
V_{OUT} = 5 V, I_{OUT} = 0 mA to 500 mA, slew rate = 1 A/µs, C_{OUT} = 10 µF

图 6-22. Load Transient, No Load to 500 mA



V_{OUT} = 5 V, I_{OUT} = 0 mA to 500 mA, slew rate = 1 A/µs, C_{OUT} = 10 µF

图 6-23. Load Transient, No Load to 500-mA Rising Edge



V_{IN} = V_{OUT} + 1 V, V_{OUT} = 90% × $V_{OUT(NOM)}$

图 6-24. Output Current Limit vs Temperature

6.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF (unless otherwise noted)

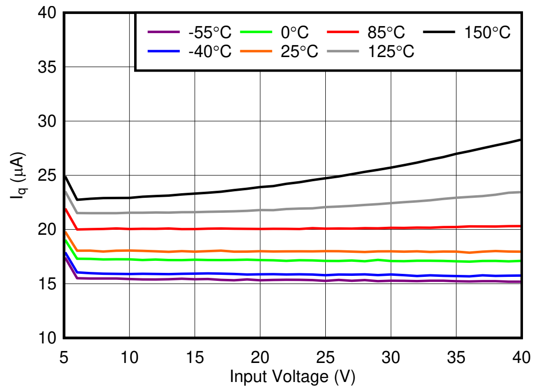
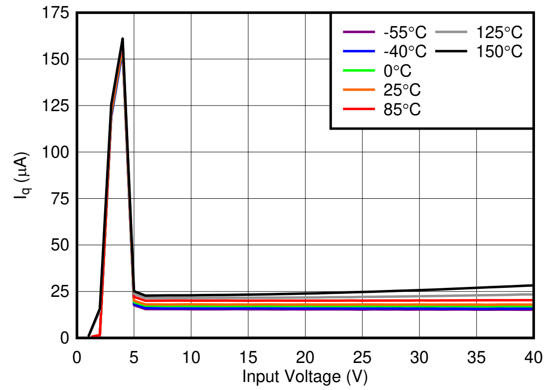


图 6-25. Quiescent Current (I_Q) vs V_{IN}



V_{OUT} = 5 V

图 6-26. Quiescent Current (I_Q) vs V_{IN}

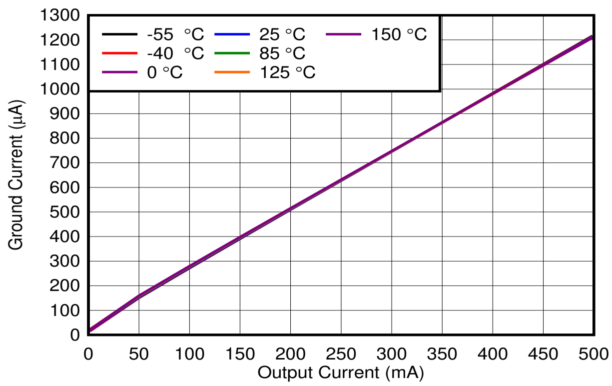


图 6-27. Ground Current (I_{GND}) vs I_{OUT}

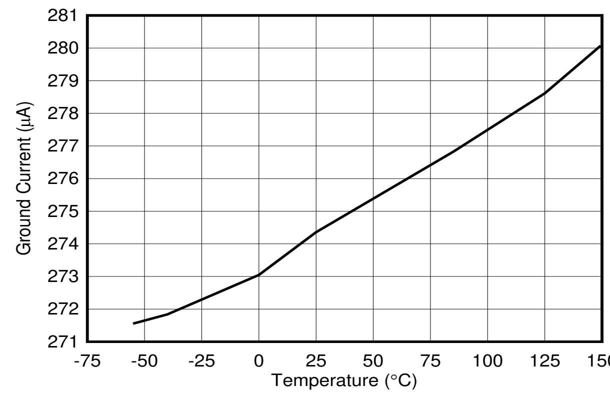


图 6-28. Ground Current at 100 mA

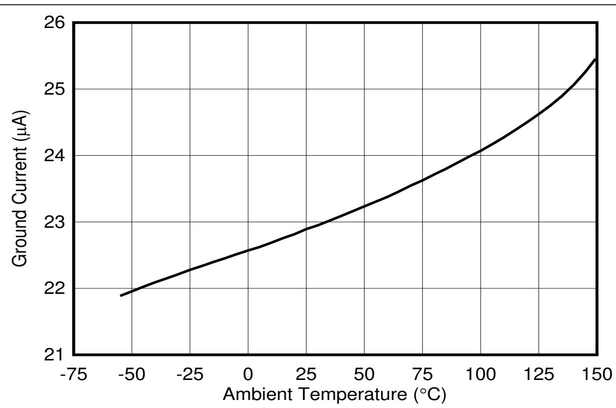
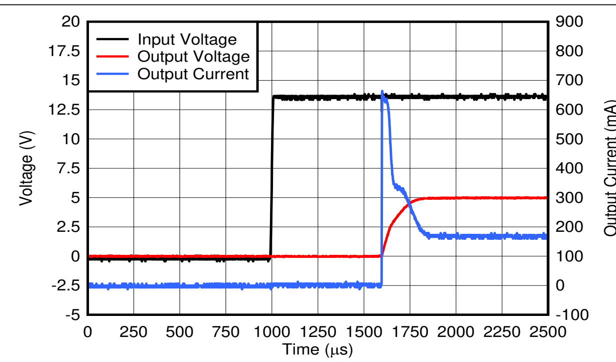


图 6-29. Ground Current at 500 µA



V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 150 mA, C_{OUT} = 10 µF

图 6-30. Startup Plot Inrush Current

6.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF (unless otherwise noted)

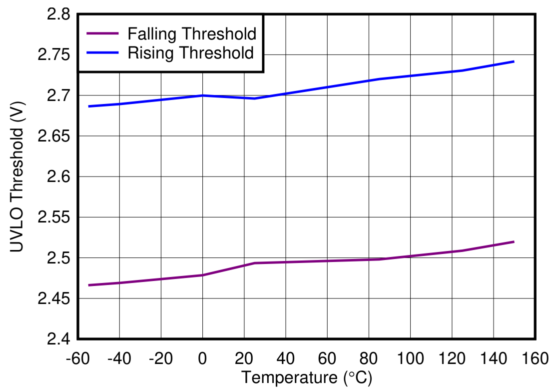


图 6-31. Undervoltage Lockout (UVLO) Threshold vs Temperature

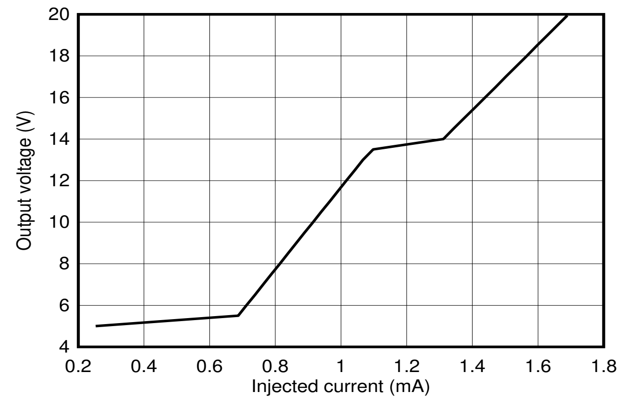


图 6-32. Output Voltage vs Injected Current

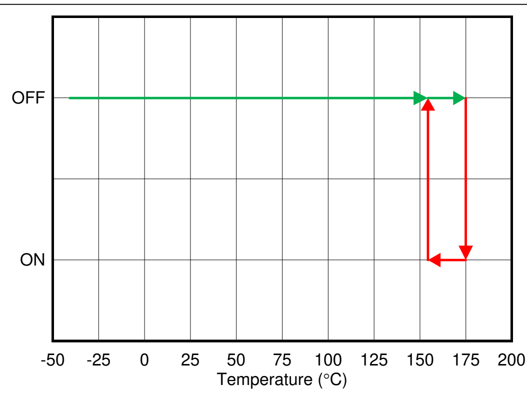


图 6-33. Thermal Shutdown

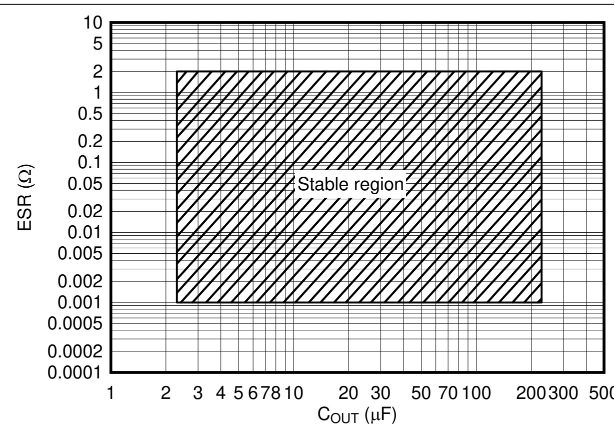


图 6-34. Stability, ESR vs C_{OUT}

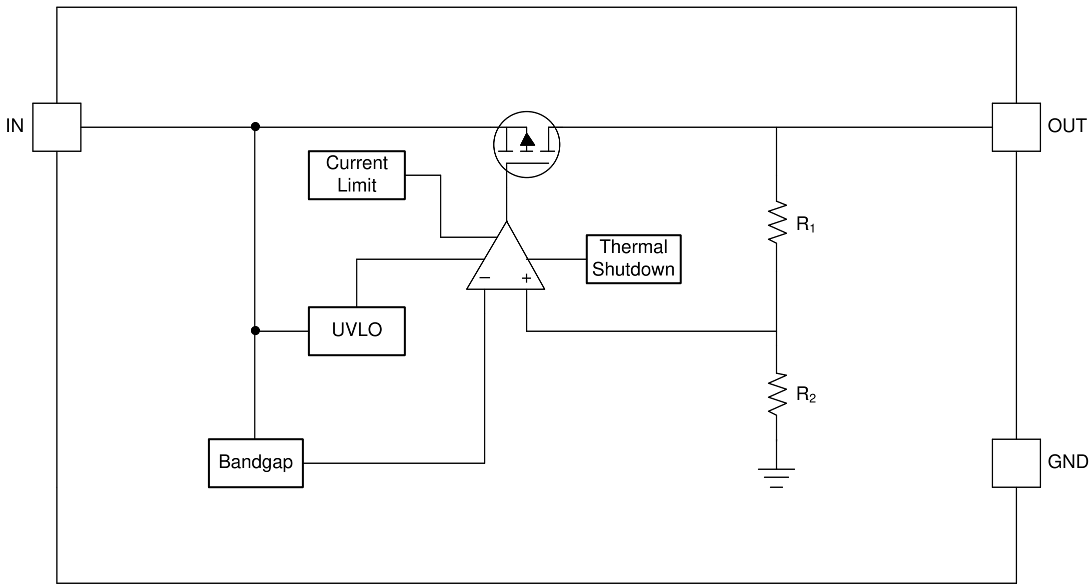
7 Detailed Description

7.1 Overview

The TPS7B88-Q1 is a low-dropout linear regulator (LDO) with improved transient performance that allows for quick response to changes in line or load conditions. The device aslo features a novel output overshoot reduction feature that minimizes output overshoot during cold-crank conditions.

During normal operation, the device has a tight DC accuracy of ±1.15% over line, load, and temperature. The increased accuracy allows for the powering of sensitive analog loads or sensors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.2 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brickwall scheme. In a high-load current fault, the brickwall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

图 7-1 shows a diagram of the current limit.

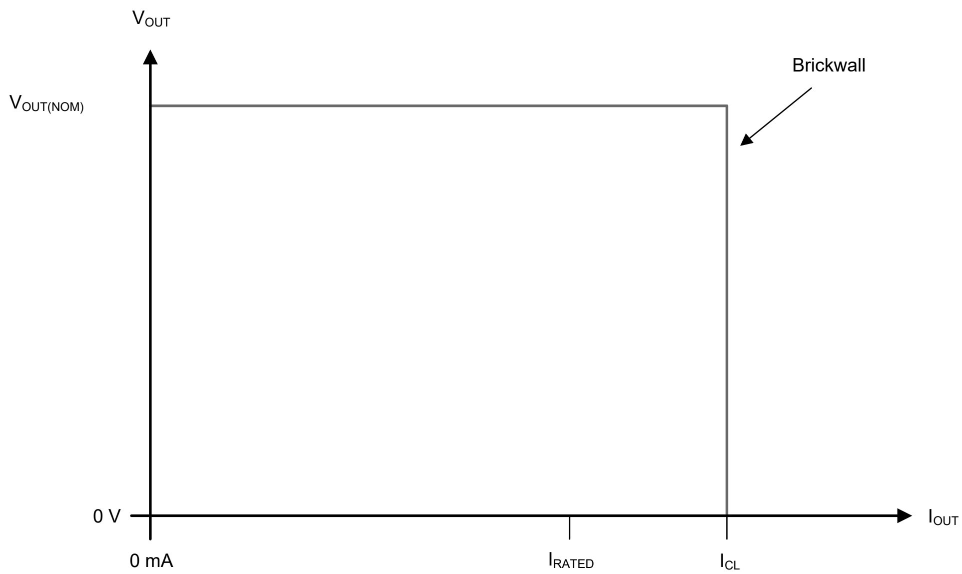


图 7-1. Current Limit

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the input voltage below the UVLO falling threshold (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shutdown.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TPS7B88-Q1 requires an output capacitor of 2.2 µF or larger (1 µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 2 Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

8.1.3 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leqslant V_{IN}$ + 0.3 V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

8.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{2}$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{3}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.4.1 Power Dissipation Versus Ambient Temperature

图 8-1 is based off of a JESD51-7 4-layer, high-K board. The allowable power dissipation was estimated using the following equation. As disscussed in the *An empirical analysis of the impact of board layout on LDO thermal performance* application report, thermal dissipation can be improved in the JEDEC high-K layout by adding top layer copper and increasing the number of thermal vias. If a good thermal layout is used, the allowable thermal dissipation can be improved by up to 50%.

$$T_A + R_{\theta JA}\, x\, P_D \leq 150\,°C \tag{4}$$

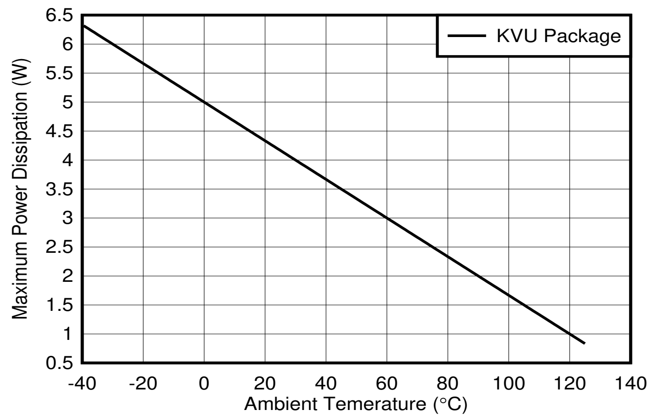


图 8-1. TPS7B88-Q1 Allowable Power Dissipation

8.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{5}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \tag{6}$$

where

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.2 Typical Application

图 8-2 shows a typical application circuit for the TPS7B88-Q1. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

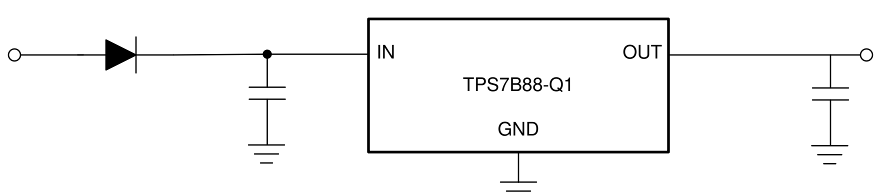


图 8-2. Typical Application Schematic for the TPS7B88-Q1

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6 V to 40 V
Output voltage	5 V
Output current	350 mA
Output capacitor	10 µF

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 1 µF. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value must be between 2.2 µF and 200 µF and the ESR range must be between 1 mΩ and 2 Ω. For this design, a low ESR, 10-µF ceramic capacitor was used to improve transient performance.

8.2.3 Application Curves

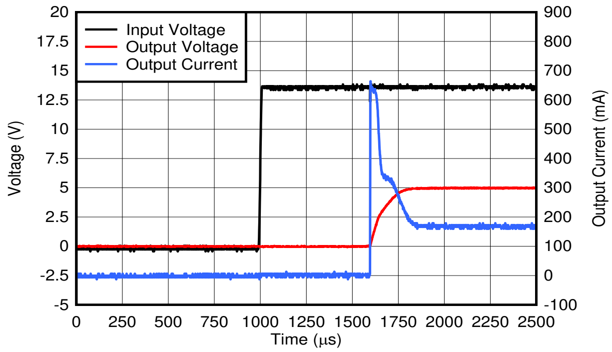


图 8-3. Power-Up Waveform

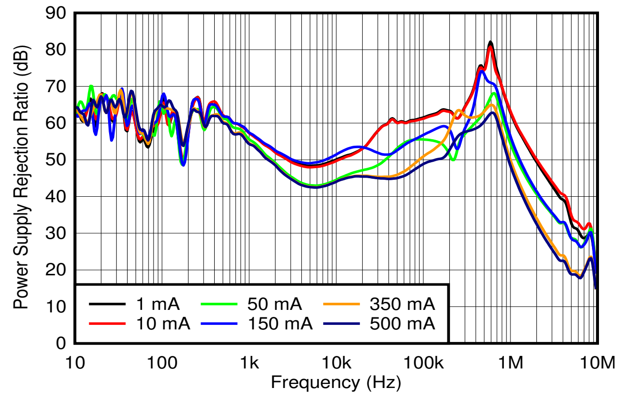


图 8-4. PSRR

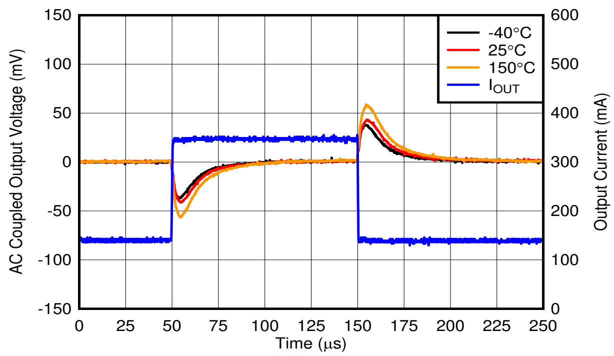


图 8-5. Transient Response

9 Power Supply Recommendations

This device is designed for operation from an input voltage supply with a range between 3 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B88-Q1, add an electrolytic capacitor with a value of 22 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. TI also recommends a ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7B88-Q1 are available at the end of this document and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

As depicted in 图 10-1, place the input and output capacitors close to the device for the layout of the TPS7B88-Q1. In order to enhance the thermal performance, place as many vias as possible around the device. These vias improve the heat transfer between the different GND planes in the PCB.

To improve AC performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place each capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces to connect the capacitors because may negatively affect system performance and even cause instability.

If possible, and to ensure the maximum performance specified in this document, use the same layout pattern used for the TPS7B88-Q1 evaluation board, available at www.ti.com.

10.2 Layout Example

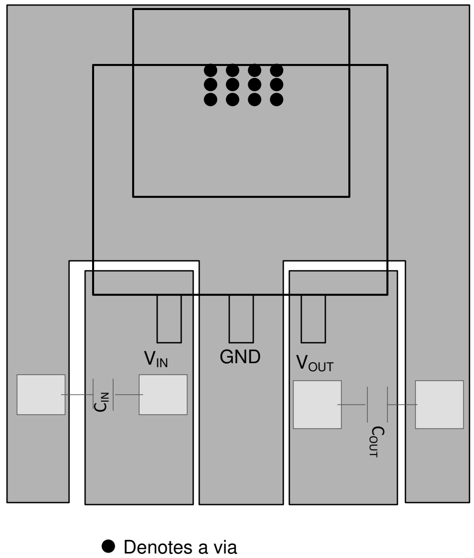


图 10-1. KVU Package Fixed Output

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

表 11-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS7B88**xx**QKVURQ1	**xx** is the nominal output voltage (for example, 33 = 3.3 V V; 50 = 5.0 V). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

11.1.2 Development Support

For the PSpice model, see the TPS7B4250 PSpice Transient Model.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Various Applications for Voltage-Tracking LDO* application report
- Texas Instruments, *TPS7B4250 Evaluation Module* user's guide
- Texas Instruments, *TPS7B5250-Q1 Pin FMEA* application report

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B8833QKVURQ1	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	7B8833	Samples
TPS7B8850QKVURQ1	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	7B8850	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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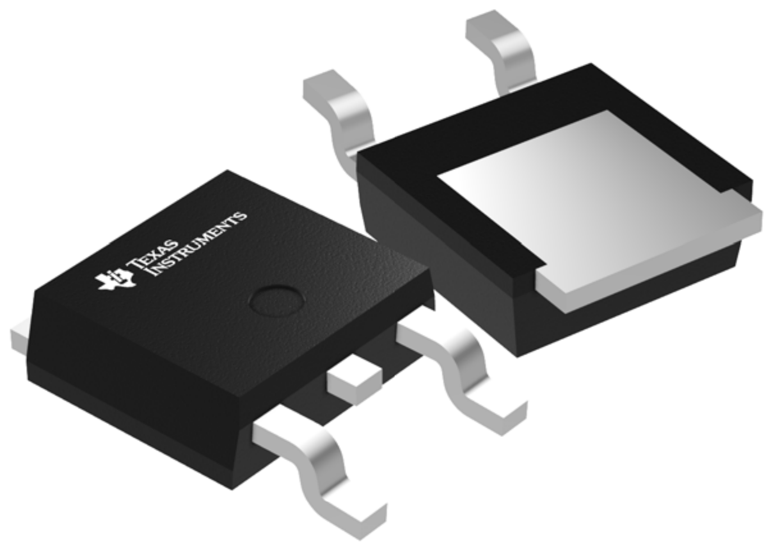
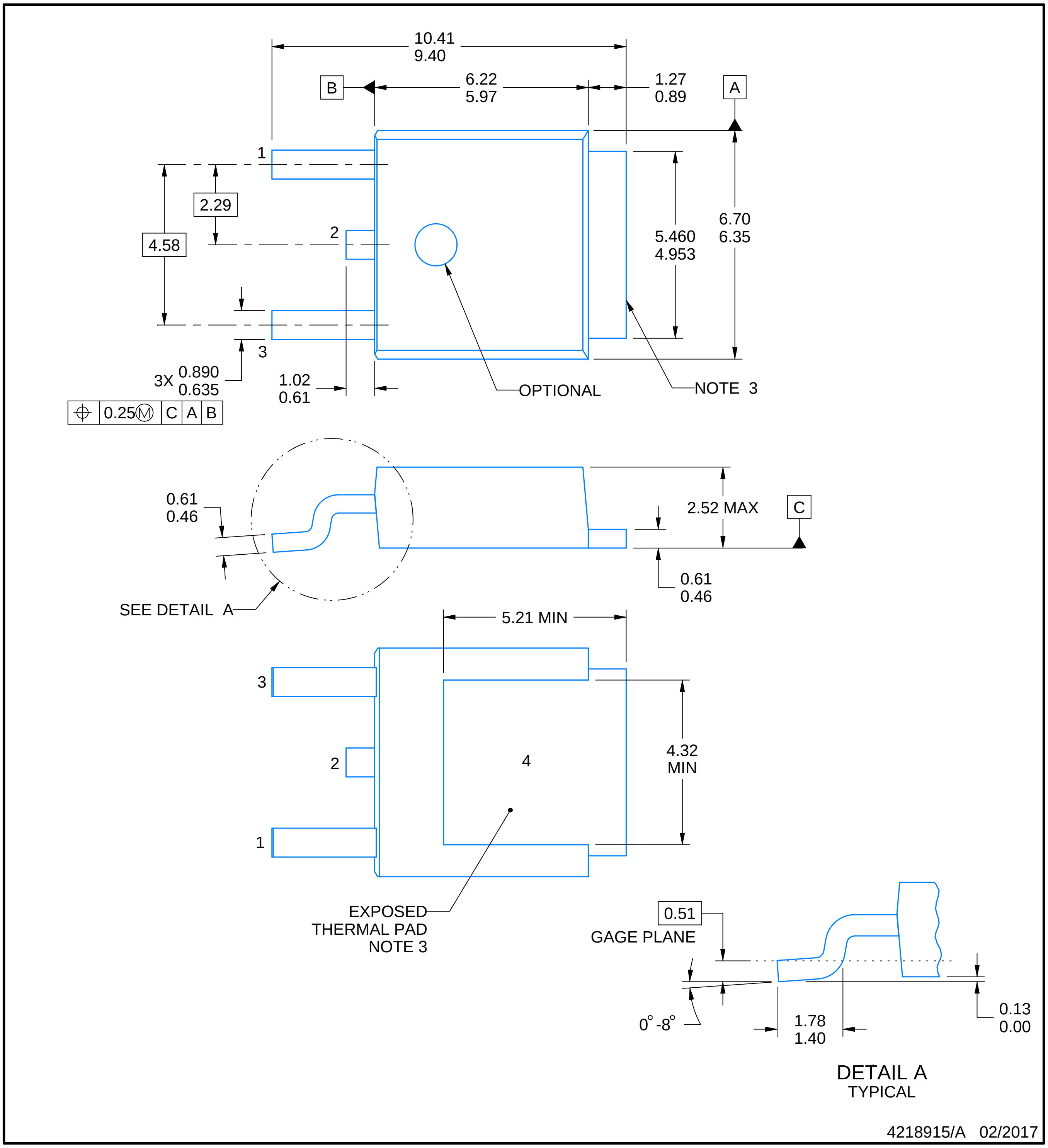
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

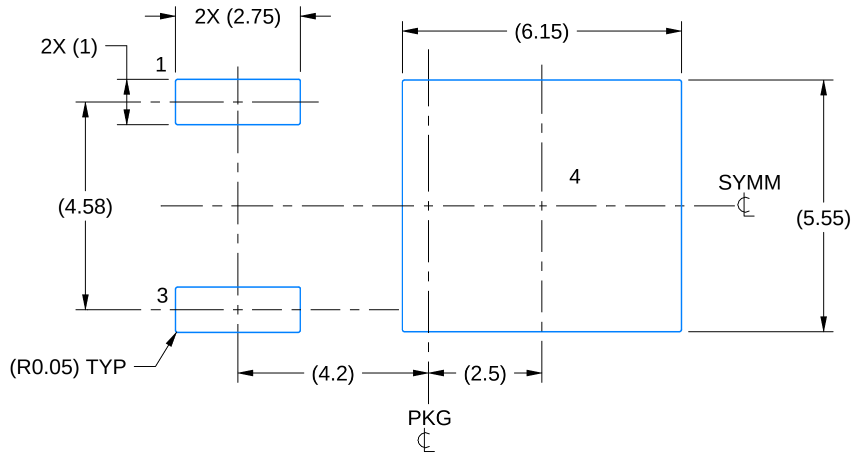


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

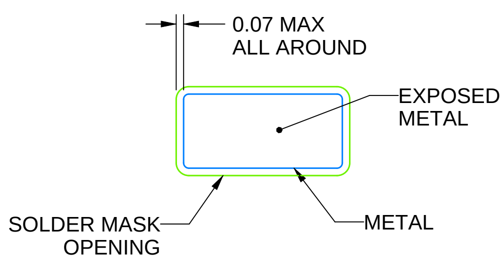


NOTES:

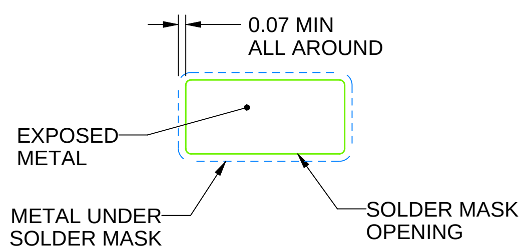
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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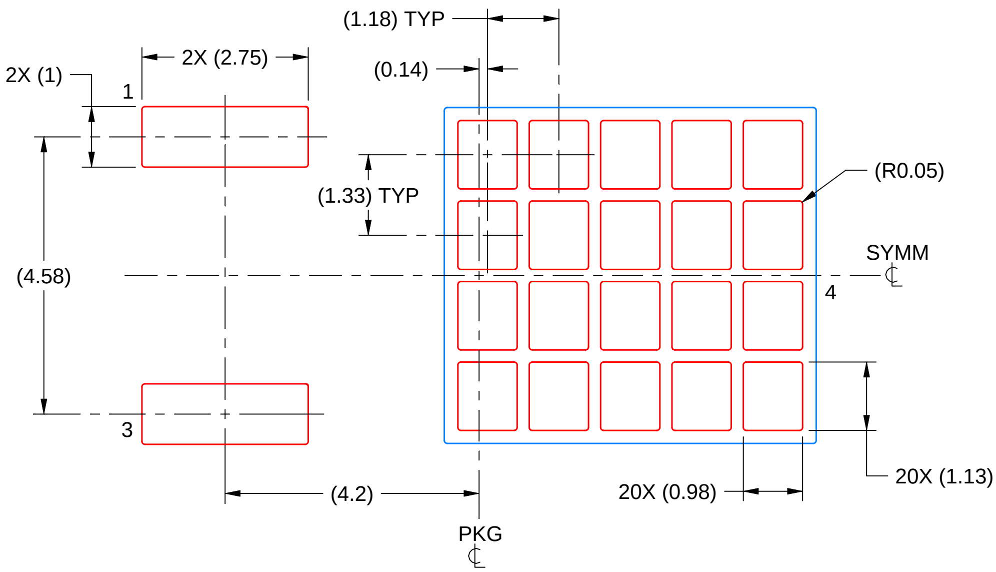
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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