TEXAS INSTRUMENTS
LM5123-Q1
ZHCSMW2 – JUNE 2020

具有 VOUT 跟踪功能的 LM5123-Q1 2.2MHz 宽 VIN 低 IQ 同步升压控制器

ADVANCE INFORMATION

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C 至 +125°C，T_A
- 适用于宽工作电压范围的汽车类电池供电应用
  - 3.8V 至 42V 输入电压工作范围
  - 5V 至 20V 或 15V 至 57V 的动态可编程 VOUT
  - BIAS 电压大于等于 3.8V 时最小升压输入为 0.8V
  - V_{SUPPLY} > V_{LOAD} 时进行旁路操作
- 最小电池消耗
  - 关断电流 ≤ 3 µA
  - 自动模式转换
  - 睡眠模式下的电池消耗 ≤ 11 µA（旁路操作，电荷泵关闭）
  - 睡眠模式下的电池消耗 ≤ 33 µA（旁路操作，电荷泵打开）
  - 睡眠模式下的偏置电流 I_Q ≤ 11 µA（跳跃模式）
  - 强大的 5V MOSFET 驱动器
- 解决方案尺寸小、成本低
  - 最大开关频率：2.2MHz
  - 内部自举二极管
  - 在 VIN 范围内峰值电流限制保持恒定
  - 支持 DCR 电感器电流感应
  - 具有可湿性侧面的 QFN-20 封装
- 避免 AM 频带干扰和串扰
  - 可选的时钟同步
  - 开关频率范围为 100kHz 至 2.2MHz
  - 可选开关模式（FPWM、二极管仿真和跳跃模式）
- 降低 EMI
  - 可选可编程扩展频谱
  - 无引线封装
- 可编程性和灵活性
  - 动态 VOUT 跟踪
  - 动态开关频率编程
  - 可编程线路 UVLO
  - 可调软启动
  - 自适应死区时间
  - PGOOD 指示器
- 集成型保护特性
  - 逐周期峰值电流限制
  - 过压保护
  - HB-SW 短路保护
  - 热关断

2 应用

- 具有跟踪功能的汽车音频电源
- 汽车 LED 偏置电源
- 汽车 HVAC 控制器电源
- 汽车电机电源

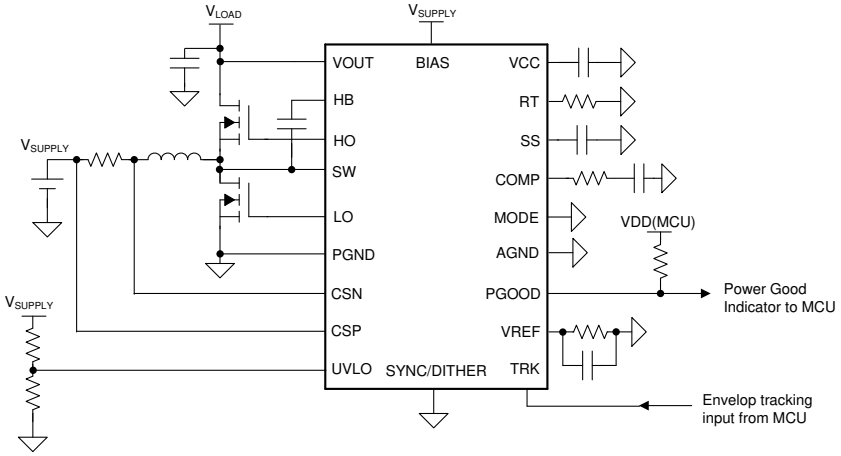
3 说明

LM5123-Q1 器件是一款采用峰值电流模式控制的宽输入范围同步升压控制器。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM5123-Q1	QFN (20)	3.5mm x 3.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2020	*	Initial release

5 Description (continued)

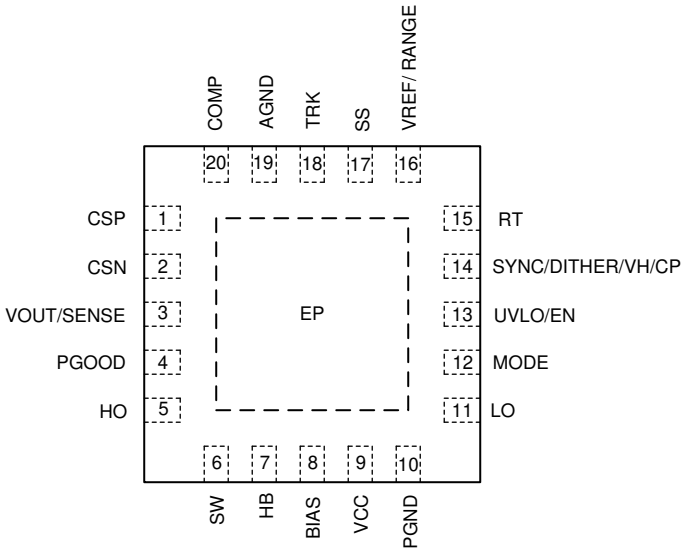
The device features a low shutdown I_Q and a low I_Q sleep mode, which minimizes battery drain at no and light load condition. The device also supports an ultra-low I_Q deep sleep mode with bypass operation, which eliminates the need for an external bypass switch when the supply voltage is greater than the boost output regulation target.

The output voltage can be dynamically programmed by using the tracking function. Controller architecture simplifies thermal management at harsh ambient temperature conditions when compared to converter architectures.

Wide input range supports automotive cold-crank and load dump. Minimum input voltage can be as low as 0.8 V when BIAS is equal to or greater than 3.8 V. The switching frequency is dynamically programmed with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz minimizes AM band interference and allows a small solution size and fast transient response.

The device has built-in protection features such as peak current limit, which is constant over VIN, overvoltage protection, and thermal shutdown. External clock synchronization, programmable spread spectrum modulation, and a lead-less package with minimal parasitic help to reduce EMI and avoid cross talk. Additional features include line UVLO, FPWM, diode emulation, DCR inductor current sensing, programmable soft start, and power-good indicator.

6 Pin Configuration and Functions



20-pin QFN with Wettable Flanks RGR Package (Top View)

表 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	CSP	I	Current sense amplifier input. The pin works as a positive input pin.
2	CSN	I	Current sense amplifier input. The pin works as a negative input pin.
3	VOUT/SENSE	I	Output voltage sensing pin. An internal feedback resistor voltage divider is connected from the pin to AGND. Connect a 0.1- µ F local VOUT capacitor from the pin to ground.
			High-side MOSFET drain voltage sensing pin. Connect the pin to the drain of the high-side MOSFET through a short, low inductance path.
4	PGOOD	O	Power-good indicator with open-drain output stage. The pin is grounded when the output voltage is less than the undervoltage threshold. The pin can be left floating if not used.
5	HO	O	High-side gate driver output. Connect directly to the gate of the high-side N-channel MOSFET through a short, low inductance path.
6	SW	P	Switching node connection and the high-side MOSFET source voltage sensing pin. Connect directly to the source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET through a short, low inductance path. Connect to PGND for non-synchronous boost configuration.
7	HB	P	High-side driver supply for bootstrap gate drive. Boot diode is internally connected from VCC to the pin. Connect a 0.1- µ F capacitor between the pin and SW. Connect to VCC for non-synchronous boost configuration.
8	BIAS	P	Supply voltage input to the VCC regulator. Connect a 1- µ F local BIAS capacitor from the pin to ground.
9	VCC	P	Output of the internal VCC regulator and supply voltage input of the internal MOSFET drivers. Connect 4.7- µ F VCC capacitor between the pin and PGND.
10	PGND	G	Power ground pin. Connect directly to the source of the low-side N-channel MOSFET and the power ground plane through a short, low inductance path.
11	LO	O	Low-side gate driver output. Connect directly to the gate of the low-side N-channel MOSFET through a short, low inductance path.

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表 6-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
12	MODE	I	Device switching mode (FPWM, diode emulation, or skip) selection pin. The device is configured to skip mode if the pin is open or if a resistor that is greater than 500 kΩ is connected from the pin to AGND during initial power-on. The device is configured to FPWM mode by connecting the pin to VCC or if the pin voltage is greater than 2.0 V during power-on. The device is configured to diode emulation mode by connecting the pin to ground or the pin voltage is less than 0.4 V during initial power-on. The switching mode can be dynamically programmed between the FPWM and the DE mode during operation.
13	UVLO/EN	I	Enable pin. The pin enables/disables the device. If the pin is less than 0.35 V, the device shuts down. The pin must be raised above 0.65 V to enable the device.
			Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting the pin to the supply voltage through a resistor voltage divider. The low-side UVLO resistor must be connected to AGND. Connect to BIAS if not used.
14	SYNC/DITHER/VH/CP	I/O	Synchronization clock input. The internal oscillator can be synchronized to an external clock during operation. Connect to AGND if not used.
			Clock dithering/spread spectrum modulation frequency programming pin. If a capacitor is connected between the pin and AGND, the clock dithering/spread spectrum function is activated. During the dithering operation, the capacitor is charged and discharged with an internal 20-μA current source/sink. As the voltage on the pin ramps up and down, the oscillator frequency is modulated between –7% and +7% of the nominal frequency set by the RT resistor. The clock dithering/spread spectrum can be deactivated during operation by pulling down the pin to ground.
			VCC hold pin. If the pin is greater than 2.0 V, the device holds the VCC pin voltage when the EN pin is grounded, which helps to restart fast without reconfiguration.
			Charge pump enable pin. If the pin is greater than 2.0 V, the internal charge pump maintains the HB pin voltage above its HB UVLO threshold for bypass operation, which allows the high-side switch to turn on 100% during bypass operation.
15	RT	I	Switching frequency setting pin. If no external clock is applied to the SYNC pin, the switching frequency is programmed by a single resistor between the pin and AGND. Switching frequency is dynamically programmable during operation.
16	VREF/RANGE	I/O	1.0-V internal reference voltage output. Connect a 470-pF capacitor from the pin to AGND. The VOUT regulation target can be programmed by connecting a resistor voltage divider from the pin to TRK. The resistance from the pin to AGND must be always greater than 20 kΩ if used. Connect the low-side resistor of the divider to AGND.
			VOUT range selection pin. Lower VOUT range (5 V - 20 V) is selected if the resistance from the pin to AGND is in the range of 75 kΩ and 100 kΩ during initial power-on. Upper VOUT range (15 V - 57 V) is selected if the resistance from the pin to AGND is in the range of 20 kΩ and 35 kΩ during initial power-on. Boost converter output voltage can be dynamically programmed within the pre-programmed range. The accuracy of the output voltage regulation is guaranteed within the selected range.
17	SS	I/O	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. The device forces diode emulation during soft-start time.
18	TRK	I	Output regulation target programming pin. The VOUT regulation target can be programmed by connecting the pin to VREF through a resistor voltage divider or by controlling the pin voltage directly from a D/A. The recommended operating range of the pin is from 0.25 V to 1.0 V.
19	AGND	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
20	COMP	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between the pin and AGND.
-	EP		Exposed pad of the package. The EP must be soldered to a large analog ground plane to reduce thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	MAX	UNIT
Input(2)	BIAS to AGND	–0.3	50	V
	UVLO to AGND	–0.3	BIAS + 0.3	
	CSP to AGND	–0.3	50	
	CSP to CSN	–0.3	0.3	
	VOUT to AGND	–0.3	65	
	HB to AGND	–0.3	65	
	HB to SW	–0.3	5.8(3)	
	SW to AGND (100ns)	–5		
	MODE, SYNC, TRK to AGND	–0.3	5.5	
	PGOOD to AGND	–0.3	VOUT + 0.3	
	RT to AGND	–0.3	2.5	
	PGND to AGND	–0.3	0.3	
Output(2)	VCC to AGND	–0.3	5.8(3)	V
	HO to SW (100ns)	–5		
	LO to PGND (100ns)	–5		
	VREF, SS, COMP to AGND(4)	–0.3	5.5	
Operating junction temperature, T_J (5)		–40	150	°C
Storage temperature, T_{STG}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) It is not allowed to apply an external voltage directly to VREF, COMP, SS, RT, LO, HO pins.
(3) Operating lifetime is de-rated when the pin voltage is greater than 5.5V.
(4) Maximum VREF pin sourcing current is 50uA.
(5) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
$V_{SUPPLY(BOOST)}$	Boost Converter Input (when BIAS ⩾ 3.8V)	0.8		42	V
$V_{LOAD(BOOST)}$	Boost Converter Output	5		57	
V_{BIAS}	BIAS Input	3.8		42	
V_{UVLO}	UVLO Input	0		42	
V_{CSP}, V_{CSN}	Current Sense Input	0.8		42	
V_{VOUT}	Boost Output Sense	5		57	
V_{TRK}	TRK Input	0.25		1(3)	
V_{SYNC}	Synchronization Pulse Input	0		5.25	
f_{SW}	Typical Switching Frequency	100		2200	kHz
f_{SYNC}	Synchronization Pulse Frequency	200		2200	
T_J	Operating Junction Temperature(2)	– 40		150	°C

(1) *Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(3) The maximum TRK pin voltage is limited to 0.95V when upper VOUT range is seleted.

7.4 Thermal Information

THERMAL METRIC(1)		LM5123-Q1 RGR(QFN) 20 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	43.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	36.8	°C/W
R_{qJB}	Junction-to-board thermal resistance	17.6	°C/W
y_{JT}	Junction-to-top characterization parameter	0.8	°C/W
y_{JB}	Junction-to-board characterization parameter	17.6	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the application report.

7.5 Electrical Characteristics

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 125 °C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT(BIAS, VCC, VOUT)						
$I_{BIAS-SD}$	BIAS current in shutdown	V_{UVLO} = 0 V		2.5	5	µA
$I_{BIAS-DS1}$	BIAS current in deep sleep (Diode emulation mode, Charge pump off, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 0 V		9	15	µA
$I_{BIAS-DS2}$	BIAS current in deep sleep (FPWM mode, Charge pump on, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 2.5 V		32	60	µA
$I_{BIAS-SLEEP}$	BIAS current in sleep (Skip mode, EA disabled, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, MODE = OPEN		11	17	µA
$I_{BIAS-ACTIVE}$	BIAS current in active (Non-switching, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.6 V, MODE = VCC		1.2	1.5	mA

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VCC-DS1}$	VCC current in deep sleep (Diode emulation mode, Charge pump off)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 0 V		0.029	2	µA
$I_{VOUT-SD}$	VOUT current in shutdown	V_{UVLO} = 0 V			1	µA
$I_{VOUT-DS}$	VOUT current in deep sleep (Diode emulation mode)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V		1.2	1.5	µA
$I_{VOUT-ACTIVE}$	VOUT current in active (Non-switching)	V_{UVLO} = 2.5 V, V_{TRK} = 0.6 V, MODE = VCC		42	55	µA
$I_{BATTERY-SD}$	Battery drain in shutdown	V_{UVLO} = 0 V		2.5	5	µA
$I_{BATTERY-DS1}$	Battery drain in deep sleep (Diode emulation mode, Charge pump off)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 0 V		10	17	µA
$I_{BATTERY-DS2}$	Battery drain in deep sleep (FPWM mode, Charge pump on)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{SYNC} = 2.5 V		33	62	µA
ENABLE, UVLO						
$V_{EN-RISING}$	Enable threshold	EN rising	0.45	0.55	0.65	V
$V_{EN-FALLING}$	Enable threshold	EN falling	0.35	0.45	0.55	V
V_{EN-HYS}	Enable hysteresis	EN falling	70	100	125	mV
$I_{UVLO-HYS}$	UVLO pull-down hysteresis current	V_{UVLO} = 0.7 V	9	10	11	µA
$V_{UVLO-RISING}$	UVLO threshold	UVLO rising	1.05	1.1	1.15	V
$V_{UVLO-FALLING}$	UVLO threshold	UVLO falling	1.025	1.075	1.125	V
$V_{UVLO-HYS}$	UVLO hysteresis	UVLO falling		25		mV
SYNC/DITHER/VH/CP						
$V_{SYNC-RISING}$	SYNC threshold/SYNC detection threshold	SYNC rising			2	V
$V_{SYNC-FALLING}$	SYNC threshold	SYNC falling	0.4			V
	Minimum SYNC pull up pulse width				100	ns
I_{DITHER}	Dither source/sink current		16	20	24	µA
Δf_{SW1}	f_{SW} Modulation (Upper Limit)		5	7	9	%
Δf_{SW2}	f_{SW} Modulation (Lower Limit)		-9	-7	-5	%
$V_{DITHER-FALLING}$	Dither disable threshold		0.65	0.75	0.85	V
VCC						
$V_{VCC-REG1}$	VCC regulation	I_{VCC} = 100 mA	4.75	5	5.25	V
$V_{VCC-REG2}$	VCC regulation	No load	4.75	5	5.25	V
$V_{VCC-REG3}$	VCC regulation during dropout	V_{BIAS} = 3.8 V, I_{VCC} = 100 mA	3.45			V
$V_{VCC-UVLO-RISING}$	VCC UVLO threshold	VCC rising	3.55	3.65	3.75	V
$V_{VCC-UVLO-FALLING}$	VCC UVLO threshold	VCC falling	3.2	3.3	3.4	V
I_{VCC-CL}	VCC sourcing current limit	V_{VCC} = 4 V	100			mA
CONFIGURATION (MODE)						
$V_{MODE-RISING}$	FPWM mode threshold	MODE rising			2.0	V
$V_{MODE-FALLING}$	Diode emulation mode threshold	MODE falling	0.4			V
RT						
V_{RT}	RT regulation			0.5		V
VREF, TRK, VOUT						
V_{REF}	VREF regulation target		0.995	1	1.005	V

ADVANCE INFORMATION

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT-REG}$	VOUT regulation target1 with resistor divider (Lower VOUT range)	VREF resistor divider to make V_{TRK} = 0.25 V, R_{VREF} = 75 kΩ	4.925	5	5.075	V
	VOUT regulation target2 with resistor divider (Lower VOUT range)	VREF resistor divider to make V_{TRK} = 0.5 V, R_{VREF} = 75 kΩ	9.9	10	10.1	V
	VOUT regulation target3 with resistor divider (Lower VOUT range)	VREF resistor divider to make V_{TRK} = 1.0 V, R_{VREF} = 75 kΩ	19.8	20	20.2	V
	VOUT regulation target4 with resistor divider (Upper VOUT range)	VREF resistor divider to make V_{TRK} = 0.25 V, R_{VREF} = 35 kΩ	14.775	15	15.225	V
	VOUT regulation target5 with resistor divider (Upper VOUT range)	VREF resistor divider to make V_{TRK} = 0.5 V, R_{VREF} = 35 kΩ	29.7	30	30.3	V
	VOUT regulation target6 with resistor divider (Upper VOUT range)	VREF resistor divider to make V_{TRK} = 0.95 V, R_{VREF} = 35 kΩ	56.43	57	57.57	V
	VOUT regulation target1 using TRK (Lower VOUT range)	V_{TRK} = 0.25 V, R_{VREF} = 75 kΩ	4.95	5	5.05	V
	VOUT regulation target2 using TRK (Lower VOUT range)	V_{TRK} = 0.5 V, R_{VREF} = 75 kΩ	9.95	10	10.05	V
	VOUT regulation target3 using TRK (Lower VOUT range)	V_{TRK} = 1.0 V, R_{VREF} = 75 kΩ	19.9	20	20.1	V
	VOUT regulation target4 using TRK (Upper VOUT range)	V_{TRK} = 0.25 V, R_{VREF} = 35 kΩ	14.85	15	15.15	V
	VOUT regulation target5 using TRK (Upper VOUT range)	V_{TRK} = 0.5 V, R_{VREF} = 35 kΩ	29.85	30	30.15	V
	VOUT regulation target6 using TRK (Upper VOUT range)	V_{TRK} = 0.95 V, R_{VREF} = 35 kΩ	56.715	57	57.285	V
I_{TRK}	TRK bias current				1	uA
SOFT START, DE to FPWM TRANSITION						
I_{SS}	Soft-start current		17	20	23	µA
$V_{SS-DONE}$	MODE transition start	SS rising	1.3	1.5	1.7	V
R_{SS}	SS pull-down switch R_{DSON}			30	70	Ω
V_{SS-DIS}	SS discharge detection threshold		45	50	55	mV
V_{FB-SS}	internal FB to SS clamp	V_{FB} = 0 V		55	75	mV
CURRENT SENSE (CSP, CSN, SW, SENSE)						
V_{SLOPE}	Peak slope compensation amplitude	R_T = 220 kΩ , Referenced to CS input		45		mV
A_{CS}	Current sense amplifier gain	CSP = 3.0 V		10		V/V
	Current sense amplifier gain	CSP = 1.5 V		10		V/V
V_{CLTH}	Positive peak current limit threshold (CSP-CSN)	CSP = 3.0 V, MODE = GND	54	60	66	mV
	Positive peak current limit threshold (CSP-CSN)	CSP = 1.5 V, MODE = GND	54	60	66	mV
V_{ZCD-DE}	ZCD threshold (SW-SENSE)	MODE = GND	3	5	7	mV
I_{CSN}	CSN bias current				1	µA
I_{CSP}	CSP bias current			110		µA
BOOT FAULT PROTECTION (HB)						
	Maximum replenish pulse cycles			4		cycles

ADVANCE INFORMATION

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Replenish off cycles			12		cycles
	Number of sets to enter hiccup mode protection			4		sets
	Off-cycle during hiccup mode off			512		cycles
ERROR AMPLIFIER (COMP)						
Gm	Transconductance			1		mA/V
$I_{SOURCE-MAX}$	Maximum COMP sourcing current	V_{COMP} = 0 V	100			µA
$I_{SINK-MAX}$	Maximum COMP sinking current	V_{COMP} = 1.8 V	100			µA
$V_{CLAMP-MAX}$	COMP maximum clamp voltage	COMP rising	1.9	2.2	2.5	V
$V_{CLAMP-MIN}$	COMP minimum clamp voltage, active in sleep and deep sleep mode.	COMP falling		0.25		V
PULSE WIDTH MODULATION (PWM)						
f_{SW1}	Switching frequency	R_T = 220 kΩ	85	100	115	kHz
f_{SW2}	Switching frequency	R_T = 9.09 kΩ	1980	2200	2420	kHz
t_{ON-MIN}	Minimum controllable on-time	R_T = 9.09 kΩ	15	22	50	ns
$t_{OFF-MIN}$	Minimum forced off-time	R_T = 9.09 kΩ	70	90	110	ns
D_{MAX1}	Maximum duty cycle limit	R_T = 220kΩ	90	93	96	%
D_{MAX1}	Maximum duty cycle limit	R_T = 9.09 kΩ	75	80	82	%
LOW IQ SLEEP MODE						
	Pulse skip to enter sleep mode			16		cycles
V_{WAKE}	Internal wakeup threshold	VOUT falling (referenced to $V_{OUT-REG}$)		98.9		%
	Sleep to Wake-up delay	R_T = 9.09 kΩ		5		us
PGOOD, OVP						
$V_{OVTH-RISING}$	Overvoltage threshold (OVP threshold)	VOUT rising (referece to $V_{OUT-REG}$)	105	107	109	%
$V_{OVTH-FALLING}$	Overvoltage threshold (OVP threshold)	VOUT falling (referece to $V_{OUT-REG}$)	103	105	107	%
$V_{UVTH-RISING}$	Undervoltage threshold (PGOOD threshold)	VOUT rising (referece to $V_{OUT-REG}$)	93	95	97	%
$V_{UVTH-FALLING}$	Undervoltage threshold (PGOOD threshold)	VOUT falling (referece to $V_{OUT-REG}$)	91	93	95	%
	UV comparator deglich filter	Rising edge		30		µs
	UV comparator deglich filter	Falling edge		25		µs
R_{PGOOD}	PGOOD pull-down switch R_{DSON}			90	180	Ω
	Minimum BIAS for valid PGOOD				2.5	V
MOSFET DRIVER						
	High-state voltage drop (HO driver)	100-mA sinking		0.08	0.15	V
	Low-state voltage drop (HO driver)	100-mA sourcing		0.04	0.1	V
	High-state voltage drop (LO driver)	100-mA sinking		0.08	0.15	V
	Low-state voltage drop (LO driver)	100-mA sourcing		0.04	0.1	V
$V_{HB-UVLO}$	HB-SW UVLO threshold	HB-SW falling	2.5	2.65	2.90	V
$I_{HB-SLEEP}$	HB quiescent current in sleep	HB-SW = 5 V		3.5	7	µA

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Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 125 °C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	HO off to LO on deadtime		12	18	30	ns
t_{DLH}	LO off to HO on deadtime		13	19	31	ns
	HB diode resistance			0.7		Ω
THERMAL SHUTDOWN						
$T_{TSD-RISING}$	Thermal shutdown threshold	Temperature rising		175		°C
$T_{TSD-HYS}$	Thermal shutdown hysteresis			15		°C

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8 Detailed Description

8.1 Overview

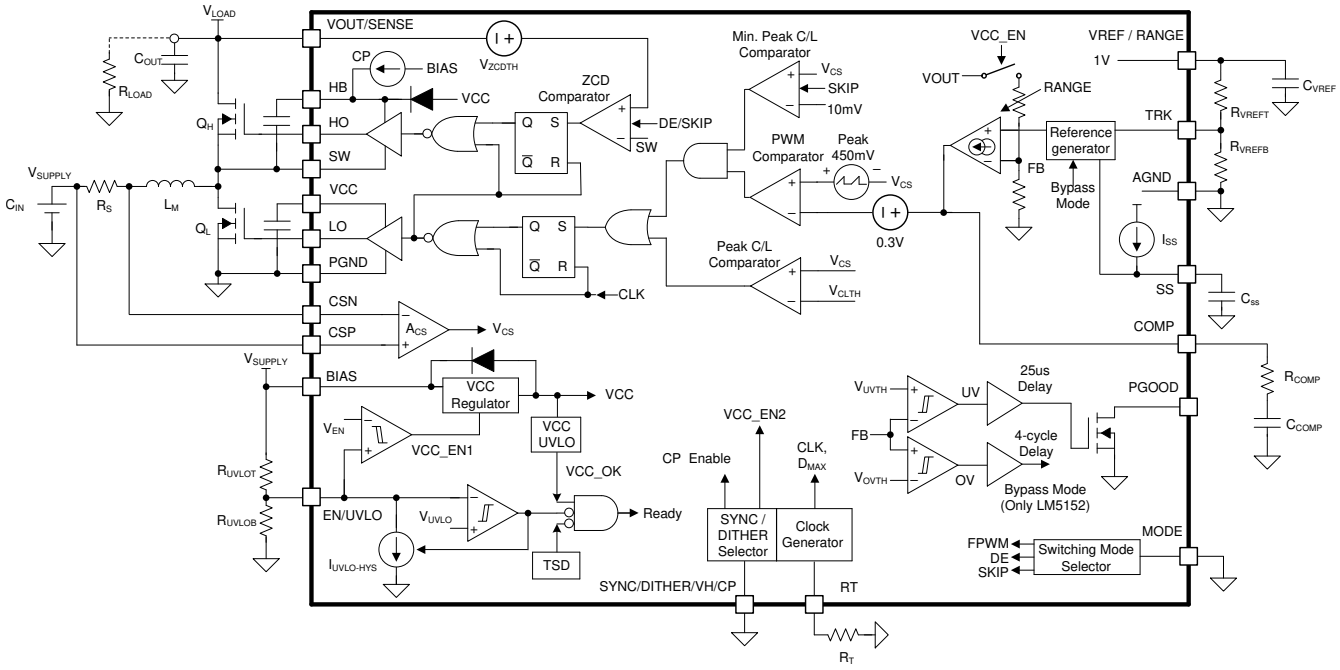
The LM5123-Q1 device is a wide input range synchronous boost controller that employs peak current mode control. The device features a low shutdown I_Q and a low I_Q sleep mode, which minimizes battery drain at no/light load condition. The device also supports an ultra-low I_Q deep sleep mode with bypass operation, which eliminates the need for an external bypass switch when the supply voltage is greater than the boost output regulation target.

The output voltage can be dynamically programmed by using the tracking function. Controller architecture simplifies thermal management at harsh ambient temperature conditions when compared to converter architectures.

Wide input range supports automotive cold-crank and load dump. Minimum input voltage can be as low as 0.8 V when BIAS is equal to or greater than 3.8 V. The switching frequency is dynamically programmed with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response.

The device has built-in protection features such as peak current limit, which is constant over VIN, overvoltage protection, and thermal shutdown. External clock synchronization, programmable spread spectrum modulation, and a lead-less package with minimal parasitic help reduce EMI and avoid cross talk. Additional features include line UVLO, FPWM, diode emulation, DCR inductor current sensing, programmable soft start, and a power-good indicator.

8.2 Functional Block Diagram



8.3 Feature Description

Note

Read through 节 8.4 before reading the feature description of the device. It is recommended to understand which device functional modes and what type of light load switching modes are supported by the device.

The parameters or thresholds values mentioned in this section are reference values unless otherwise specified. Refer to the *Electrical Characteristics* to find the ensured minimum, maximum, and typical values.

8.3.1 Device Enable/Disable (EN, VH Pin)

The device shuts down when EN is less than the EN threshold (V_{EN}) and VH is less than the SYNC threshold (V_{SYNC}). The device is enabled when EN is greater than V_{EN} or VH is greater than V_{SYNC}. The VH pin provides a 40-μs internal delay before the device shuts down.

The device provides a 33-kΩ internal EN pulldown resistor to prevent a false turnon when the pin is floating. The EN pulldown resistor is connected to ground during the device configuration time or when the device shuts down. If the device configuration is finished and VH is greater than V_{SYNC}, EN hysteresis is accomplished by disconnecting/connecting the resistor when EN is greater/less than V_{EN}.

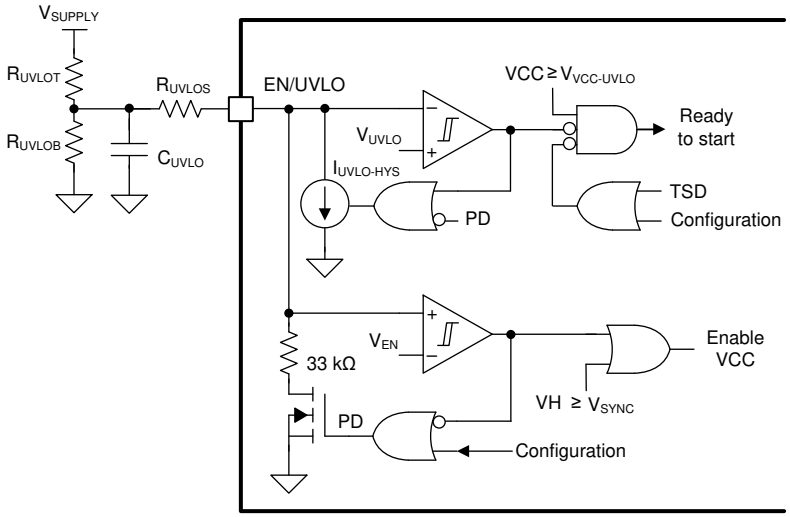


图 8-1. EN/UVLO Circuit

8.3.2 High Voltage VCC Regulator (BIAS, VCC Pin)

The device features a high voltage 5-V VCC regulator which is sourced from the BIAS pin. The internal VCC regulator turns on 50 μs after the device is enabled, and 120 μs device configuration starts when VCC is above VCC UVLO threshold ($V_{VCC-UVLO}$). The device configuration is reset when the device shuts down or VCC falls down below 2.2 V. The preferred way to reconfigure the device is to shut down the device. During configuration time, the light load switching mode and VOUT range are selected.

The high voltage VCC regulator allows you to connect the BIAS pin directly to supply voltages from 3.8 V to 42 V. When BIAS is less than the 5-V VCC regulation target ($V_{VCC-REG}$), the VCC output tracks the BIAS pin voltage with a small dropout voltage which is caused by 1.7-Ω resistance of the VCC regulator.

The recommended VCC capacitor value is 4.7 μF. The VCC capacitor should be populated between VCC and PGND as close to the device. The recommended BIAS capacitor value is 1.0 μF. The BIAS capacitor must be populated between BIAS and PGND as close to the device.

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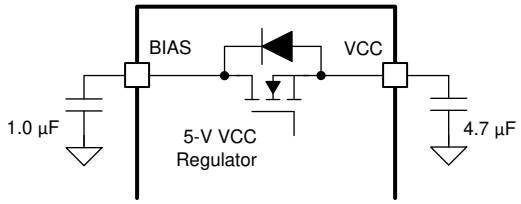

图 8-2. High Voltage VCC Regulator

The VCC regulator features VCC current limit function that prevents device damage when the VCC pin is short to ground accidentally. The minimum sourcing capability of the VCC regulator is 100 mA (I_{VCC-CL}) during either the device configuration time or active mode operation. The minimum sourcing capability of the VCC regulator is reduced to 1 mA during sleep mode or deep sleep mode, or when EN is less than V_{EN} and VH is greater than V_{SYNC}. The VCC regulator supplies the internal drivers and other internal circuits. The external MOSFETs must be carefully selected to make the driver current consumption less than I_{VCC-CL}. The driver current consumption can be calculated in 方程式 1.

$$I_G = 2 \times Q_{G@5V} \times f_{SW} \quad (1)$$

If the bypass operation is required, the BIAS pin must be connected to the output of the boost converter (V_{LOAD}). By connecting the BIAS pin to V_{LOAD}, the boost converter input voltage (V_{SUPPLY}) can drop down to 0.8 V if BIAS is greater than 3.8 V. See *节 8.3.17* for more detailed information about the minimum V_{SUPPLY}.

8.3.3 Light Load Switching Mode Selection (MODE Pin)

The light load switching mode is selected during the device configuration. The device is configured to skip mode when the MODE pin is floating or a resistor which is greater than 500 kΩ is connected between MODE and AGND during the device configuration. Once the device is configured to skip mode, the light load switching mode cannot be changed until reconfiguring the device.

If the MODE pin voltage is less than 0.4 V ($V_{MODE-FALLING}$) or grounded during the device configuration, the device is configured to diode emulation (DE) mode. If the MODE pin voltage is greater than 2.0 V ($V_{MODE-RISING}$) or connected to VCC during the device configuration, the device is configured to Forced PWM (FPWM) mode. If the device is configured to DE or FPWM mode, the light load switching mode can be dynamically changed between DE and FPWM modes during operation without reconfiguration.

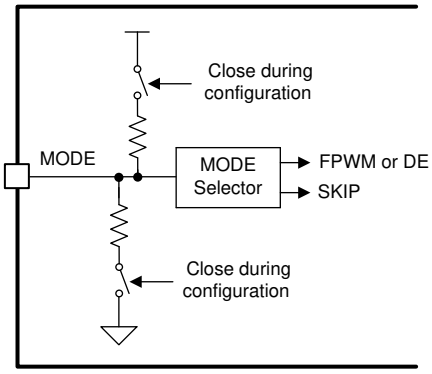

图 8-3. MODE Selection Circuit

8.3.4 VOUT Range Selection (RANGE Pin)

The programmable VOUT range is selected during the device configuration and it cannot be changed until you reconfigure the device. Lower VOUT range (5 V - 20 V) is selected if the resistance from VREF to AGND (R_{VREFT} + R_{VREFB}) is in the range of 75 kΩ to 100 kΩ during the device configuration. Upper VOUT range (15 V - 57 V) is selected if the resistance from VREF to AGND is in the range of 20 kΩ to 35 kΩ during the device configuration. The accuracy of the VOUT regulation is ensured within the selected range.

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8.3.5 Line Undervoltage Lockout (UVLO Pin)

When UVLO is greater than the UVLO threshold (V_{UVLO}), the device enters active mode if the device configuration is finished. UVLO hysteresis is accomplished with an internal 25-mV voltage hysteresis ($V_{UVLO-HYS}$) at the UVLO pin, and an additional 10-μA current sink ($I_{UVLO-HYS}$) that is switched on or off. When the UVLO pin voltage exceeds V_{UVLO}, the current sink is disabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below V_{UVLO} or during the device configuration time, the current sink is enabled, causing the voltage at the UVLO pin to fall quickly.

The external UVLO resistor voltage divider (R_{UVLOT}, R_{UVLOB}) must be designed so that the voltage at the UVLO pin is greater than V_{UVLO} when V_{SUPPLY} is in the desired operating range. The values of R_{UVLOT} and R_{UVLOB} can be calculated as follows.

$$R_{UVLOT} = \frac{\left(V_{SUPPLY-ON} - \frac{V_{UVLO-RISING}}{V_{UVLO-FALLING}} \times V_{SUPPLY-OFF}\right)}{I_{UVLO-HYS}} \quad (2)$$

$$R_{UVLOB} = \frac{V_{UVLO-FALLING} \times R_{UVLOT}}{V_{SUPPLY-OFF} - V_{UVLO-FALLING}} \quad (3)$$

A UVLO capacitor (C_{UVLO}) is required in case V_{SUPPLY} drops below $V_{SUPPLY-OFF}$ momentarily during the start-up or during a severe load transient at the low input voltage. If the required UVLO capacitor is large, an additional series UVLO resistor (R_{UVLOS}) can be used to quickly raise the voltage at the UVLO pin when $I_{UVLO-HYS}$ is disabled.

The UVLO pin can be connected to the BIAS pin if not used. Drive the UVLO pin through a minimum of a 5-kΩ resistor if the BIAS pin voltage is less than the UVLO pin voltage in any conditions.

8.3.6 Fast Restart using VCC HOLD (VH Pin)

After the device configuration, a fast restart can be achieved without reconfiguration by toggling EN when VH is greater than V_{SYNC}. The device stops switching, but keeps the VCC regulator active when EN is less than V_{EN} and VH is greater than V_{SYNC} (See 图 8-5).

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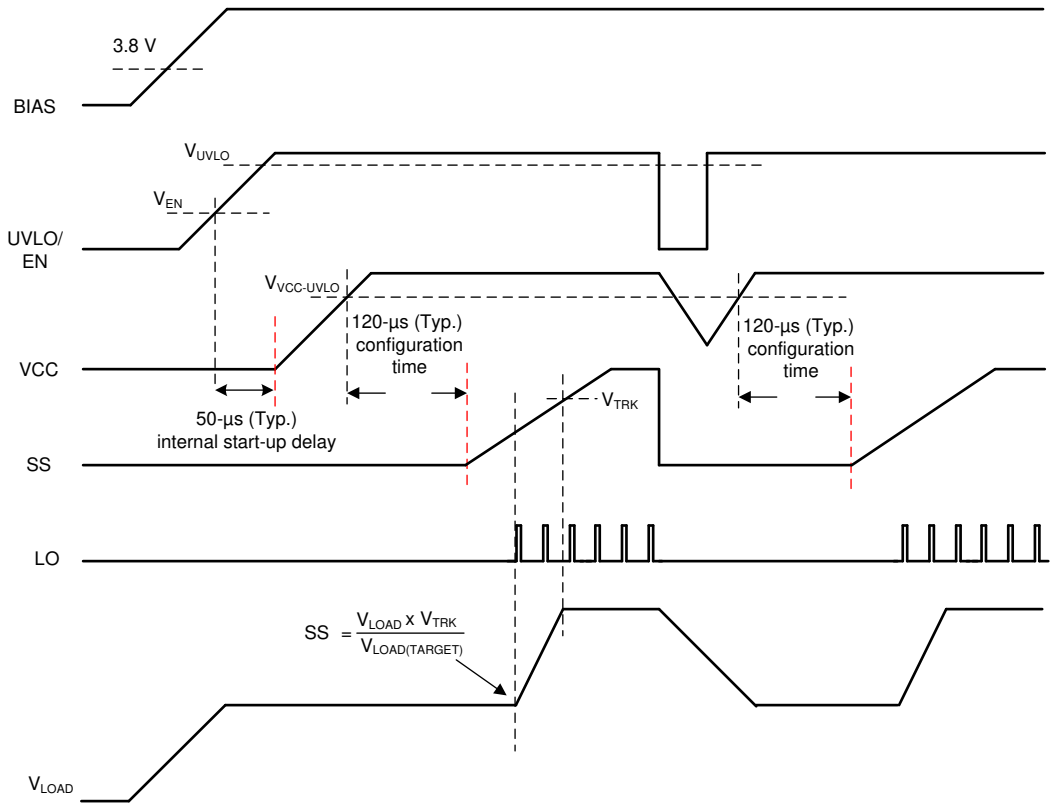

图 8-4. Boost Start-up Waveforms Case 1: Start-up by EN/UVLO, Restart when VH < V_{SYNC}

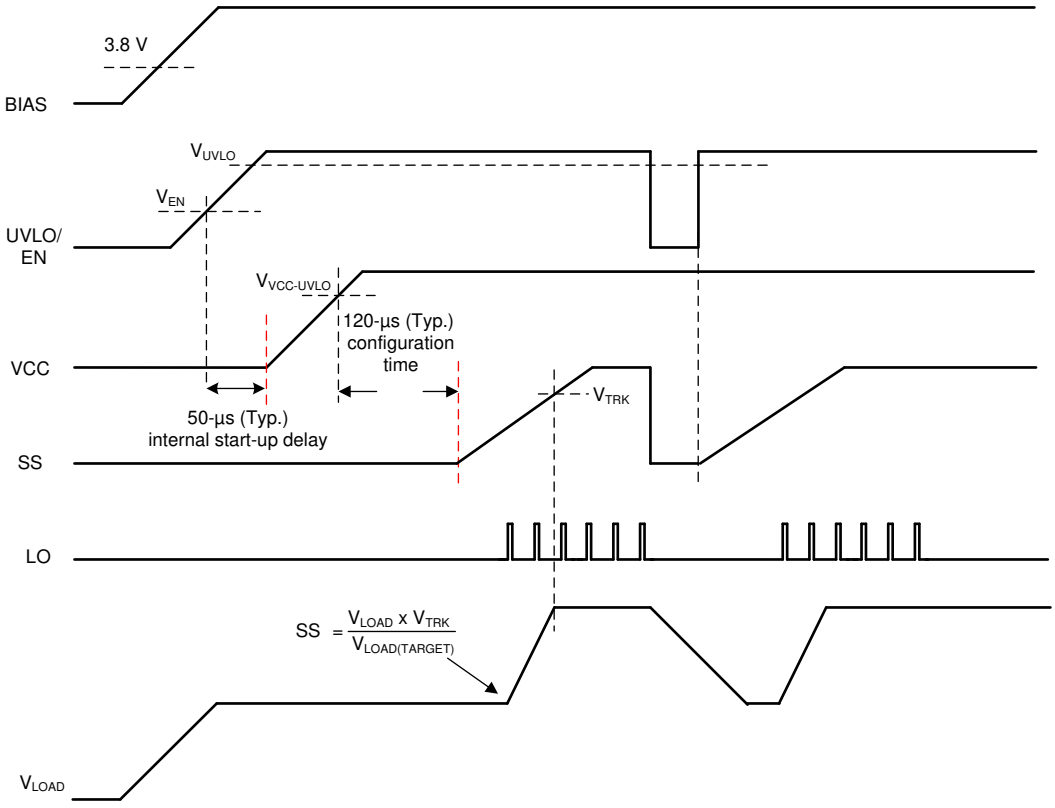

图 8-5. Boost Start-up Waveforms Case 2: Start-up by EN/UVLO, Restart when VH > V_{SYNC}

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8.3.7 Adjustable Output Regulation Target (VOUT, TRK, VREF Pin)

The VOUT regulation target ($V_{OUT-REG}$) is adjustable by programming the TRK pin voltage which is the reference of the internal error amplifier. The accuracy of $V_{OUT-REG}$ is ensured when the TRK voltage is between 0.25 V and 1.0 V. The high impedance TRK pin allows users to program the pin voltage directly by a D/A converter or by connecting to a resistor voltage divider (R_{VREFT}, R_{VREFB}) between VREF and AGND.

The device provides a 1-V voltage reference (V_{REF}) which can be used to program the TRK pin voltage through a resistor voltage divider. It is not recommended to use VREF as a reference voltage of an external circuit because the device periodically disables VREF in sleep or deep sleep mode. The recommended VREF capacitor (C_{VREF}) is 470 pF.

When R_{VREFT} and R_{VREFB} are used to program the TRK pin voltage, $V_{OUT-REG}$ can be calculated as follows.

Lower VOUT Range

$$V_{OUT-REG} = \frac{20 \times R_{VREFB}}{R_{VREFB} + R_{VREFT}} \quad (4)$$

Upper VOUT Range

$$V_{OUT-REG} = \frac{60 \times R_{VREFB}}{R_{VREFB} + R_{VREFT}} \quad (5)$$

The TRK pin voltage can be dynamically programmed in active mode, which makes an envelop tracking power supply design easy. When designing a tracking power supply, it is required to adjust the TRK pin voltage slow enough so that the VOUT pin voltage can track the command and the internal overvoltage or undervoltage comparator is not triggered during the transient operation. An RC filter must be used at the TRK pin to slow down the slew rate of the command signal at the TRK pin, especially when a step input is applied. When a trapezoidal or sinusoidal input is applied, the slew rate or the frequency of the command signal must be limited.

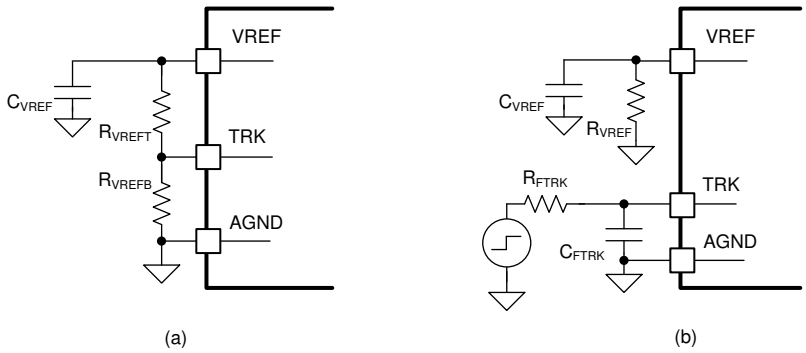

图 8-6. TRK Control (a) using VREF (b) by External Step Input

The TRK pin voltage also can be dynamically programmed during deep sleep mode, but during deep sleep mode, $V_{OUT-REG}$ tracks the TRK pin voltage with a maximum of a 20-ms delay. Take extra care when programming TRK if V_{SUPPLY} is greater than $V_{OUT-REG}$ in any conditions. The device enters active mode with a 5-μs delay if V_{LOAD} falls down below $V_{OUT-REG}$ in deep sleep mode, but the device enters active mode with maximum of a 20-ms delay if $V_{OUT-REG}$ is increased by TRK above V_{LOAD} in deep sleep mode.

8.3.8 Overvoltage Protection (VOUT Pin)

The device provides an overvoltage protection (OVP) for boost converter output. The OVP comparator monitors the VOUT pin through an internal resistor voltage resistors. If the VOUT pin voltage rises above the overvoltage threshold (V_{OVTH}), OVP is activated. When OVP is triggered, the device turns off the low-side driver by force and turns on the high-side driver until zero current is detected in diode emulation or skip mode. In FPWM mode, the low-side driver is not turned off when the OVP is triggered.

After four cycles in OVP status, the device enters deep sleep mode. The device turns on the high-side driver 100% in deep sleep mode if the light load switching mode of the device is FPWM or DE, and the CP is greater than V_{SYNC} before entering deep sleep mode. The recommended VOUT capacitor (C_{VOUT}) is 0.1 μF.

8.3.9 Power Good Indicator (PGOOD Pin)

The device provides a power-good indicator (PGOOD) to simplify sequencing and supervision. PGOOD is an open-drain output and a pullup resistor between 5 kΩ and 100 kΩ can be externally connected. The PGOOD switch opens when the VOUT pin voltage is greater than the undervoltage threshold (V_{UVTH}). The PGOOD pin is pulled down to ground when the VOUT pin voltage is less than V_{UVTH}, UVLO is less than V_{UVLO}, VCC is less than $V_{VCC-UVLO}$, or during thermal shutdown. A 25-μs bi-directional deglitch filter prevents any false pulldown of the PGOOD due to transients. The PGOOD pin voltage cannot be greater than V_{VOUT} + 0.3 V

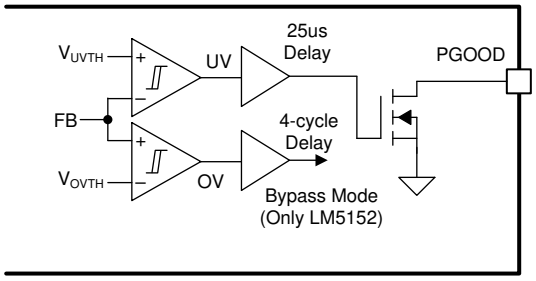

图 8-7. PGOOD Indicator

8.3.10 Dynamically Programmable Switching Frequency (RT)

The switching frequency of the device is set by a single RT resistor connected between RT and AGND if no external synchronization clock is applied to the SYNC pin. The resistor value to set the RT switching frequency (R_T) is calculated as follows.

$$R_T = \frac{2.21 \times 10^{10}}{f_{RT(typical)}} - 955 \quad (6)$$

The RT pin is regulated to 0.5 V by an internal RT regulator when the device is in active mode or during the device configuration. The switching frequency can be dynamically programmed during operation as shown in 图 8-8.

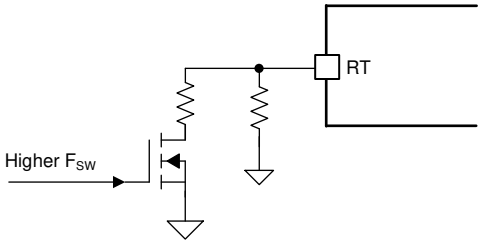

图 8-8. Frequency Hopping Example

8.3.11 External Clock Synchronization (SYNC Pin)

The switching frequency of the device can be synchronized to an external clock by directly applying an external pulse signal to the SYNC pin. The internal clock is synchronized at the rising edge of the external synchronization pulse using an internal PLL. Connect the SYNC pin to ground if not used.

The external synchronization pulse must be greater than V_{SYNC} in high logic state and must be less than V_{SYNC} in low logic state. The duty cycle of the external synchronization pulse is not limited, but the minimum on-pulse and the minimum off-pulse widths must be greater than 100 ns. The frequency of the external synchronization pulse must satisfy the following two inequalities.

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$$200kHz \le f_{SYNC} \le 2.2MHz \quad (7)$$

$$0.75 \times f_{RT(typical)} \le f_{SYNC} \le 1.5 \times f_{RT(typical)} \quad (8)$$

For example, an RT resistor is required for typical 350-kHz switching to cover from 263-kHz to 525-kHz clock synchronization without changing the RT resistor.

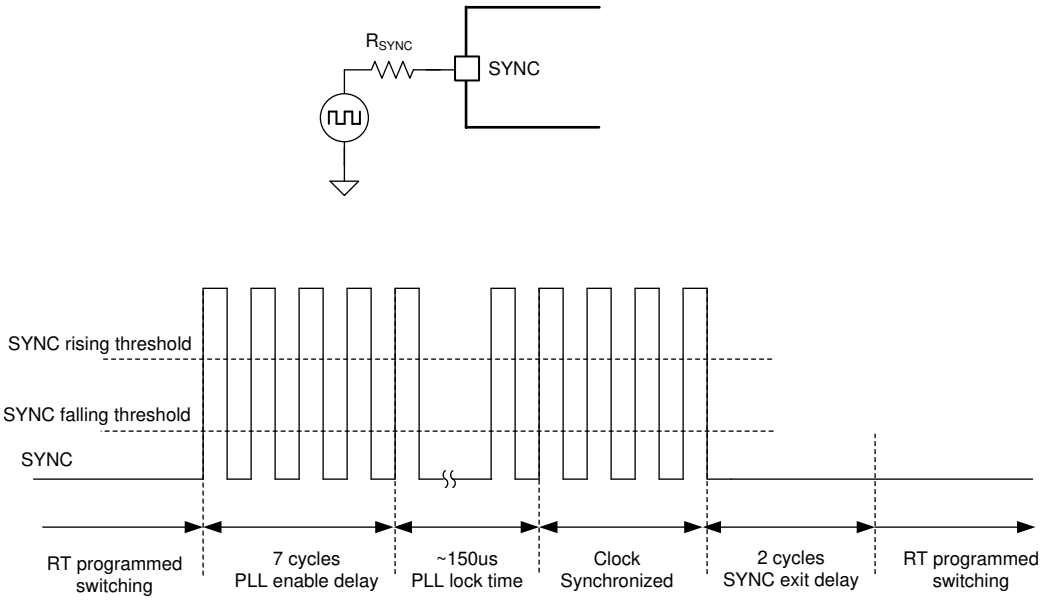

图 8-9. External Clock Synchronization

Drive the SYNC pin through a minimum 1-kΩ resistor if the BIAS pin voltage is less than the SYNC pin voltage in any conditions.

8.3.12 Programmable Spread Spectrum (DITHER Pin)

The device provides an optional programmable spread spectrum (clock dithering) function that is activated by connecting a capacitor between DITHER and AGND. A triangular waveform centered at 1.0 V is generated across the dither capacitor. This triangular waveform modulates the oscillator frequency by ±7% of the frequency set by the RT resistor. The dither capacitance value sets the rate of the low frequency modulation.

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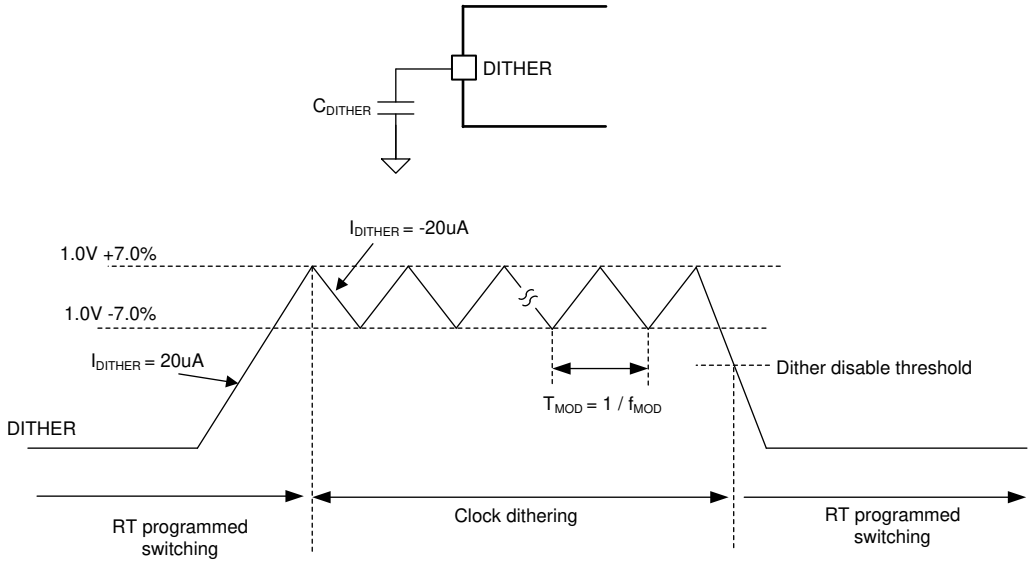

图 8-10. Switching Frequency Dithering

For the dithering circuit to effectively reduce peak EMI, the modulation frequency must be much less than the RT switching frequency. The dither capacitance which is required for a given modulation frequency (f_{MOD}), can be calculated from 方程式 9. Setting the f_{MOD} to 9 kHz or 10 kHz is a good starting point.

$$C_{DITHER} = \frac{20\mu A}{f_{MOD} \times 0.29} \tag{9}$$

Connecting DITHER to AGND deactivates clock dithering, and the internal oscillator operates at a fixed frequency set by the RT resistor. Clock dithering is also disabled when an external synchronization pulse is applied.

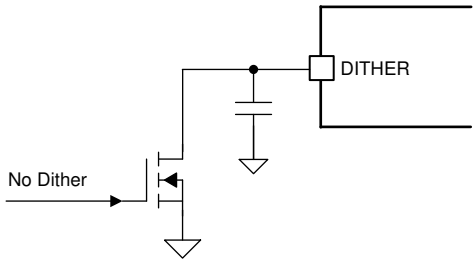

图 8-11. Dynamic Dither On/Off Example

8.3.13 Programmable Soft-start (SS Pin)

The soft-start feature helps the converter gradually reach the steady state operating point. To reduce start-up stresses and surges, the device regulates the error amplifier reference to the SS pin voltage or the TRK pin voltage (V_{TRK}), whichever is lower.

The internal 20- μA soft-start (I_{SS}) current turns on 120 μs after the VCC pin crosses $V_{VCC-UVLO}$. I_{SS} gradually increases the voltage on an external soft-start capacitor (C_{SS}). This results in a gradual rise of the output voltage.

In FPWM mode, the device forces diode emulation while the SS pin voltage is less than 1.5 V. When the SS pin voltage is greater than 1.5 V, the device changes the zero current detection (ZCD) threshold gradually from 5 mV to -145 mV to achieve a smooth transition from diode emulation to FPWM mode.

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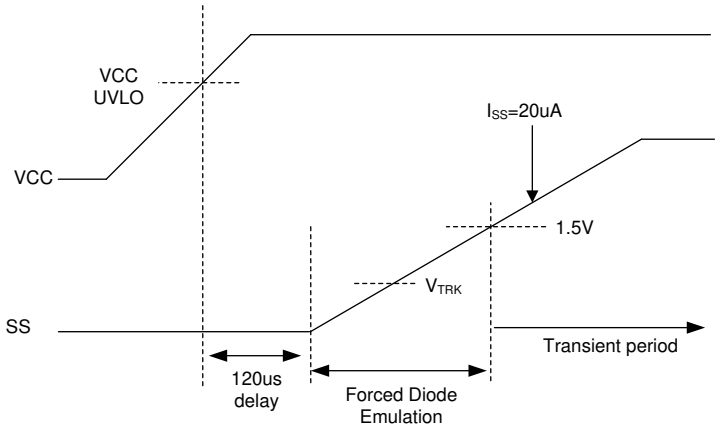

图 8-12. Soft Start and Smooth Transition to FPWM

In boost topology, the soft-start time (t_{SS}) varies with the input supply voltage because the boost output voltage is equal to the boost input voltage at the beginning of the soft-start switching. t_{SS} in boost topology is calculated in 方程式 10.

$$t_{SS} = V_{TRK} \times \frac{C_{SS}}{20\mu A} \times \left(1 - \frac{V_{SUPPLY}}{V_{LOAD}}\right) \quad (10)$$

In general, it is recommended to choose a soft-start time long enough so that the converter can start up without going into an overcurrent state. If the device is used for a pre-boost in automotive application, it is recommended to use 100-pF C_{SS} to reach steady state as soon as possible.

The device also features an internal 55-mV FB-to-SS clamp (V_{FB-SS}), which is activated if 256 consecutive switching cycles occur with current limit. The FB-to-SS clamp is deactivated if 32 consecutive switching cycles occur without exceeding the current limit threshold. This clamp helps to minimize surges after output shorts or over load situations. The device can enter deep sleep mode when SS is greater than 1.5 V. It is not recommended to pulldown SS to stop switching.

8.3.14 Wide Bandwidth Transconductance Error Amplifier and PWM (TRK, COMP Pin)

The device includes an internal feedback resistor voltage divider. The internal feedback resistor voltage divider is connected to the negative input of the internal transconductance error amplifier, and the TRK pin voltage programs the positive input of the internal transconductance error amplifier after the soft start is finished. The internal transconductance error amplifier features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 3 MHz) and sinks (or sources) current which is proportional to the difference between the negative and the positive inputs of the error amplifier.

The output of the error amplifier is connected to the COMP pin, allowing the use of a Type-2 loop compensation network. R_{COMP}, C_{COMP}, and an optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. This compensation network creates a pole at very low frequency, a mid-band zero, and a high frequency pole.

The PWM comparator in 图 8-13 compares the sum of the amplified sensed inductor current and the slope compensation ramp with the sum of the COMP pin voltage and a 0.3-V internal offset, and terminates the present cycle if the sum of the amplified sensed inductor current and the slope compensation ramp is greater than the sum of the COMP pin voltage and the 0.3-V internal offset.

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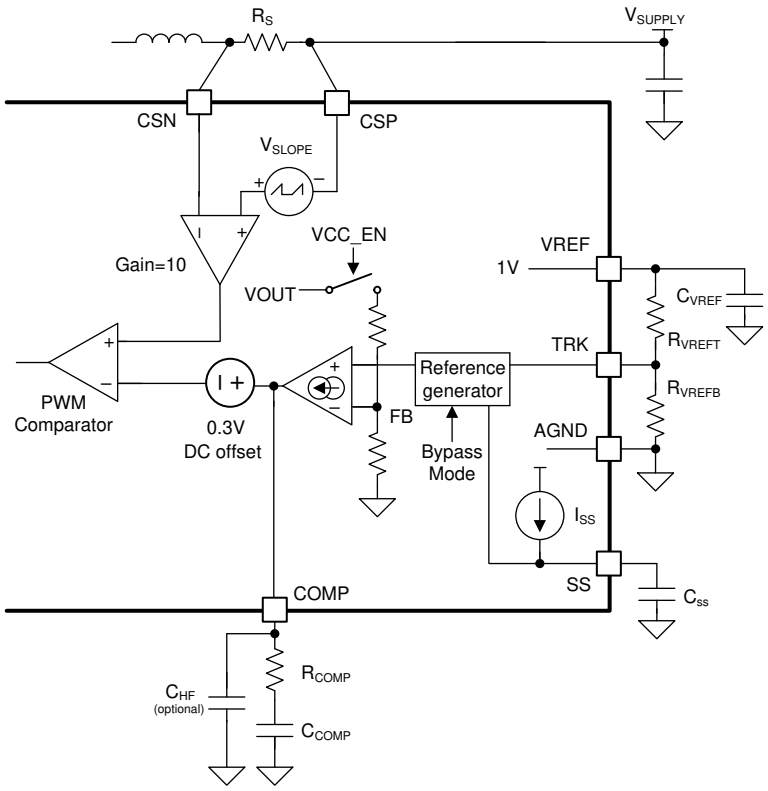

图 8-13. Error Amplifier, Current Sense Amplifier and PWM

8.3.15 Current Sensing and Slope Compensation (CSP, CSN Pin)

The device features a high-side current sense amplifier with an effective gain of 10 (A_{CS}), and provides an internal slope compensation ramp to the PWM comparator to prevent a subharmonic oscillation at high duty cycle. The device generates the 45-mV peak slope compensation ramp (V_{SLOPE}) at the input of the current sense amplifier which is 0.45-V peak (at 100% duty cycle) slope compensation ramp at the PWM comparator input.

According to peak current mode control theory, the slope of the slope compensation ramp must be greater than at least half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the minimum amount of the slope compensation must satisfy 方程式 11.

$$0.5 \times (V_{LOAD} - V_{SUPPLY}) / L_M \times R_S \times \text{Margin} < V_{SLOPE} \times f_{SW} \text{ (in Boost)} \quad (11)$$

where

- 1.5-1.7 is recommended as the Margin to cover non-ideal factors.

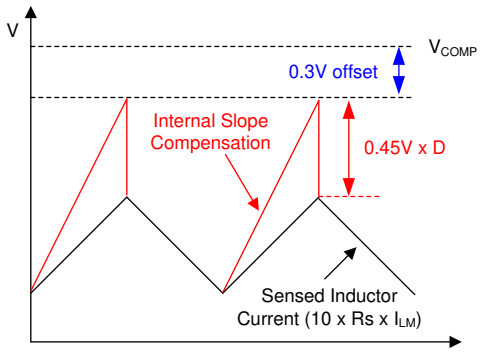

图 8-14. PWM Comparator Input

8.3.16 Constant Peak Current Limit (CSP, CSN Pin)

When the CSP-CSN voltage exceeds the 60-mV cycle-by-cycle current limit threshold (V_{CLTH}), the current limit comparator immediately terminates the LO output. The device provides an constant peak current limit whose peak inductor current limit is constant over the input and output voltage. For the case where the inductor current can overshoot, such as inductor saturation, the current limit comparator skips pulses until the current has decayed below the current limit threshold.

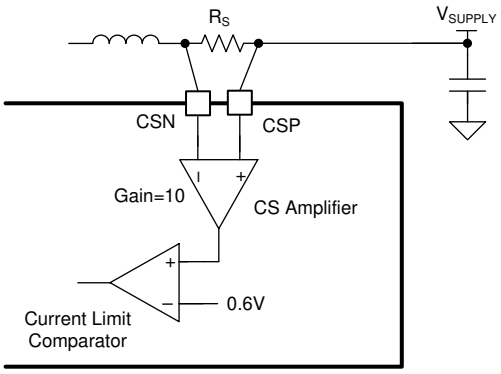

图 8-15. Current Limit Comparator

Cycle-by-cycle peak current limit is calculated as follows:

$$I_{PEAK-CL} = \frac{0.06}{R_S} \quad (12)$$

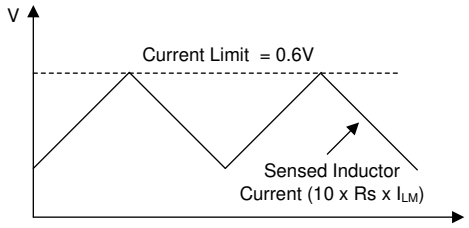

图 8-16. Current Limit Comparator Input

Boost converters have a natural pass-through path from the supply to the load through the high-side MOSFET body diode. Due to this path, boost converters cannot provide the peak current limit protection when the output voltage is close to or less than the input supply voltage, especially the peak current limit protection that does not work during the minimum on-time (t_{ON-MIN}).

8.3.17 Maximum Duty Cycle and Minimum Controllable On-time Limits

The device provides the maximum duty cycle limit (D_{MAX}) / minimum off-time to cover the non-ideal factors caused by resistive elements. D_{MAX} decides the minimum input supply voltage ($V_{SUPPLY(MIN)}$) which can achieve the target output voltage (V_{LOAD}) during CCM operation, but $V_{SUPPLY(MIN)}$ which can achieve the target output voltage during DCM operation is not limited by D_{MAX}. $V_{SUPPLY(MIN)}$, which can achieve the target output voltage during CCM operation, can be estimated as follows.

$$V_{SUPPLY(MIN)} \approx V_{LOAD} \times (1 - D_{MAX}) + I_{SUPPLY(MAX)} \times (R_{DCR} + R_S + R_{DS(ON)}) \quad (13)$$

where

- $I_{SUPPLY(MAX)}$ is the maximum input current at $V_{SUPPLY(MIN)}$
- R_{DCR} is the DC resistance of the inductor
- $R_{DS(ON)}$ is the turnon resistance of the MOSFET

At very light load condition or when V_{SUPPLY} is close to $V_{OUT-REG}$, the device skips the low-side driver pulses if the required on-time is less than t_{ON-MIN}. This pulse skipping appears as a random behavior. If V_{SUPPLY} is further increased to the voltage higher than $V_{OUT-REG}$, the required on-time becomes zero and eventually the device can start bypass operation which turns on the high-side driver 100% when the VOUT pin voltage is greater than V_{OVTH}.

8.3.18 Deep Sleep Mode and Bypass Operation (HO, CP Pin)

When SS is greater than 1.5 V, the device enters deep sleep mode after four cycles in OVP status. The device re-enters active mode if VOUT falls down below V_{OVP}. In FPWM or DE mode, the device turns on the high-side driver at 100% duty cycle (bypass operation) if the CP pin voltage is greater than V_{SYNC} or an external synchronization clock is applied before entering deep sleep mode. During bypass operation, the loss which is caused by the body diode of the high-side MOSFET is minimized. See *节 8.4.1.5* for more information.

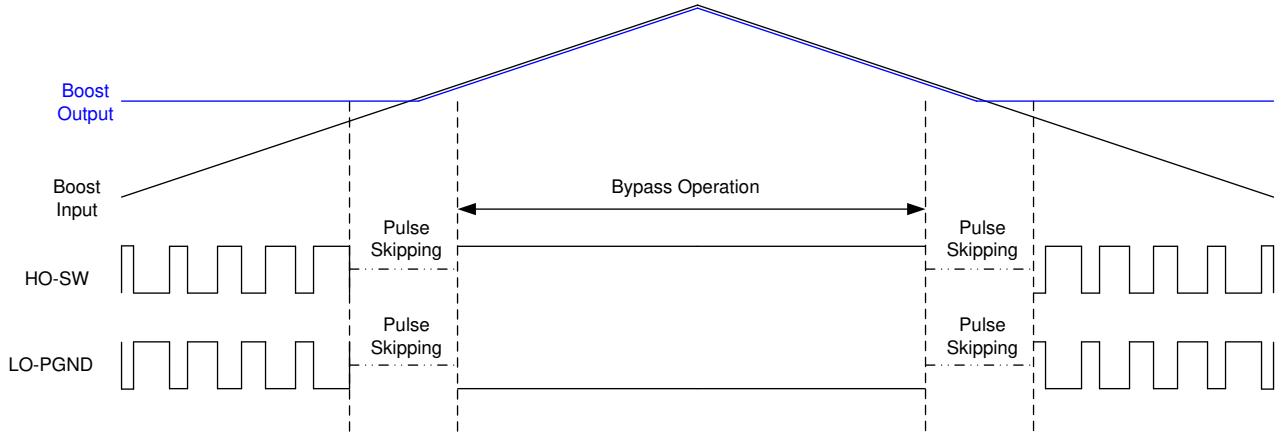

图 8-17. PWM to Bypass Transition in CCM Operation

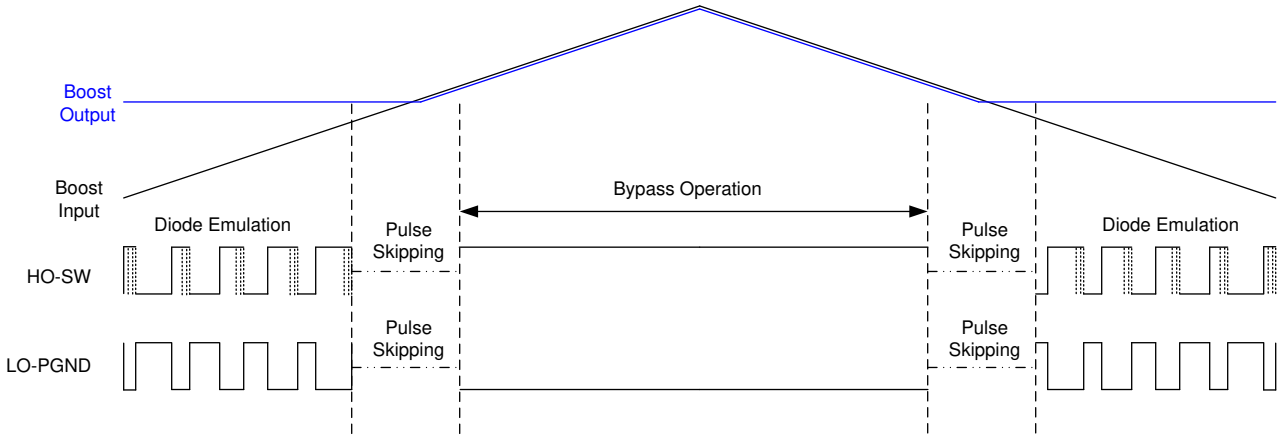

图 8-18. PWM to Bypass Transition in DCM Operation

8.3.19 MOSFET Drivers, Integrated Boot Diode, and Hiccup Mode Fault Protection (LO, HO, HB Pin)

The device provides N-channel logic MOSFET drivers, which can source a peak current of 2.2 A and sink a peak current of 3.3 A. The LO driver is powered by VCC, and is enabled when EN is greater than V_{EN} and VCC is greater than $V_{VCC-UVLO}$. The HO driver is powered by HB, and is enabled when EN is greater than V_{EN} and HB-SW voltage is greater than HB UVLO threshold ($V_{HB-UVLO}$).

When the SW pin voltage is approximately 0 V by turning on the low-side MOSFET, the C_{HB} is charged from VCC through the internal boot diode. The recommended value of the C_{HB} is 0.1 μF.

The LO and HO outputs are controlled with an adaptive dead-time methodology which ensures that both outputs are not turned on at the same time. When the device commands LO to be turned on, the adaptive dead-time

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logic first turns off HO and waits for HO-SW voltage to drop. LO is then turned on after a small delay (t_{DHL}). Similarly, the HO turnon is delayed until the LO-PGND voltage has discharged. HO is then turned on after a small delay (t_{DLH}).

If the BIAS pin voltage is below the 5-V VCC regulation target, take extra care when selecting the MOSFETs. The gate plateau voltage of the MOSFET switch must be less than the BIAS pin voltage to completely enhance the MOSFET, especially during start-up at low BIAS pin voltage. If the driver output voltage is lower than the MOSFET gate plateau voltage during start-up, the converter may not start up properly and it can stick at the maximum duty cycle in a high-power dissipation state. This condition can be avoided by selecting a lower threshold MOSFET or by turning on the device when the BIAS pin voltage is sufficient. Care should be taken when the converter operates in bypass at any conditions. During the bypass operation, the minimum HO-SW voltage is 4.0 V.

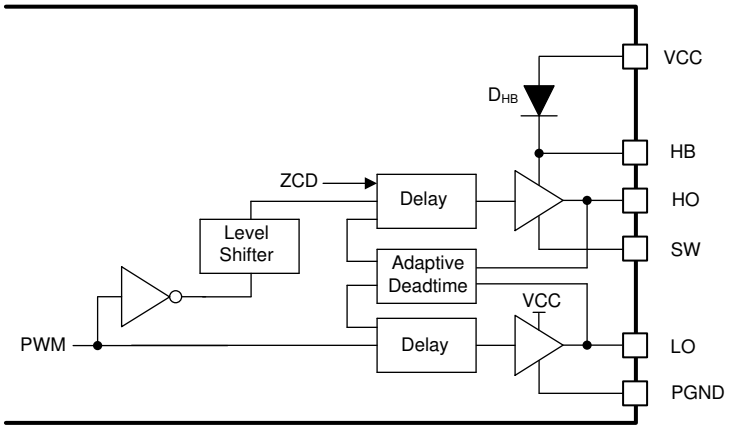

图 8-19. Driver Structure with Internal Boot Diode

The hiccup mode fault protection is triggered by the HB UVLO. If the HB-SW voltage is less than the HB UVLO threshold ($V_{HB-UVLO}$), the LO turns on by force for 75 ns to replenish the boost capacitor. The device allows up to four consecutive replenish switching. After the maximum four consecutive boot replenish switching, the device skips switching for 12 cycles. If the device fails to replenish the boost capacitor after the four sets of the four consecutive replenish switching, the device stops switching and enters 512 cycles of hiccup mode off-time. During the hiccup mode off-time, PGOOD and SS are grounded.

If required, the slew rate of the switching node voltage can be adjusted by adding a gate resistor in parallel with pulldown PNP transistor. Extra care should be taken when adding the gate resistor since it can decrease the effective dead-time.

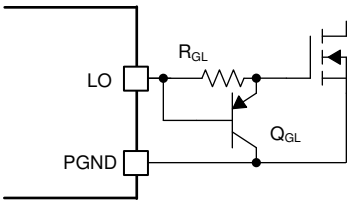

图 8-20. Slew Rate Control

8.3.20 Thermal Shutdown Protection

An internal thermal shutdown (TSD) is provided to protect the device if the junction temperature (T_J) exceeds 175°C. When TSD is activated, the device is forced into a low-power thermal shutdown state with the MOSFET drivers and the VCC regulator disabled. After the T_J is reduced (typical hysteresis is 15ºC), the device restarts. The TSD is disabled during sleep or deep sleep mode.

8.4 Device Functional Modes

8.4.1 Device Status

8.4.1.1 Shutdown Mode

When EN is less than V_{EN} and VH is less than V_{SYNC}, the device shuts down, consuming 3 μA from BIAS. In shutdown mode, COMP, SS, and PGOOD are grounded. The device is enabled when EN is greater than V_{EN} or VH is greater than V_{SYNC}.

8.4.1.2 Configuration Mode

When the device is enabled initially, the 120-μs device configuration starts if VCC is greater than $V_{VCC-UVLO}$. During device configuration, the light load switching mode and VOUT range are selected. The device configuration is reset when the device shuts down or VCC falls down below 2.2 V. The preferred way to reconfigure the device is to shut down the device. During the configuration time, a 33-kΩ internal EN pulldown resistor is connected, the minimum sourcing capability of the VCC regulator is 100 mA and the RT pin is regulated to 0.5 V by the internal RT regulator.

8.4.1.3 Active Mode

After the 120-μs initial device configuration is finished, the device enters active mode with all functions enabled if UVLO is greater than V_{UVLO}. In active mode, a soft-start sequence starts and the error amplifier is enabled.

8.4.1.4 Sleep Mode

When skip mode is selected as the light load switching mode and SS is greater than 1.5 V, the device enters sleep mode if the low-side driver skips switching for 16 consecutive cycles. Once the device enters sleep mode, the device cannot re-enter active mode during 8 μs minimum sleep time. During sleep mode, the device stops internal oscillator to reduce the operating current, disables UVLO comparator, disables the error amplifier, and parks the COMP pin at 0.25 V. The device re-enters active mode if the VOUT pin voltage falls down below the wake up threshold (V_{WAKE}) which is 1.1% lower than the $V_{OUT-REG}$.

8.4.1.5 Deep Sleep Mode

When SS is greater than 1.5 V, the device enters deep sleep mode after four cycles in OVP status. During deep sleep mode, the device stops the internal oscillator to reduce the operating current, disables UVLO comparator, disables the error amplifier, and parks the COMP pin at 0.25 V. In FPWM or DE mode, the device turns on the high-side driver 100% (bypass operation) if CP is greater than V_{SYNC} before entering deep sleep mode. In skip mode, the high-side switch turns off during deep sleep mode.

In FPWM or DE mode, the device re-enters active mode if VOUT falls down below V_{OVTH}. In skip mode, the device re-enters active mode if VOUT falls down below V_{OVTH}, then immediately enters sleep mode after 16 consecutive cycles of pulse skipping.

8.4.2 Light Load Switching Mode

The device provides three light load switching modes. Inductor current waveforms in each mode are different at the light/no load condition.

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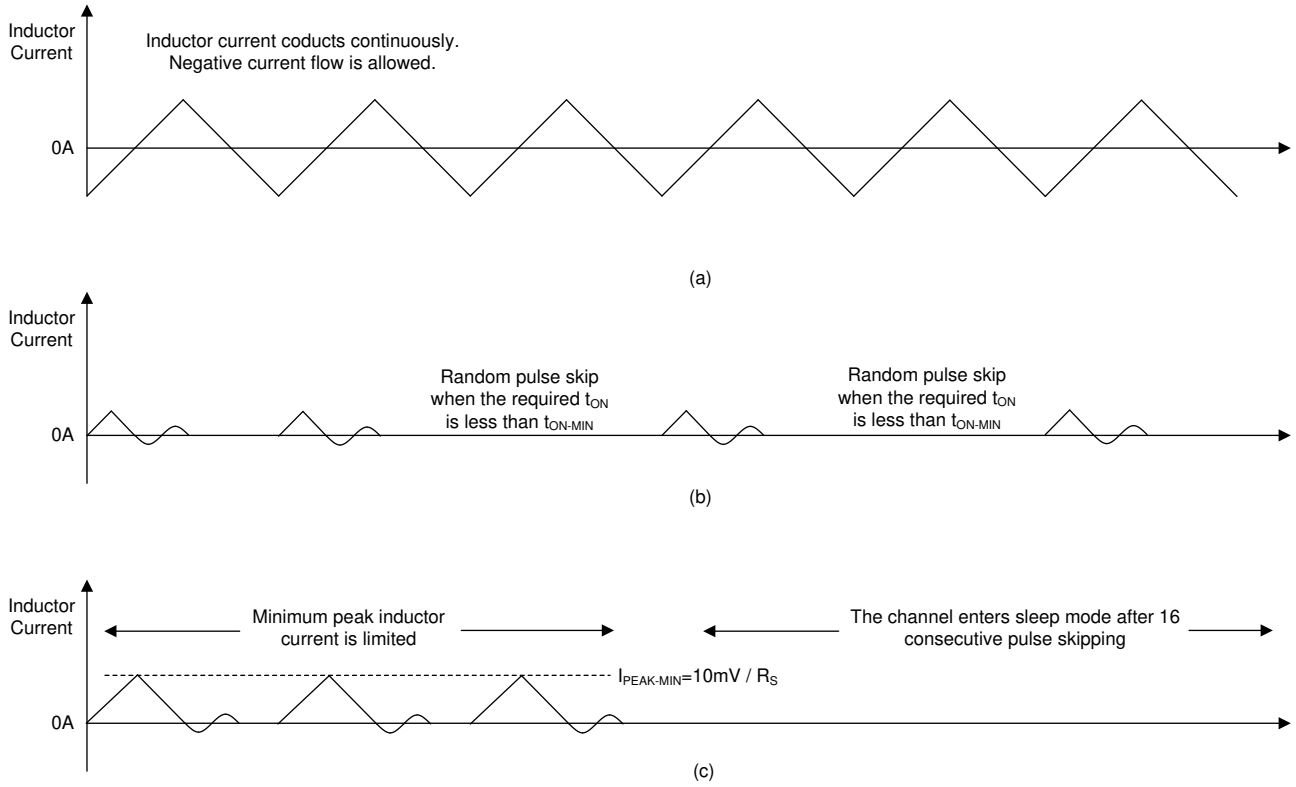

图 8-21. Inductor Current Waveform at Light Load (a) FPWM (b) Diode Emulation (c) Skip Mode

8.4.2.1 Forced PWM (FPWM) Mode

In FPWM mode, the inductor current conducts continuously at light or no load conditions, allowing a continuous conduction mode (CCM) operation. The benefits of the FPWM mode are a fast light load to heavy load transient response, and constant switching frequency at light or no load conditions. The maximum reverse current is limited to 145 mV/$R_{DS(ON)}$ in FPWM mode.

8.4.2.2 Diode Emulation (DE) Mode

In diode emulation (DE) mode, inductor current flow is allowed only in one direction - from the input source to the output load. The device monitors the SENSE-SW voltage during the high-side switch on-time and turns off the high-side switch for the remainder of the PWM cycle when the SENSE-SW voltage falls down below the 5 mV zero current detection (ZCD) threshold (V_{ZCD}). The benefit of the diode emulation is a higher efficiency than FPWM mode efficiency at light load condition.

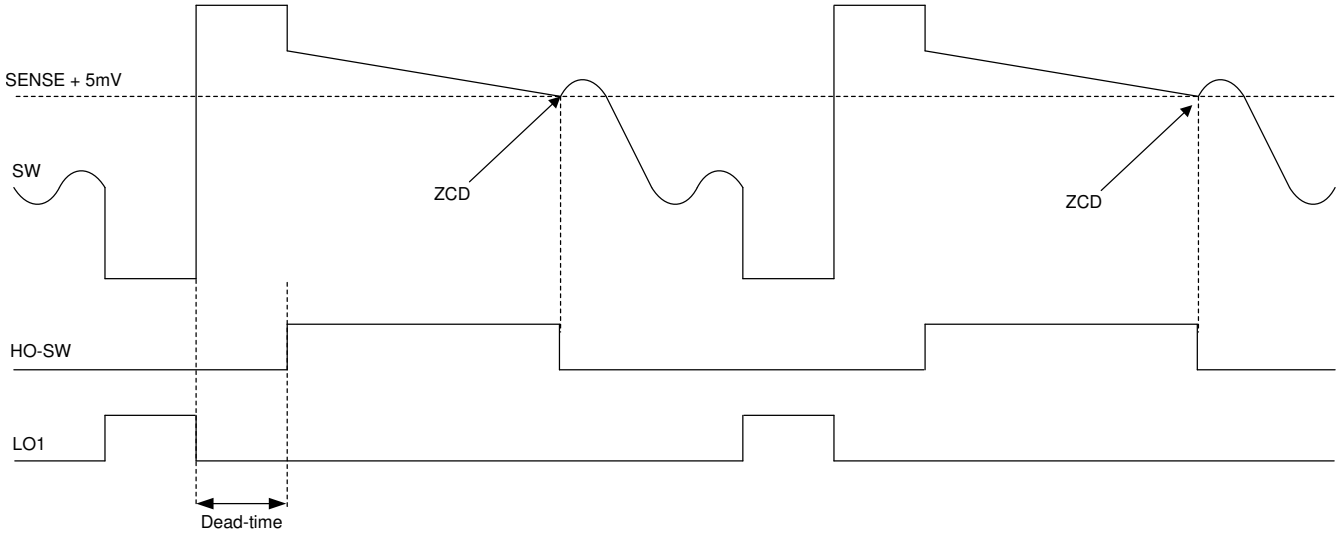

图 8-22. Zero Current Detection

8.4.2.3 Forced Diode Emulation Operation in FPWM Mode

During soft start, the device forces diode emulation while the SS pin voltage is less than 1.5 V. When the SS pin is greater than 1.5 V, the device reduces the zero current detection (ZCD) threshold down to -145 mV. The peak-to-peak inductor current must satisfy 方程式 14 for a proper FPWM operation at no load.

(14)

8.4.2.4 Skip Mode

When skip mode is selected as the light load switching mode, the device enters sleep mode when the pulse skip counter detects 16 consecutive cycles of pulse skipping in the active mode, and re-enters the active mode if VOUT falls down below V_{WAKE}.

The light load efficiency can be increased by entering sleep mode more frequently and staying in sleep mode longer. In skip mode and when SS is greater than 1.5 V, the device works in the diode emulation, but the minimum peak current is limited to 10 mV/R_S once the low-side driver turns on. By limiting the minimum peak current, the boost converter is able to supply more current than what is required when switching, and enters sleep mode more frequently and stays longer in the sleep mode.

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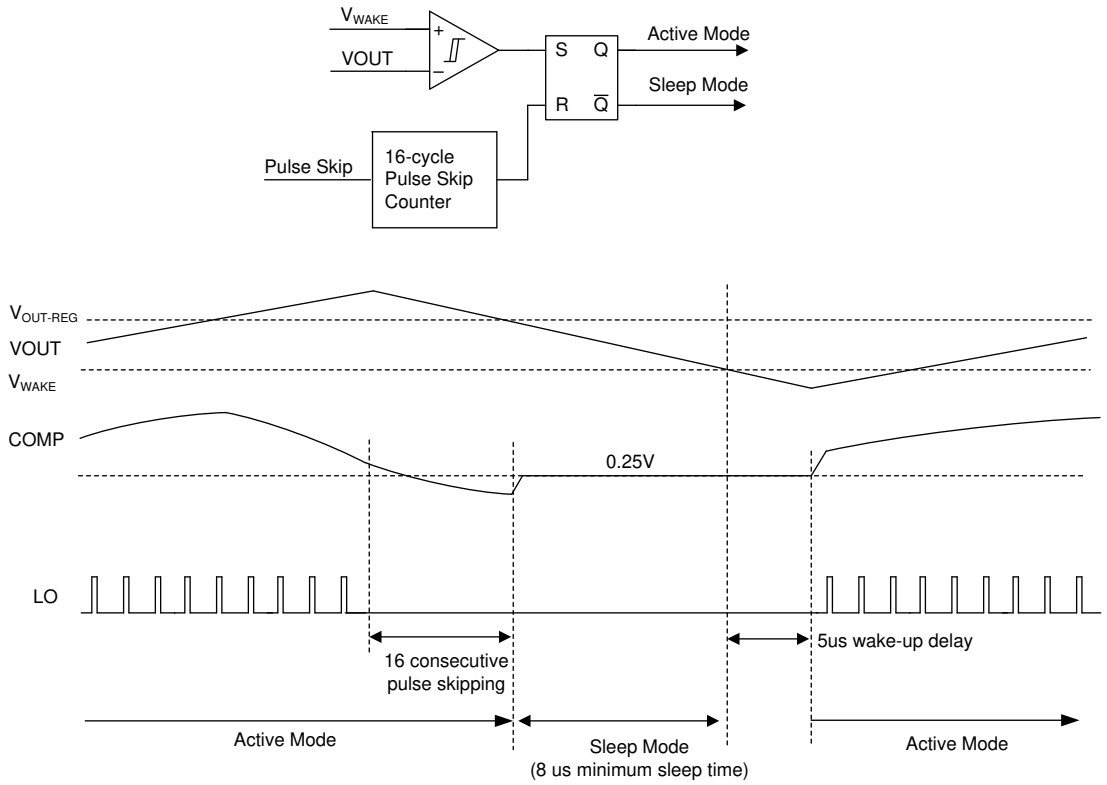

图 8-23. Skip Mode Operation

When skip mode is selected as the light load switching mode, L_M should be selected for the peak inductor to reach the 10m-V minimum peak current limit before LO turns off by D_{MAX} at the minimum V_{SUPPLY}.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

TI provides an application note that explains how to design boost converter using the device. This comprehensive application note includes component selections and loop response optimization.

See the *How to Design a Boost Using the LM5123* application note for more information on loop response and component selection.

9.2 Typical Application

图 9-1 shows all optional components to design a boost converter.

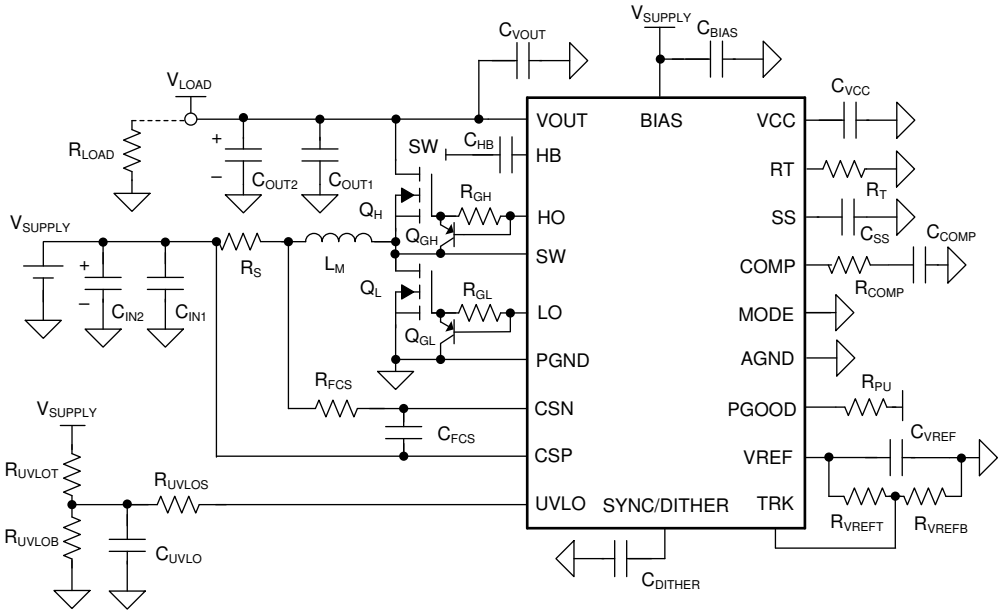

图 9-1. Typical Synchronous Boost Converter with Optional Components

9.2.1 Design Requirements

表 9-1 shows the intended input, output, and performance parameters for this application example.

表 9-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Minimum input supply voltage ($V_{SUPPLY(MIN)}$)	9 V
Target output voltage (V_{LOAD})	24 V
Maximum load current (I_{LOAD})	4 A (96 Watt)
Typical switching frequency (f_{SW})	440 kHz

9.2.2 Detailed Design Procedure

Use the Quick Start Calculator to expedite the process of designing of a regulator for a given application. Download the *LM5123 Quick Start Calculator* for detailed design procedure.

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See the *LM5123EVM-BST Evaluation Module* EVM user guide for recommended components and typical application curves.

9.2.3 Application Ideas

For applications requiring the lowest cost with minimum conduction loss, inductor DC resistance (DCR) can be used to sense the inductor current rather than using a sense resistor. R_{DCRC} and C_{DCRC} must meet 方程式 15 to match a time constant.

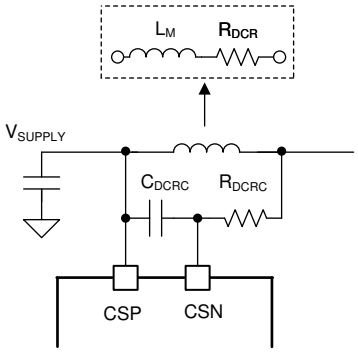

图 9-2. DCR Current Sensing

$$\frac{L_M}{R_{DCR}} = R_{DCRC} \times C_{DCRC} \tag{15}$$

If required, an additional PGOOD delay can be programmed using an external circuit.

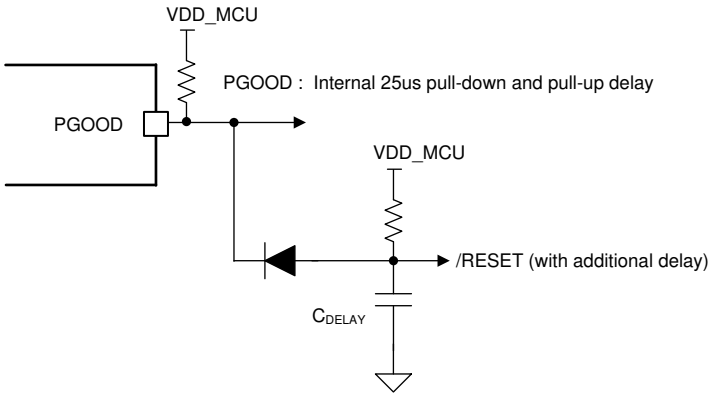

图 9-3. Additional PGOOD Delay

9.3 System Example

To configure non-synchronous boost converter, please connect SW to PGND, and connect HB to VCC.

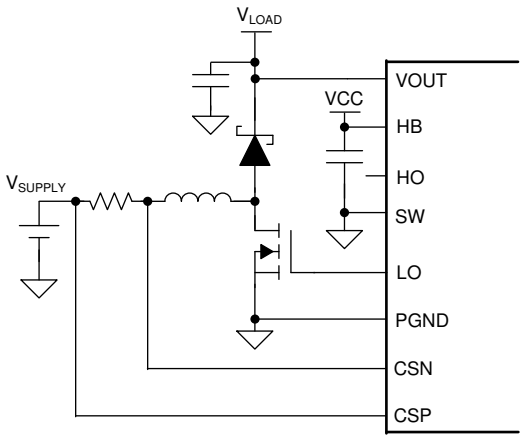

图 9-4. Non-synchronous Boost Configuration

10 Power Supply Recommendations

The device is designed to operate from a power supply or a battery whose voltage range is from 0.8 V to 42 V. The input power supply must be able to supply the maximum boost supply voltage and handle the maximum input current at 0.8 V. The impedance of the power supply and battery including cables must be low enough that an input current transient does not cause an excessive drop. Additional input ceramic capacitors can be required at the supply input of the converter.

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11 Layout

11.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Place C_{VCC}, C_{BIAS}, C_{HB}, and C_{VOUT} as close to the device. Make direct connections to the pins.
- Place Q_H, Q_L, and C_{OUT}. Make the switching loop (C_{OUT} to Q_H to Q_L to C_{OUT}) as small as possible. A small size ceramic capacitor helps to minimize the loop length. Leave a copper area near the drain connection of Q_H for a thermal dissipation.
- Place L_M, R_S, and C_{IN}. Make the loop (C_{IN} to R_S to L_M to C_{IN}) as small as possible. A small size ceramic capacitor helps to minimize the loop length.
- Connect R_S to CSP-CSN. The CSP-CSN traces must be routed in parallel and surrounded by ground.
- Connect VOUT, HO, and SW. These traces must be routed in parallel using a short, low inductance path. VOUT must be directly connected the drain connection of Q_H. SW must be directly connected to the source connection of Q_H
- Connect LO and PGND. The LO-PGND traces must be routed in parallel using a short, low inductance path. PGND must be directly connected the source connection of Q_L
- Place R_{COMP}, C_{COMP}, C_{SS}, C_{VREF}, R_{VREFT}, R_{VREFB}, R_T, and R_{UVLOB} as close to the device, and connect to a common analog ground plane.
- Connect power ground plane (the source connection of the Q_L) to EP through PGND. Connect the common analog ground plane to EP through AGND. PGND and AGND must be connected underneath the device.
- Add several vias under EP to help conduct heat away from the device. Connect the vias to a large analog ground plane on the bottom layer.
- Do not connect C_{OUT} and C_{IN} grounds underneath the device and through the large analog ground plane which is connected to EP.

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11.2 Layout Example

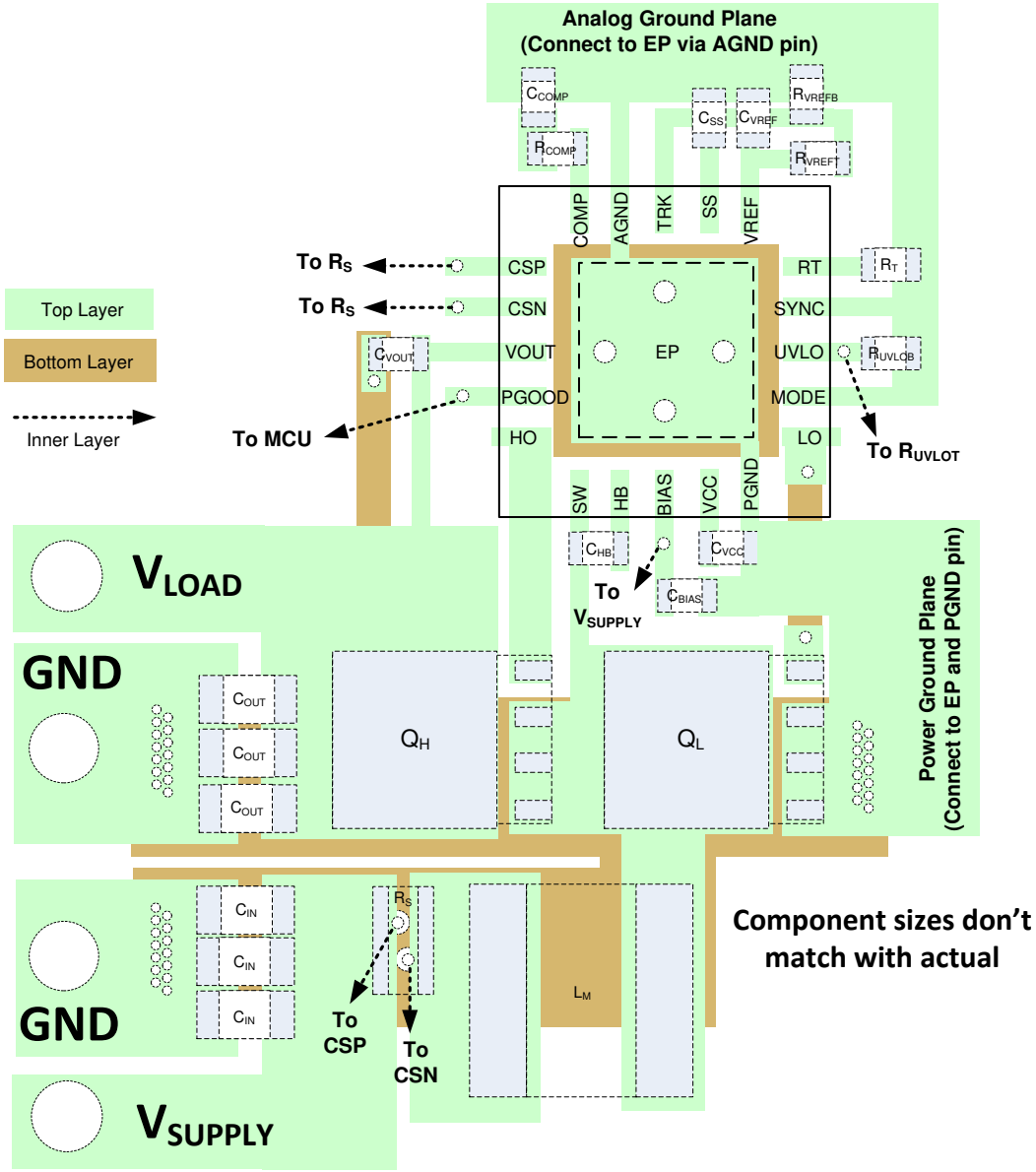

图 11-1. PCB Layout Example

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12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5123QRGRRQ1	PREVIEW	VQFN	RGR	20	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 150		
XLM5123QRGRRQ1	ACTIVE	VQFN	RGR	20	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

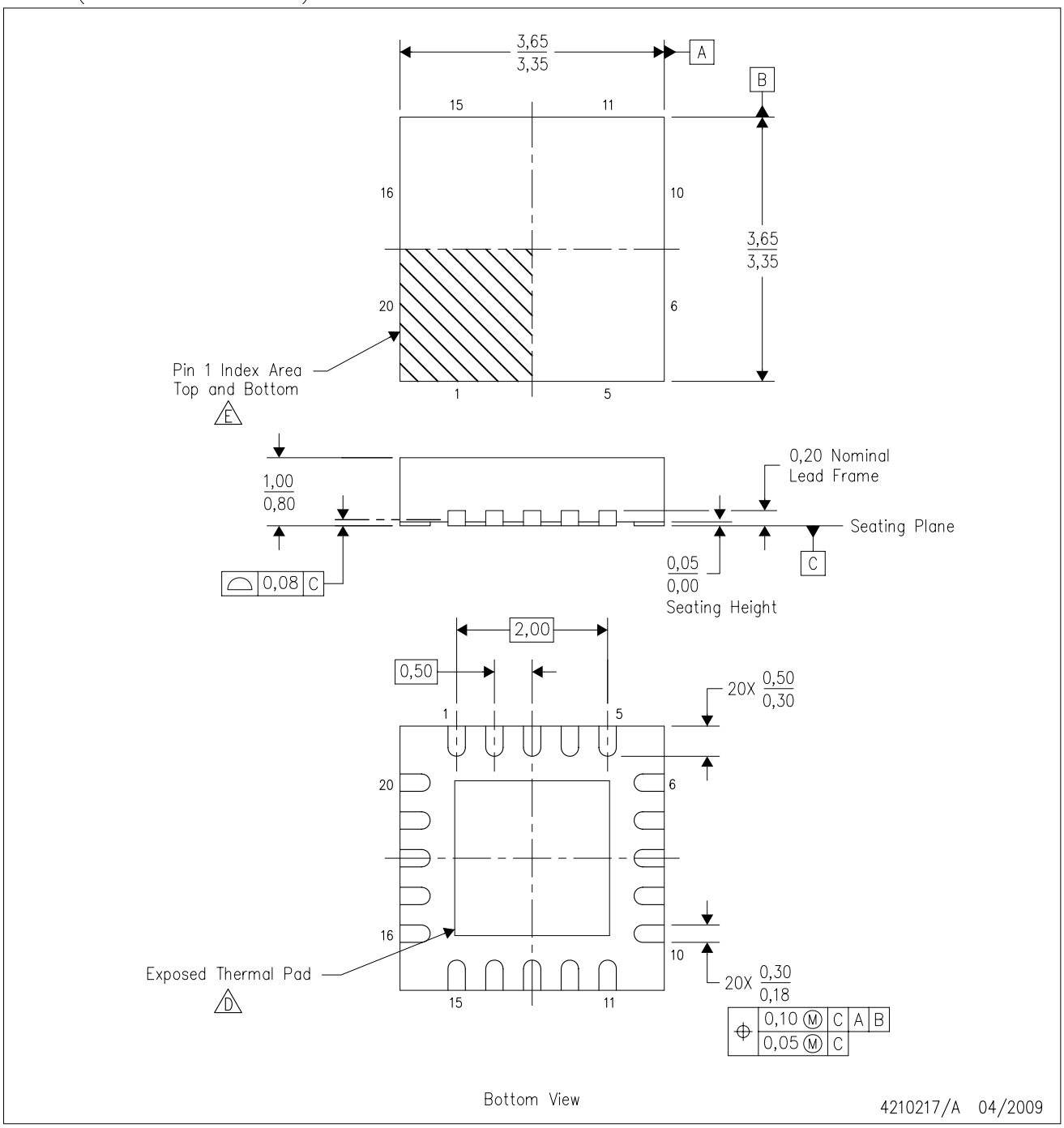
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

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