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## 4 Revision History

<b>Changes from Revision B (February 2021) to Revision C (June 2021)</b>	<b>Page</b>
• Updated resistor from FB to GND values.....	<b>3</b>
• Updated voltage reference specifications.....	<b>6</b>
• Updated <a href="#">Section 9.2.2.1</a> .....	<b>16</b>

<b>Changes from Revision A (October 2020) to Revision B (February 2021)</b>	<b>Page</b>
• Added TPS613783-Q1 and TPS613785-Q1 variants to data sheet.....	<b>6</b>

<b>Changes from Revision * (May 2020) to Revision A (October 2020)</b>	<b>Page</b>
• Changed TPS61378-Q1 device status from Advance Information to Production Data.....	<b>1</b>
• Updated the numbering format for tables, figures and cross-references throughout the document.....	<b>1</b>

## 5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE (V)	RESISTOR FROM FB TO GND ( $R_{FB\_LOW}$ )	SPREAD SPECTRUM
TPS61378-Q1	5	$0\Omega \leq R_{FB\_LOW} \leq 2.4\text{ k}\Omega$	Enable
	5.25	$3.6\text{ k}\Omega \leq R_{FB\_LOW} \leq 4.8\text{ k}\Omega$	
	5.5	$7.2\text{ k}\Omega \leq R_{FB\_LOW} \leq 9.6\text{ k}\Omega$	
	Adjustable	$14.4\text{ k}\Omega \leq R_{FB\_LOW} \leq 100\text{ k}\Omega$	
TPS613781-Q1 <sup>(1)</sup>	5.7	$0\Omega \leq R_{FB\_LOW} \leq 2.4\text{ k}\Omega$	Enable
	6.2	$3.6\text{ k}\Omega \leq R_{FB\_LOW} \leq 4.8\text{ k}\Omega$	
	7	$7.2\text{ k}\Omega \leq R_{FB\_LOW} \leq 9.6\text{ k}\Omega$	
	8	$14.4\text{ k}\Omega \leq R_{FB\_LOW} \leq 100\text{ k}\Omega$	
TPS613782-Q1 <sup>(1)</sup>	9	$0\Omega \leq R_{FB\_LOW} \leq 2.4\text{ k}\Omega$	Enable
	10	$3.6\text{ k}\Omega \leq R_{FB\_LOW} \leq 4.8\text{ k}\Omega$	
	11	$7.2\text{ k}\Omega \leq R_{FB\_LOW} \leq 9.6\text{ k}\Omega$	
	12	$14.4\text{ k}\Omega \leq R_{FB\_LOW} \leq 100\text{ k}\Omega$	
TPS613783-Q1	5	$0\Omega \leq R_{FB\_LOW} \leq 2.4\text{ k}\Omega$	Disable
	5.25	$3.6\text{ k}\Omega \leq R_{FB\_LOW} \leq 4.8\text{ k}\Omega$	
	5.5	$7.2\text{ k}\Omega \leq R_{FB\_LOW} \leq 9.6\text{ k}\Omega$	
	Adjustable	$14.4\text{ k}\Omega \leq R_{FB\_LOW} \leq 100\text{ k}\Omega$	
TPS613784-Q1 <sup>(1)</sup>	5.7	$0\Omega \leq R_{FB\_LOW} \leq 2.4\text{ k}\Omega$	Disable
	6.2	$3.6\text{ k}\Omega \leq R_{FB\_LOW} \leq 4.8\text{ k}\Omega$	
	7	$7.2\text{ k}\Omega \leq R_{FB\_LOW} \leq 9.6\text{ k}\Omega$	
	8	$14.4\text{ k}\Omega \leq R_{FB\_LOW} \leq 100\text{ k}\Omega$	
TPS613785-Q1	9	$0\Omega \leq R_{FB\_LOW} \leq 2.4\text{ k}\Omega$	Disable
	10	$3.6\text{ k}\Omega \leq R_{FB\_LOW} \leq 4.8\text{ k}\Omega$	
	11	$7.2\text{ k}\Omega \leq R_{FB\_LOW} \leq 9.6\text{ k}\Omega$	
	12	$14.4\text{ k}\Omega \leq R_{FB\_LOW} \leq 100\text{ k}\Omega$	

(1) Product Preview. Contact TI factory for more information.

## 6 Pin Configuration and Functions

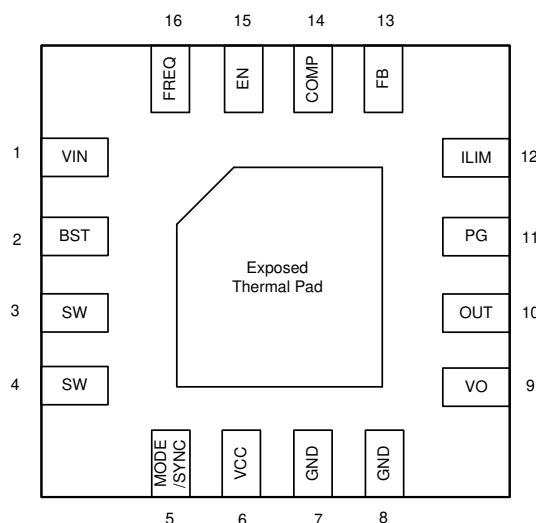


Figure 6-1. 16-Pin WQFN RTE Package (Transparent Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	IC power supply input
BST	2	I	Power supply for high-side N-MOSFET gate drivers. A capacitor must be connected between this pin and the SW pin.
SW	3, 4	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side FET and the source of the high-side FET.
MODE / SYNC	5	I	Mode selection pin. MODE = high, forced PWM mode MODE = low or floating, auto PFM mode This pin can also be used to synchronize the external clock. Refer to <a href="#">Table 8-1</a> for details.
VCC	6	O	Output of internal regulator. A ceramic capacitor with more than 1 $\mu$ F must be connected between this pin and GND.
GND	7, 8	PWR	Power ground of the IC. It is connected to the source of the low-side FET.
VO	9	PWR	Output of the isolation FET. Connect load to this pin to achieve input/output isolation.
OUT	10	PWR	Output of the drain of the HS FET. Connect this pin because the output can disable the load disconnect/short protection feature (or short this pin with the VO pin).
PG	11	O	Power good indicator and open drain output
ILIM	12	I	Current limit setting pin. Use a resistor to set the desired peak current limit. Refer to <a href="#">Section 8.3.7</a> for details.
FB	13	I	Feedback pin. Use a resistor divider to set the desired output voltage. Refer to <a href="#">Section 9.2.2.1</a> for details.
COMP	14	I	Output of the internal transconductance error amplifier. An external RC network is connected to this pin to optimize the loop stability and response time.
EN	15	I	Enable logic input
FREQ	16	I	Frequency setting pin. Connect a resistor between this pin and GND pin to set the desired frequency.
Thermal Pad	-	-	The thermal pad must be connected to the power ground plane for good power dissipation.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage range at terminals <sup>(2)</sup>	VIN	-0.3	16	V
Voltage range at terminals <sup>(2)</sup>	VO, SW, OUT	-0.3	23	V
	BST	-0.3	SW + 6	V
	MODE/SYNC, FB, FREQ, ILIM, VCC, COMP, EN	-0.3	6	V
	PG	-0.3	20	V
T <sub>J</sub> <sup>(3)</sup>	Operating junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperatures greater than 125°C

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub> <sup>(1)</sup>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(2)</sup>	±2000	V
		Charged-device model (CDM), per AEC Q100-011, all pins <sup>(3)</sup>	±500	
V <sub>(ESD)</sub> <sup>(1)</sup>	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011, corner pins (1,4,5,8,9,12,13,16) <sup>(3)</sup>	±750	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	2.3		14	V
V <sub>OUT</sub>	Output voltage	4		18.5	V
T <sub>A</sub>	Operating ambient temperature	-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS61378-Q1	UNIT
		RTE	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	46.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	43.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	18.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	18.5	°C/W

THERMAL METRIC <sup>(1)</sup>		TPS61378-Q1	UNIT
		RTE	
		16 PINS	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	8.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

T<sub>J</sub> = -40 to 125°C, L = 1 μH, V<sub>IN</sub> = 3.3 V and V<sub>OUT</sub> = 9 V (VO pin). Typical values are at T<sub>J</sub> = 25°C, (unless otherwise noted)

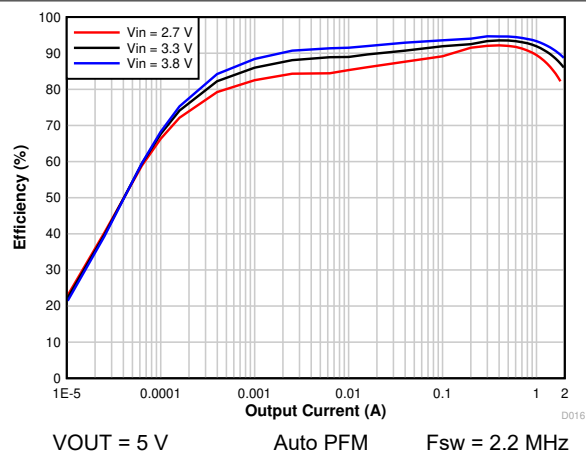
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
V <sub>IN</sub>	Input voltage range		2.3		14	V
V <sub>IN_UVLO</sub>	VIN under voltage lockout threshold	V <sub>IN</sub> rising		2.2	2.3	V
		V <sub>IN</sub> falling		2.04	2.2	V
V <sub>IN_HYS</sub>	VIN UVLO hysteresis			160		mV
V <sub>CC_UVLO</sub>	VCC UVLO threshold	V <sub>CC</sub> rising		2.2		V
V <sub>CC_HYS</sub>	VCC UVLO hysteresis	V <sub>CC</sub> hysteresis		150		mV
V <sub>CC</sub>	VCC regulation	I <sub>VCC</sub> = 6 mA, V <sub>OUT</sub> = 9V		4.8		V
I <sub>Q</sub>	Quiescent current into V <sub>IN</sub> pin	IC enabled, no load, V <sub>IN</sub> = 3.3 V, V <sub>OUT</sub> = 18.5 V, V <sub>FB</sub> = V <sub>REF</sub> + 0.1 V,		25	35	μA
I <sub>Q</sub>	Quiescent current into OUT pin	IC enabled, no load, V <sub>IN</sub> = 3.3 V, V <sub>OUT</sub> = 18.5 V, V <sub>FB</sub> = V <sub>REF</sub> + 0.1 V,		10	20	μA
I <sub>SD</sub>	Shutdown current into VIN pin	IC disabled, V <sub>IN</sub> = 14 V, EN = GND		0.6	5	μA
I <sub>SW_LKG</sub>	Leakage current into SW	IC disabled, V <sub>IN</sub> = OUT = SW = 14 V			5	μA
I <sub>VO_LKG</sub>	Reverse leakage current into VO	IC disabled, OUT = VO = 5 V, SW = 0			5	μA
<b>OUTPUT VOLTAGE</b>						
V <sub>OVP</sub>	Output over-voltage protection threshold	V <sub>IN</sub> = 3.3 V, V <sub>OUT</sub> rising	19.3	20	20.5	V
V <sub>OVP_HYS</sub>	Output over-voltage protection hysteresis	V <sub>IN</sub> = 3.3 V, OVP threshold		0.5		V
<b>VOLTAGE REFERENCE</b>						
V <sub>REF</sub>	Reference Voltage at FB pin	T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 16.0 kΩ	0.788	0.800	0.812	V
V <sub>OUT_5V</sub>		T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 2.0 kΩ	4.85	5.00	5.15	V
V <sub>OUT_5.25V</sub>		T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 4.0 kΩ	5.10	5.25	5.35	V
V <sub>OUT_5.5V</sub>		T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 8.0 kΩ	5.35	5.50	5.65	V
V <sub>OUT_5V</sub>		TPS613783Q1, T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 2.0 kΩ	4.85	5.00	5.15	V
V <sub>OUT_5.25V</sub>		TPS613783Q1, T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 4.0 kΩ	5.10	5.25	5.35	V
V <sub>OUT_5.5V</sub>		TPS613783Q1, T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 8.0 kΩ	5.35	5.50	5.65	V
V <sub>OUT_9V</sub>		TPS613785Q1, T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 2.0 kΩ	8.75	9.00	9.15	V
V <sub>OUT_10V</sub>		TPS613785Q1, T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 4.0 kΩ	9.75	10.00	10.20	V
V <sub>OUT_11V</sub>		TPS613785Q1, T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 8.0 kΩ	10.70	11.00	11.20	V
V <sub>OUT_12V</sub>		TPS613785Q1, T <sub>J</sub> = -40 to 125°C, R <sub>FB</sub> = 16.0 kΩ	11.70	12.00	12.22	V
I <sub>FB_LKG</sub>	Leakage current into FB pin				50	nA
<b>POWER SWITCH</b>						
R <sub>DS(on)</sub>	Low-side MOSFET on resistance	V <sub>CC</sub> = 4.85 V		50		mΩ
R <sub>DS(on)</sub>	High-side MOSFET on resistance	V <sub>CC</sub> = 4.85 V		50		mΩ
R <sub>DS(on)</sub>	Isolation MOSFET on resistance	V <sub>CC</sub> = 4.85 V		100		mΩ
<b>CURRENT LIMIT</b>						

$T_J = -40$  to  $125^\circ\text{C}$ ,  $L = 1\ \mu\text{H}$ ,  $V_{IN} = 3.3\ \text{V}$  and  $V_{OUT} = 9\ \text{V}$  (VO pin). Typical values are at  $T_J = 25^\circ\text{C}$ , (unless otherwise noted)

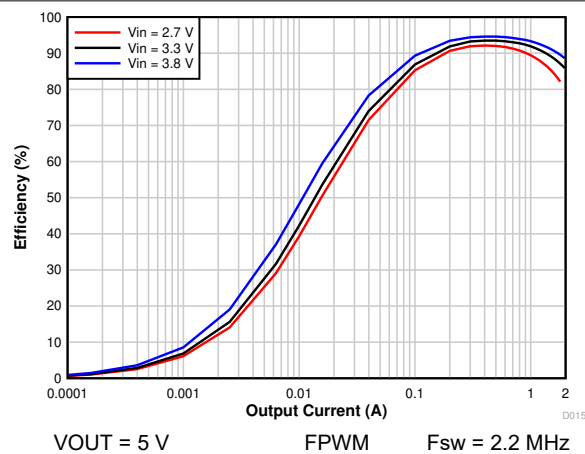
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LIM\_SW}$	Peak switching current limit FPWM	$R_{LIM} = 20\ \text{k}\Omega$ , Duty cycle = 65%	4	4.8	5.55	A
$I_{LIM\_SW}$	Peak switching current limit Auto PFM	$R_{LIM} = 20\ \text{k}\Omega$ , Duty cycle = 65%	4	4.8	5.55	A
$I_{LIM\_SW}$	Peak switching current limit FPWM	$R_{LIM} = 102\ \text{k}\Omega$ , Duty cycle = 65%, 4.7 $\mu\text{H}$		0.75		A
$I_{LIM\_SW}$	Peak switching current limit Auto PFM	$R_{LIM} = 102\ \text{k}\Omega$ , Duty cycle = 65%, 4.7 $\mu\text{H}$		0.75		A
$I_{LIM\_SS\_1}$	Peak switching current limit at softstart	$V_{IN} = 3.3\ \text{V}$ , $V_{OUT} = 0\ \text{V}$ , $R_{LIM} = 20\ \text{k}\Omega$	0.9	1.15	1.4	A
<b>SWITCHING FREQUENCY</b>						
Fsw	Switching frequency	$R_{FREQ} = 18\ \text{k}\Omega$	2050	2200	2400	kHz
Fsw	Switching frequency	$R_{FREQ} = 218\ \text{k}\Omega$	180	200	230	kHz
$D_{max}$	Maximum Duty Cycle	$R_{FREQ} = 18\ \text{k}\Omega$	78			%
$t_{ON\_min}$	Minimal on time			70		ns
F <sub>DITHER</sub>				10%		Fsw
F <sub>pattern</sub>				0.4%		Fsw
<b>ERROR AMPLIFIER</b>						
$I_{SINK}$	COMP pin sink current	$V_{FB} = V_{REF} + 0.2\text{V}$		6		$\mu\text{A}$
$I_{SOURCE}$	COMP pin source current	$V_{FB} = V_{REF} - 0.2\text{V}$		6		$\mu\text{A}$
$V_{CCLPH}$	COMP pin high clamp voltage	$V_{FB} = V_{REF} - 0.2\text{V}$ , $I_{LIM} = 4.8\ \text{A}$		1.3		V
$V_{CCLPL}$	COMP pin high low voltage	$V_{FB} = V_{REF} + 0.2\text{V}$ ,		0.6		V
$G_{mEA}$	Error amplifier trans conductance	$V_{COMP} = 1.0\ \text{V}$		70		$\mu\text{S}$
<b>POWER GOOD</b>						
$V_{PG\_TH}$	PG threshold for rising FB voltage	Reference to $V_{REF}$		90%		
$V_{PG\_HYS}$	PG hysteresis	Reference to $V_{REF}$		5%		
$I_{PG\_SINK}$	PG pin sink current capability	$V_{PG} = 0.4\ \text{V}$		20		mA
$t_{PG\_DELAY}$	PG delay time		2.5	3.4	4.3	ms
<b>DOWN MODE</b>						
$t_{EN\_DELAY}$	Delay time between EN high and device working			0.4		ms
$t_{SS}$	Softstart time			2.5		ms
$t_{HCP\_ON}$	Hiccup on time			1.8		ms
$t_{HCP\_OFF}$	Hiccup off time			67		ms
<b>SYNC TIMING</b>						
$f_{SYNC\_MIN}$				200		kHz
$f_{SYNC\_MAX}$				2200		kHz
<b>EN/SYNC LOGIC</b>						
$V_{IH}$	EN, MODE/SYNC pins Logic high threshold				1.2	V
$V_{IL}$	EN, MODE/SYNC pins Logic Low threshold		0.4			V
$R_{DOWN}$	EN, MODE/SYNC pins internal pull down resistor			800		k $\Omega$
<b>THERMAL SHUTDOWN</b>						
$t_{SD\_R}$	Thermal shutdown rising threshold	$T_J$ rising		165		$^\circ\text{C}$
$t_{SD\_F}$	Thermal shutdown falling threshold	$T_J$ falling		145		$^\circ\text{C}$

## 7.6 Typical Characteristics

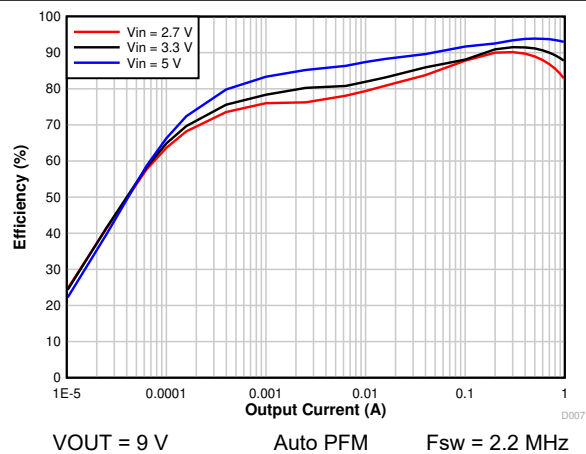
$V_{IN} = 3.3\text{ V}$ ,  $V_{OUT} = 9\text{ V}$  (VO pin),  $T_A = 25^\circ\text{C}$ ,  $F_{sw} = 2.2\text{ MHz}$ , unless otherwise noted.



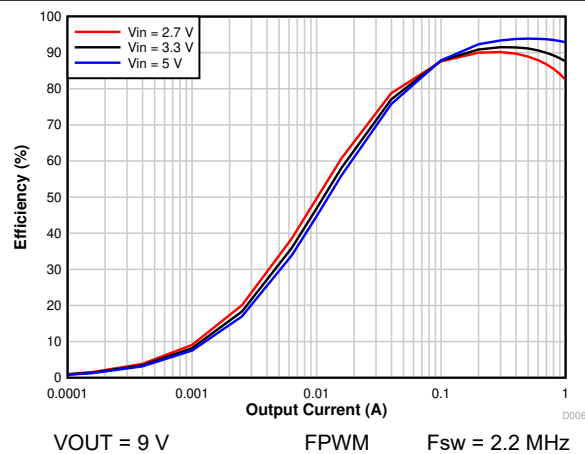
**Figure 7-1. 5 V<sub>OUT</sub> Efficiency vs Output Current**



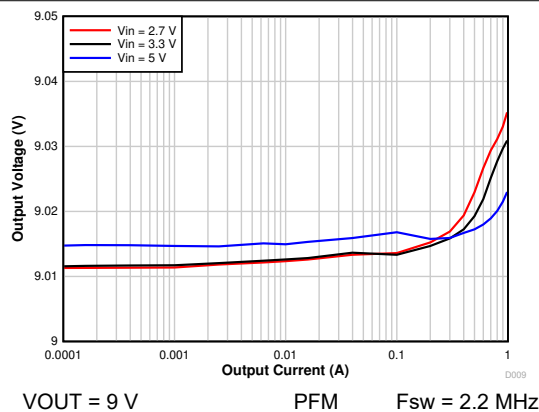
**Figure 7-2. 5 V<sub>OUT</sub> Efficiency vs Output Current**



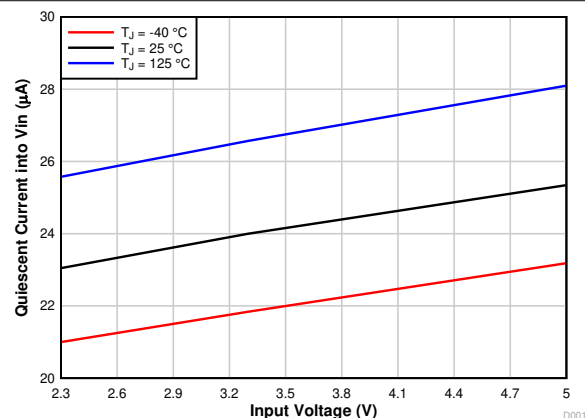
**Figure 7-3. 9 V<sub>OUT</sub> Efficiency vs Output Current**



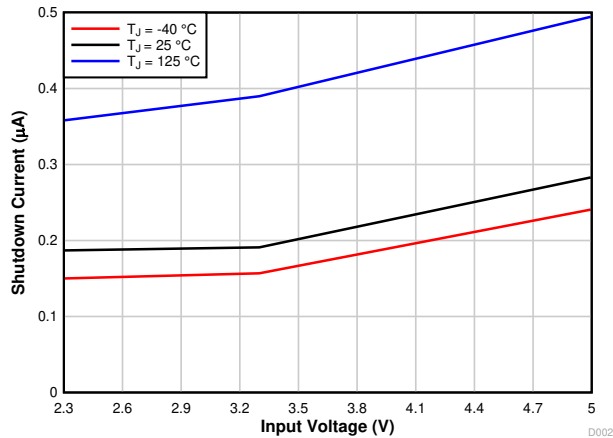
**Figure 7-4. 9 V<sub>OUT</sub> Efficiency vs Output Current**



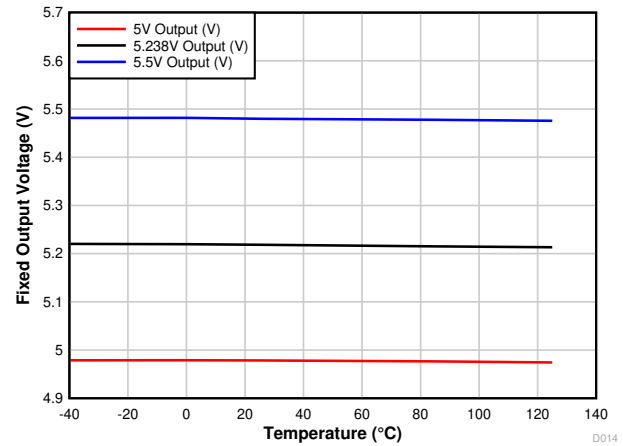
**Figure 7-5. 9 V<sub>OUT</sub> Regulation vs Output Current**



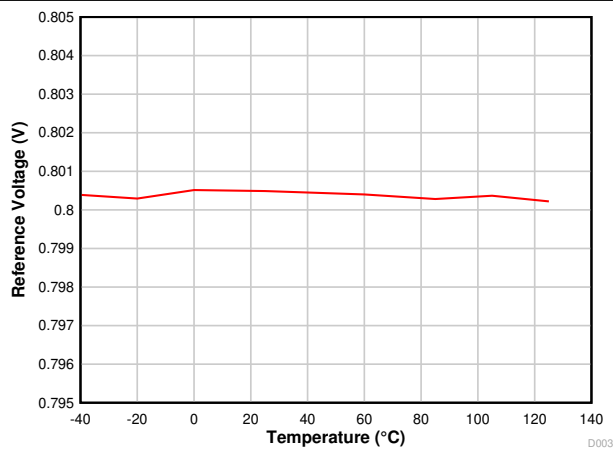




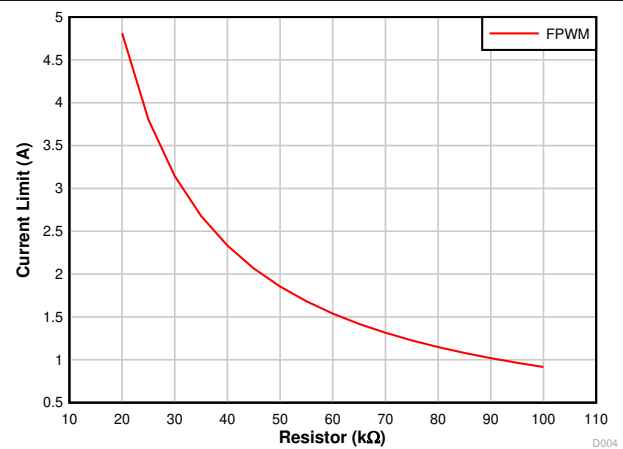
**Figure 7-7. Shutdown Current vs Input Voltage**



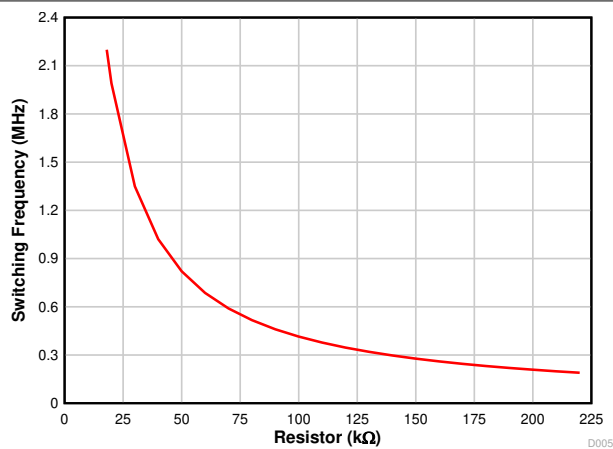
**Figure 7-8. Fixed Output Voltage vs Temperature**



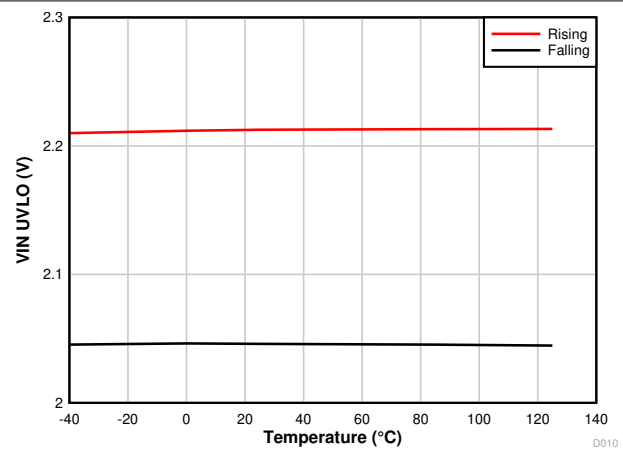
**Figure 7-9. Reference Voltage vs Temperature**



**Figure 7-10. Current Limit vs Setting Resistance**



**Figure 7-11. Switching Frequency vs Setting Resistance**



**Figure 7-12.  $V_{IN}$  UVLO Threshold Voltage vs Temperature**

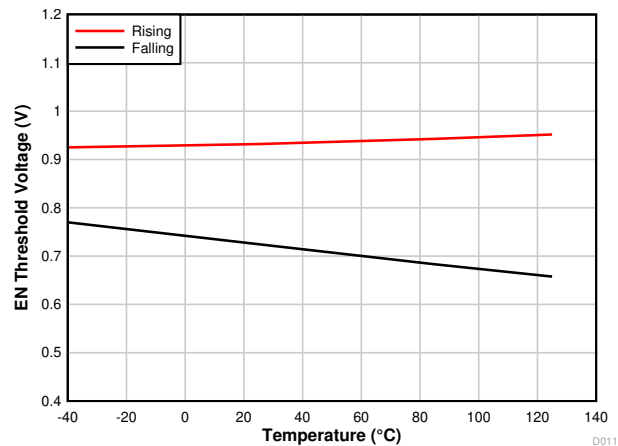


Figure 7-13. EN Threshold Voltage vs Temperature

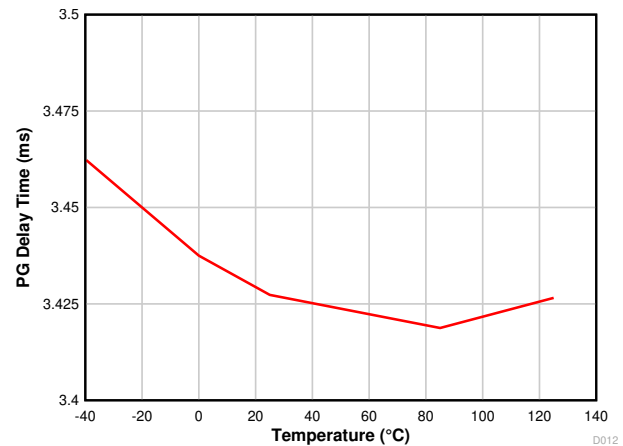


Figure 7-14. PG Delay Time vs Temperature

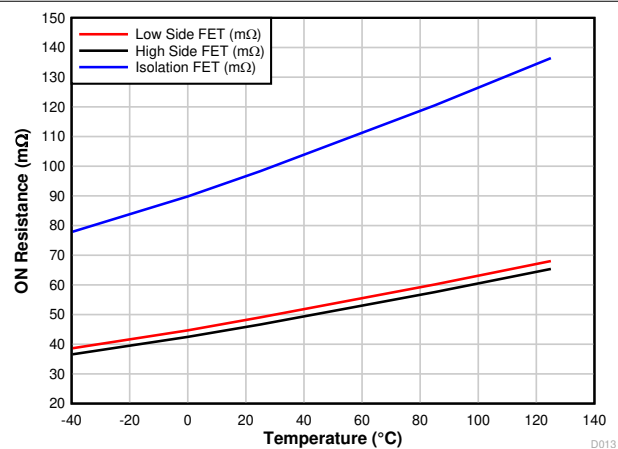


Figure 7-15.  $R_{DS(on)}$  vs Temperature

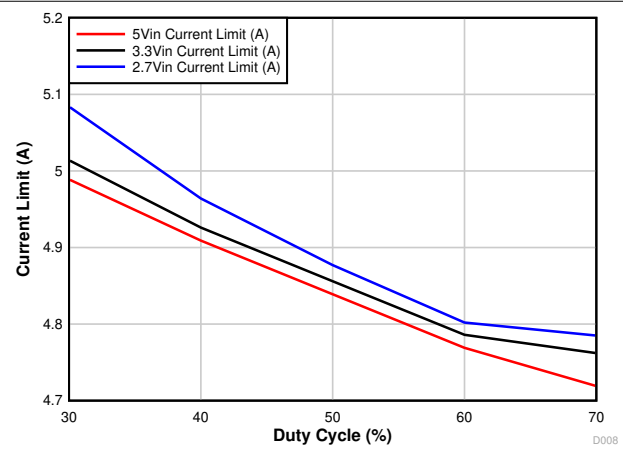


Figure 7-16. Duty Cycle vs Current Limit

## 8 Detailed Description

### 8.1 Overview

The TPS61378-Q1 is a fully-integrated synchronous boost converter with load disconnect function. It supports output voltage up to 18.5 V with a maximum of a 4.8-A programmable switching peak current limit. The input voltage ranges from 2.3 V to 14 V while consuming 25- $\mu$ A quiescent current.

The TPS61378-Q1 utilizes the fixed-frequency peak current control scheme, which has an internal oscillator and supports adjustable switching frequency from 200 kHz to 2.2 MHz.

The TPS61378-Q1 operates with fixed-frequency pulse width modulation (PWM) from medium to heavy load. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on. The inductor current ramps up to a peak current that is determined by the output of the internal error amplifier (EA). Once the switching peak current triggers the output of the EA, the low-side N-MOSFET is turned off and the high-side N-MOSFET is turned on after a short dead time. The high-side N-MOSFET switch is not turned off until the next cycle as determined by the internal oscillator. The low-side switch turns on again after a short dead time and the switching cycle is repeated.

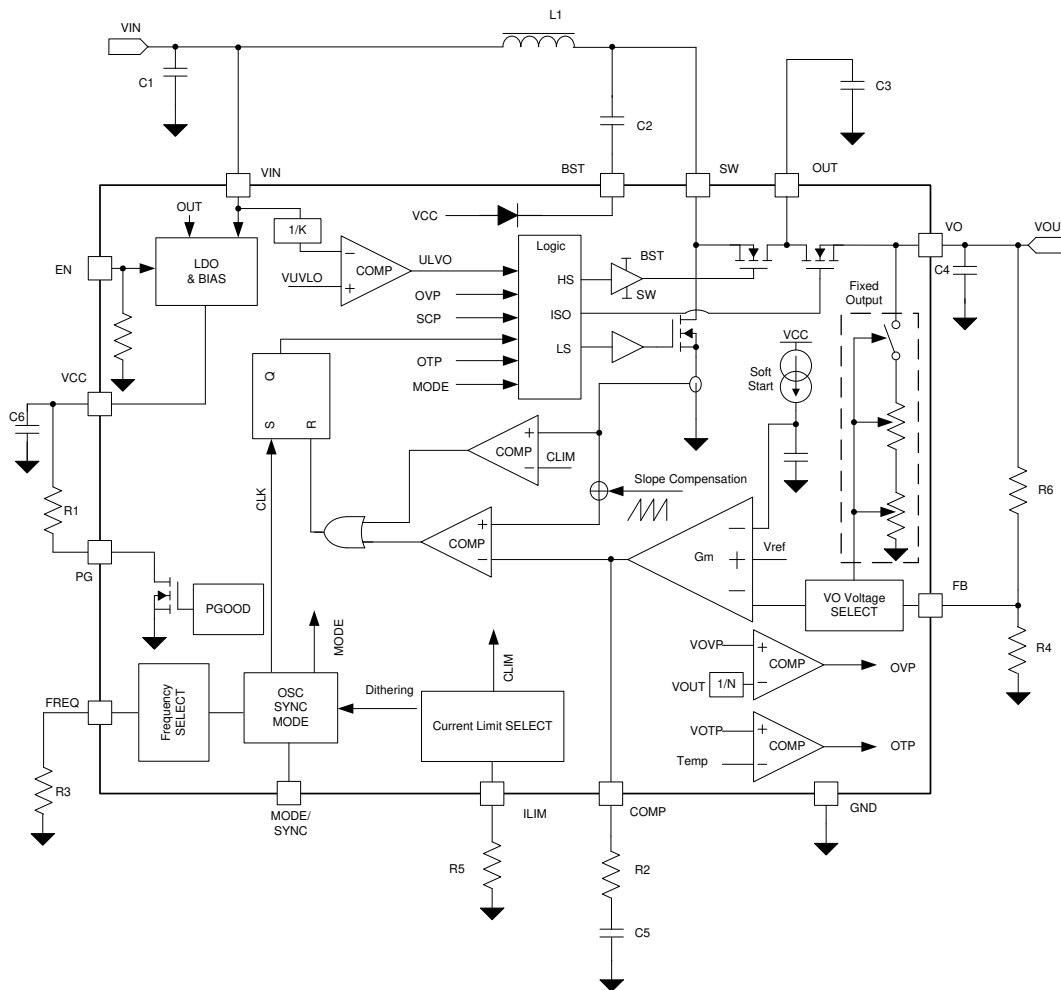
The TPS61378-Q1 provides either auto PFM or forced PWM for the light load operation by configuring the MODE/SYNC pin. In forced PWM mode, the switching frequency remains constant across the entire load range, which helps avoid frequency variation with load. The internal oscillator can be synchronized to an external clock applied on the MODE/SYNC pin. Spread spectrum modulation of the frequency in forced PWM mode helps optimize the EMI performance for automotive applications. In auto PFM mode, the switching frequency can decrease, resulting in higher efficiency.

The TPS61378-Q1 implements a cycle-by-cycle current limit to protect the device from overload during the boost operation phase. If the output current further increases and triggers the output voltage to fall below the input voltage, the TPS61378-Q1 enters into hiccup mode short protection.

There is a built-in soft-start time, which prevents the inrush current during the start-up. The TPS61378-Q1 also provides a power good (PG) indicator to enable the power sequence control for start-up.

The TPS61378-Q1 also has a number of protection features including output short protection, output overvoltage protection (OVP), and thermal shutdown protection (OTP).

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 VCC Power Supply

The internal LDO in the TPS61378-Q1 outputs a regulated voltage of 4.8 V with 10-mA output current capability. A ceramic capacitor is connected between the VCC pin and GND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. The value of this ceramic capacitor should be above 1  $\mu$ F. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10 V is recommended.

### 8.3.2 Input Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.04 V (typical). A hysteresis of 160 mV (typical) is added so that the device cannot be enabled again until the input voltage exceeds 2.2 V (typical). This function is implemented to prevent the device from malfunctioning when the input voltage is between 2.04 V and 2.2 V.

### 8.3.3 Enable and Soft Start

When the input voltage is above the UVLO threshold and the EN pin is pulled above 1.2 V, the TPS61378-Q1 is enabled. The device starts to monitor the FB pin. With a typical 400- $\mu$ s delay time after EN is pulled high, the TPS61378-Q1 starts switching. There is an internal built-in start-up time, typically 2.5 ms, to limit the inrush current during start-up.

### 8.3.4 Shut Down

When the input voltage is below the UVLO threshold or the EN pin is pulled low, the TPS61378-Q1 is in shutdown mode and all the functions are disabled. The input voltage is isolated from the output to minimize the leakage currents.

### 8.3.5 Switching Frequency Setting

The TPS61378-Q1 uses a fixed-frequency control scheme. The switching frequency can be programmed between 200 kHz and 2.2 MHz using a resistor from the FREQ pin to GND. The resistor must be connected when the oscillator is synchronized by an external clock. The resistance is defined by [Equation 1](#).

$$F_{SW}(\text{MHz}) = \frac{41.9}{R_{FREQ}(\text{k}\Omega) + 1.05} \quad (1)$$

where

- $R_{FREQ}$  is the resistance between the FREQ pin and the GND pin

For example, the switching frequency is 2.2 MHz if the resistance between the FREQ pin and GND is 18 k $\Omega$ . This pin cannot be left floating or tied to VCC.

### 8.3.6 Spread Spectrum Frequency Modulation

The TPS61378-Q1 uses a triangle waveform to spread the switching frequency with  $\pm 10\%$  of normal frequency. The frequency of the triangle waveform is typically 0.4% of the switching frequency. For example, if the normal switching frequency of the TPS61378-Q1 is programmed to 2.2 MHz, the spread spectrum function modulates the switching frequency in the range of 1.98 MHz to 2.42 MHz in a triangle behavior with an 8.8-kHz rate.

The spread spectrum is only available while the clock of the TPS61378-Q1 is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- An external clock is applied to the MODE/SYNC pin.
- The device works in PFM operation at light load.

### 8.3.7 Adjustable Peak Current Limit

The TPS61378-Q1 adopts a cycle-by-cycle peak current limit internally. The low-side switch is turned off immediately as soon as the switch peak current triggers the limit threshold. The peak switch current limit can be set by a resistor from the ILIM pin to ground. The relationship between the current limit and the resistor is shown in [Equation 2](#).

$$R_{LIM}(\text{k}\Omega) = 1.184 + \frac{90.56}{I_{LIM}(\text{A})} \quad (2)$$

where

- $R_{LIM}$  is the resistance between the ILIM pin and the GND pin
- $I_{LIM}$  is switch peak current limit

For instance, the current limit is set to 4.8 A if the  $R_{LIM}$  is 20 k $\Omega$ . This pin cannot be left floating or connected to VCC.

### 8.3.8 Bootstrap

The TPS61378-Q1 has an integrated bootstrap regulator circuit. A small ceramic capacitor is needed between the BST pin and SW pin to provide the gate drive supply voltage for high-side switches. The bootstrap capacitor is charged during the time when the low-side switch is in the ON state. The value of this ceramic capacitor should be above 0.1  $\mu\text{F}$ . A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 6.3 V is recommended.

### 8.3.9 Load Disconnect

The TPS61378-Q1 integrates a load disconnect function when the input source is DC, completely cutting off the path between the input side and output side during shutdown.

The output disconnect function also allows the output short protection and minimizes the inrush current at start-up.

### 8.3.10 MODE/SYNC Configuration

Table 8-1 summarizes the MODE/SYNC function and the entry condition.

**Table 8-1. MODE/SYNC Configuration**

MODE/SYNC PIN CONFIGURATION	MODE
Logic Low or Floating	Auto PFM Mode
Logic High	Forced PWM Mode
External Synchronization	Forced PWM Mode

The TPS61378-Q1 can be synchronized to an external clock applied to the MODE/SYNC pin.

### 8.3.11 Overvoltage Protection (OVP)

If the output voltage exceeds the OVP threshold (typically 20 V), the TPS61378-Q1 immediately stops switching until the output voltage drops below the recovery threshold (typically 19.5 V). This function protects the device against excessive voltage.

### 8.3.12 Output Short Protection/Hiccup

In addition to the cycle-by-cycle current limit function, the TPS61378-Q1 also has output short protection. If the output current causes the low-side FET to reach current limit and pull the output voltage below the input voltage, the device enters into short circuit protection mode, triggering the hiccup timer. When the hiccup timer is triggered, the device limits the current to a relative lower level for 1.8 ms and then shuts down. After 67 ms, it will restart. If the short condition disappears, the device will automatically restart.

When FB voltage is below  $\leq 0.1$  V during fault condition, the current limit threshold is reduced to 1/5 of the programmed current limit. Frequency is clamped to 1.1 MHz if the FREQ pin setting is greater than 1.1 MHz.

### 8.3.13 Power Good Indicator

The TPS61378-Q1 integrates a power good function. The PG pin asserts when the output voltage rises above 90% of the target output voltage. The PG pin is an open-drain output before  $V_{OUT}$  reaches the 90% target output voltage. The PG pin becomes active low after a typical 3.4-ms delay time after  $V_{OUT}$  reaches 90% of the target output voltage. When the output voltage drops below 85% of the target output voltage, the PG logic immediately goes low without delay.

### 8.3.14 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown occurs at junction temperatures exceeding 165°C. When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 145°C (typical).

## 8.4 Device Functional Modes

### 8.4.1 Forced PWM Mode

The TPS61378-Q1 enters forced PWM mode by pulling the MODE/SYNC pin to logic high for more than five switching cycles. In forced PWM mode, the TPS61378-Q1 keeps the switching frequency constant at light load condition. When the load current decreases, the output of the internal error amplifier also decreases to keep the inductor peak current down. When the output current decreases further, the high-side switch is not turned off even if the current of the high-side switch goes negative to keep the frequency constant.

### 8.4.2 Auto PFM Mode

The TPS61378-Q1 enters auto PFM Mode by pulling the MODE/SYNC pin to logic low for more than five switching cycles or leaving the pin floating. The TPS61378-Q1 improves the efficiency at light load when operating in PFM mode. When the output current decreases to a certain level, the output voltage of the error amplifier is clamped by the internal circuit. If the output current reduces further, the inductor current through the

high-side switch will be clamped but not lowered further. Pulses are skipped to improve the efficiency at light load.

### 8.4.3 External Clock Synchronization

The TPS61378-Q1 supports external clock synchronization with a range of 200 kHz to 2.2 MHz. The TPS61378-Q1 remains in forced PWM mode and operates in CCM across the entire load range if the oscillator is synchronized by an external clock. The spread spectrum feature is disabled when external synchronization is used.

### 8.4.4 Down Mode

The TPS61378-Q1 features down mode operation when input voltage is close to or higher than output voltage. In down mode, output voltage is regulated at target value, even when  $V_{IN} > V_O$ . The TPS61378-Q1 high-side and low-side FETs are switching devices that always work in boost operation, where the isolation FET always works as a linear device.

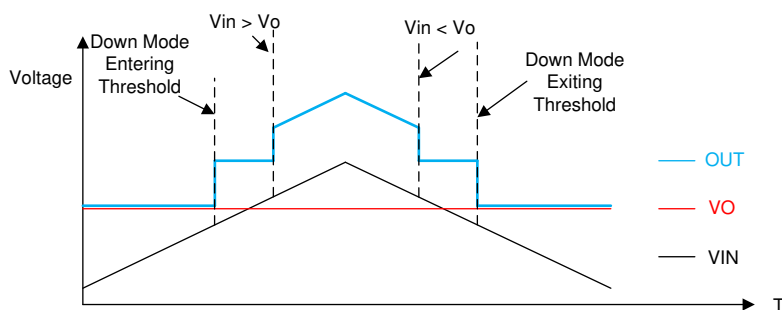
For boost circuits, on-time or duty cycle is reduced as input voltage approaches output voltage. The TPS61378-Q1 enters down mode when  $V_{IN}$  reaches 85% (typical) of  $V_O$  voltage at 2.2 MHz. Exiting down mode requires  $V_{IN}$  to be reduced below 85% (typical) of  $V_O$  voltage at 2.2 MHz.

In normal operation, the isolation FET is fully on.

When down mode is triggered and  $V_{IN}$  is less than  $V_O$  pin voltage, the OUT pin has a fixed 2 V (typical) above  $V_O$  pin voltage. An isolation FET works in LDO mode to regulate  $V_O$  pin voltage with a 2-V constant voltage drop.

When down mode is triggered and  $V_{IN}$  is 100 mV (typical) higher than  $V_O$  pin voltage, the OUT pin has an approximated 3 V (typical) above the  $V_{IN}$  pin voltage. As  $V_{IN}$  keeps rising, the OUT pin continues rising with 3 V on top of  $V_{IN}$ . In addition, an isolation FET works in LDO mode to regulate  $V_O$  pin voltage with a voltage differential of the OUT pin and  $V_O$  pin.

Refer to [Figure 8-1](#).



**Figure 8-1. Down Mode**

Take care during short-to-ground condition when operation  $V_{IN}$  is above 6 V. During hiccup on, the device operates in down mode and the isolation FET voltage drop is  $V_{IN} + 3$  V (OUT pin to  $V_O$  pin).

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS61378-Q1 is a 25- $\mu$ A quiescent current boost converter that supports a 2.3-V to 14-V input voltage range. The device also supports load disconnect to minimize the leakage current. The following design procedure can be used to select component values for the TPS61378-Q1.

### 9.2 Typical Application

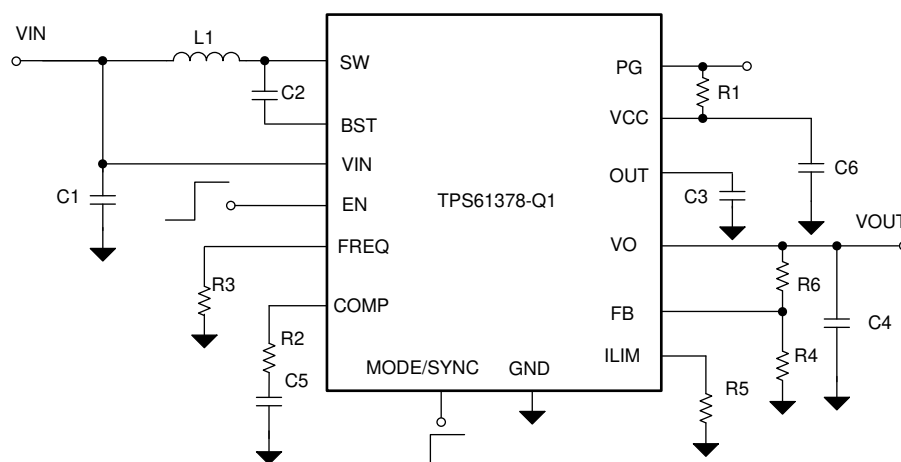


Figure 9-1. Typical Application

#### 9.2.1 Design Requirements

A typical application example is dual cameras powered through a coax cable, which normally requires 9.0-V output as its bias voltage and consumes less than 600 mA current. 800-mA load current is designed to provide margin. The following design procedure can be used to select external component values for the TPS61378-Q1.

Table 9-1. Design Requirements

PARAMETERS	VALUES
Input Voltage	3.3 V to 6.4 V
Output Voltage	9.0 V
Switching Frequency	2.2 MHz
Output Current	800 mA
Output Voltage Ripple	$\pm 25$ mV

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Programming the Output Voltage

There are two ways to set the output voltage of the TPS61378-Q1: adjustable or fixed. If the resistance between FB and GND is higher than 14.4 k $\Omega$  and less than 100k $\Omega$  during start-up, the TPS61378-Q1 works as an adjustable output version. The FB pin is connected to the negative input of the internal error amplifier directly. The output voltage can be programmed by adjusting the external resistor divider  $R_{Upper}$  and  $R_{Lower}$  according to Equation 3. When the output voltage is in well regulation, the typical voltage at the FB pin is  $V_{REF}$  of 0.8 V.



$$V_{OUT} = V_{REF} \times \frac{(R_{Upper} + R_{Lower})}{R_{Lower}} \quad (3)$$

For some applications where the resistor needs to be as low as possible, the low-side divider can be 20 kΩ. The reference voltage is 0.8 V and the high-side divider is 205 kΩ for 9-V output voltage.

For other applications without specific requirements on divider resistance, you can choose  $R_{Lower}$  to be approximately 80.6 kΩ. Slightly increasing or decreasing  $R_{Lower}$  can result in closer output voltage matching when using standard values resistors.

For the best accuracy,  $R_{Lower}$  is recommended to be smaller than 100 kΩ to ensure that the current flowing through  $R_{Lower}$  is at least 100 times larger than FB pin leakage current. Changing  $R_{Lower}$  towards the lower value increases the robustness against noise injection. Changing  $R_{Lower}$  to higher values reduces the quiescent current to achieve higher efficiency at light load.

If the resistance between FB and GND is less than 9.6kΩ during start-up, the TPS61378-Q1 works as a fixed output voltage version. The TPS61378-Q1 uses the internal resistor divider.

For 5-V fixed output voltage,  $R_{Lower}$  is between 0Ω and 2.4kΩ and  $R_{Upper}$  should be removed.

For 5.25-V fixed output voltage,  $R_{Lower}$  is between 3.6kΩ and 4.8 kΩ and  $R_{Upper}$  should be removed.

For 5.5-V fixed output voltage,  $R_{Lower}$  is between 7.2kΩ and 9.6kΩ and  $R_{Upper}$  should be removed.

#### 9.2.2.2 Setting the Switching Frequency

The switching frequency of the TPS61378-Q1 is set at 2.2 MHz. Use [Equation 1](#) to calculate the required resistor value. The calculated value is 18 kΩ to get the frequency of 2.2 MHz.

#### 9.2.2.3 Setting the Current Limit

The current limit of the TPS61378-Q1 can be programmed by an external resistor. For a target current limit of 4.8 A, use [Equation 2](#). The calculated resistor value is 20 kΩ.

#### 9.2.2.4 Selecting the Inductor

A boost converter normally requires two main passive components for storing energy during power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency), transient behavior, and loop stability, which makes the inductor the most critical component in application.

When selecting the inductor and the inductance, the other important parameters are:

- The maximum current rating (RMS and peak current should be considered)
- The series resistance
- Operating temperature

The TPS61378-Q1 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too low and makes the inductor peak-to-peak ripple higher than 2 A, the slope compensation may not be adequate, and the loop can be unstable. Therefore, it is recommended to make the peak-to-peak current ripple between 800 mA to 2 A when selecting the inductor.

The inductance can be calculated by [Equation 4](#), [Equation 5](#), and [Equation 6](#):

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (4)$$

$$\Delta I_{L\_R} = \text{Ripple\%} \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \quad (5)$$

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}} \quad (6)$$

where

- $\Delta I_L$  is the peak-peak inductor current ripple
- $V_{IN}$  is the input voltage
- $D$  is the duty cycle
- $L$  is the inductor
- $f_{SW}$  is the switching frequency
- Ripple % is the ripple ration versus the DC current
- $V_{OUT}$  is the output voltage
- $I_{OUT}$  is the output current
- $\eta$  is the efficiency

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

Inductor values can have  $\pm 20\%$ , or even  $\pm 30\%$ , tolerance with no current bias. When the inductor current approaches the saturation level, the inductance can decrease 20% to 35% from the value at 0-A bias current, depending on how the inductor vendor defines saturation. When selecting an inductor, make sure the rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, switching frequency, and input and output voltages. The peak current can be calculated with [Equation 7](#) and [Equation 8](#).

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L \quad (7)$$

where

- $I_{PEAK}$  is the peak current of the inductor
- $I_{IN}$  is the input average current
- $\Delta I_L$  is the ripple current of the inductor

The input DC current is determined by the output voltage. The output current can be calculated by:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (8)$$

where

- $I_{IN}$  is the input current of the inductor
- $V_{OUT}$  is the output voltage
- $V_{IN}$  is the input voltage
- $\eta$  is the efficiency

While the inductor ripple current depends on the inductance, the frequency, the input voltage, and duty cycle are calculated by [Equation 4](#). Replace [Equation 4](#) and [Equation 8](#) into [Equation 7](#) and get the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \quad (9)$$

where

- $I_{PEAK}$  is the peak current of the inductor
- $I_{OUT}$  is the output current
- $D$  is the duty cycle
- $\eta$  is the efficiency
- $V_{IN}$  is the input voltage
- $L$  is the inductor

- $f_{SW}$  is the switching frequency

The heat rating current (RMS) is can be calculated with [Equation 10](#):

$$I_{L\_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2} \quad (10)$$

where

- $I_{L\_RMS}$  is the RMS current of the inductor
- $I_{IN}$  is the input current of the inductor
- $\Delta I_L$  is the ripple current of the inductor

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature-related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency-dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print. [Table 9-2](#) lists some recommended inductors.

**Table 9-2. Recommended Inductors**

PART NUMBER	L (μH)	DCR TYP (mΩ) MAX	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR <sup>(1)</sup>
XEL4030-471MEB	0.47	4.1	15.5	4 × 4 × 3	Coilcraft
XEL4030-102MEB	1	8.9	9	4 × 4 × 3	Coilcraft
DFE2HCAHR47MJ0L	0.47	25	5.1	2.5 × 2 × 1.2	Murata
DFE322520FD-1R0M	1	22	7.5	3.2 × 2.5 × 2	Murata
TFM322512ALMAR47MTAA	0.47	16	7.6	3.2 × 2.5 × 1.2	TDK
TFM322512ALMA1R0MTAA	1	30	5.1	3.2 × 2.5 × 1.2	TDK

(1) See the [Third-party Products Disclaimer](#).

### 9.2.2.5 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. The loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by [Equation 11](#):

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (11)$$

where

- $C_{OUT}$  is the output capacitor
- $I_{OUT}$  is the output current
- $V_{OUT}$  is the output voltage
- $V_{IN}$  is the input voltage
- $\Delta V$  is the output voltage ripple required
- $f_{SW}$  is the switching frequency

The additional output ripple component caused by ESR is calculated by [Equation 12](#):

$$\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}} \quad (12)$$

where

- $\Delta V_{\text{ESR}}$  is the output voltage ripple caused by ESR
- $R_{\text{ESR}}$  is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using [Equation 13](#):

$$C_{\text{OUT}} = \frac{\Delta I_{\text{STEP}}}{2\pi \times f_{\text{BW}} \times \Delta V_{\text{TRAN}}} \quad (13)$$

where

- $\Delta I_{\text{STEP}}$  is the transient load current step
- $\Delta V_{\text{TRAN}}$  is the allowed voltage dip for the load current step
- $f_{\text{BW}}$  is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero)

For the output capacitor on the OUT pin, the effective capacitance is recommended between 0.22  $\mu\text{F}$  to 1  $\mu\text{F}$ .

Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate by as much as 70% of the capacitance at the respective rated voltage. Therefore, enough margins on the voltage rating must be considered to ensure adequate capacitance at the required output voltage.

#### 9.2.2.6 Selecting the Input Capacitors

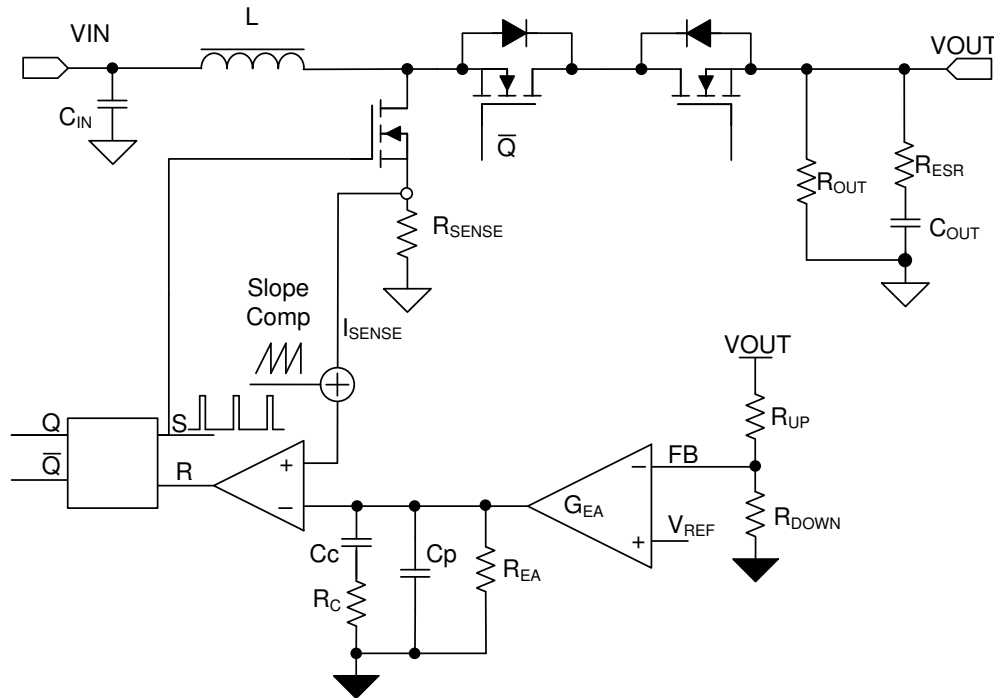
Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter since they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 22- $\mu\text{F}$  input capacitor or equivalent is sufficient for the most applications, larger values can be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the device. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, must be placed between  $C_{\text{IN}}$  and the power source lead to reduce ringing that can occur between the inductance of the power source leads and  $C_{\text{IN}}$ .

#### 9.2.2.7 Loop Stability and Compensation

##### 9.2.2.7.1 Small Signal Model

The TPS61378-Q1 uses the fixed frequency peak current mode control. There is an internal adaptive slope compensation to avoid subharmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by  $L$  and  $C_{\text{OUT}}$ , to a single-pole system, created by  $R_{\text{OUT}}$  and  $C_{\text{OUT}}$ . The single-pole system is easily used with the loop compensation. [Figure 9-2](#) shows the equivalent small signal elements of a boost converter.



**Figure 9-2. TPS61378-Q1 Control Equivalent Circuitry Model**

The small signal of power stage is:

$$K_{PS}(S) = \frac{R_{OUT} \times (1 - D)}{2 \times R_{SENSE}} \times \frac{(1 + \frac{S}{2\pi \times f_{ESR}})(1 - \frac{S}{2\pi \times f_{RHP}})}{(1 + \frac{S}{2\pi \times f_p})} \quad (14)$$

where

- D is the duty cycle
- $R_{OUT}$  is the output load resistor
- $R_{SENSE}$  is the equivalent internal current sense resistor, which is typically 118 mΩ

The single pole of the power stage is:

$$f_p = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \quad (15)$$

where

- $C_{OUT}$  is the output capacitance. For a boost converter having multiple identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (16)$$

where

- $R_{ESR}$  is the equivalent resistance in series of the output capacitor

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1 - D)^2}{2\pi \times L} \quad (17)$$

where

- D is the duty cycle
- $R_{OUT}$  is the output load resistor
- L is the inductance

Equation 18 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}(S) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \times \frac{1 + \frac{S}{2\pi \times f_Z}}{\left(1 + \frac{S}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{S}{2\pi \times f_{P2}}\right)} \quad (18)$$

where

- $R_{EA}$  is the output impedance of the error amplifier, typically  $R_{EA} = 500 \text{ M}\Omega$
- $f_{P1}$ ,  $f_{P2}$  is the pole's frequency of the compensation
- $f_Z$  is the zero's frequency of the compensation network

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_C} \quad (19)$$

where

- $C_C$  is the zero capacitor compensation

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (20)$$

where

- $C_P$  is the pole capacitor compensation
- $R_C$  is the resistor of the compensation network

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (21)$$

#### 9.2.2.7.2 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

##### 1. Set the Crossover Frequency, $f_C$ .

The first step is to set the loop crossover frequency,  $f_C$ . The higher the crossover frequency, the faster the loop response is. It is generally accepted that the loop gain crosses over no higher than the lower of either 1/10 of the switching frequency,  $f_{SW}$ , or 1/5 of the RHPZ frequency,  $f_{RHPZ}$ . Then, calculate the loop compensation network values of  $R_C$ ,  $C_C$ , and  $C_P$  by the following equations.

##### 2. Set the Compensation Resistor, $R_C$ .

By placing  $f_Z$  below  $f_C$ , for frequencies above  $f_C$ ,  $R_C \parallel R_{EA} \approx R_C$ , so  $R_C \times G_{EA}$  sets the compensation gain. Setting the compensation gain,  $K_{COMP-dB}$ , at  $f_Z$  results in the total loop gain,  $T(s) = K_{PS(s)} \times H_{EA(s)}$ , being zero at  $f_C$ .

Therefore, to approximate a single-pole rolloff up to  $f_{P2}$ , rearrange Equation 18 to solve for RC so that the compensation gain,  $K_{EA}$ , at  $f_C$  is the negative of the gain,  $K_{PS}$ . Read at frequency  $f_C$  for the power stage bode plot or more simply:

$$K_{EA}(f_C) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}) = -K_{PS}(f_C) \quad (22)$$

where

- $K_{EA}$  is gain of the error amplifier network
- $K_{PS}$  is the gain of the power stage
- $G_{EA}$  is the transconductance of the amplifier, the typical value of  $G_{EA} = 70 \mu A / V$

### 3. Set the Compensation Zero capacitor, $C_C$ .

Place the compensation zero at the power stage  $R_{OUT}$ ,  $C_{OUT}$  pole's position to get:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (23)$$

Set  $f_Z = f_P$ , and get:

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C} \quad (24)$$

### 4. Set the Compensation Pole Capacitor, $C_P$ .

Place the compensation pole at the zero produced by  $R_{ESR}$  and  $C_{OUT}$ . It is useful for canceling unhelpful effects of the ESR zero.

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (25)$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (26)$$

Set  $f_{P2} = f_{ESR}$ , and get:

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \quad (27)$$

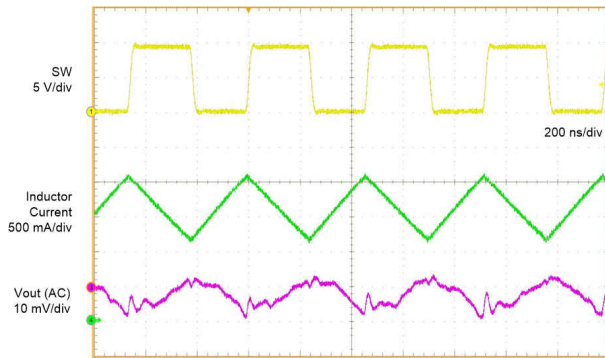
#### 9.2.2.7.3 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during the turnon of each cycle. The gate current also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1  $\mu F$  to 1  $\mu F$ .  $C_{BST}$  must be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1  $\mu F$  was selected for this design example.

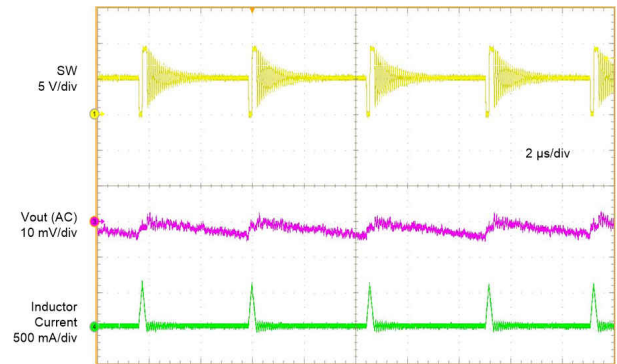
#### 9.2.2.7.4 $V_{CC}$ Capacitor

The primary purpose of the  $V_{CC}$  capacitor is to supply the peak transient currents of the driver and bootstrap capacitor and provide stability for the  $V_{CC}$  regulator. The value of  $C_{VCC}$  must be at least 10 times greater than the value of  $C_{BST}$ , and must be a good quality, low-ESR ceramic capacitor.  $C_{VCC}$  must be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 2.2  $\mu F$  was selected for this design example.

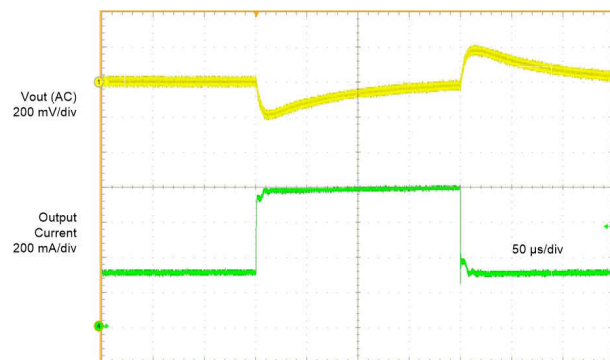
### 9.2.3 Application Curves



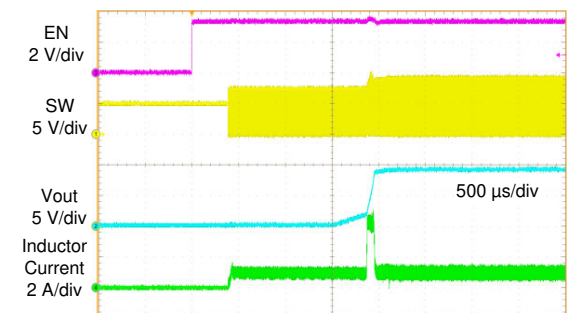
**Figure 9-3. Switching Waveform  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 9\text{ V}$ ,  $I_{OUT} = 800\text{ mA}$ , FPWM**



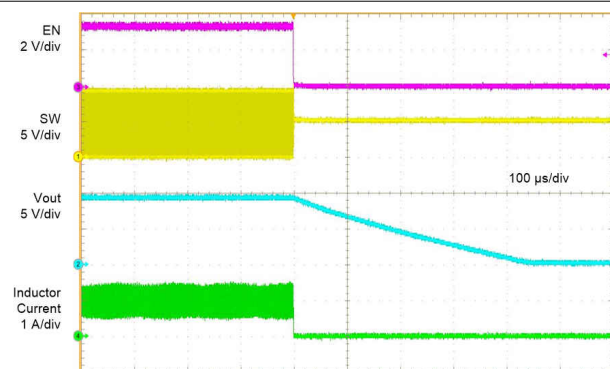
**Figure 9-4. Switching Waveform  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 9\text{ V}$ ,  $I_{OUT} = 0\text{ mA}$ , Auto PFM**



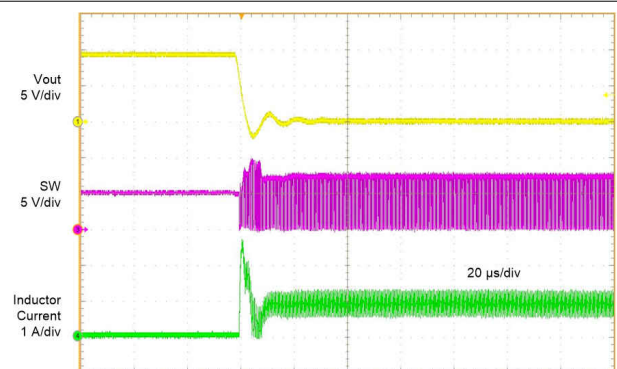
**Figure 9-5. Load Transient  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 9\text{ V}$ ,  $I_{OUT} = 300\text{ mA}$  to  $800\text{ mA}$ , FPWM**



**Figure 9-6. Start-up from EN Waveform  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 9\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ , FPWM**

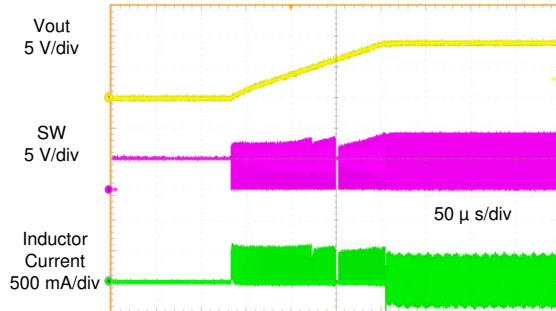


**Figure 9-7. Shutdown from EN Waveforms  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 9\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ , FPWM**

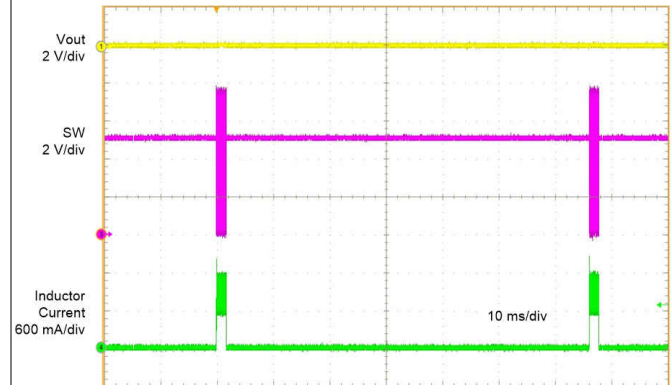


**Figure 9-8. Short Circuit Protection  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 9\text{ V}$ , FPWM**





**Figure 9-9. Short Circuit Recovery**  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 9\text{ V}$ ,  $I_{OUT} = 0\text{ mA}$ , FPWM



**Figure 9-10. Hiccup Short Circuit Protection**  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 9\text{ V}$ , FPWM

## 10 Power Supply Recommendations

The TPS61378-Q1 is designed to operate from an input voltage supply range between 2.3 V to 14 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47  $\mu\text{F}$  is a typical choice.

## 11 Layout

### 11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor must be placed as close as possible to the IC.

### 11.2 Layout Example

The bottom layer is a large GND plane connected by vias.

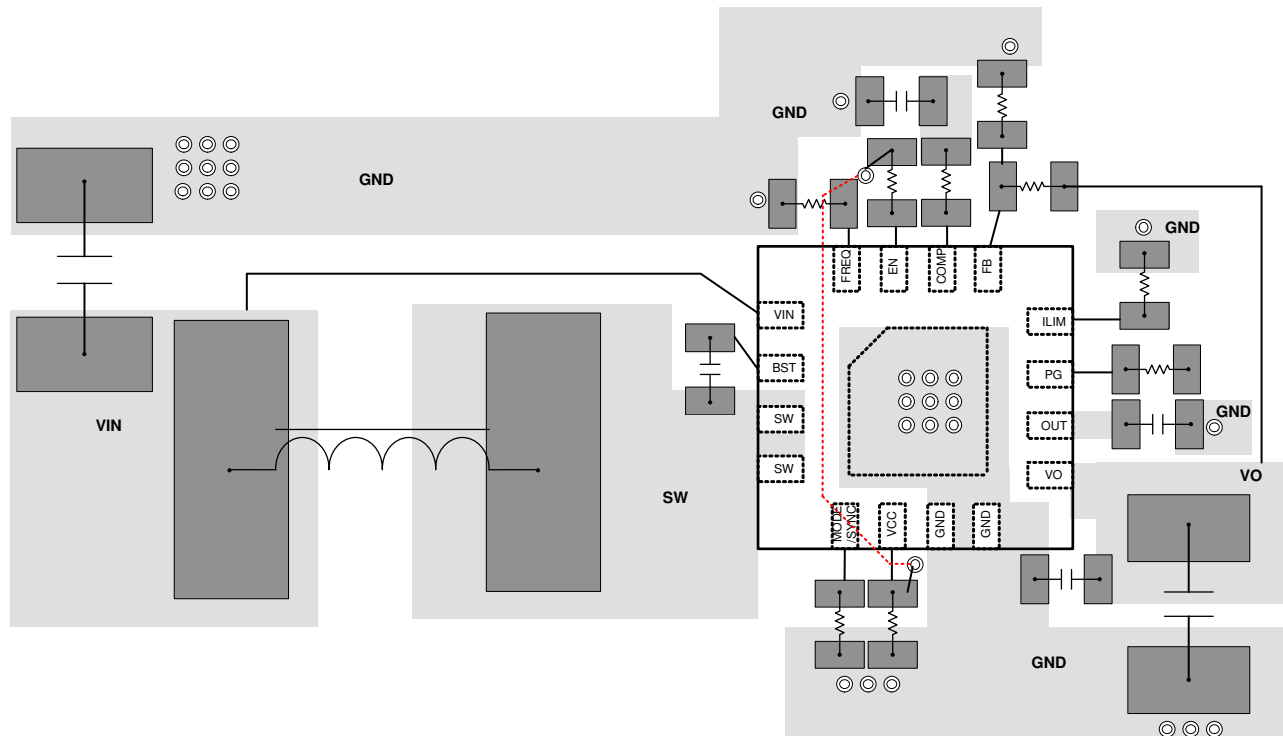


Figure 11-1. Recommended Layout

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

#### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS613783QWRTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2G8H	<a href="#">Samples</a>
TPS613785QWRTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2G9H	<a href="#">Samples</a>
TPS61378QWRTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2ELH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS613783QWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS613785QWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61378QWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS

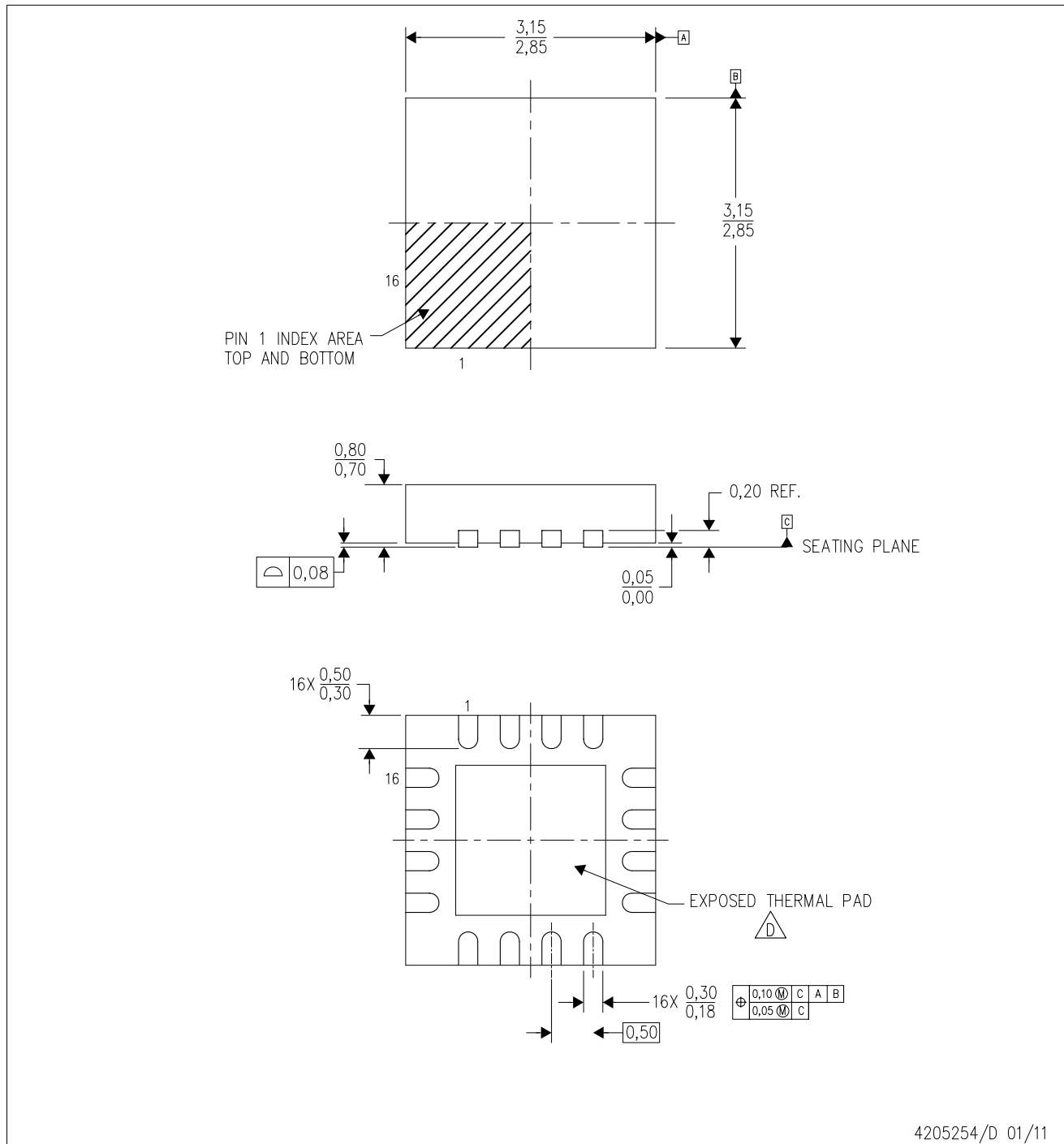


\*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS613783QWRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS613785QWRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS61378QWRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

RTE (S-PWQFN-N16)

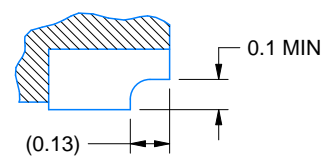
PLASTIC QUAD FLATPACK NO-LEAD



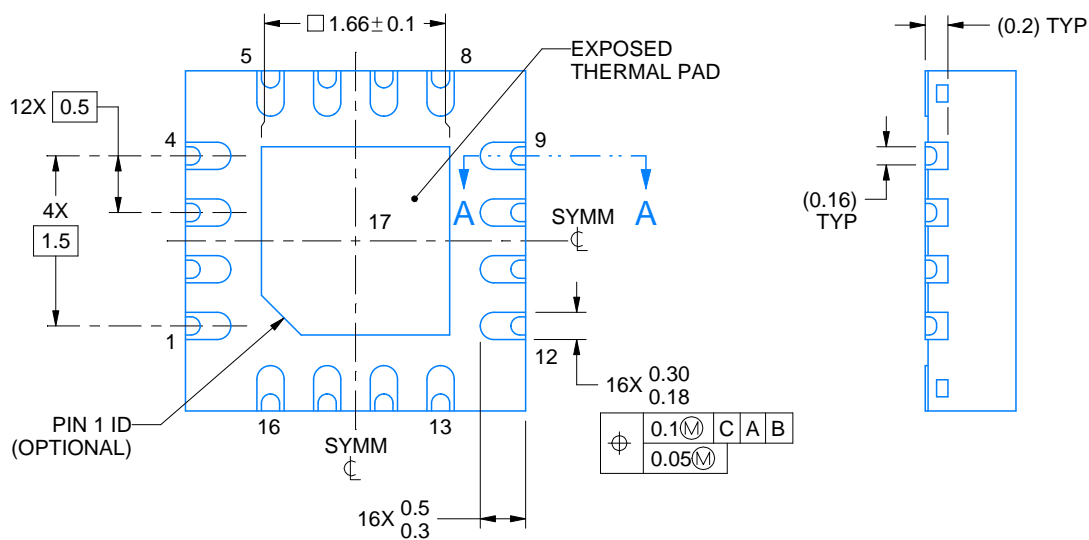
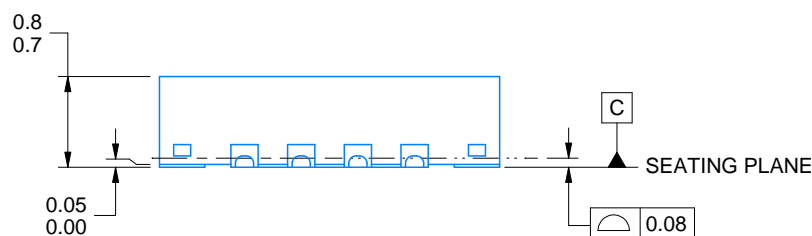
4205254/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.





SECTION A-A  
TYPICAL

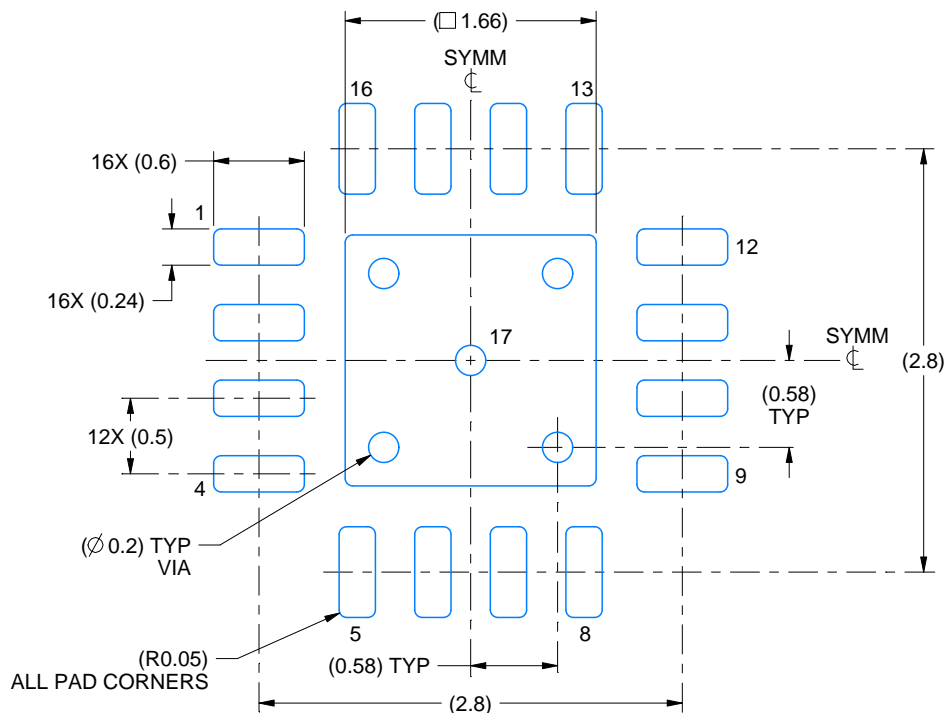


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

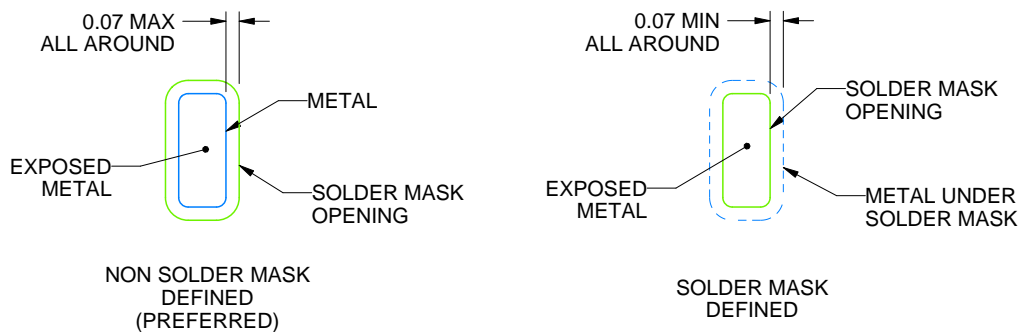
# RTE0016K

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



## SOLDER MASK DETAILS

4224938/B 06/2019

NOTES: (continued)

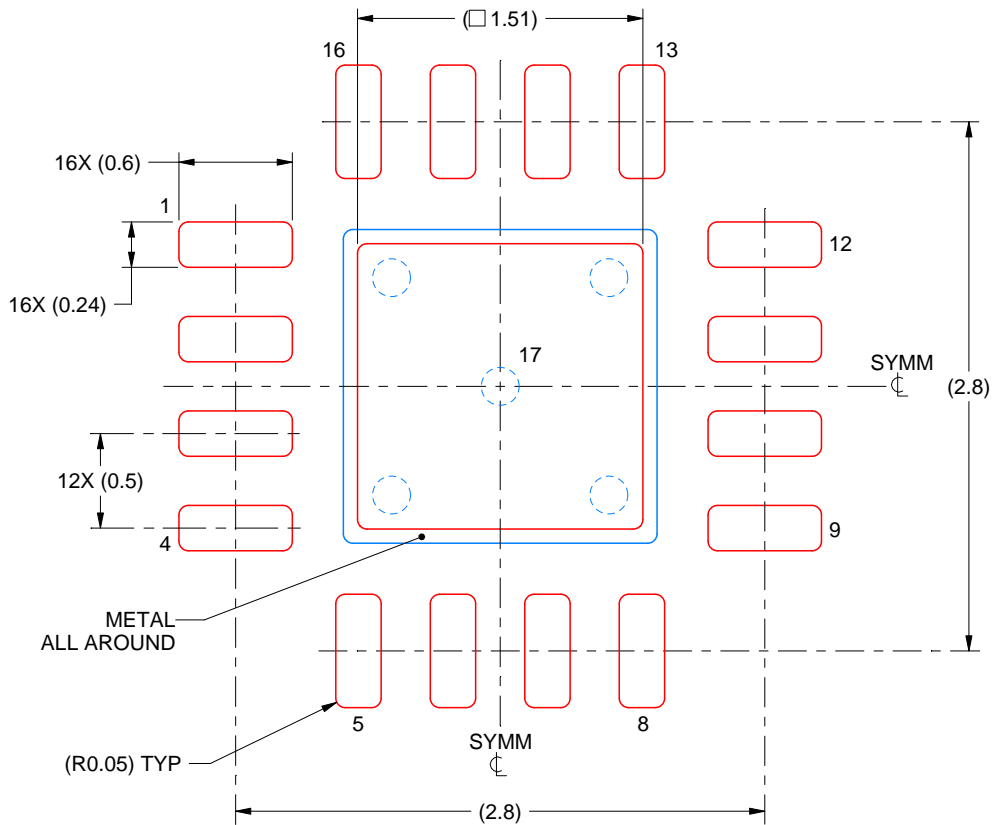
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4224938/B 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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