TPS6206x 3-MHz, 1.6-A, Step Down Converter in 2-mm × 2-mm WSON Package

1 Features

- 3-MHz Switching Frequency
- V_{IN} Range from 2.7 V to 6 V
- 1.6-A Output Current
- Up to 97% Efficiency
- Power Save Mode and 3-MHz Fixed PWM Mode
- Output Voltage Accuracy in PWM Mode ±1.5%
- Output Discharge Function
- Typical 18-µA Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Voltage Positioning
- Clock Dithering
- Supports Maximum 1-mm Height Solutions
- Available in a 2 mm × 2 mm × 0.75 mm WSON

2 Applications

- Point of Load (POL)
- Notebooks, Pocket PCs
- Portable Media Players
- DSP Supplies

3 Description

The TPS6206x is a family of highly efficient synchronous step-down DC-DC converters. They provide up to 1.6-A output current.

With an input voltage range of 2.7 V to 6 V, the device is a perfect fit for power conversion from a single Li-Ion battery as well from 5-V or 3.3-V system supply rails. The TPS6206x operates at 3-MHz fixed frequency and enters power save mode operation at light load currents to maintain high efficiency over the entire load current range. The power save mode is optimized for low output voltage ripple. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high.

In the shutdown mode, the current consumption is reduced to less than 1 µA and an internal circuit discharges the output capacitor.

TPS6206x family is optimized for operation with a tiny 1-µH inductor and a small 10-µF output capacitor to achieve smallest solution size and high regulation performance.

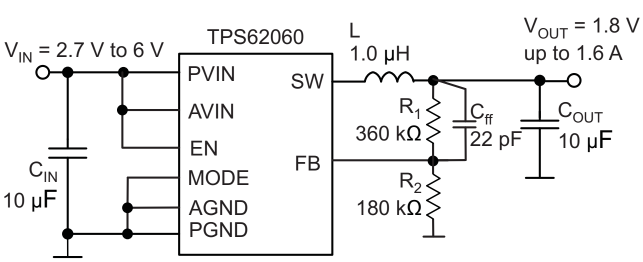
The TPS6206x operates over a free air temperature of –40°C to 85°C. The device is available in a small 2-mm × 2-mm × 0.75-mm 8-pin WSON PowerPAD™ integrated circuit package.

Device Information(1)

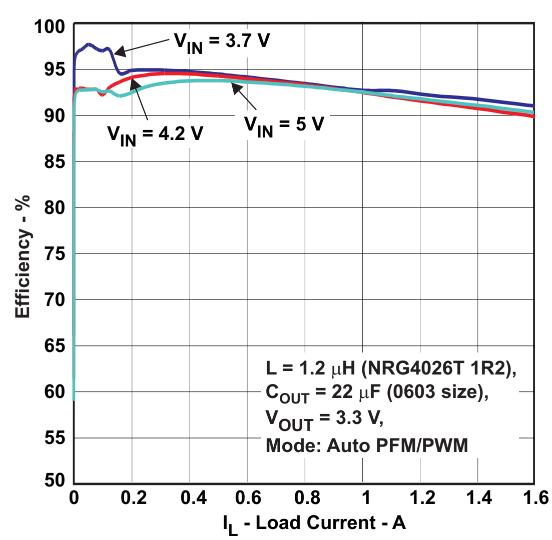
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62060 TPS62061 TPS62063	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2011) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

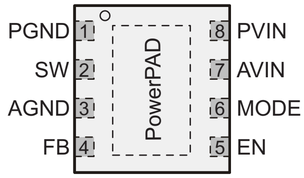
5 Device Comparison Table(1)

PART NUMBER	OUTPUT VOLTAGE(1)	FUNCTION		MAXIMUM OUTPUT CURRENT	PACKAGE DESIGNATOR	PACKAGE MARKING
		MODE	Power Good (PG)			
TPS62060	Adjustable	Selectable	No	1.6 A	DSG	CGY
TPS62061	1.8 V fix	Selectable	No	1.6 A		CGX
TPS62063	3.3 V fix	Selectable	No	1.6 A		QXD
TPS6206x(1)	Adjustable	no	yes	1.6 A		—

(1) For the most current package and ordering information, see the *Mechanical, Packaging, and Orderable Information* section at the end of this document, or see the TI website at www.ti.com.
(1) Contact TI for fixed output voltage options / Power Good output options

6 Pin Configuration and Functions

DSG Package
8-Pin WSON With PowerPAD
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	3	I	Analog GND supply pin for the control circuit.
AVIN	7	I	Analog V_{IN} power supply for the control circuit. Must be connected to PVIN and input capacitor.
EN	5	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated
FB	4	I	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
MODE	6	I	When MODE pin = High forces the device to operate in fixed frequency PWM mode. When MODE pin = Low enables the power save mode with automatic transition from PFM mode to fixed frequency PWM mode.
PGND	1	PWR	GND supply pin for the output stage.
PVIN	8	PWR	V_{IN} power supply pin for the output stage.
SW	2	O	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
PowerPAD		—	For good thermal performance, this PAD must be soldered to the land pattern on the PCB. This PAD should be used as device GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage[2]	AVIN, PVIN	–0.3	7	V
	EN, MODE, FB	–0.3	V_{IN} +0.3 < 7	
	SW	–0.3	7	
Current (source)	Peak output	Internally limited		A
Temperature	Junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AV_{IN} , PV_{IN}	Supply voltage	2.7		6	V
	Output current capability			1600	mA
	Output voltage for adjustable voltage	0.8		V_{IN}	V
L	Effective inductance	0.7	1	1.6	µH
C_{OUT}	Effective output capacitance	4.5	10	22	µF
T_A	Operating ambient temperature[1]	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application (PD(max)), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

7.4 Thermal Information

THERMAL METRIC[1]		TPS62060, TPS62061, TPS62063	UNIT
		DSG (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.68	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.63	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.65	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.02	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.61	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 10 µF 0603, C_{OUT} = 10 µF 0603, L = 1 µH, see the parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.7		6	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA, device operating in PFM mode and device not switching		18	25	µA
I_{SD}	Shutdown current	EN = GND, current into AVIN and PVIN		0.1	1	µA
V_{UVLO}	Undervoltage lockout threshold	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	
ENABLE, MODE						
V_{IH}	High level input voltage	2.7 V ≤ V_{IN} ≤ 6 V	1		6	V
V_{IL}	Low level input voltage	2.7 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current	Pin tied to GND or VIN		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		120	180	mΩ
		V_{IN} = 5 V(1)		95	150	
	Low-side MOSFET on-resistance	V_{IN} = 3.6 V(1)		90	130	mΩ
		V_{IN} = 5 V(1)		75	100	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	2.7V ≤ V_{IN} ≤ 6 V	1800	2250	2700	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		10		°C
OSCILLATOR						
f_{SW}	Oscillator frequency	2.7 V ≤ V_{IN} ≤ 6 V	2.6	3	3.4	MHz
OUTPUT						
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage PWM mode	PWM operation, MODE = V_{IN} , 2.7 V ≤ V_{IN} ≤ 6 V, 0 mA load	–1.5%	0%	1.5%	
$V_{FB(PFM)}$	Feedback voltage PFM mode, voltage positioning	device in PFM mode, voltage positioning active(2)		1%		
V_{FB}	Load regulation			–0.5		%/A
	Line regulation			0		%/V
$R_{(Discharge)}$	Internal discharge resistor	Activated with EN = GND, 2 V ≤ V_{IN}≤ 6 V, 0.8 ≤ V_{OUT} ≤ 3.6 V	75	200	1450	Ω
t_{START}	Start-up time	Time from active EN to reach 95% of V_{OUT}		500		µs

(1) Maximum value applies for T_J = 85°C
(2) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the parameter measurement information.

7.6 Dissipation Ratings[(1)][(2)]

PACKAGE	$R_{\theta JA}$	POWER RATING T_A = ≤ 25°C	DERATING FACTOR ABOVE T_A = 25°C
DSG	75°C/W	1300 mW	13 mW/°C

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is PD = ($T_{J(max)}$ – T_A)/ θ_{JA}.
(2) This thermal data measured with high-K board (4 layers according to JESD51-7 JEDEC Standard).

7.7 Typical Characteristics

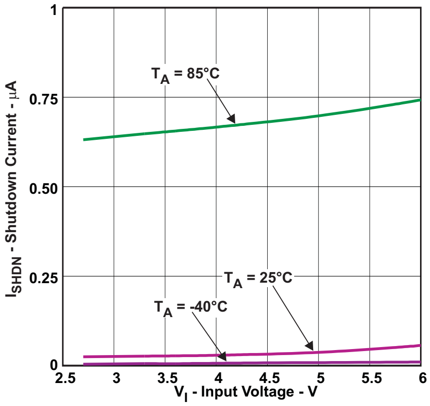


Figure 1. Shutdown Current vs Input Voltage and Ambient Temperature

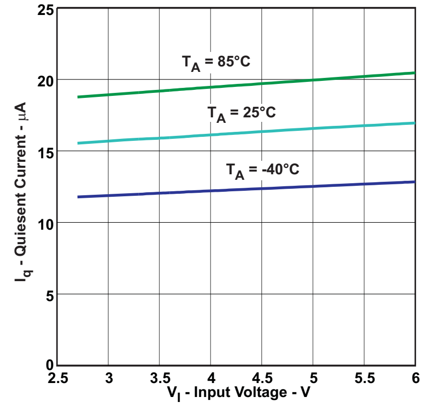


Figure 2. Quiescent Current vs Input Voltage

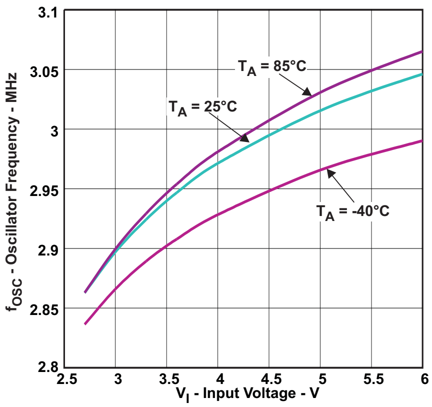


Figure 3. Oscillator Frequency vs Input Voltage

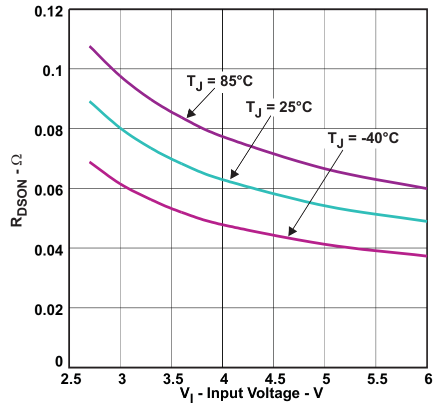


Figure 4. R_{DSON} Low-Side Switch

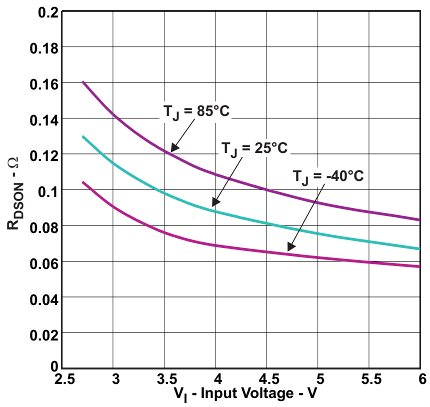


Figure 5. R_{DSON} High-Side Switch

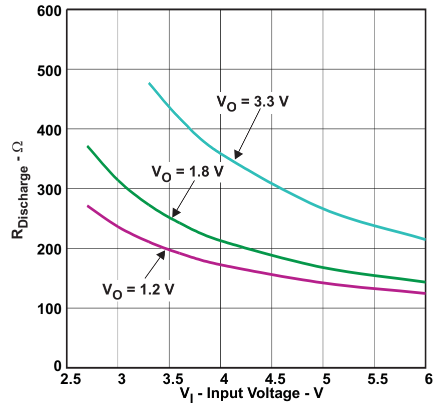


Figure 6. $R_{DISCHARGE}$ vs Input Voltage

8 Detailed Description

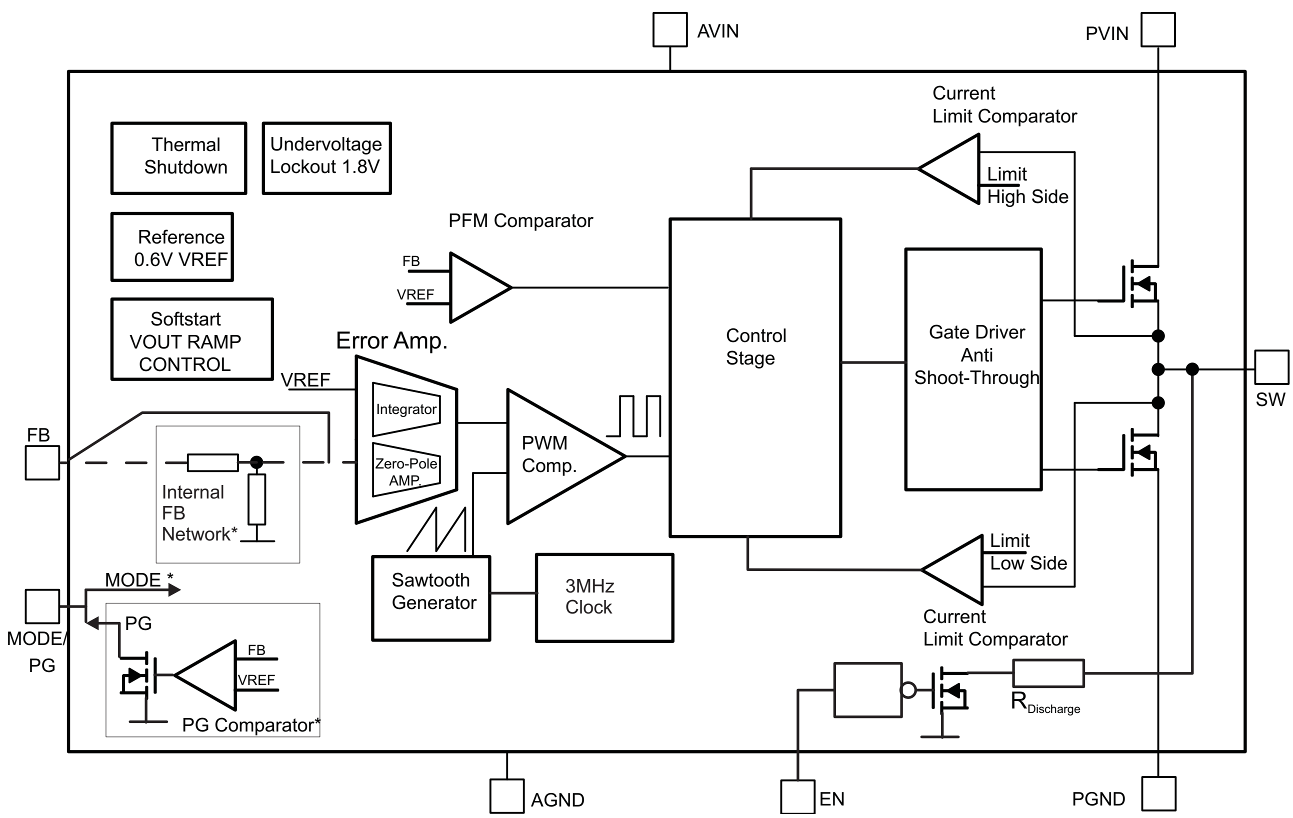
8.1 Overview

The TPS62060 step down converter operates with typically 3-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter can automatically enter power save mode and operates then in pulse frequency modulation (PFM) mode.

During PWM operation the converter use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows now from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle will be initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

8.2 Functional Block Diagram



* Function depends on device option

8.3 Feature Description

8.3.1 Mode Selection

The MODE pin allows mode selection between forced PWM mode and power save mode.

Connecting this pin to GND enables the power save mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

8.3.2 Enable

The device is enabled by setting EN pin to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltages reaches 95% of its nominal value within t_{START} of typically 500 µs after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled and the SW pin is connected to PGND through an internal resistor to discharge the output.

8.3.3 Clock Dithering

To reduce the noise level of switch frequency harmonics in the higher RF bands, the TPS6206x family has a built-in clock-dithering circuit. The oscillator frequency is slightly modulated with a sub clock causing a clock dither of typically 6 ns.

8.3.4 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling V_{IN} trips the undervoltage lockout threshold V_{UVLO}. The undervoltage lockout threshold V_{UVLO} for falling V_{IN} is typically 1.78 V. The device starts operation once the rising V_{IN} trips undervoltage lockout threshold V_{UVLO} again at typically 1.95 V.

8.3.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

8.4 Device Functional Modes

8.4.1 Soft Start

The TPS6206x has an internal soft start circuit that controls the ramp up of the output voltage. Once the converter is enabled and the input voltage is above the undervoltage lockout threshold V_{UVLO} the output voltage ramps up from 5% to 95% of its nominal value within t_{Ramp} of typically 250 µs.

This limits the inrush current in the converter during start-up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current limit is reduced to 1/3 of its nominal value I_{LIMF} until the output voltage reaches 1/3 of its nominal value. Once the output voltage trips this threshold, the device operates with its nominal current limit I_{LIMF}.

Device Functional Modes (continued)

8.4.2 Power Save Mode

In TPS6206x pulling the MODE pin low enables power save mode. If the load current decreases, the converter enters power save mode operation automatically. During power save mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power save mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of $V_{OUTnominal}$ +1%, the device starts a PFM current pulse. For this the high-side MOSFET switch will turn on and the inductor current ramps up. After the on-time expires the switch will be turned off and the low-side MOSFET switch will be turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typically 18 µA current consumption.

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses will be generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold due to the load current.

The PFM mode is exited and PWM mode entered in case the output current can no longer be supported in PFM mode.

8.4.3 Dynamic Voltage Positioning

This feature reduces the voltage undershoots and overshoots at load steps from light to heavy load and vice versa. It is active in power save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

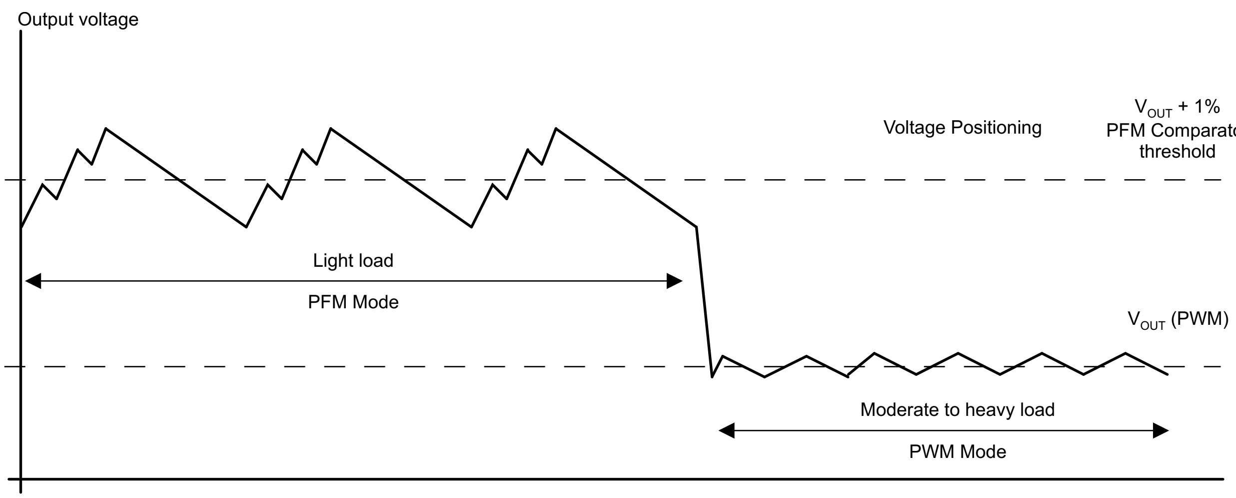


Figure 7. Power Save Mode Operation with Automatic Mode Transition

8.4.4 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode as the input voltage comes close to the nominal output voltage. To maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high-side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

Device Functional Modes (continued)

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{O}max + I_{O}max \times (R_{DS(on)}max + R_{L})$$

where

- I_{O}max = maximum output current
- $R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$
- R_{L} = DC resistance of the inductor
- V_{O}max = nominal output voltage plus maximum output voltage tolerance (1)

8.4.5 Internal Current Limit and Fold-Back Current Limit for Short Circuit Protection

During normal operation the high-side and low-side MOSFET switches are protected by its current limits I_{LIMF}. Once the high-side MOSFET switch reaches its current limit, it is turned off and the low-side MOSFET switch is turned on. The high-side MOSFET switch can only turn on again, once the current in the low-side MOSFET switch decreases below its current limit I_{LIMF}. The device is capable to provide peak inductor currents up to its internal current limit $_{ILIMF.}$.

As soon as the switch current limits are hit and the output voltage falls below 1/3 of the nominal output voltage due to overload or short circuit condition, the foldback current limit is enabled. In this case the switch current limit is reduced to 1/3 of the nominal value I_{LIMF}.

Due to the short circuit protection is enabled during start-up, the device does not deliver more than 1/3 of its nominal current limit I_{LIMF} until the output voltage exceeds 1/3 of the nominal output voltage. This needs to be considered when a load is connected to the output of the converter, which acts as a current sink.

8.4.6 Output Capacitor Discharge

With EN = GND, the devices enter shutdown mode and all internal circuits are disabled. The SW pin is connected to PGND through an internal resistor to discharge the output capacitor.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS62060, TPS62061 and TPS62063 are highly efficient synchronous step down DC-DC converters providing up to 1.6-A output current.

9.2 Typical Application

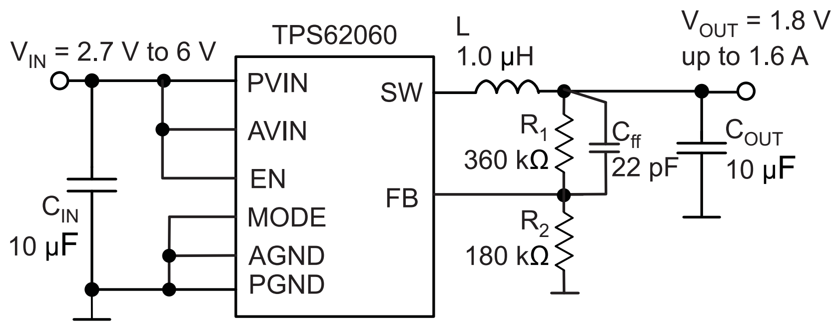


Figure 8. TPS62060 1.8-V Adjustable Output Voltage Configuration

9.2.1 Design Requirements

The device operates over an input voltage range from 2.7 V to 6 V. The output voltage is adjustable using an external feedback divider.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \tag{2}$$

with an internal reference voltage V_{REF} typically 0.6 V.

To minimize the current through the feedback divider network, R_2 should be within the range of 120 kΩ to 360 kΩ. The sum of R_1 and R_2 should not exceed ~1 MΩ, to keep the network robust against noise. An external feed-forward capacitor C_{ff} is required for optimum regulation performance. Lower resistor values can be used. R1 and C_{ff} places a zero in the loop. The right value for C_{ff} can be calculated as:

$$f_z = \frac{1}{2 \times \pi \times R_1 \times C_{ff}} = 25\,\text{kHz} \tag{3}$$

Therefore, the feed forward capacitor can be calculated to:

$$C_{ff} = \frac{1}{2 \times \pi \times R_1 \times 25\,\text{kHz}} \tag{4}$$

Typical Application (continued)

9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The internal compensation network of TPS6206x is optimized for a LC output filter with a corner frequency of:

$$f_c = \frac{1}{2 \times \pi \times \sqrt{(1\mu H \times 10\mu F)}} = 50kHz \quad (5)$$

The device operates with nominal inductors of 1 µH to 1.2 µH and with 10 µF to 22 µF small X5R and X7R ceramic capacitors. Refer to the lists of inductors and capacitors. The device is optimized for a 1 µH inductor and 10 µF output capacitor.

9.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

Equation 6 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 7. This is recommended because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (6)$$

$$I_{L\,max} = I_{out\,max} + \frac{\Delta I_L}{2} \quad (7)$$

where

- f = Switching frequency (3 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current
- I_{outmax} = Maximum output current

A more conservative approach is to select the inductor current rating just for the switch current of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC-DC conversion and consist of both the losses in the DC resistance $R_{(DC)}$ and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 1. List of Inductors

DIMENSIONS [mm^3]	INDUCTANCE µH	INDUCTOR TYPE	SUPPLIER
3.2 × 2.5 × 1.2 max	1	MIPSAZ3225D	FDK
3.2 × 2.5 × 1 max	1	LQM32PN (MLCC)	Murata
3.7 × 4 × 1.8 max	1	LQH44 (wire wound)	Murata
4 × 4 × 2.6 max	1.2	NRG4026T (wire wound)	Taiyo Yuden
3.5 × 3.7 × 1.8 max	1.2	DE3518 (wire wound)	TOKO

9.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6206x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and may not be used. For most applications a nominal 10 µF or 22 µF capacitor is suitable. At small ceramic capacitors, the DC-bias effect decreases the effective capacitance. Therefore a 22 µF capacitor can be used for output voltages higher than 2 V, see list of capacitors.

In case additional ceramic capacitors in the supplied system are connected to the output of the DC-DC converter, the output capacitor C_{OUT} must be decreased in order not to exceed the recommended effective capacitance range. In this case a loop stability analysis must be performed as described later.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{8}$$

9.2.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 10 µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2. List of Capacitors

CAPACITANCE	TYPE	SIZE [mm^3]	SUPPLIER
10 µF	GRM188R60J106M	0603: 1.6 x 0.8 x 0.8	Murata
22 µF	GRM188R60G226M	0603: 1.6 x 0.8 x 0.8	Murata
22 µF	CL10A226MQ8NRNC	0603: 1.6 x 0.8 x 0.8	Samsung
10 µF	CL10A106MQ8NRNC	0603: 1.6 x 0.8 x 0.8	Samsung

9.2.2.3 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or wrong L-C output filter combinations. As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turnon of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta_{I(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta_{I(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode at medium to high load currents.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing; that helps evaluate stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

9.2.3 Application Curves

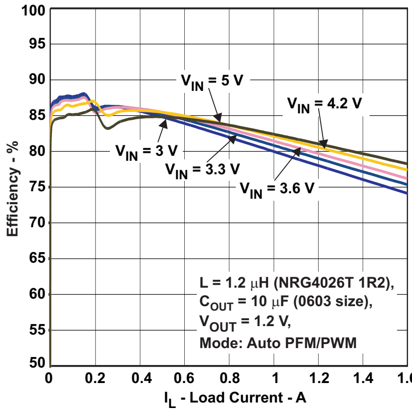


Figure 9. Efficiency vs Load Current V_{OUT} = 1.2 V, Auto PFM/PWM Mode, Linear Scale

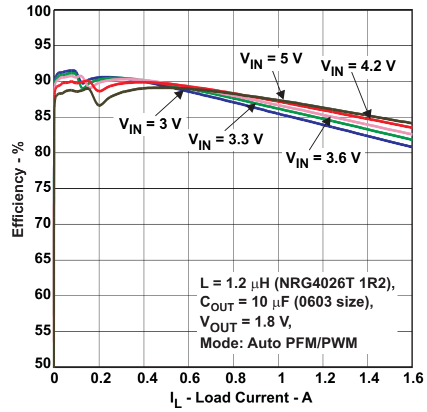


Figure 10. Efficiency vs Load Current V_{OUT} = 1.8 V, Auto PFM/PWM Mode, Linear Scale

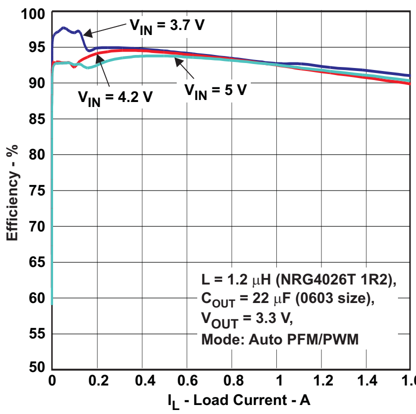


Figure 11. Efficiency vs Load Current V_{OUT} = 3.3 V, Auto PFM/PWM Mode, Linear Scale

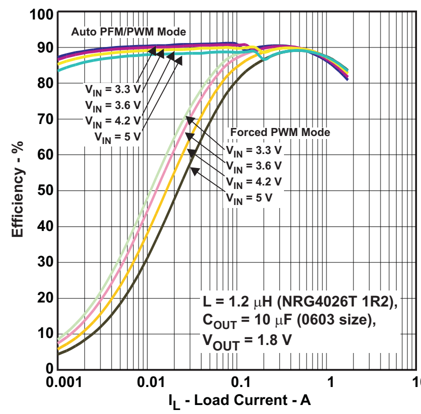


Figure 12. Efficiency vs Load Current Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale

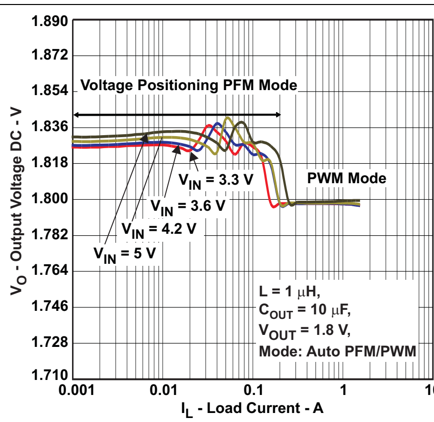


Figure 13. Output Voltage Accuracy vs Load Current Auto PFM/PWM Mode

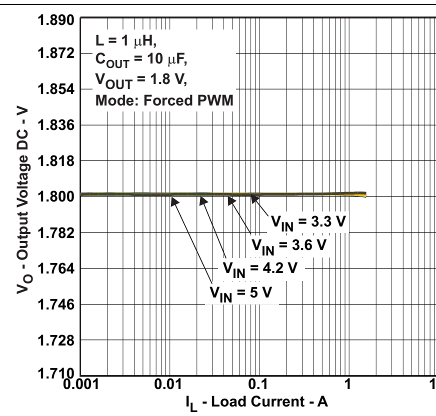


Figure 14. Output Voltage Accuracy vs Load Current Forced PWM Mode

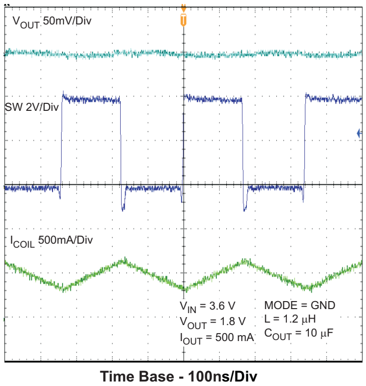


Figure 15. Typical Operation (PWM Mode)

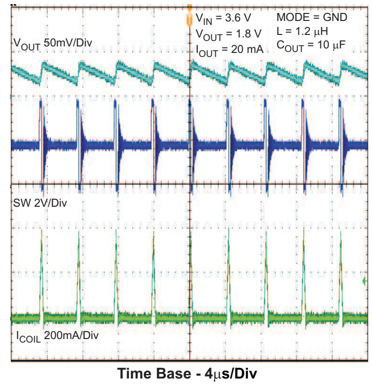


Figure 16. Typical Operation (PFM Mode)

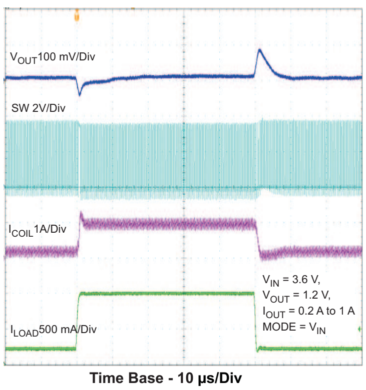


Figure 17. Load Transient Response PWM Mode 0.2 A to 1 A

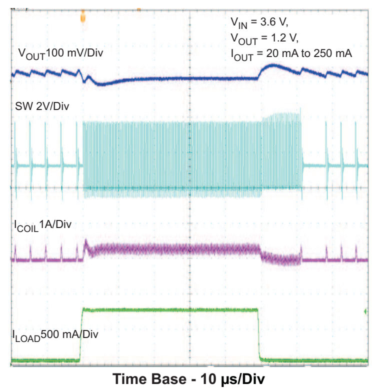


Figure 18. Load Transient PFM Mode 20 mA to 250 mA

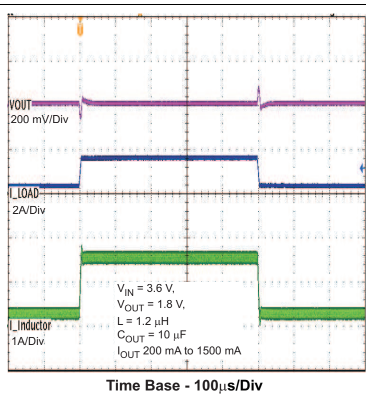


Figure 19. Load Transient Response 200 mA to 1500 mA

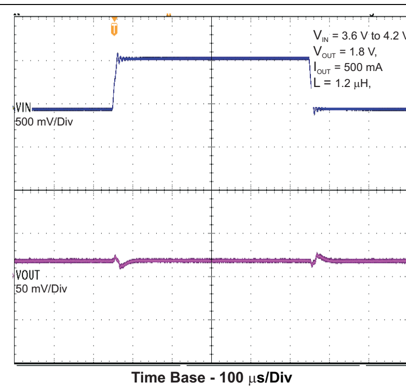


Figure 20. Line Transient Response PWM Mode

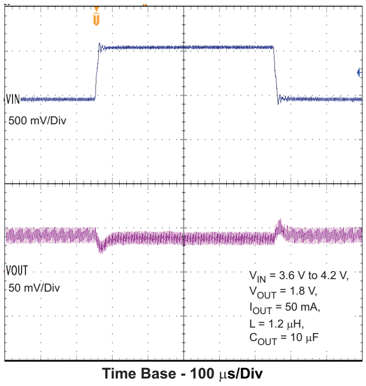


Figure 21. Line Transient PFM Mode

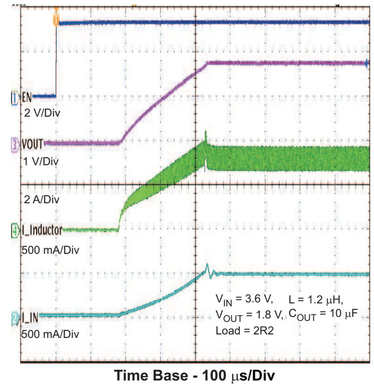


Figure 22. Start-Up into Load – V_{OUT} 1.8 V

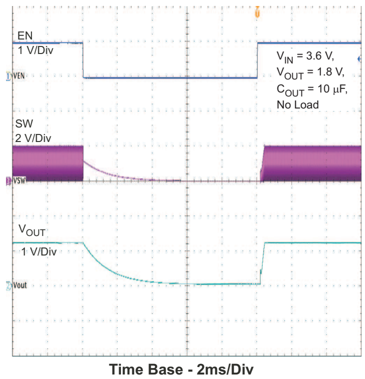


Figure 23. Output Discharge

10 Power Supply Recommendations

The power supply to the TPS6206x must have a current rating according to the supply voltage, output voltage, and output current of the TPS6206x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI and thermal problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the AGND and PGND pins of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common power PGND node and a different node for the signal AGND to minimize the effects of ground noise. The FB divider network should be connected right to the output capacitor and the FB line must be routed away from noisy components and traces (for example, SW line).

Due to the small package of this converter and the overall small solution size the thermal performance of the PCB layout is important. To get a good thermal performance a four or more Layer PCB design is recommended. The PowerPAD™ of the IC must be soldered on the power pad area on the PCB to get a proper thermal connection. For good thermal performance the PowerPAD™ on the PCB needs to be connected to an inner GND plane with sufficient via connections. Refer to the documentation of the evaluation kit.

11.2 Layout Example

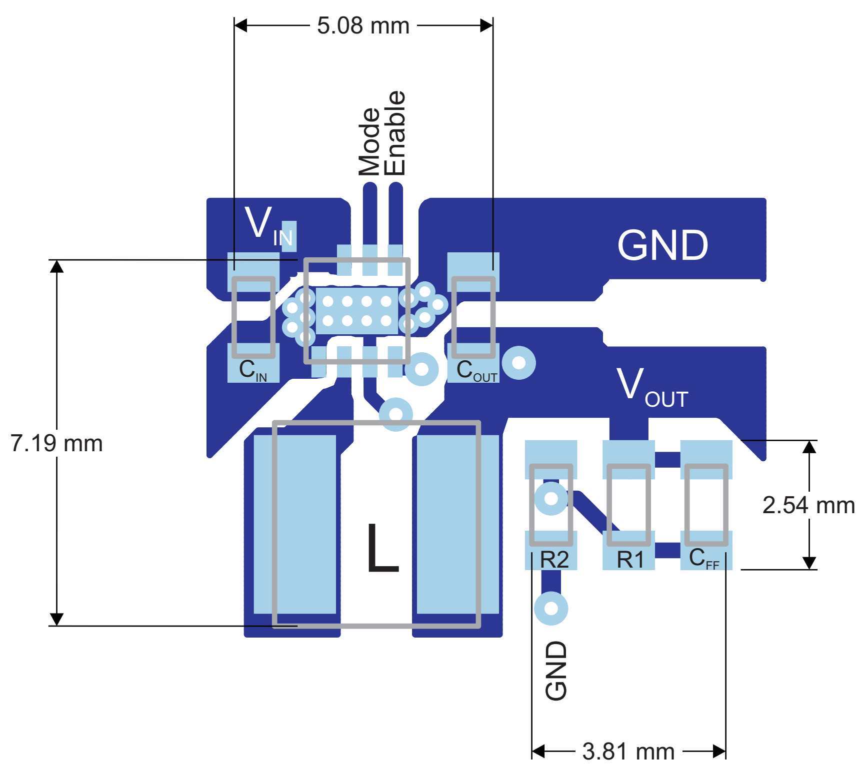


Figure 24. PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62060	Click here	Click here	Click here	Click here	Click here
TPS62061	Click here	Click here	Click here	Click here	Click here
TPS62063	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62060DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CGY	Samples
TPS62060DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CGY	Samples
TPS62061DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CGX	Samples
TPS62061DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CGX	Samples
TPS62063DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QXD	Samples
TPS62063DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QXD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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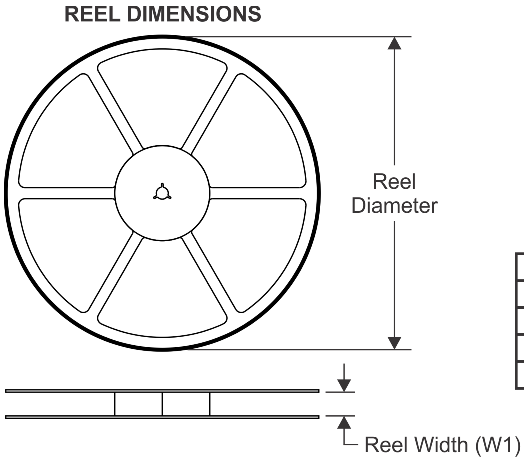
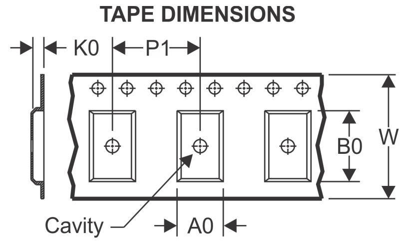
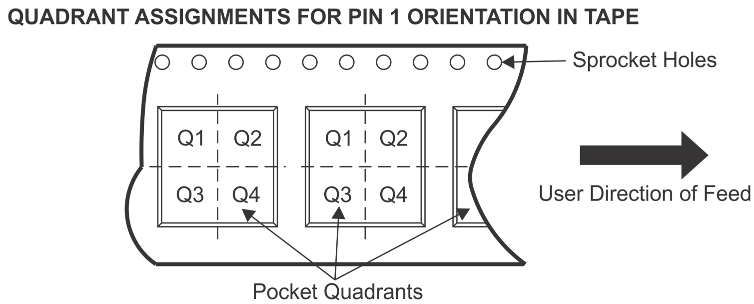
TAPE AND REEL INFORMATION





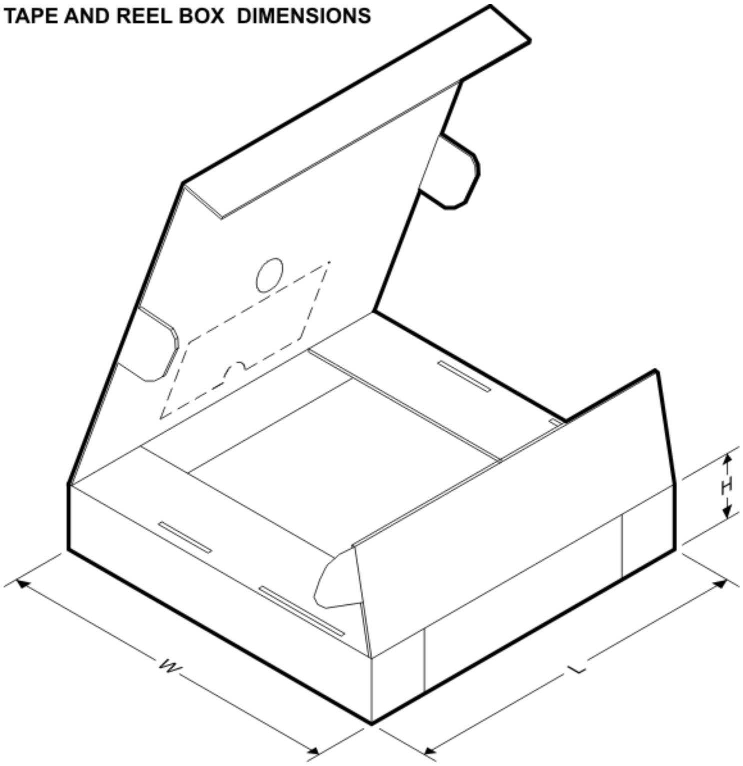
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62060DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62060DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62060DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62061DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62061DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62063DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62063DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62060DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62060DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62060DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62061DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62061DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62063DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62063DSGT	WSON	DSG	8	250	210.0	185.0	35.0

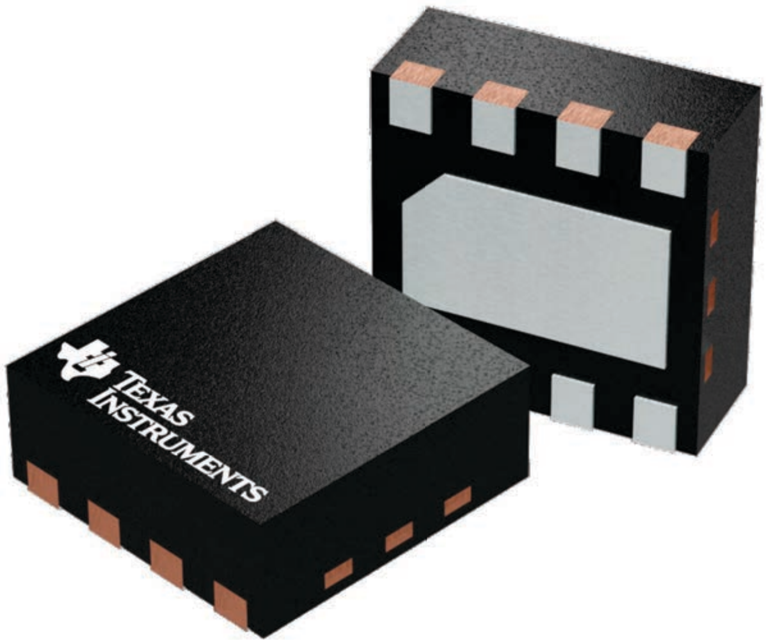
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

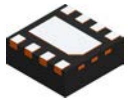
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

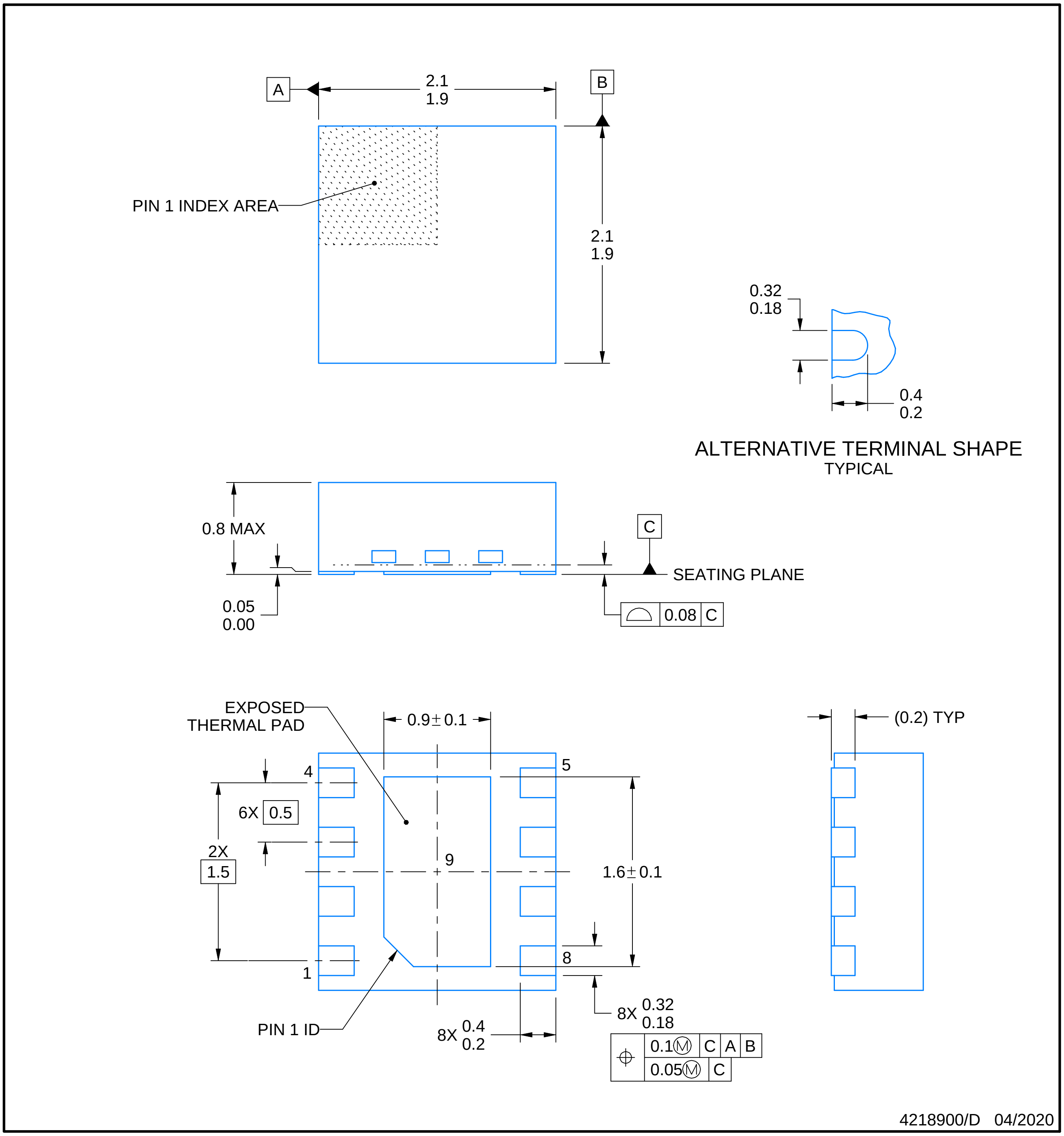
PACKAGE OUTLINE



DSG0008A

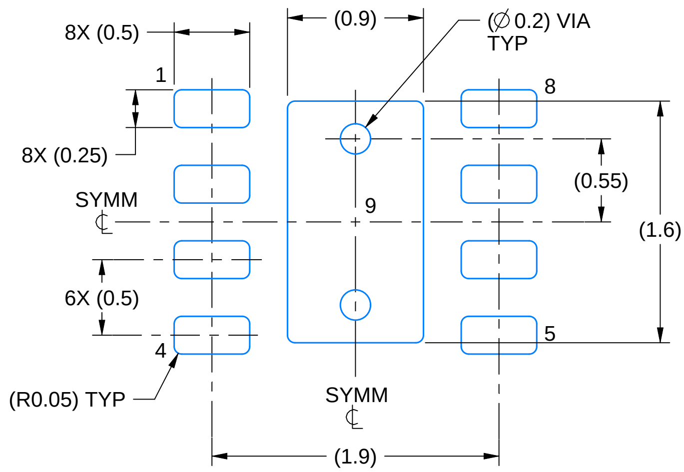
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

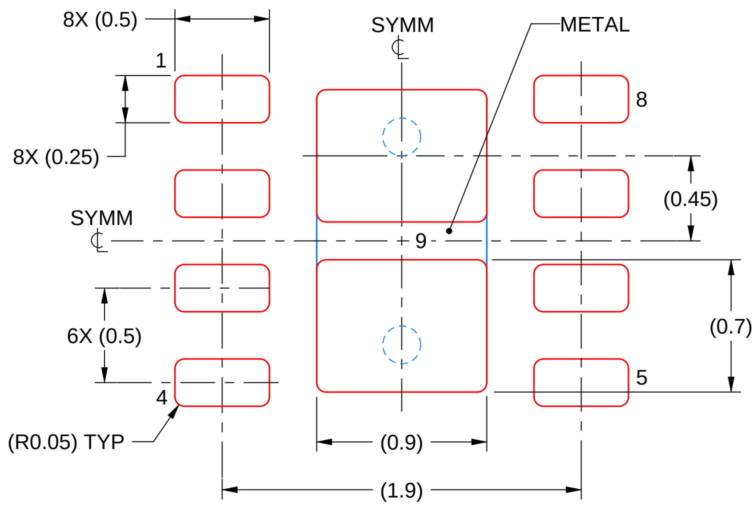
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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