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LMZ20501 1A 纳米模块

Technical

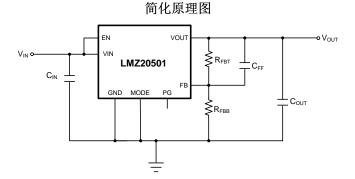
Documents

1 特性

- 集成电感
- 微型 3.5mm × 3.5mm × 1.75mm 封装
- 最大负载电流为 1A
- 输入电压范围为 2.7V 至 5.5V
- 可调输出电压范围为 0.8V 至 3.6V
- 温度范围内的反馈容差为±1%
- 关断模式下静态电流为 2.4µA (最大值)
- 3MHz 固定 PWM 开关频率
- -40°C 至 125°C 结温范围
- 电源正常状态标志功能
- 引脚可选开关模式
- 内部补偿和软启动
- 电流限制、热关断和 UVLO 保护
- 使用 LMZ20501 及其 WEBENCH[®] 电源设计器创 建定制设计

2 应用

- 负载点稳压
- 空间受限型应用 传感器



3 说明

🧷 Tools &

Software

LMZ20501 纳米模块稳压器是一款易于使用的同步降 压直流/直流转换器,能够从最高 5.5V 的输入电压驱动 高达 1A 的负载电流,以极小的解决方案尺寸提供优异 的效率和输出精度。这种创新型封装将稳压器和电感器 包含在 3.5mm × 3.5mm × 1.75mm 的小体积中,节省 了布板空间以及电容器选型所需的时间和开销。 LMZ20501 仅需要五个外部组件,其引脚设计可实现 简单、最优的 PCB 布局。该器件可使用最少数量的外 部组件和 TI WEBENCH[®]设计工具提供一套易于使用 的完整设计。TI 的 WEBENCH 工具包括 诸如 外部组 件计算、电路模拟和 WebTherm™等特性。有关焊接 信息,请参见 SNOA401。

Support &

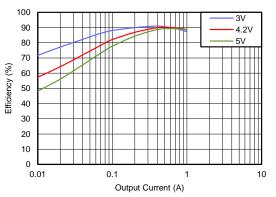
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器件信息⁽¹⁾

器件型号	封装	封装尺寸(标称值)		
LMZ20501	USIP (8)	3.50mm x 3.50mm		

(1) 如需了解所有可用封装,请参阅产品说明书末尾的可订购产品 附录。



Vour = 1.8V 时自动模式下的典型效率

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4 修订历史记录

注: 之前版本的页码可能与当前版本有所不同。

nanges from Revision C (April 2015) to Revision D Page				
• 己删除 Simple Switcher 品牌, 添加了 WEBENCH 链接	1			
Changes from Revision B (December 2014) to Revision C	Page			
• 已添加 手动封装选项附录	1			
Changes from Revision A (November 2014) to Revision B	Page			
 已更改器件信息表,ESD额定值表,特性描述,器件功能模式,应用和实施,电源相关建议,布局,器件和文档支 持以及机械、封装和可订购信息部分;已将一些曲线移至应用曲线部分。 	1			

Changes from Original (September 2013) to Revision A

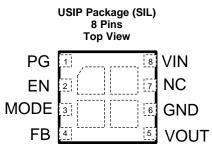
已添加 完整文档。.....1



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5 Pin Configuration and Functions



Pin Functions

PIN			DESCRIPTION		
NUMBER	NAME	ITPE	DESCRIPTION		
1	PG	0	Power good flag; open drain. Connect to logic supply through a resistor. High = power good; Low = power bad. If not used, leave unconnected.		
2	EN	I	Enable input. High = On, Low = Off. A valid input voltage, on pin 8, must be present before EN is asserted. Do not float.		
3	MODE	I	Mode selection input. High = forced PWM. Low = AUTO mode, with PFM at light load . Do not float.		
4	FB	Ι	Feedback input to controller. Connect to output through feedback divider.		
5	VOUT	Р	Regulated output voltage; connect to C _{OUT} .		
6	GND	G	Ground for all circuitry. Reference point for all voltages.		
7	NC		This pin must be left floating. Do not connect to ground or any other node.		
8	VIN	Р	Input supply to regulator. Connect to input capacitor(s) as close as possible to the VIN pin and GND pin of the module.		
EP	EP	G	Ground and heat-sink connection. See Layout Guidelines section for more information.		

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

Under the recommended operating junction temperature range of -40°C to 125°C (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT	
VIN to GND	-0.2	6		
EN, MODE, FB, PG, to GND ⁽²⁾	-0.2	V _{IN} +0.2	V	
VOUT to GND ⁽²⁾	-0.2	V _{IN} +0.2		
Junction temperature		150	°C	
Peak soldering reflow temperature for Pb ⁽³⁾		240	*0	
Peak soldering reflow temperature for No-Pb ⁽³⁾		260	°C	
Storage temperature range	-65	150	°C	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The absolute maximum voltage on this pin must not exceed 6V with respect to ground. Do not allow the voltage on the output pin to exceed the voltage on the input pin by more than 0.2 V.

(3) For soldering information, please refer to the following document: SNOA401.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101, all $\ensuremath{pins^{(2)}}$	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Under the recommended operating junction temperature range of -40°C to 125°C (unless otherwise noted) ⁽¹⁾

	MIN	NOM MAX	UNIT
Input voltage	2.7	5.5	V
Output voltage programming	0.8	3.6	V
Output voltage range ⁽²⁾	0	3.6	V
Load current	0	1	А
Power good flag current	0	4	mA
Junction temperature	-40	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Under no conditions should the output voltage be allowed to fall below zero volts.

6.4 Thermal Information

		LMZ20501	
	THERMAL METRIC ⁽¹⁾	USIP (SIL)	UNIT
		8 PINS	
R_{\thetaJA}	Junction-to-ambient thermal resistance	42.6	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	20.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	°C/W
ΤLΨ	Junction-to-top characterization parameter	1.5	°C/W
ΨJB	Junction-to-board characterization parameter	9.3	°C/W

(1) The values given in this table are only valid for comparison with other packages and can not be used for design purposes. For design information please see the *Maximum Ambient Temperature* section. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.



Thermal Information (continued)

	LMZ20501	
THERMAL METRIC ⁽¹⁾	USIP (SIL)	UNIT
	8 PINS	
R _{0JC(bot)} Junction-to-case (bottom) thermal resistance	1.8	°C/W

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6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of -40° C to 125° C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^{\circ}$ C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 3.6$ V

	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNIT
V _{FB}	Feedback voltage	V _{IN} = 3.6 V	0.594	0.6	0.606	V
I _{Q_AUTO}	Operating quiescent current in AUTO mode	AUTO mode, $V_{FB} = 0.8V$		72	90	μA
I _{Q_PWM}	Operating quiescent current in forced PWM mode	PWM mode, V _{FB} = 0.8V		490	620	μΑ
I _{Q_off}	Shutdown quiescent current ⁽²⁾	V _{IN} = 3.6 V, V _{EN} = 0.0 V		0.7	1.5	
		$V_{IN} = 5.5 \text{ V}, V_{EN} = 0.0 \text{ V}$		1.0	2.4	μA
V _{UVLO}	Input supply under-voltage	Rising		2.5		V
	lock-out thresholds	Falling		2.3		v
V _{EN}	High level input voltage	V _{IH}	1.4			N/
	Low level input voltage	V _{IL}			0.4	V
V _{MODE}	High level input voltage	V _{IH}	1.2			V
	Low level input voltage	VIL			0.4	
I _{LIM}	Peak switch current limit ⁽³⁾		1.3	1.7		А
Fosc	Internal oscillator frequency		2.5	3.0	3.2	MHz
T _{ON}	Minimum switch on-time ⁽⁴⁾			50		ns
T _{ss}	Soft start time ⁽⁴⁾			800		μs
R _{PG}	Power good flag pull-down R _{dson}		40	70	110	Ω
V _{PG1}	Power good flag, under- voltage trip ⁽⁵⁾	% of feedback voltage, rising		92%		
V _{PG2}	Power good flag, under- voltage trip ⁽⁵⁾	% of feedback voltage, falling		88%		
V _{PG3}	Power good flag, over-voltage trip ⁽⁵⁾	% of feedback voltage, rising		112%		
V _{PG4}	Power good flag, over-voltage trip ⁽⁵⁾	% of feedback voltage, falling		108%		
T _{SD}	Thermal shutdown ⁽⁴⁾	Rising threshold		159		°C
	Thermal shutdown hysteresis ⁽⁴⁾			15		°C

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

(2) Shutdown current includes leakage current of the switching transistors.

(3) This is the peak switch current limit measured with a slow current ramp. Due to inherent delays in the current limit comparator, the peak current limit measured at 3MHz will be larger.

(4) This parameter is not tested in production.

(5) See *Power Good Flag Function* for explanation of voltage levels.



6.6 System Characteristics

The following specifications apply to the circuit found in Figure 16 with the appropriate modifications from Table 2. These parameters are not tested in production and represent typical performance only. Unless otherwise stated the following conditions apply: $T_A = 25^{\circ}C$.

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		V_{OUT} = 1.2 V, V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, PWM	0.14%		
Load Regulation	Percent output voltage change for the given load current change	$V_{OUT} = 1.8 V$ $V_{IN} = 5 V$, $I_{OUT} = 0 A$ to 1 A, PWM	0.15%		
		$V_{OUT} = 3.3 V$ $V_{IN} = 5 V$, $I_{OUT} = 0 A$ to 1 A, PWM	0.11%		
			0.16%		
Line Regulation	Percent output voltage change for the given change in input voltage	V_{OUT} = 1.8 V I _{OUT} = 1 A, V _{IN} = 3 V to 5 V, PWM	0.12%		
		$V_{OUT} = 3.3 V$ $I_{OUT} = 1 A, V_{IN} = 4 V to 5 V, PWM$	0.1%		
		$V_{OUT} = 1.2 V$ $I_{OUT} = 1 A, V_{IN} = 5 V, PWM$	3.3		
V _{R-PWM}	Output voltage ripple in PWM	$V_{OUT} = 1.8 V$ $I_{OUT} = 1 A, V_{IN} = 5 V, PWM$	3.3		mV pk-pk
		$V_{OUT} = 3.3V$ $I_{OUT} = 1 A, V_{IN} = 5 V, PWM$	4.2		
		$V_{OUT} = 1.2V$ $I_{OUT} = 1 \text{ mA}, V_{IN} = 3 \text{ V}, \text{ PFM}$	22		
V _{R-PFM}	Output voltage ripple in PFM	$V_{OUT} = 1.8 V$ $I_{OUT} = 1 mA, V_{IN}=3 V, PFM$	22		mV pk-pk
		$V_{OUT} = 3.3 V$ $I_{OUT} = 1 mA, V_{IN} = 5 V, PFM$	40		
	Output voltage deviation from nominal due to a load current step	V_{OUT} = 1.2 V V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, Tr = Tf = 2 $\mu s,$ PWM	± 60		mV
Load Transient		V_{OUT} = 1.8 V V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, Tr = Tf = 2 $\mu s,$ PWM	±50		
		V_{OUT} = 3.3 V V_{IN} = 5 V, I_{OUT} = 0 A to 1 A, Tr = Tf = 2 $\mu s,$ PWM	±60		
		V_{OUT} = 1.2V I_{OUT} = 1 A, V_{IN} = 3 V to 5 V, Tr = Tf = 50 $\mu s,$ PWM	25		
Line Transient	Output voltage deviation due to an input voltage step	V_{OUT} = 1.8 V I_{OUT} = 1 A, V_{IN} = 3 V to 5 V, Tr = Tf = 50 $\mu s,$ PWM	30		mV pk-pk
		V_{OUT} = 3.3 V I_{OUT} = 1 A, V_{IN} = 4 V to 5 V, Tr = Tf = 50 $\mu s,$ PWM	20		
		V _{OUT} = 1.2 V V _{IN} = 3 V	87%		
	Peak efficiency	V _{OUT} = 1.8 V V _{IN} = 3 V	91%		
		V _{OUT} = 3.3 V V _{IN} = 4.2 V	94%		
η		V _{OUT} = 1.2 V V _{IN} = 3 V, I _{OUT} = 1 A	83%		
	Full load efficiency	V _{OUT} = 1.8 V V _{IN} = 3 V, I _{OUT} = 1 A	87%		
		V _{OUT} = 3.3 V V _{IN} = 4.2 V, I _{OUT} = 1 A	93%		

INSTRUMENTS

EXAS

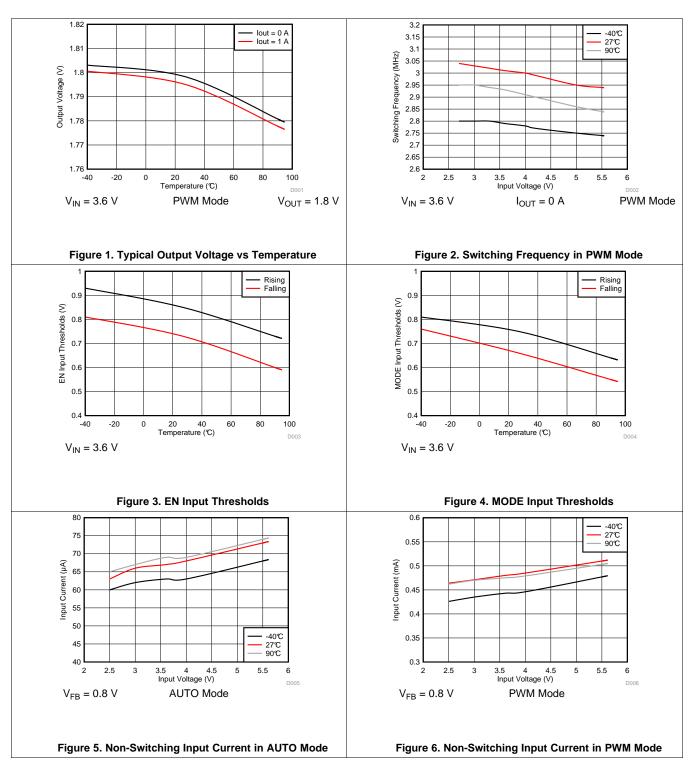
LMZ20501

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6.7 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 3.6 V, $T_A = 25^{\circ}C$.



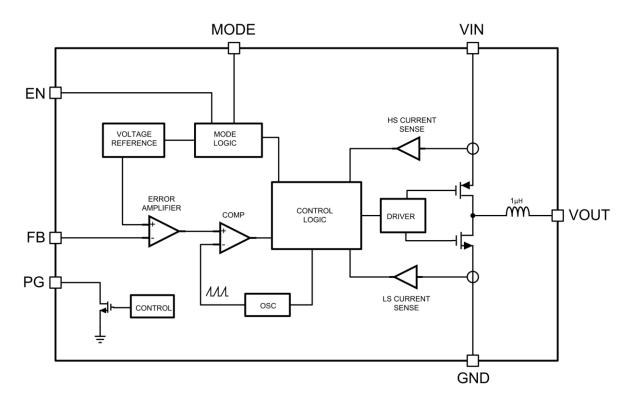


7 Detailed Description

7.1 Overview

The LMZ20501 nano module is a voltage mode buck regulator with an integrated inductor. Input voltage feedforward is used to compensate for loop gain variation with input voltage. Two operating modes allow the user to tailor the regulator to their specific requirements. In forced PWM mode, the regulator operates as a full synchronous device with a 3 MHz (typ.) switching frequency and very low output voltage ripple. In AUTO mode, the regulator moves into PFM when the load current drops below the mode change threshold (see *Application Curves*). In PFM, the device regulates the output voltage between wider ripple limits than in PWM. This results in much smaller supply current than in PWM, at light loads and high efficiency. A simplified block diagram is shown in *Functional Block Diagram*.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Nano Scale Package

The LMZ20501 incorporates world class package technology to provide a 1 A power supply with a total volume of only 21 mm³ (excluding external components). All that is required for a complete power supply is the addition of feed-back resistors to set the output voltage and the input and output filter capacitors. Figure 7 and Figure 8 show the LMZ20501 package. The regulator die is embedded into a PCB substrate while the power inductor is mounted on top. Vias and copper clad are used to make the connections to the die, inductor and the external components. This package is MSL3 compliant.

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Feature Description (continued)

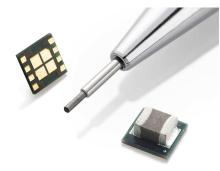


Figure 7. Package Photo

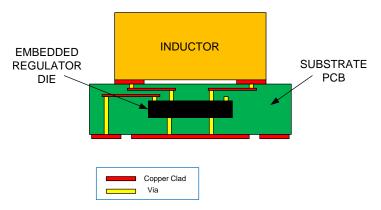


Figure 8. Package Side View Drawing

7.3.2 Internal Synchronous Rectifier

The LMZ20501 uses an internal NMOS FET as a synchronous rectifier to minimize switch voltage drop and increase efficiency. The NMOS is designed to conduct through its body diode during switch dead time. This dead time is imposed to prevent supply current "shoot-through".

7.3.3 Current Limit Protection

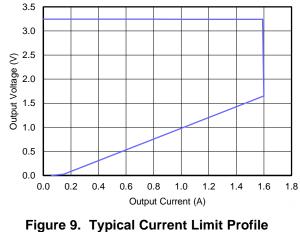
The LMZ20501 incorporates cycle-by-cycle peak current limit on both the high and low side MOSFETs. This feature limits the output current in case the output is overloaded. During the overload, the peak inductor current is limited to that value found in the *Electrical Characteristics* table under the heading of " I_{LIM} ".

In addition to current limit, a short circuit protection mode is also implemented. When the feedback voltage is brought down to less than 300 mV, but greater than 150 mV, by a short circuit, the synchronous rectifier is turned off. This provides more voltage across the inductor to help maintain the required volt-second balance. If a "harder" short brings the feedback voltage to below 150 mV, the current limit and switching frequency are both reduced to about $\frac{1}{2}$ of the nominal values. In addition, when the current limit is tripped, the device stops switching for about 85 µs. At the end of the time-out, switching resumes and the cycle repeats until the short is removed.

The effect of both overload and short circuit protection can be seen in Figure 9. This graph demonstrates that the device will supply slightly more than 1 A to the load when in overload and much less current during fold-back mode. This is typical behavior for any regulator with this type of current limit protection.



Feature Description (continued)



 $V_{IN} = 5 V, V_{OUT} = 1.8 V$

7.3.4 Start-Up

Start-up and shutdown of the LMZ20501 is controlled by the EN input. The characteristics of this input are found in the *Electrical Characteristics* table. A valid input voltage must be present on VIN before the enable control is asserted. The maximum voltage on the EN pin is 5.5 V or V_{IN} , whichever is smaller. Do not allow this input to float.

The LMZ20501 features a current limit based soft-start, that prevents large inrush currents and output overshoots as the regulator is starting up. The peak inductor current is stepped-up in a staircase fashion during the soft start period. A typical start-up event is shown in Figure 10:

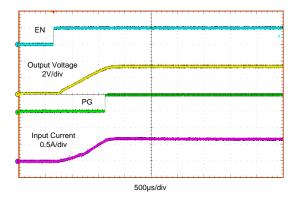


Figure 10. Typical Start-Up Waveforms, V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A

7.3.5 Drop-Out Behavior

When the input voltage is close to the output voltage the regulator will operate at very large duty cycles. Normal time delays of the internal circuits prevents the attainment of controlled duty cycles near 100%. In this condition the LMZ20501 will skip switching cycles in order to maintain regulation with the highest possible input-to-output ratio. Some increase in output voltage ripple may appear as the regulator skips cycles. As the input voltage gets closer to the output voltage, the regulator will eventually reach 100% duty cycle, with the high side switch turned on. The output will then follow the input voltage minus the drop across the high side switch and inductor resistance. Figure 11 and Figure 12 show typical drop-out behavior for output voltages of 2.5 V and 3.3 V.



Feature Description (continued)

Since the internal gate drive levels of the LMZ20501 Are dependent on input voltage, the R_{dson} of the power FETs will increase at low input voltages. This will result in degraded efficiency at input voltages below about 2.9 V. Also, combinations of low input voltage and high output voltage increases the effective switch duty cycle which may result in increased output voltage ripple.

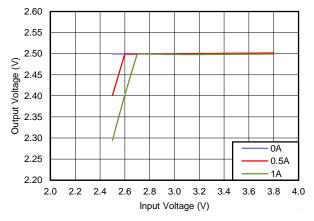


Figure 11. Typical Drop-Out Behavior, V_{OUT} = 2.5 V

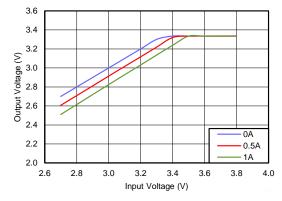


Figure 12. Typical Drop-Out Behavior, V_{OUT} = 3.3 V

7.3.6 Power Good Flag Function

The operation of the power good flag function is described in the diagram shown in Figure 13.



Feature Description (continued)

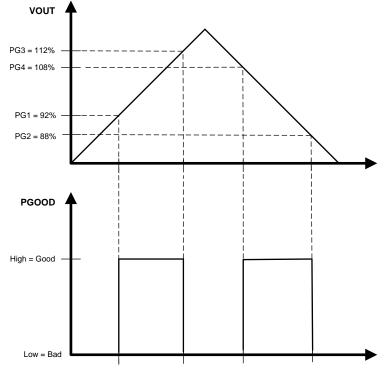


Figure 13. Typical Power Good Flag Operation

This output consists of an open drain NMOS with an R_{dson} of about 70 Ω . When used, the power good flag should be connected to a logic supply through a pull-up resistor. It can also be pulled-up to either V_{IN} or V_{OUT} , through an appropriate resistor, as desired. If this function is not needed, the PG output should be left floating. The current through this flag pin should be limited to less than 4 mA. A pull-up resistor of $\geq 1.5 \ k\Omega$ will satisfy this requirement. When the EN input is pulled low, the PG flag output will also be forced low, assuming a valid input voltage is present at the VIN pin.

7.3.7 Thermal Shutdown

The LMZ20501 incorporates a thermal shutdown feature to protect the device from excessive die temperatures. The device will stop switching when the internal die temperature reaches about 159°C. Switching will resume when the die temperature drops to about 144°C.

7.4 Device Functional Modes

Please refer to Table 1 and the following paragraphs for a detailed description of the functional modes of the LMZ20501. These modes are controlled by the MODE input as shown in Table 1. The maximum voltage on the MODE pin is 5.5 V or V_{IN} , whichever is smaller. This input must not be allowed to float.

MODE PIN VOLTAGE	OPERATION
> 1.2 V	Forced PWM: The regulator operates in constant frequency, PWM mode for all loads from no-load to full load; no diode emulation is used.
< 0.4 V	AUTO Mode: The regulator operates in constant frequency mode for loads greater than the mode change threshold. For loads less than the mode change threshold, the regulator operates in PFM with diode emulation.

Table 1. Mode Selection

LMZ20501

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7.4.1 PWM Operation

In forced PWM mode, the converter operates as a constant frequency voltage mode regulator with input voltage feed-forward. This provides excellent line and load regulation and low output voltage ripple. This operation is maintained, even at no-load, by allowing the inductor current to reverse its normal direction. While in PWM mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This mode trades off reduced light load efficiency for low output voltage ripple and constant switching frequency. In this mode, a negative current limit of about 750mA is imposed to prevent damage to the regulator power FETs.

7.4.2 PFM Operation

When in AUTO mode, and at light loads, the device enters PFM. The regulator estimates the load current by measuring both the high side and low side switch currents. This estimate is only approximate, and the exact load current threshold, to trigger PFM, can vary greatly with input and output voltage. The *Application Curves* show mode change thresholds for several typical operating points. When the regulator detects this threshold, the reference voltage is increased by approximately 10 mV. This causes the output voltage to rise to meet the new regulation point. When this point is reached, the converter stops switching and much of the internal circuitry is shut off, while the reference is returned to the PWM value. This saves supply current while the output voltage naturally starts to fall under the influence of the load current. When the output voltage reaches the PWM regulation point, switching is again started and the reference voltage is again increased by about 10 mV; thus starting the next cycle. Typical waveforms are shown in Figure 14.

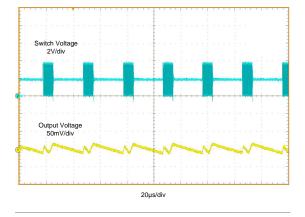


Figure 14. Typical PFM Mode Waveforms: V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA

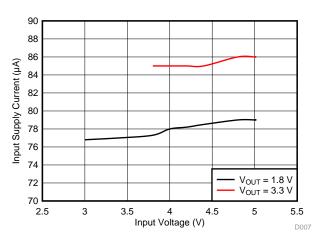


Figure 15. Typical No Load Input Supply Current



The actual output voltage ripple will depend on the feedback divider ratio and on the delay in the PFM comparator. The frequency of the PFM "bursts" will depend on the input voltage, output voltage, load and output capacitor. Within each "burst" the device switches at 3 MHz (typ.). If the load current increases above the threshold, normal PWM operation is resumed. This mode provides high light load efficiency by reducing the amount of supply current required to regulate the output at small load currents. This mode trades off very good light load efficiency for larger output voltage ripple and variable switching frequency. An example of the typical input supply current, while regulating with no load, is shown in Figure 15.

Because of normal part-to-part variation, the LMZ20501 may not switch into PFM mode at high input voltages. This may be seen with output voltages of about 1.2 V and below, at input voltages of about 4.2 V and above.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ20501 is a step down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LMZ20501. Alternately, the WEBENCH design tool may be used to generate a complete design. WEBENCH utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various design options.

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8.2 Typical Application

Figure 16 shows the minimum required application circuit, set up for a 1.8 V output. Figure 17 shows a full featured application circuit. Please refer to Figure 16 and Figure 17 during the following design procedures.

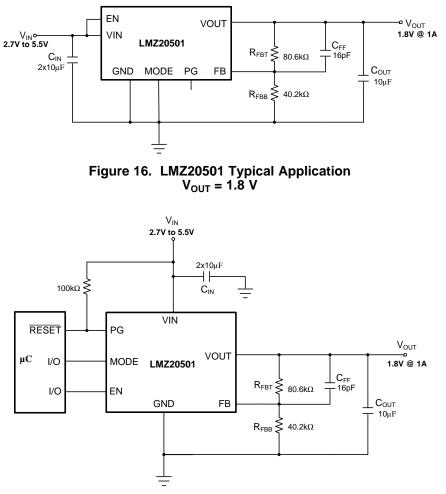


Figure 17. LMZ20501 Full Featured Application



Typical Application (continued)

8.2.1 Detailed Design Procedure

Please refer to Table 2 while following the detailed design procedure. This procedure applies to both Figure 16 and to Figure 17. Also, the Application Curves apply to both schematics.

V _{OUT} (V)	R_{FBB} (k Ω)	R_{FBT} (k Ω)	C _{OUT} (µF)	EFFECTIVE C _{OUT} (µF) ⁽²⁾	C _{FF} (pF)	C _{IN} (μF)	EFFECTIVE C _{IN} (µF) ⁽²⁾
0.8	121	40.2	2 x 10	18 µF	39	2 x 10	14
1.2	30.1	30.1	10	8.8 µF	20	2 x 10	14
1.8	40.2	80.6	10	8.4 µF	16	2 x 10	14
2.5	47.5	150	10	7.8 µF	12	2 x 10	14
3.3	53.2	237	10	7.1 µF	82	2 x 10	14
3.6	53.2	267	10	6.8 µF	82	2 x 10	14

Table 2. I	Recommended	Component	Values ⁽¹⁾
------------	-------------	-----------	-----------------------

 $C_{IN} = C_{OUT} = 10 \ \mu$ F, 16 V, 0805, X7R, Samsung CL21B106KOQNNNE. C_{OUT} measured at V_{OUT}; C_{IN} measured at 3.3 V. The effective value takes into account the capacitor voltage coefficient. (1)

(2)

8.2.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZ20501 device with the WEBENCH® Power Designer.

- 1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
- 2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
- 3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2 Setting The Output Voltage

The LMZ20501 regulates its feedback voltage to 0.6 V (typical). A feedback divider, shown in Figure 16, is used to set the desired output voltage. Equation 1 can be used to select R_{FBB} .

$$\mathbf{R}_{\rm FBB} = \frac{0.6}{(\mathbf{V}_{\rm OUT} - 0.6)} \cdot \mathbf{R}_{\rm FBT}$$

(1)

For best results, R_{FBT} should be chosen between 30 k Ω and 300 k Ω . See Table 2 for recommended values for typical output voltages.

8.2.1.3 Output and Feed-Forward Capacitors

The LMZ20501 is designed to work with low ESR ceramic capacitors. The effective value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have large voltage coefficients, in addition to normal tolerances and temperature coefficients. Under D.C. bias, the capacitance value drops considerably. Larger case sizes and/or higher voltage capacitors are better in this regard. To help mitigate these effects, multiple small capacitors can be used in parallel to bring the minimum effective capacitance up to the desired value. This can also ease the RMS current requirements on a single capacitor. Typically, 10 V, X5R, 0805 capacitors are adequate for the output, while 16-V caps may be used on the input. Some recommended component values are provided in Table 2. Also, shown are the measured values of effective input and output capacitance for the given capacitor. If smaller values of output capacitance are used, C_{FF} must be adjusted to give good phase margin. In any case, load transient response will be compromised with lower values of output capacitance. Values much lower than those found in Table 2 should be avoided.

In practice, the output capacitor and C_{FF} , are adjusted for the best transient response and highest loop phase margin. Load transient testing and Bode plots are the best way to validate any given design. Application report SLVA289 should prove helpful when optimizing the feed-forward capacitor. Also, SNVA364 details a simple method of creating a Bode plot with basic laboratory equipment. The values of C_{FF} found in Table 2 provide a good starting point.

A careful study of the temperature and bias voltage variation of any candidate ceramic capacitor should be made in order to ensure that the minimum values of **effective** capacitance are provided. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH tool.

The maximum value of total output capacitance should be limited to between 100 μ F and 200 μ F. Large values of output capacitance can prevent the regulator from starting-up correctly and adversely affect the loop stability. If values in the range given above, or larger, are to be used, then a careful study of start-up at full load and loop stability must be performed.

8.2.1.4 Input Capacitors

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. An **effective** value of at least 14 μ F is normally sufficient for the input capacitor. If the main input capacitor(s) can not be placed close to the module, then a small 10 nF to 100 nF capacitor should be placed directly at the module, across the supply and ground pins.

Many times it is desirable to use an electrolytic capacitor on the input, in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by long power leads. This method can also help to reduce voltage spikes that may exceed the maximum input voltage rating of the LMZ20501. The use of this additional capacitor will also help with voltage dips caused by input supplies with unusually high impedance.

Most of the switching current passes through the input ceramic capacitor(s). The approximate RMS value of this current can be calculated with Equation 2 and should be checked against the manufactures maximum ratings.

$$I_{\rm RMS} \approx \frac{I_{\rm OUT}}{2}$$

8.2.1.5 Maximum Ambient Temperature

18

As with any power conversion device, the LMZ20501 will dissipate internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter, above ambient. The internal die temperature is a function of the ambient temperature, the power loss and the effective thermal resistance $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LMZ20501 is 125°C, thus establishing a limit on the maximum device power dissipation and therefore load current at high ambient temperatures. Equation 3 shows the relationships between the important parameters.

$$I_{OUT} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1 - \eta)} \cdot \frac{1}{V_{OUT}}$$
(3)

It is easy to see that larger ambient temperatures and larger values of $R_{\theta,JA}$ will reduce the maximum available output current. As stated in SPRA953, the values given in the *Thermal Information* table are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that never obtain in an actual application. The effective $R_{\theta,JA}$ is a critical parameter and depends on many factors such as power dissipation, air temperature, PCB area, copper heatsink area, air flow, and adjacent component placement. The resources found in $\frac{1}{8}$ 3 can be used as a guide to estimate the $R_{\theta,JA}$ for a given application environment. A typical example of $R_{\theta,JA}$ versus copper board area is shown in Figure 18. The copper area in this graph is that for each layer; the inner layers are 1 oz (35µm). An $R_{\theta,JA}$ of 44°C/W is the approximate value for the LMZ20501 evaluation board. The efficiency found in Equation 3, η , should be taken at the elevated ambient temperature. For the LMZ20501 the efficiency is about two to three percent lower at high temperatures. Therefore, a slightly lower value than the typical efficiency can be used in the calculation. In this way Equation 3 can be used to estimate the maximum output current for a given ambient, or to estimate the maximum ambient for a given load current.

A typical curve of maximum load current vs. ambient temperature is shown in Figure 19. This graph assumes a $R_{\theta JA}$ of 44°C/W and an input voltage of 5 V.

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(2)



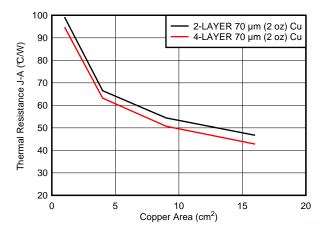


Figure 18. $R_{\theta JA}$ versus Copper Board Area

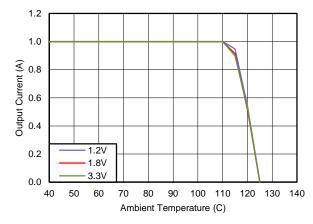


Figure 19. Maximum Output Current Vs. Ambient Temperature, R_{0JA} = 44°C/W, V_{IN} = 5 V

8.2.1.6 Options

The circuit in *Figure 17* highlights the use of the features of the LMZ20501. The PG output is open drain, and requires a pull-up resistor to a logic supply that is commensurate with the system logic voltage levels. If a reset function is not needed, the PG pin should be left open. The EN and MODE inputs are digital inputs, requiring only simple logic levels for proper operation. If the system does not need to control these features, the inputs should be connected to either VIN or GND, as appropriate. Please see *Feature Description* for details.

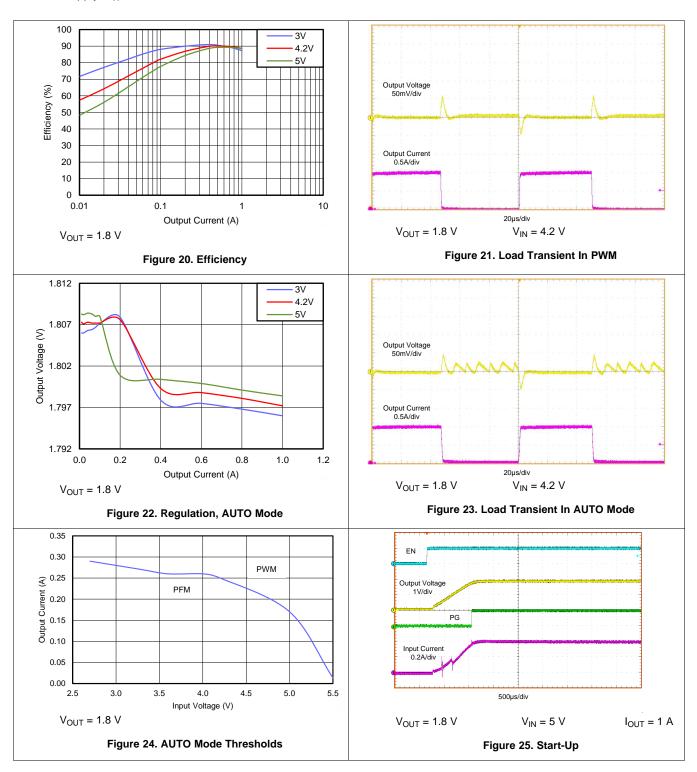
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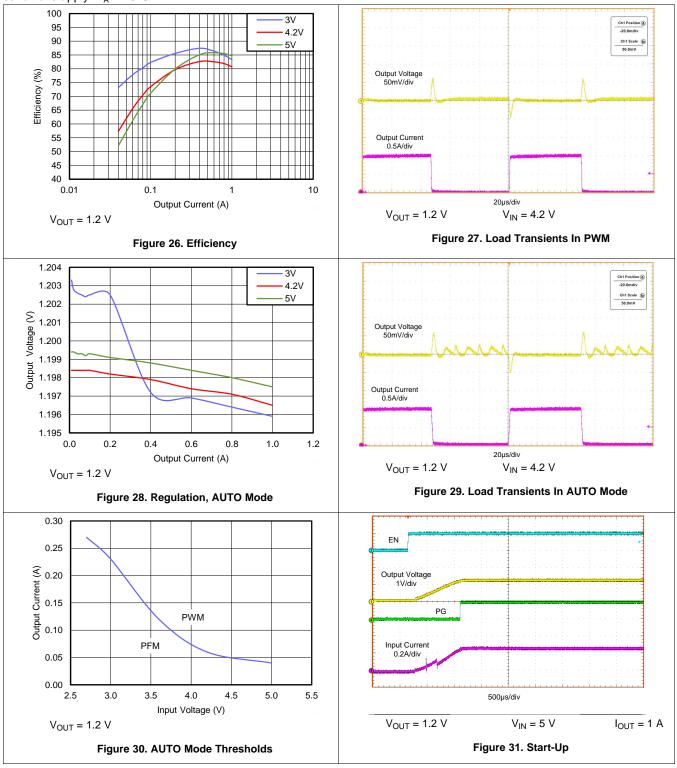
8.2.2 Application Curves

The following specifications apply to the circuit found in Figure 16 or Figure 17 with the appropriate modifications from Table 2. These parameters are not tested and represent typical performance only. Unless otherwise stated the following conditions apply: $T_A = 25^{\circ}C$.





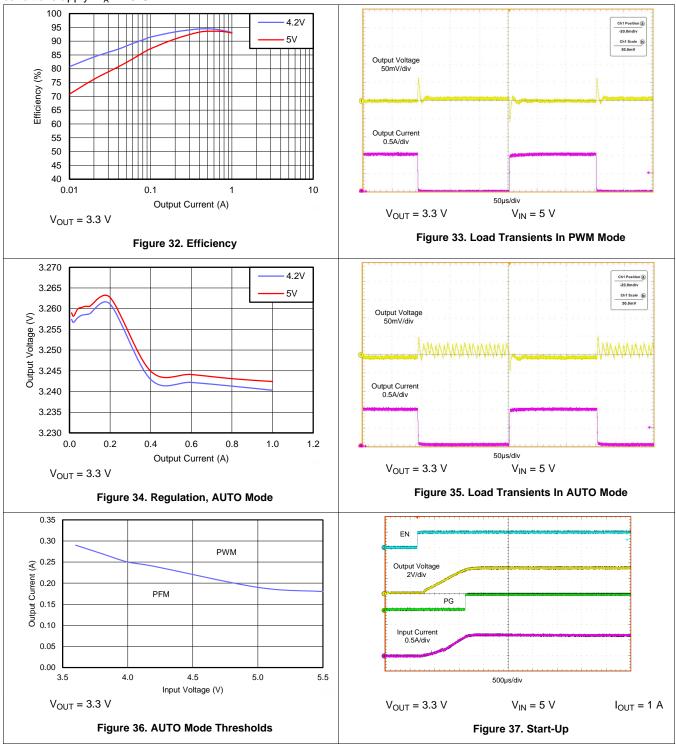
The following specifications apply to the circuit found in Figure 16 or Figure 17 with the appropriate modifications from Table 2. These parameters are not tested and represent typical performance only. Unless otherwise stated the following conditions apply: $T_A = 25^{\circ}C$.



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The following specifications apply to the circuit found in Figure 16 or Figure 17 with the appropriate modifications from Table 2. These parameters are not tested and represent typical performance only. Unless otherwise stated the following conditions apply: $T_A = 25^{\circ}C$.





8.3 Do's and Don'ts

- **Don't:** Exceed the *Absolute Maximum Ratings*.
- Don't: Exceed the ESD Ratings.
- Don't: Exceed the Recommended Operating Conditions.
- Don't: Allow the EN or MODE input to float.
- **Don't:** Allow the voltage on the EN or MODE input to exceed the voltage on the VIN pin.
- **Don't:** Allow the output voltage to exceed the input voltage.
- Don't: Use the thermal data given in the Thermal Information table to design your application.
- Do: Follow all of the guidelines and/or suggestions found in this data sheet, before committing your design to
 production. TI Application Engineers are ready to help critique your design and PCB layout to help make your
 project a success.
- Do: Refer to the helpful documents found in 表 3 and 表 4

9 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with Equation 4

$$I_{\rm IN} = \frac{V_{\rm OUT} \cdot I_{\rm OUT}}{V_{\rm IN} \cdot \eta}$$

(4)

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit may cause over-voltage transients at the VIN pin, each time the input supply is cycled on and off. The parasitic resistance will cause the voltage at the VIN pin to dip when the load on the regulator is switched on, or exhibits a transient. If the regulator is operating close to the minimum input voltage, this dip may cause the device to shutdown and/or reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors will help to damp the input resonant circuit and reduce any voltage overshoots. A value in the range of 20 μ F to 100 μ F is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator module. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The following user guide provides helpful suggestions when designing an input filter for any switching regulator: SNVA489.

In some cases a Transient Voltage Suppressor (TVS) is used on the input of regulators. One class of this device has a "snap-back" V-I characteristic (thyristor type). The use of a device with this type of characteristic is not recommend. When the TVS "fires", the clamping voltage drops to a very low value. If this holding voltage is less than the output voltage of the regulator, the output capacitors will be discharged through the regulator back to the input. This uncontrolled current flow could damage the regulator.



10 Layout

10.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor and the module ground, as shown in Figure 38. This loop carries fast transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages will disrupt the proper operation of the converter. Because of this, the traces in this loop should be wide and short, and the loop area as small as possible to reduce the parasitic inductance. Figure 39 shows a recommended layout for the critical components of the LMZ20501; the top side metal is shown in red. This PCB layout is a good guide for any specific application. The following important guidelines should also be followed:

- 1. Place the input capacitor CIN as close as possible to the VIN and GND terminals. VIN (pin 8) and GND (pin 6) are on the same side of the module, simplifying the input capacitor placement.
- Place the feedback divider as close as possible to the FB pin on the module. The divider and C_{FF} should be close to the module, while the length of the trace from VOUT to the divider can be somewhat longer. However, this latter trace should not be routed near any noise sources that can capacitively couple to the FB input.
- 3. Connect the EP pad to the GND plane. This pad acts as a heat-sink connection and a ground connection for the module. It must be solidly connected to a ground plane. The integrity of this connection has a direct bearing on the effective $R_{\theta JA}$.
- 4. Provide enough PCB area for proper heat-sinking. As stated in the Maximum Ambient Temperature section, enough copper area must be used to provide a low R_{θJA}, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers should be made with two ounce copper; and no less than one ounce.
- 5. The resources in $\frac{1}{5}$ 4 provide additional important guidelines

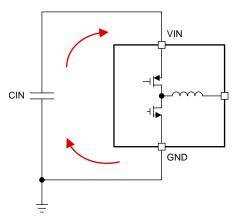


Figure 38. Current Loops With Fast Transient Currents



10.2 Layout Example

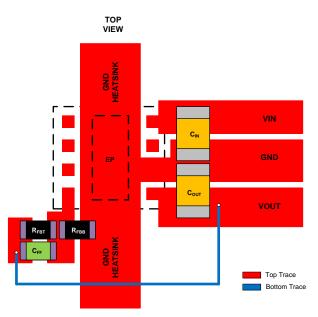


Figure 39. Example PCB Layout

10.3 Soldering Information

Proper operation of the LMZ20501 requires that it be correctly soldered to the PCB. This is especially true regarding the EP. This pad acts as a quiet ground reference for the device and a heatsink connection. Use the following recommendations when utilizing machine placement of the device:

- Dimension of area for pick-up: 2 mm x 2.5 mm.
- Use a nozzle size of less than 1.3 mm in diameter, so that the head does not touch the outer area of the package.
- Use a soft tip pick-and-place head.
- Add 0.05 mm to the component thickness so that the device will be released 0.05 mm into the solder paste without putting pressure or splashing the solder paste.
- Slow the pick arm when picking the part from the tape and reel carrier and when depositing the device on the board.
- If the machine releases the component by force, use the minimum force and no more than 3 N.
- For PCBs with surface mount components on both sides, it is suggested to put the LMZ20501 on the top side. In case the application requires bottom side placement, a re-flow fixture may be required to protect the module during the second reflow.

In addition, please follow the important guidelines found in: SNOA401. The curves in Figure 40 and Figure 41 show typical soldering temperature profiles.

Soldering Information (continued)

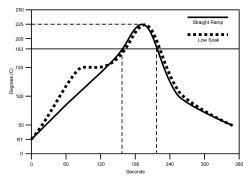


Figure 40. Typical Re-flow Profile Eutectic (63sn/37pb) Solder Paste

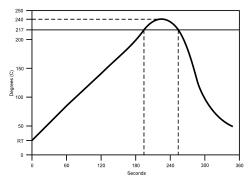


Figure 41. Typical Re-flow Profile Lead-Free (Sca305 Or Sac405) Solder Paste



11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息,不能构成与此类产品或服务或保修的适用性有关的认可,不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 开发支持

11.1.2.1 使用 WEBENCH® 工具创建定制设计

请单击此处,使用 LMZ20501 器件及其 WEBENCH® 电源设计器创建定制设计。

- 1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
- 2. 使用优化器拨盘优化该设计的关键参数,如效率、尺寸和成本。
- 3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下,可执行以下操作:

- 运行电气仿真,观察重要波形以及电路性能
- 运行热性能仿真,了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息,请访问 www.ti.com.cn/WEBENCH。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档:

表 3. 用于估算 R_{θJA} 的资源

标题	链接
AN-2020《富于洞见的热设计》	SNVA419
AN-2026《PCB 设计对 SIMPLE SWITCHER 电源模块散热性能的影响》	SNVA424
AN-1520《外露封装实现最佳热敏电阻特性的 电路板布线指南》	SNVA183
AN-1187《无引线框架封装 (LLP)》	SNOA401
SPRA953B《半导体和 IC 封装热指标》	SPRA953

表 4. PCB 布局布线资源

标题	链接
AN-1149《开关电源布局指南》	SNVA021
AN-1229《SIMPLE SWITCHER PCB 布局指 南》	SNVA054
《构建电源 - 布局注意事项》	SLUP230

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11.3 接收文档更新通知

要接收文档更新通知,请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册,即可每周接收产品信息更改摘要。有关更改的详细信息,请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点;请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 TI 的工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中,您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

WebTherm, E2E are trademarks of Texas Instruments. WEBENCH is a registered trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时,应将导线一起截短或将装置放置于导电泡棉中,以防止 MOS 门极遭受静电损 、伤。

11.7 术语表

SLYZ022 — TI 术语表。

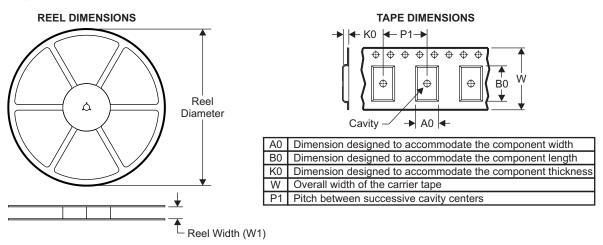
这份术语表列出并解释术语、缩写和定义。



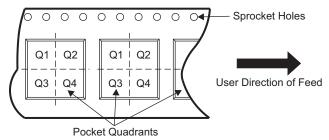
12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更, 恕不另行通知, 且 不会对此文档进行修订。如需获取此产品说明书的浏览器版本, 请查阅左侧的导航栏。

12.1 Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



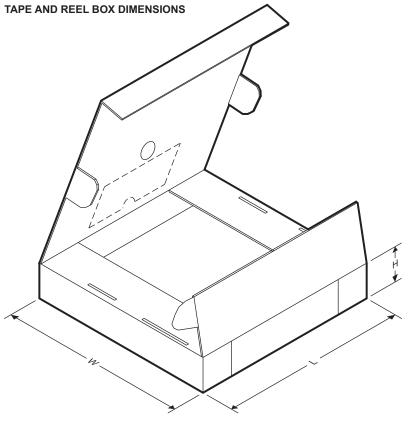
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ20501SILR	uSiP	SIL	8	3000	330.0	12.4	3.75	3.75	2.2	8.0	12.0	Q2
LMZ20501SILT	uSiP	SIL	8	250	178.0	13.2	3.75	3.75	2.2	8.0	12.0	Q2

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ20501SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
LMZ20501SILT	uSiP	SIL	8	250	223.0	194.0	35.0

重要声明和免责声明

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22-Feb-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ20501SILR	ACTIVE	uSiP	SIL	8	3000	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 125	1501 7543 EB	Samples
LMZ20501SILT	ACTIVE	uSiP	SIL	8	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 125	1501 7543 EB	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

22-Feb-2021

PACKAGE MATERIALS INFORMATION

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Texas Instruments

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ20501SILR	uSiP	SIL	8	3000	330.0	12.4	3.75	3.75	2.2	8.0	12.0	Q2
LMZ20501SILT	uSiP	SIL	8	250	178.0	13.2	3.75	3.75	2.2	8.0	12.0	Q2

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

10-Mar-2021



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ20501SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
LMZ20501SILT	uSiP	SIL	8	250	223.0	194.0	35.0

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