适用于成本敏感型应用的 TLV904x 微功耗、1.2V、RRIO、350kHz 运算放大器

1 特性

- 低静态电流：10μA/通道
- 可在电源电压低至 1.2V 的情况下运行
- 可扩展 CMOS 放大器，适用于低成本 应用
- 轨至轨输入和输出
- 低输入失调电压：±0.4mV
- 单位带宽增益积：350kHz
- 高效的静态电流与噪声比：82nV/√Hz
- 低输入偏置电流：5pA
- 单位增益稳定
- 内置 RFI 和 EMI 滤波器
- 由于具有电阻式开环输出阻抗，因此可在更高的容性负载下更轻松地实现稳定
- 工作温度范围：–40°C 至 125°C

2 应用

- 便携式电子产品
- 运动检测器（PIR、uWave 等等）
- 可穿戴设备（非医用）
- 压力变送器
- 过程分析（pH、气体、浓度、力和湿度）
- 电子销售点 (EPOS)
- 可穿戴健身和活动监测仪
- 耳麦/耳机和耳塞
- 个人电子产品
- 楼宇自动化
- 单电源、低侧、单向电流感应电路

3 说明

低功耗 TLV904x 系列包括单通道 (TLV9041)、双通道 (TLV9042) 和四通道 (TLV9044) 低压（1.2V 至 5.5V）运算放大器，具有轨至轨输入和输出摆幅功能。这类运算放大器为需要低工作电压和高容性负载驱动的电源和空间受限型 应用 （如电池供电的物联网设备、可穿戴电子产品和个人电子产品）提供了具有成本效益的解决方案。TLV904x 系列的容性负载驱动器具有 70pF 的电容，而电阻式开环输出阻抗使其能够在更高的容性负载下更轻松地实现稳定。这类运算放大器专为低工作电压（1.2V 至 5.5V）而设计，支持任何化学电池完全放电。

TLV904x 系列的稳健设计可简化电路设计。这些运算放大器具有单位增益稳定性，集成了 RFI 和 EMI 抑制滤波器，并且在过驱情况下不会出现相位反转。

TLV904x 器件具有关断模式（TLV9041S、TLV9042S 和 TLV9044S），允许放大器切换至典型电流消耗低于 1μA 的待机模式。

针对所有通道型号（单通道、双通道和四通道）提供微型封装（如 X2QFN 和 WSON）以及业界通用的封装（如 SOIC、MSOP、SOT-23 和 TSSOP 封装）。

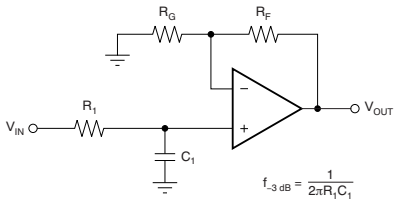
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV9042	SOIC (8)(2)	3.91mm × 4.90mm
	WSON (8)(2)	2.00mm × 2.00mm
	VSSOP (8)(2)	3.00mm × 3.00mm
	TSSOP (8)(2)	3.00mm × 4.40mm
TLV9042S	X2QFN (10)(2)	1.50mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装仅供预览。

单极低通滤波器



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2020 年 3 月	*	初始发行版。

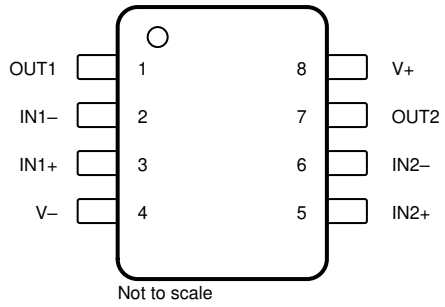
5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS											
		SC70 DCK(1)	SOIC D(1)	SOT-23 DBV(1)	SOT-23-8 DDF(1)	SOT-553 DRL(1)	TSSOP PW(1)	VSSOP DGK(1)	WQFN RTE(1)	WSON DSG(1)	X2QFN RUC(1)	X2SON DPW(1)	X2QFN RUG(1)
TLV9042(2)	2	—	8	—	8	—	8	8	—	8	—	—	—
TLV9042S(2)	2	—	—	—	—	—	—	—	—	—	—	—	10

(1) Package is preview only.
(2) Device is preview only.

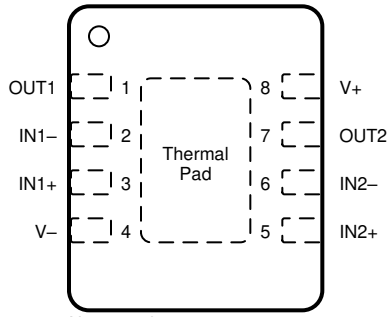
6 Pin Configuration and Functions

TLV9042 D, DDF, DGK, PW Packages
8-Pin SOIC, SOT-23 8, VSSOP, TSSOP
Top View



Not to scale

TLV9042 DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

Connect exposed thermal pad to V–. See *Packages With an Exposed Thermal Pad* section for more information.

Pin Functions: TLV9042

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I or —	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

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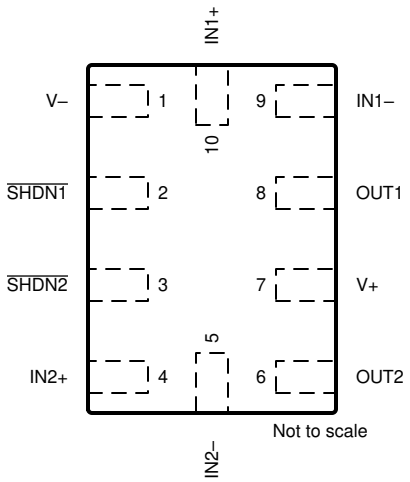
TLV9042S RUG Package
10-Pin X2QFN
Top View



Pin Functions: TLV9042S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	9	I	Inverting input, channel 1
IN1+	10	I	Noninverting input, channel 1
IN2–	5	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	8	O	Output, channel 1
OUT2	6	O	Output, channel 2
$\overline{\text{SHDN1}}$	2	I	Shutdown – low = disabled, high = enabled, channel 1
$\overline{\text{SHDN2}}$	3	I	Shutdown – low = disabled, high = enabled, channel 2
V–	1	I or —	Negative (low) supply or ground (for single-supply operation)
V+	7	I	Positive (high) supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	6.0	V
Signal input pins	Common-mode voltage (2)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (2)		V_S + 0.2	V
	Current (2)	–10	10	mA
Output short-circuit (3)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.2	5.5	V
V_I	Input voltage range	(V–)	(V+)	V
T_A	Specified temperature	–40	125	°C

7.4 Thermal Information for Dual Channel

THERMAL METRIC (1)		TLV9042, TLV9042S							UNIT
		D (2) (SOIC)	DDF (2) (SOT-23-8)	DGK (2) (VSSOP)	DGS (2) (VSSOP)	DSG (2) (WSON)	PW (2) (TSSOP)	RUG (2) (X2QFN)	
		8 PINS	8 PINS	8 PINS	10 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	148.3	203.8	TBD	TBD	99.8	203.1	196.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.8	123.9	TBD	TBD	122.2	91.9	87.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.6	121.6	TBD	TBD	66.0	133.8	117.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.6	21.7	TBD	TBD	13.8	23.7	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.9	199.6	TBD	TBD	65.9	132.1	117.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	TBD	TBD	41.9	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for TLV9042.

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7.5 Electrical Characteristics

For V_S = (V+) – (V–) = 1.2 V to 5.5 V (±0.6 V to ±2.75 V) at T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.4	±3	mV
			T_A = –40°C to 125°C			±3.5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.5		µV/°C
PSRR	Input offset voltage versus power supply	V_S = ±0.6 V to ±2.75 V , V_{CM} = V–			±10	±100	µV/V
	Channel separation	f = 10 kHz			±5.6		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±50	pA
I_{OS}	Input offset current				±5	±30	pA
NOISE							
E_N	Input voltage noise	f = 0.1 to 10 Hz			6.6		μV_{PP}
e_N	Input voltage noise density	f = 100 Hz			92.6		nV/√Hz
		f = 1 kHz			81.5		
		f = 10 kHz			84.5		
i_N	Input current noise	f = 1 kHz			20		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	(V–) V < V_{CM} < (V+) – 0.7 V, V_S = 1.2 V (PMOS Pair)	T_A = –40°C to 125°C	79	88		dB
		(V–) V < V_{CM} < (V+) – 0.7 V, V_S = 5.5 V (PMOS Pair)		80	95		
		(V–) V < V_{CM} < (V+) V, V_S = 1.2 V (Full Range)			62		
		(V–) V < V_{CM} < (V+) V, V_S = 5.5 V (Full Range)		60	74		
INPUT CAPACITANCE							
Z_{ID}	Differential				80 || 1.4		GΩ || pF
Z_{ICM}	Common-mode				100 || 0.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 1.2 V, (V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ to V_S / 2	T_A = –40°C to 125°C		95		dB
		V_S = 5.5 V, (V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ to V_S / 2			120		
		V_S = 1.2 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 100 kΩ to V_S / 2			95		
		V_S = 5.5 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 100 kΩ to V_S / 2		110	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	R_L = 1 MΩ			350		KHz
SR	Slew rate	V_S = 5.5 V, G = +1, C_L = 50 pF			0.2		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5 V, V_{STEP} = 4 V, G = +1, C_L = 20 pF			25		µs
		To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			22		
		To 0.01%, V_S = 5.5 V, V_{STEP} = 4 V, G = +1, C_L = 20 pF			35		
		To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF			30		
	Phase margin	G = +1, R_L = 100 kΩ, C_L = 20 pF			55		°
	Overload recovery time	V_{IN} × gain > V_S			20		µs
EMIRR	Electro-magnetic interference rejection ratio	f = 1 GHz, V_{IN_EMIRR} = 100 mV			80		dB
OUTPUT							

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Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.2 V to 5.5 V (±0.6 V to ±2.75 V) at T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Voltage output swing from rail	Positive rail headroom	V_S = 1.2 V, R_L = 100 kΩ		1	1.32	mV
			V_S = 5.5 V, R_L = 10 kΩ		20	30	
			V_S = 5.5 V, R_L = 100 kΩ		5	8	
		Negative rail headroom	V_S = 1.2 V, R_L = 100 kΩ		1.03	1.35	
			V_S = 5.5 V, R_L = 10 kΩ		20	30	
			V_S = 5.5 V, R_L = 100 kΩ		5	8	
I_{SC}	Short-circuit current	V_S = 5.5 V			±40		mA
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 A			10	13	µA
			T_A = –40°C to 125°C			15	
	Turn-on time	At T_A = 25°C, V_S = 5.5 V, V_S ramp rate > 0.3 V/µs			125		µs
SHUTDOWN							
I_{QSD}	Quiescent current per amplifier	All amplifiers disabled, $\overline{SHDN}$ = V–			0.3	1.5	µA
Z_{SHDN}	Output impedance during shutdown	Amplifier disabled			43 || 11.5		GΩ || pF
V_{IH}	Logic high threshold voltage (amplifier enabled)			(V–) + 1 V			V
V_{IL}	Logic low threshold voltage (amplifier disabled)					(V–) + 0.2 V	V
t_{ON}	Amplifier enable time (full shutdown) (1) (2)	G = +1, V_{CM} = V–, V_O = 0.1 × V_S / 2			160		µs
	Amplifier enable time (partial shutdown) (1) (2)	G = +1, V_{CM} = V–, V_O = 0.1 × V_S / 2			120		
t_{OFF}	Amplifier disable time (1)	V_{CM} = V–, V_O = V_S / 2			10		µs
	$\overline{SHDN}$ pin input bias current (per pin)	(V+) ≥ $\overline{SHDN}$ ≥ (V–) + 1 V			100		pA
		(V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.2 V			50		

(1) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

(2) Full shutdown refers to the dual TLV9042S having both channels 1 and 2 disabled ($\overline{SHDN1}$ = $\overline{SHDN2}$ = V–) and the quad TLV9044S having all channels 1 to 4 disabled ($\overline{SHDN12}$ = $\overline{SHDN34}$ = V–). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in this mode, the internal biasing circuitry remains operational and the enable time is shorter.

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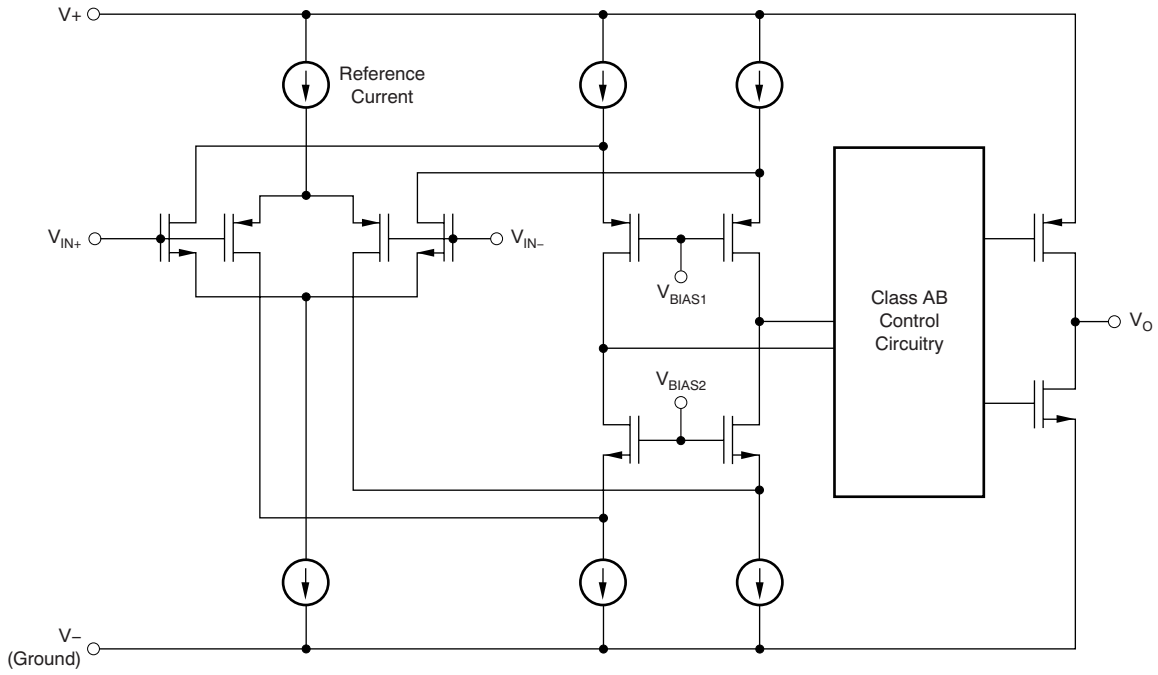
8 Detailed Description

8.1 Overview

The TLV904x is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for battery powered applications. This family of amplifiers utilizes unique low voltage transistors that enable operation from 1.2 V to 5.5 V. These unity-gain stable amplifiers provide 350-kHz of GBW with an IQ of only 10 µA. This makes them suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the TLV904x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices ideal for driving sampling analog-to-digital converters (ADCs).

The TLV904x features 350-kHz bandwidth and 0.25-V/µs slew rate with only 10-µA supply current per channel, providing good AC performance at very low power consumption. DC applications are also well served with a best in class input noise voltage of 82 nV/√Hz at 1 kHz, low input bias current (5 pA), and an input offset voltage of 0.4 mV (typical).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV904x series of operational amplifiers is fully specified and ensured for operation from 1.2 V to 5.5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in the typical characteristic section, which will be added at time of product release. Bypass power-supply pins with 0.01-µF ceramic capacitors.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV904x series extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair; see the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 0.7 V to 200 mV above the positive supply, and the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 0.7 V. There is a small transition

Feature Description (接下页)

region, typically (V+) – 0.6 V to (V+) – 0.8 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1 V to (V+) – 0.8 V on the low end, up to (V+) – 0.4 V to (V+) – 0.6 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the TLV904x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 1 kΩ, the output typically swings to within 20 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 Common-Mode Rejection Ratio (CMRR)

The CMRR for the TLV904x is specified in several ways so the best match for a given application can be used; see the Electrical Characteristics table. First, the CMRR of the device in the common-mode range below the transition region [VCM < (V+) – 0.7 V] is given. This specification is the best indicator of the capability of the device when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (VCM = 0 V to 5.5 V). This last value includes the variations measured through the transition region.

8.3.5 Capacitive Load and Stability

The TLV904x is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLV904x can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the TLV904x remains stable with a pure capacitive load up to approximately 70 pF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10 Ω to 20 Ω) in series with the output, as shown in 图 1. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

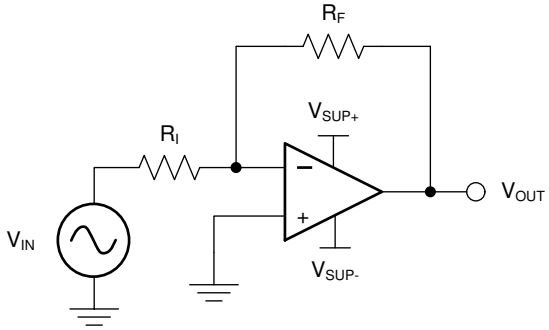


图 1. Improving Capacitive Load Drive

Feature Description (接下页)

8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The TLV904x operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity.

Detailed information can also be found in application report, *EMI rejection ratio of operational amplifiers* SBOA128, available for download from www.ti.com.

8.3.7 Packages With an Exposed Thermal Pad

The TLV904x family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other then V– is not allowed, and the performance of the device is not assured when doing so.

8.4 Device Functional Modes

The TLV904x family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.2 V (±0.6 V) and 5.5 V (±2.75 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV904x family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable applications. The devices operate from 1.2 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10-kΩ loads connected to any point between V+ and V–. The input common-mode voltage range includes both rails, and allows the TLV904x devices to be used in any single-supply application.

9.2 Typical Application

9.2.1 TLV904x Low-Side, Current Sensing Application

图 2 shows the TLV904x configured in a low-side current sensing application.

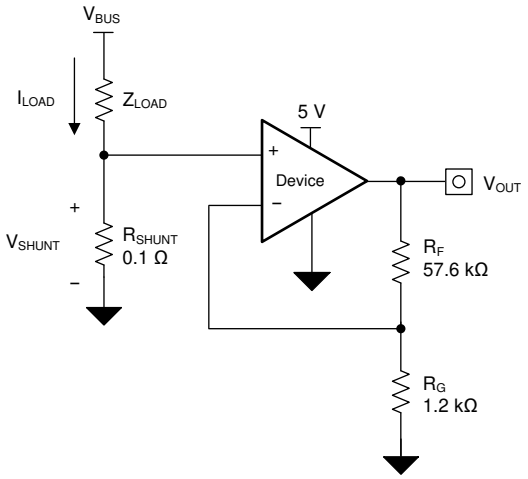


图 2. TLV904x in a Low-Side, Current-Sensing Application

ADVANCE INFORMATION

Typical Application (接下页)

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 2 is given in 公式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is shown using 公式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using 公式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV904x to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the TLV904x to produce the necessary output voltage is calculated using 公式 3.

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \quad (3)$$

Using 公式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 公式 4 sizes the resistors R_F and R_G, to set the gain of the TLV904x to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49 V/V. 图 3 shows the measured transfer function of the circuit shown in 图 2. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

9.2.1.3 Application Curve

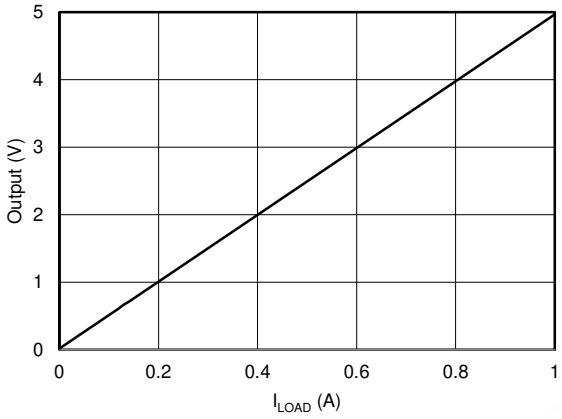


图 3. Low-Side, Current-Sense Transfer Function

10 Power Supply Recommendations

The TLV904x family is specified for operation from 1.2 V to 5.5 V (±0.6 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Electrical Characteristics* section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see the Absolute Maximum Ratings table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10.1 Input and ESD Protection

The TLV904x family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA. 图 4 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

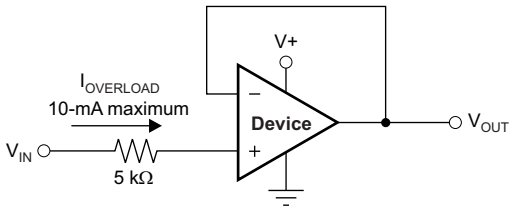


图 4. Input Current Protection

ADVANCE INFORMATION

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in 图 6. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

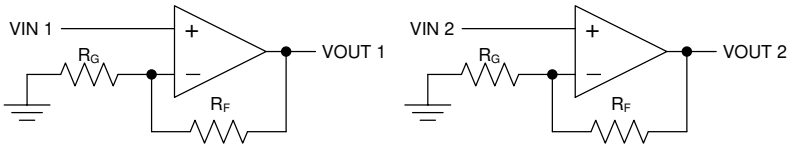


图 5. Schematic Representation for 图 6

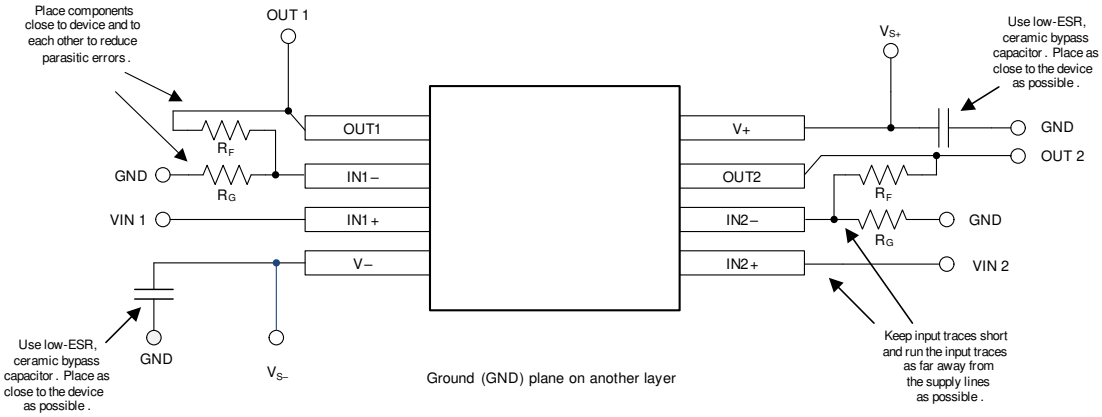


图 6. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《运算放大器的 EMI 抑制比》*
- *《QFN/SON PCB 连接》*
- *《四方扁平封装无引线逻辑封装》*

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 商标

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12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9042IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T042	Samples
TLV9042IDGKR	PREVIEW	VSSOP	DGK	8	2500	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		
TLV9042IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9042D	Samples
TLV9042IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T42G	Samples
TLV9042IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9042P	Samples
TLV9042SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	HTF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

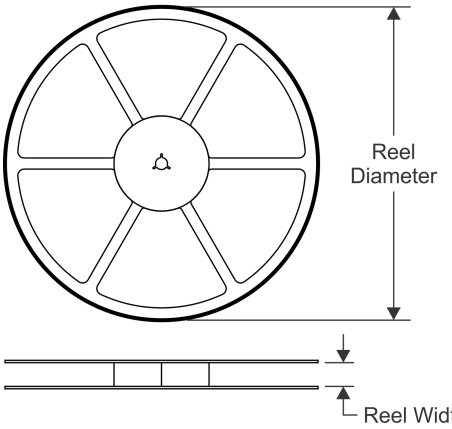
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

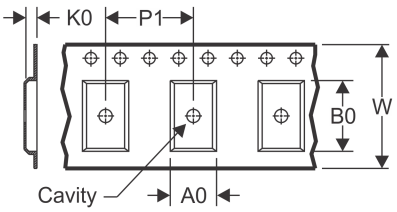
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

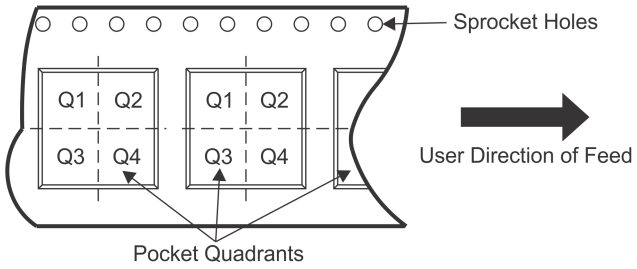


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

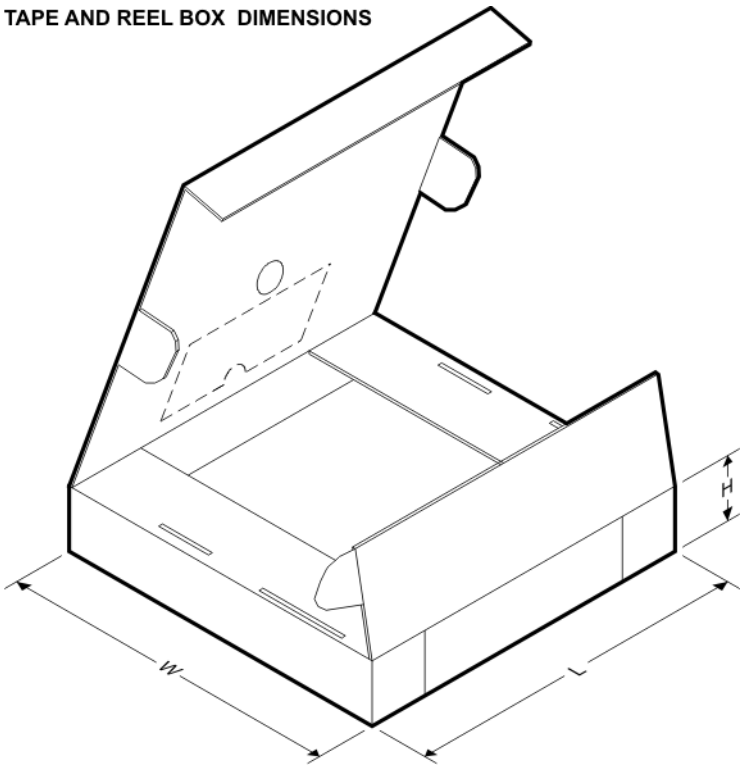
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9042IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9042IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9042IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9042IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9042SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1

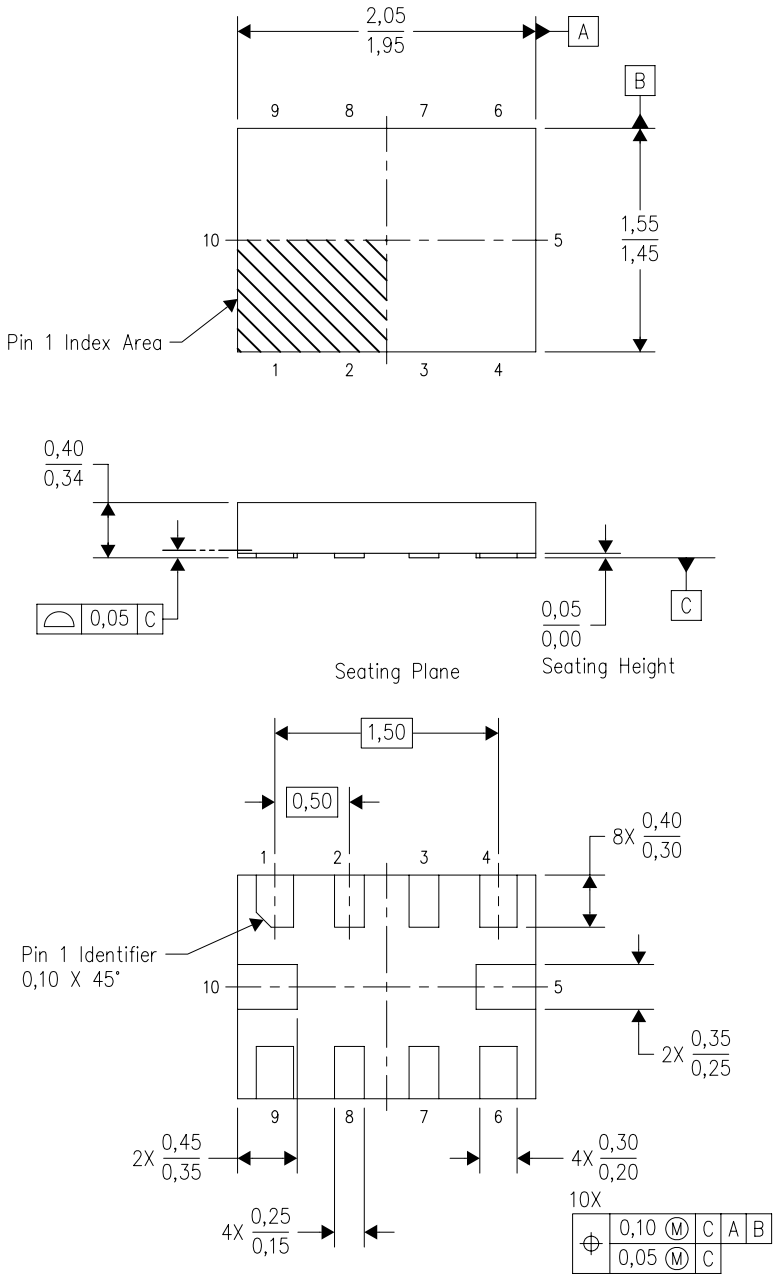
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9042IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9042IDR	SOIC	D	8	2500	853.0	449.0	35.0
TLV9042IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9042IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV9042SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0

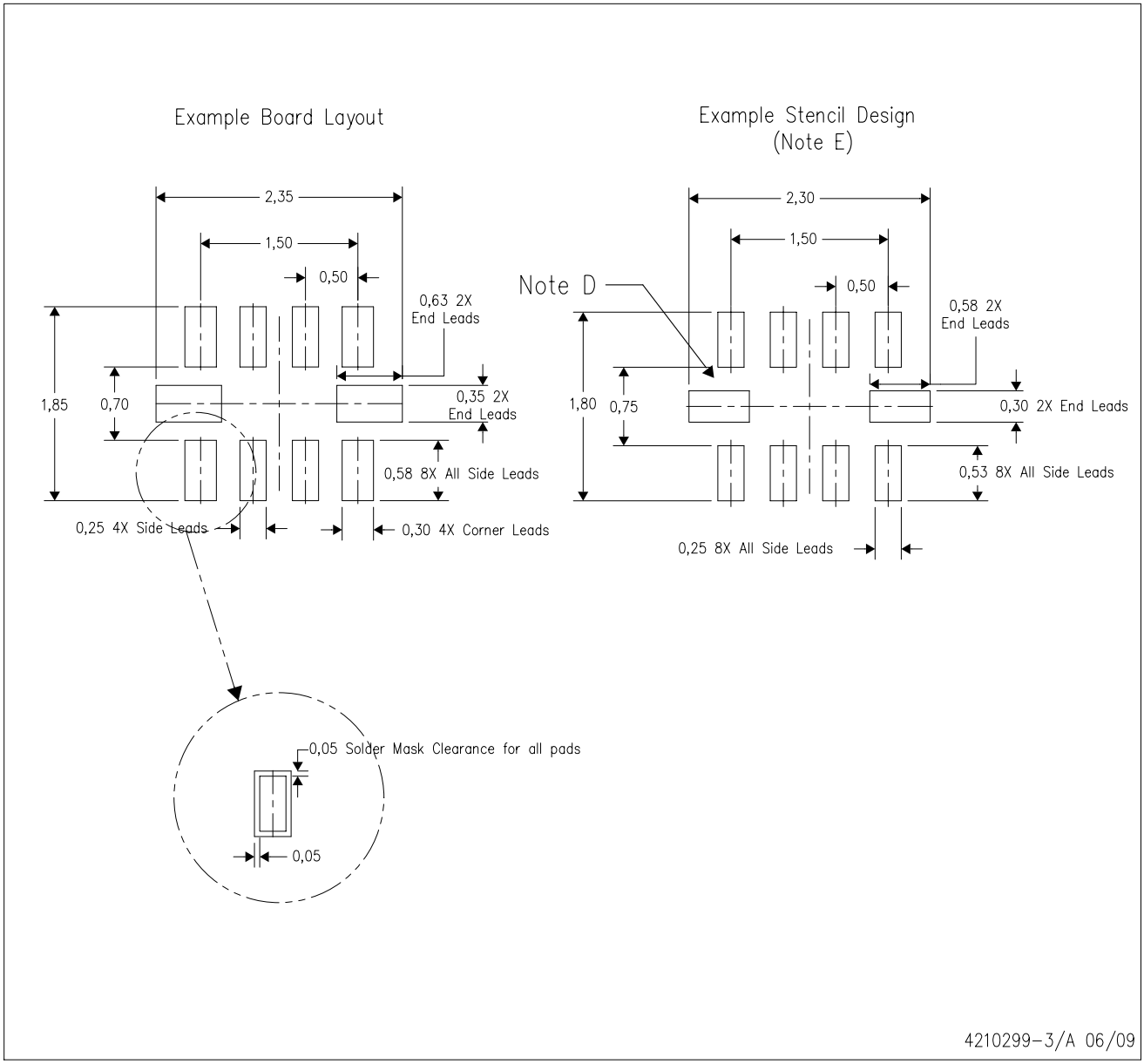
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



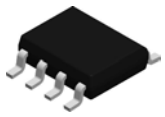
4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

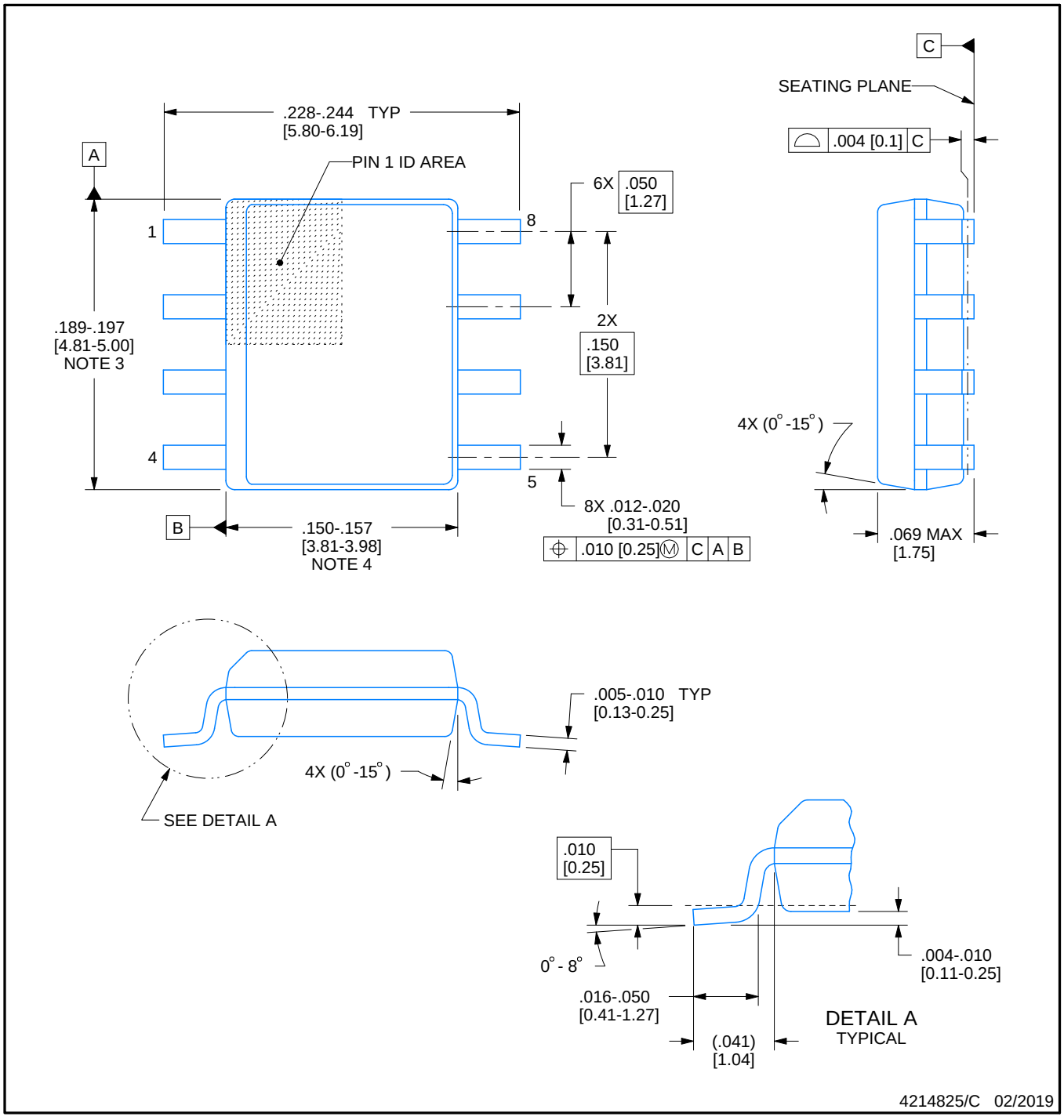


PACKAGE OUTLINE

D0008A

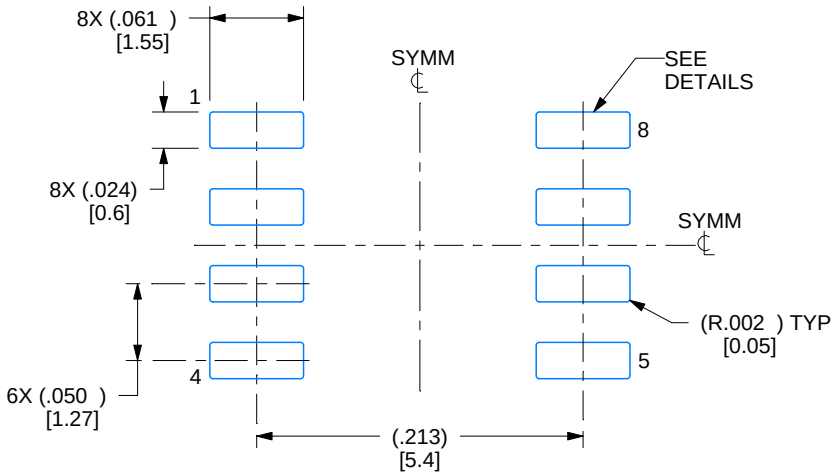
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

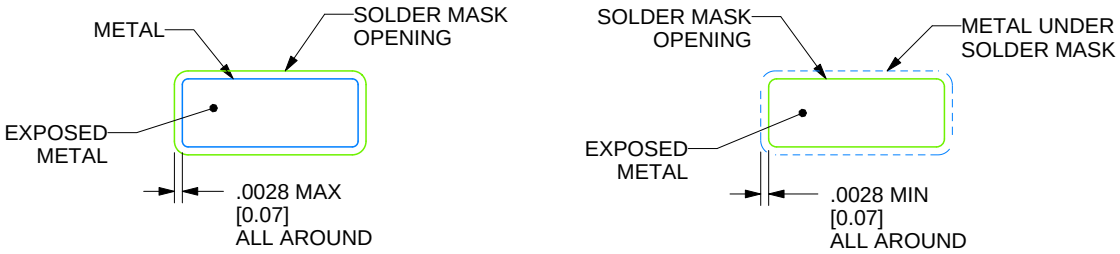


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

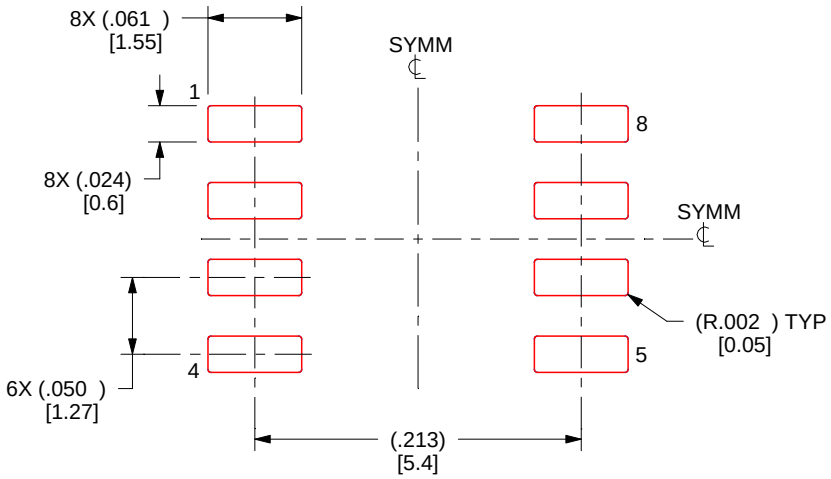
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

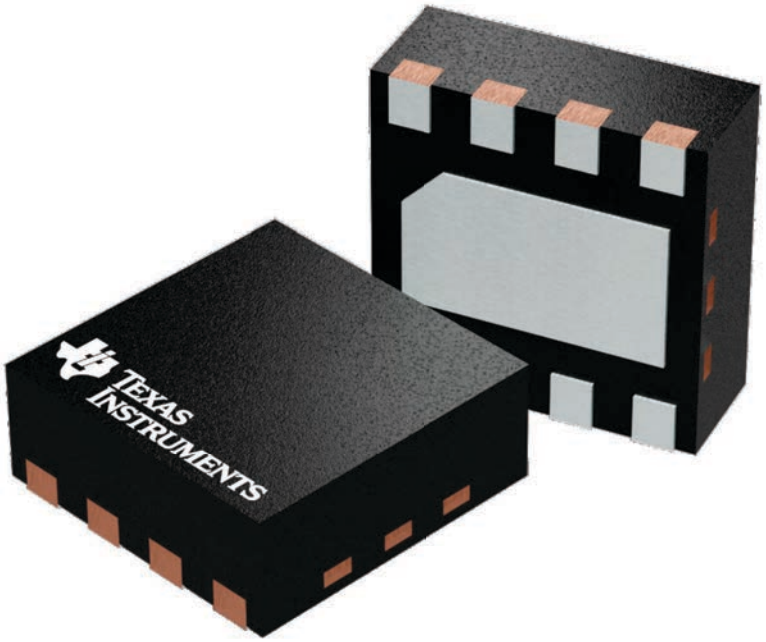
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



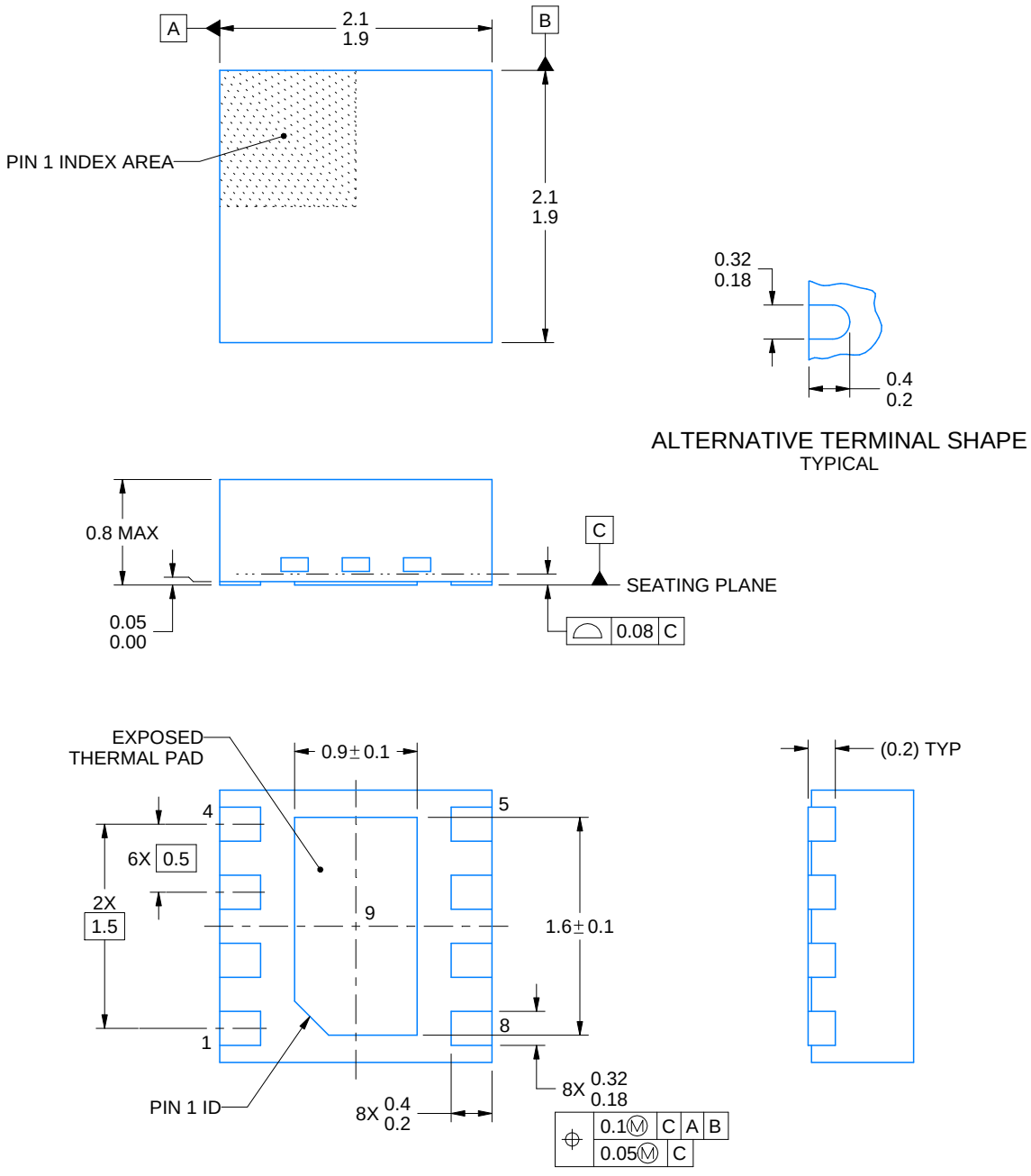
4224783/A

PACKAGE OUTLINE

DSG0008A

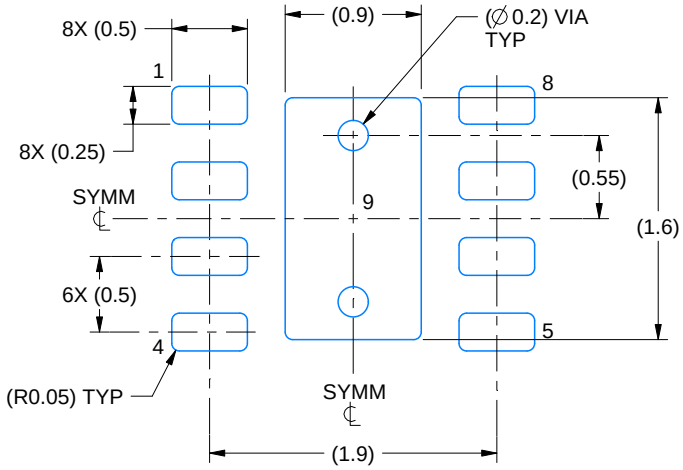
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

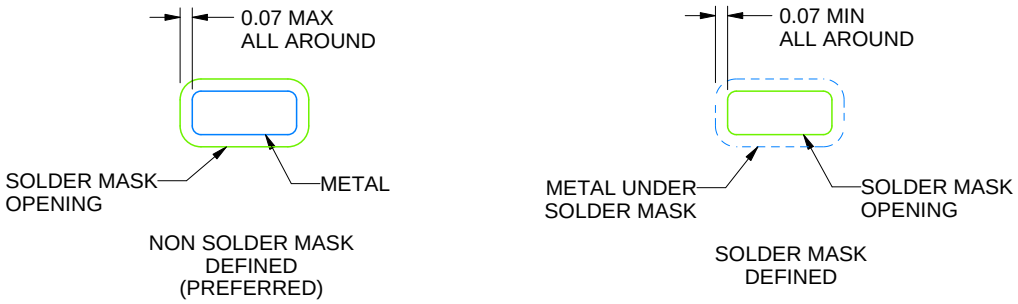


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

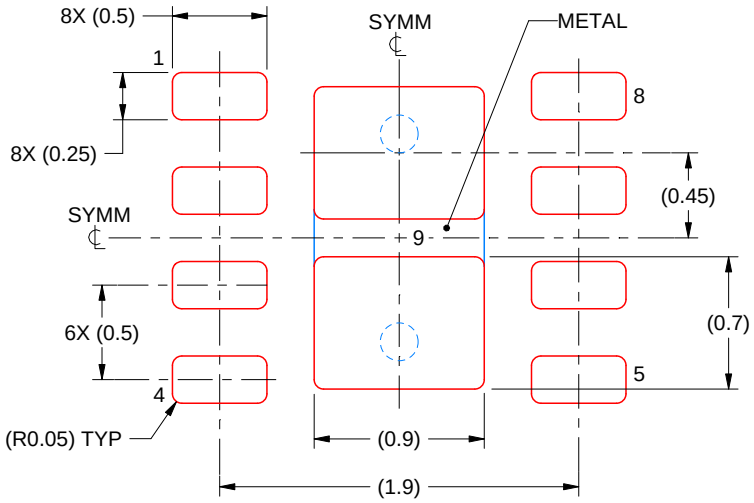
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

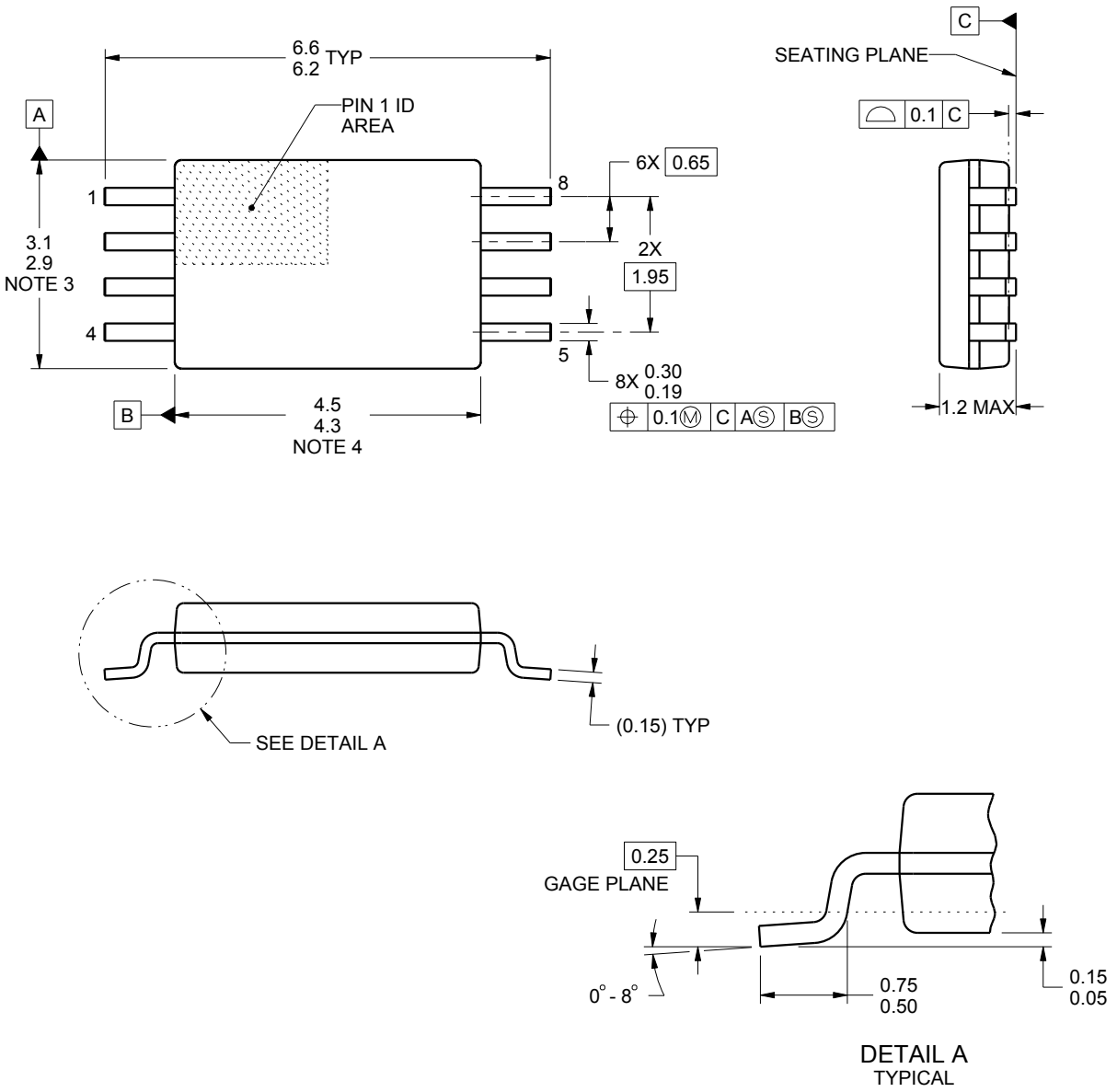
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

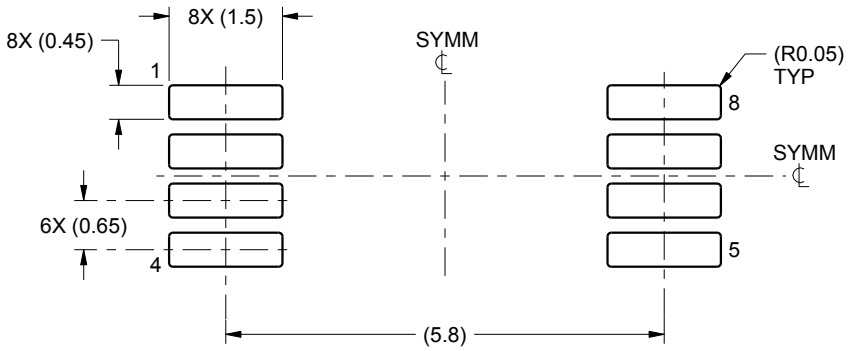
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

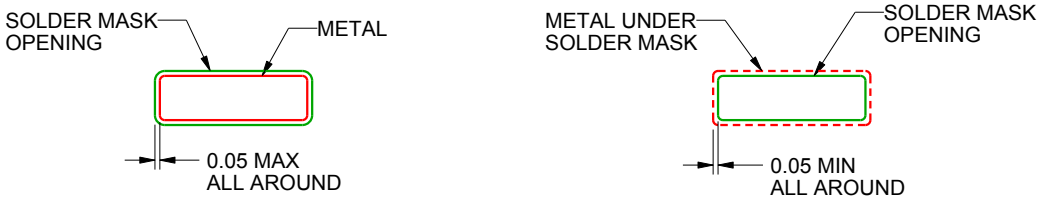


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

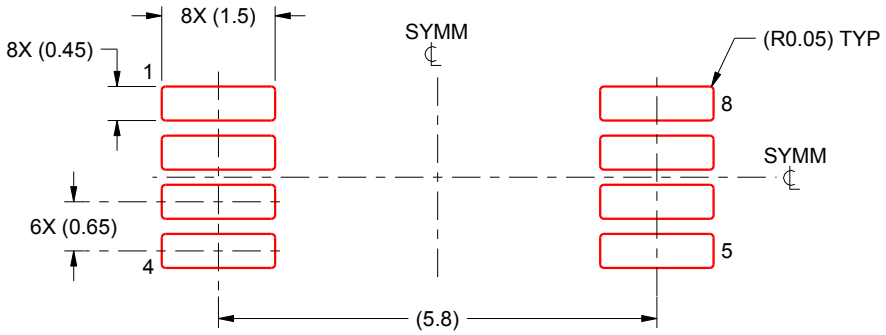


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

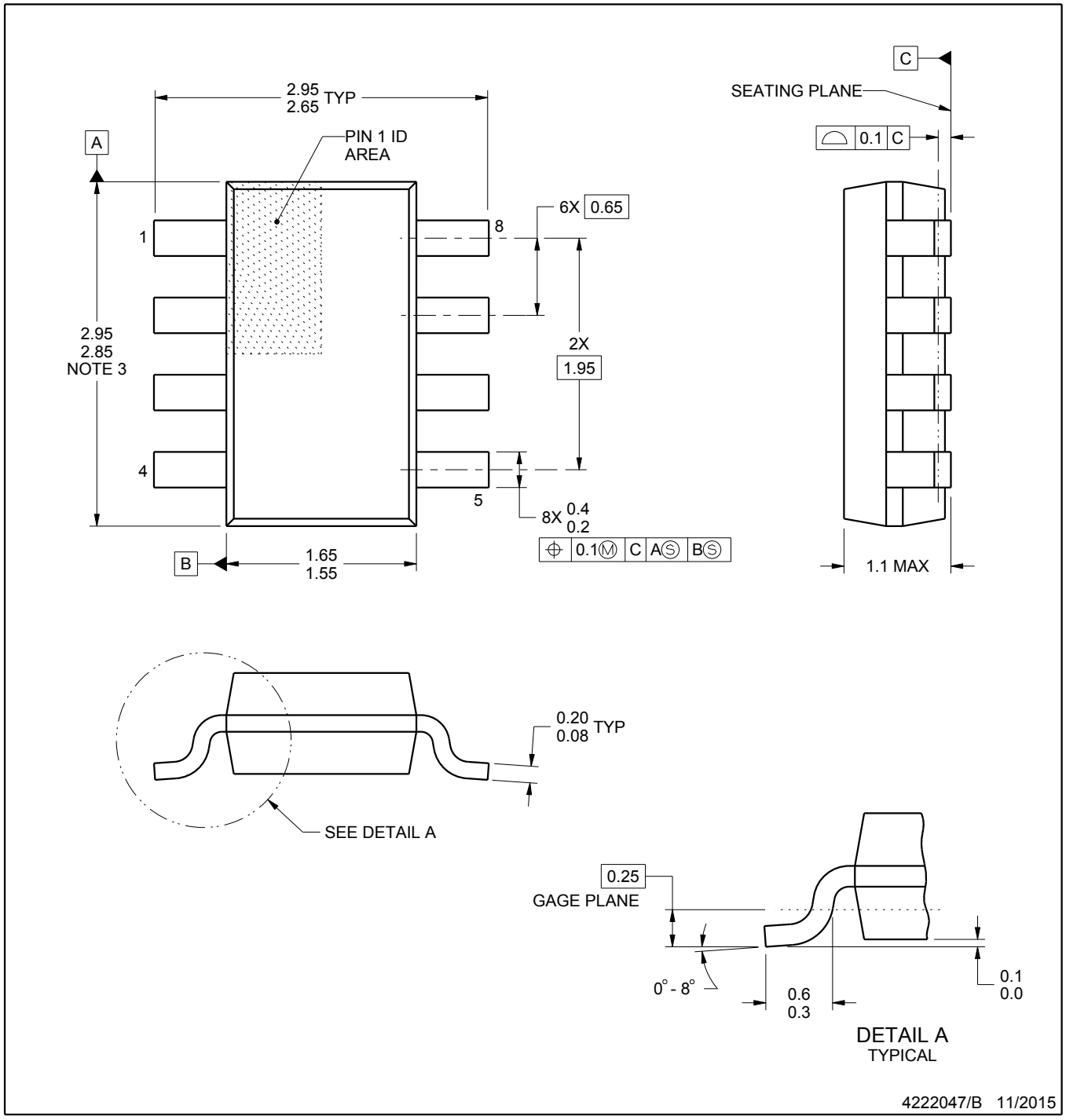
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

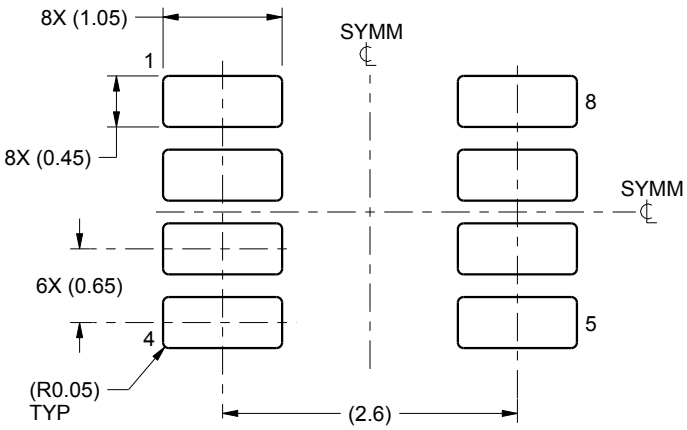
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

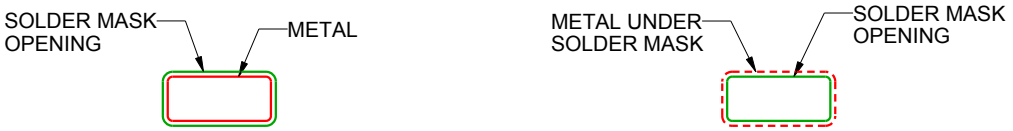


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

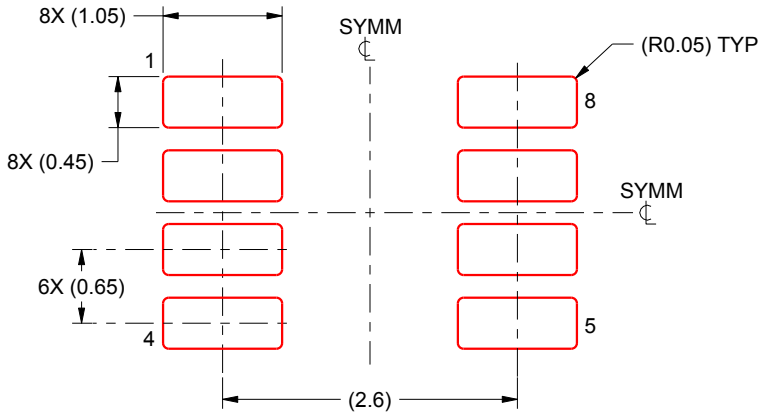
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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