TLV4011 Precision Comparator with Integrated Reference

1 Features

- Adjustable thresholds down to 1.226 V
- Precision ±1.5% threshold voltage accuracy
- Supply current: 3 μA
- Open-drain output
- Temperature range: –40°C to 85°C
- 5-Pin SC-70 package

2 Applications

- Electricity meters
- Circuit breakers
- Thermostats
- Cordless power tools

3 Description

The TLV4011 is a low-power, high-accuracy comparator with a precision, integrated reference. Two external resistors can be connected to the input to create an adjustable voltage threshold down to 1.226 V.

The factory-trimmed switching threshold and precision hysteresis combine to make the TLV4011 appropriate for voltage and current monitoring in harsh, noisy environments where slow moving input signals must be converted into clean digital outputs. Similarly, brief glitches on the input are rejected thereby ensuring stable output operation without false triggering.

During power on, $\overline{\text{RESET}}$ is asserted (LOW) when the supply voltage V_{DD} becomes higher than 0.8 V. Thereafter, the TLV4011 monitors the input and keeps $\overline{\text{RESET}}$ active (LOW) while the input remains below the threshold voltage V_{IT}. As soon as the input rises above the threshold voltage V_{IT}, $\overline{\text{RESET}}$ is de-asserted (HIGH). The product spectrum is designed for 1.8-V, 3.3-V, 5-V, and adjustable supply voltages.

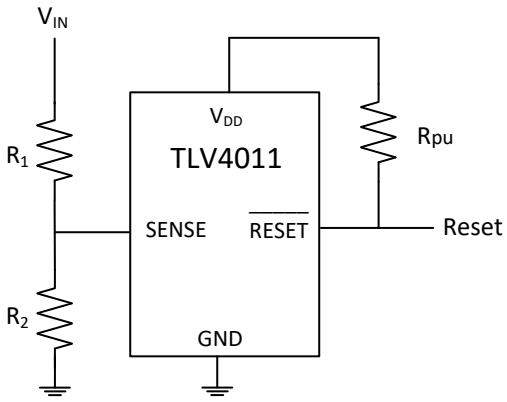
The TLV4011 is available in a 5-pin SC-70 package and are characterized for operation over a temperature range of –40°C to 85°C.

Device Information[1]

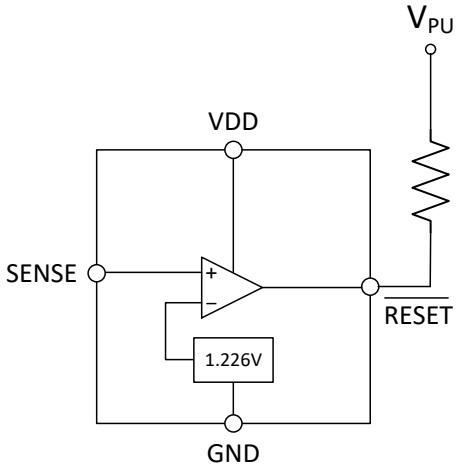
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV4011	SC-70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Block Diagram



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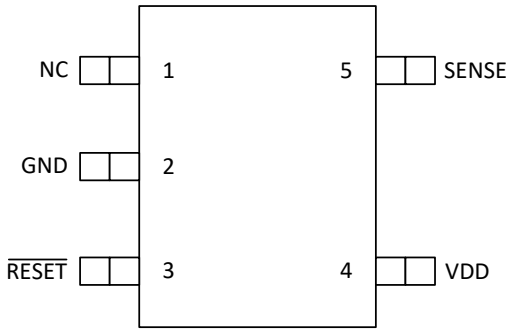
4 Revision History

DATE	REVISION	NOTES
March 2020	*	Initial release

5 Pin Configuration and Functions

DCK Package
5-Pin SC-70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	I	Ground
$\overline{\text{RESET}}$	3	O	Active-low reset output (open-drain)
SENSE	5	I	Input
NC	1	—	No internal connection
V_{DD}	4	I	Input supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage(2)		–0.3	7	V
	Voltage applied to all other pins(2)		–0.3	7	V
I_{OL}	Maximum low-level output current			5	mA
I_{OH}	Maximum high-level output current			–5	mA
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$		±10	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$		±10	mA
P_D	Continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature		–40	85	°C
T_{solder}	Soldering temperature			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device should not be continuously operated at 7 V for more than t = 1000 h.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	1.3	6	V
V_I	Input voltage	0	V_{DD} + 0.3	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV4011 DCK (SC-70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	246.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 1.5 V, I_{OL} = 1 mA				V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.3	
			V_{DD} = 6 V, I_{OL} = 3 mA				
V_{POR}	Power-up reset voltage(1)		VOL(max) = 0.2 V, IOL = 50 µA, T_A = 25°C	0.8			V
V_{IT}	Negative-going input threshold voltage(2)	SENSE		1.2	1.226	1.244	V
V_{hys}	Hysteresis		T_A = 25°C		15		mV
I_I	Input current	SENSE		–25		25	nA
I_{OH}	High-level output current at $\overline{\text{RESET}}$	$\overline{\text{RESET}}$	SENSE = V_{IT} + 0.2 V, V_{OH} = V_{DD}			300	nA
I_{DD}	Supply current		V_{DD} = 3.3 V, Output unconnected		2	4	µA
			V_{DD} = 6 V, Output unconnected		2	4	
C_I	Input capacitance		V_I = 0 V to V_{DD}		1		pF

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ (V_{OL}(max) = 0.2 V, I_{OL} = 50 µA) becomes active. $t_r(V_{DD})$ ≥ 15 µs/V.
(2) To ensure the best stability of the threshold voltage, place a bypass capacitor (ceramic, 0.1-µF) near the supply terminals.

6.6 Timing Requirements

R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C (unless otherwise noted)

				MIN	MAX	UNIT
t_w	Pulse duration	SENSE	V_{IH} = 1.05 × V_{IT}, V_{IL} = 0.95 × V_{IT}	5.5		µs

6.7 Switching Characteristics

R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation (delay) time, high-to-low-level output	SENSE to $\overline{\text{RESET}}$ delay	V_{IH} = 1.05 × V_{IT}, V_{IL} = 0.95 × V_{IT}		5	100	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	SENSE to $\overline{\text{RESET}}$ delay	V_{IH} = 1.05 × V_{IT}, V_{IL} = 0.95 × V_{IT}		5	100	µs

6.8 Dissipation Ratings

PACKAGE	POWER RATING T_A < 25°C	DERATING FACTOR ABOVE T_A = 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
DCK	321 mW	2.6 mW/°C	206 mW	167 mW

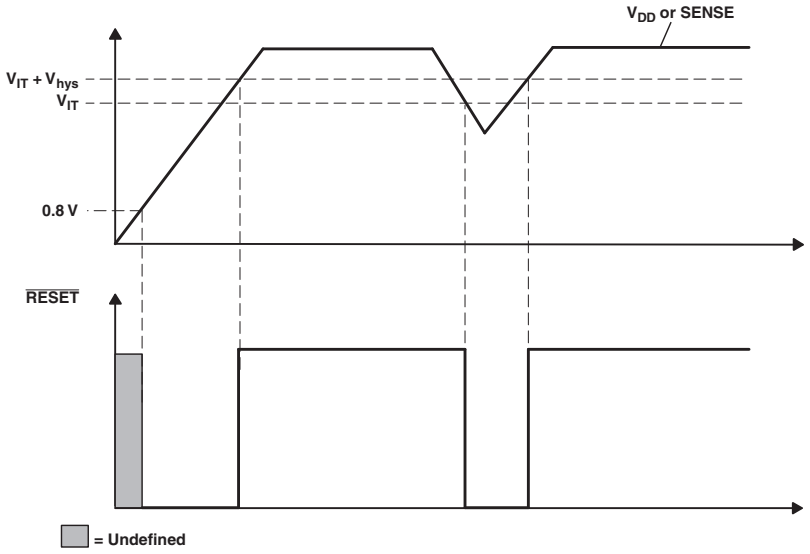


Figure 1. Timing Requirements

6.9 Typical Characteristics

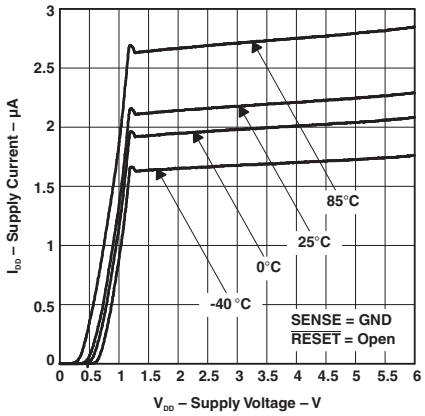


Figure 2. Supply Current vs Supply Voltage

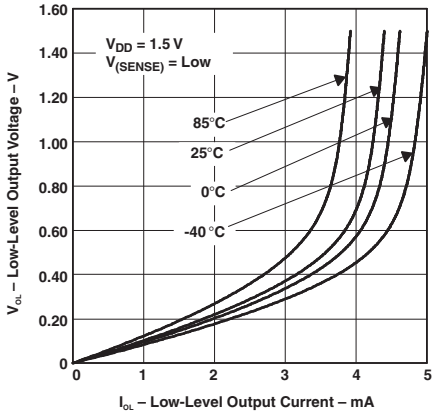


Figure 3. Low-Level Output Voltage vs Low-Level Output Current

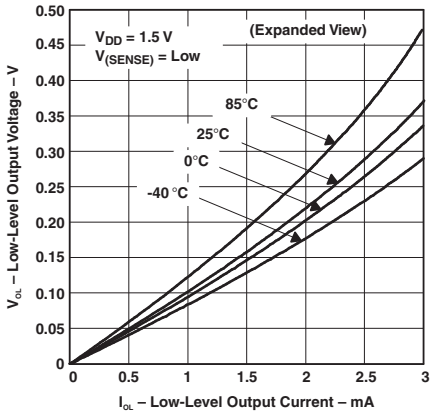


Figure 4. Low-Level Output Voltage vs Low-Level Output Current

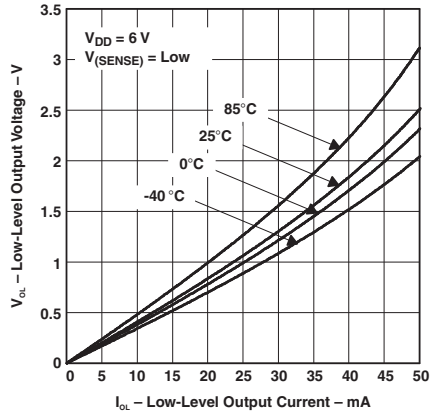


Figure 5. Low-Level Output Voltage vs Low-Level Output Current

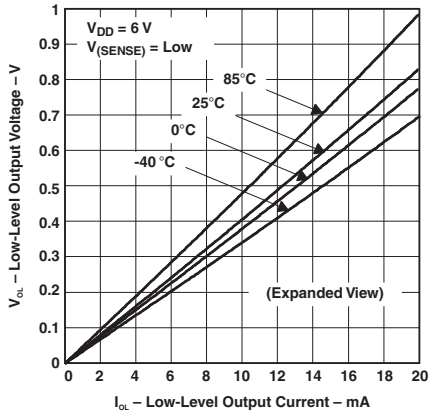


Figure 6. Low-Level Output Voltage vs Low-Level Output Current

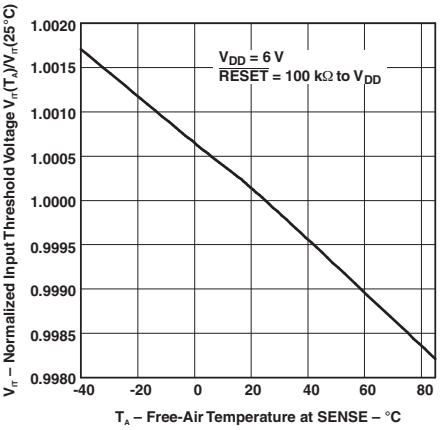


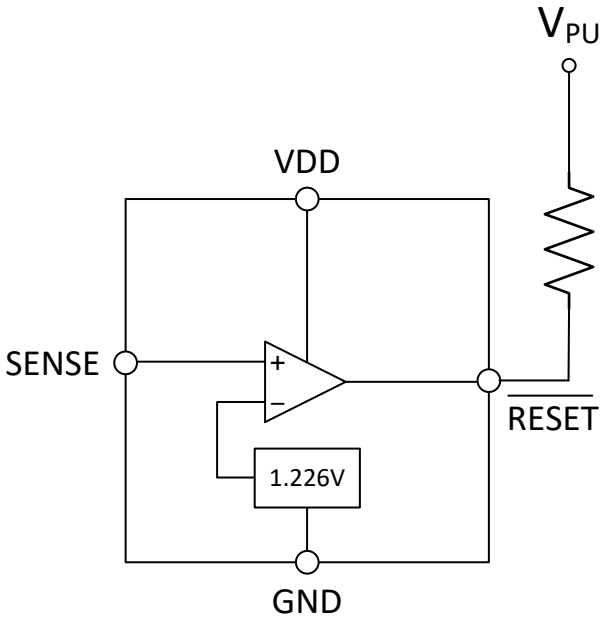
Figure 7. Normalized Input Threshold Voltage vs Free-Air Temperature At Sense

7 Detailed Description

7.1 Overview

The TLV4011 is a low-current comparator used to monitor system voltages above 1.226 V. The comparators assert an active low $\overline{\text{RESET}}$ signal when the SENSE voltages drop below VIT. The $\overline{\text{RESET}}$ output remains low until the SENSE voltage returns above VIT plus the integrated hysteresis level. The TLV4011 is also designed to be immune to short negative transients on the SENSE pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 SENSE Monitoring

The SENSE input is where a system voltage can be monitored. If the voltage on this pin drops below V_{IT}, $\overline{\text{RESET}}$ is asserted low. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and de-assertions. By connecting a resistor divider network to the SENSE input as shown in the circuit below, VIN is divided down so $\overline{\text{RESET}}$ will assert when the divided down value of VIN reaches VIT (1.226 V). The TLV4011 is capable of monitoring any input voltage down to 1.226 V.

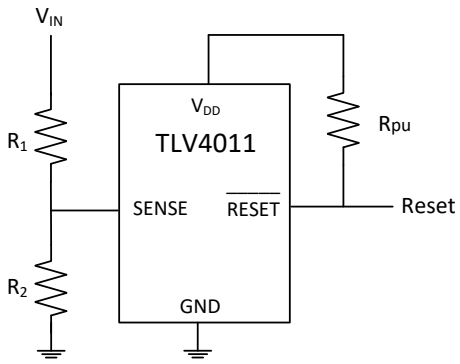


Figure 8. Voltage Monitor

Feature Description (continued)

7.3.2 Transient Immunity

The TLV4011 is immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive as shown in Figure 9 and Figure 10. These graphs show the duration that the transient is below V_{IT} compared to the magnitude of the voltage drop below V_{IT}, called the threshold overdrive voltage. Any combination of transient duration and overdrive voltage which lies above the curves will result in $\overline{\text{RESET}}$ being asserted low. Any transient which lies below the curves will be ignored by the device.

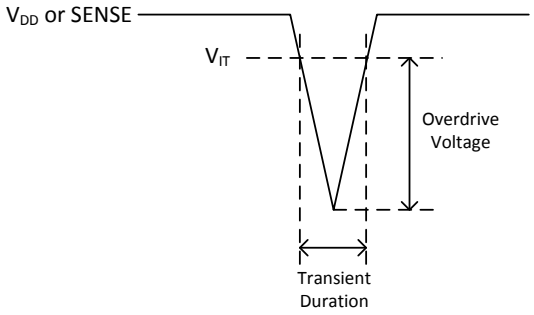


Figure 9. SENSE Overdrive Voltage

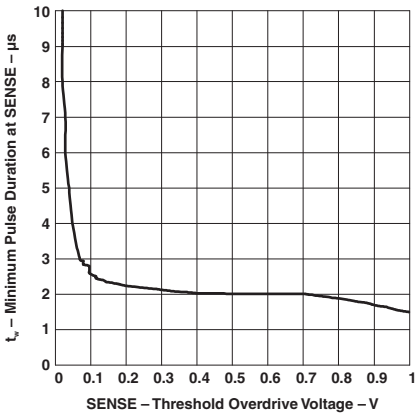


Figure 10. Minimum Pulse Duration at Sense vs Sense Threshold Overdrive Voltage

7.4 Device Functional Modes

The SENSE input is used to monitor one supply. When that supply is above the V_{IT} threshold, $\overline{\text{RESET}}$ will be high. Otherwise, $\overline{\text{RESET}}$ will be low.

Table 1. Function and Truth Table

TLV4011	
SENSE > V_{IT}	**$\overline{\text{RESET}}$**
0 (False)	L
1 (True)	H

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV4011 comparator is designed to assert an active-low $\overline{\text{RESET}}$ signal when the SENSE input drops below the voltage threshold V_{IT}. The $\overline{\text{RESET}}$ signal remains low until the voltages return above their respective threshold plus the hysteresis. If additional hysteresis is required, positive feedback can be implemented similar to how it is done on a discrete comparator. See Application Note for details on how to implement external hysteresis in a non-inverting configuration.

8.2 Typical Application

8.2.1 Under-Voltage Detection

Under-voltage detection is frequently required in battery-powered, portable electronics to alert the system that a battery voltage has dropped below the usable voltage level. Figure 11 shows a simple under-voltage detection circuit using the TLV4011 which is a non-inverting comparator with an integrated 1.226 V reference and an open-drain output stage. A non-inverting is well suited for this application since the micro-controller requires an active low signal when an undervoltage level occurs.

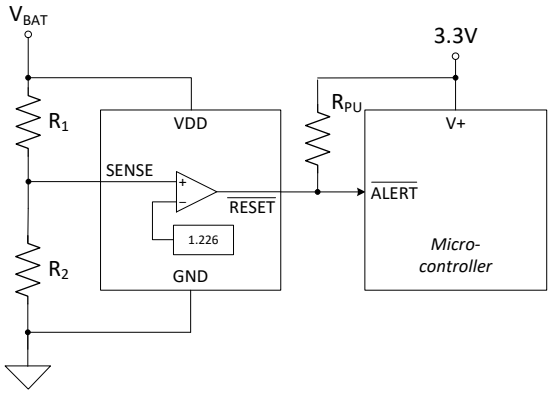


Figure 11. Under-Voltage Detection

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- TLV4011 operates from the V_{BAT} directly
- Output is level-shifted to the 3.3 V power supply that powers the microcontroller.
- Under-voltage alert is active low.
- Logic low output when V_{BAT} decreases below 2.0V.

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 11. Note that VDD of the comparator is connected directly to V_{BAT} (the battery being monitored) and the output of the comparator is level shifted with its open-drain ouput to 3.3 V which powers the micro-controller. Resistors R_1 and R_2 divide down V_{BAT} so that the resistor divided output equals 1.226 V when V_{BAT} reaches an under-voltage alert level of 2.0 V.

Typical Application (continued)

When the battery voltage sags down to 2.0 V, the resistor divider voltage crosses the (V_{IT} = 1.226 V) threshold of the TLV4011. This causes the comparator output to transition from a logic high to a logic low. An open-drainj comparator is selected so the comparator output is compatible with the input logic level of the microcontroller. In addition, selecting a comparator with an integrated reference value of 1.226 V is favorable because it is the closest internal reference option that is less than the critical under-voltage level of 2.0 V. Choosing the internal reference option that is closest to the critical under-voltage level minimizes the resistor divider ratio which optimizes the accuracy of the circuit. Error at the falling edge threshold of (V_{IT}) is amplified by the inverse of the resistor divider ratio. So minimizing the resistor divider ratio is a way of optimizing voltage monitoring accuracy.

Equation 1 is derived from the analysis of Figure 11.

$$V_{IT} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \quad (1)$$

where

- R_1 and R_2 are the resistor values for the resistor divider connected to SENSE
- V_{BAT} is the voltage source that is being monitored for an undervoltage condition.
- V_{IT} is the falling edge threshold where the comparator output changes state from high to low

Rearranging Equation 1 and solving for R_1 yields Equation 2.

$$R_1 = \frac{(V_{BAT} - V_{IT})}{V_{IT}} \times R_2 \quad (2)$$

For the specific undervoltage detection of 2.0 V using the TLV4011, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.226)}{1.226} \times 1M = 631\ k\Omega \quad (3)$$

where

- R_2 is set to 1 MΩ
- V_{BAT} is set to 2.0 V
- V_{IT} is set to1.226 V

Choose R_{TOTAL} (R_1 + R_2) such that the current through the divider is at approximately 100 times higher than the input bias current (I_{BIAS}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

8.2.1.3 Application Curve

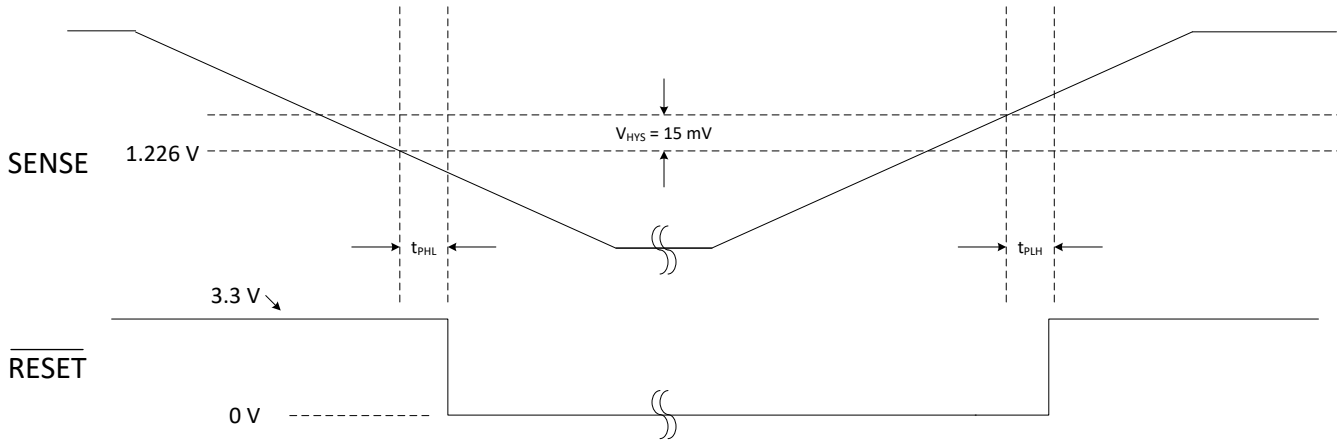


Figure 12. Under-Voltage Detection

Typical Application (continued)

8.2.2 Additional Application Information

8.2.2.1 Pull-up Resistor Selection

Since the TLV4011 has an open drain output, care should be taken in selecting the pull-up resistor (R_{PU}) value to ensure proper output voltage levels. First, consider the required output high logic level requirement of the logic device that is being driven by the comparator when calculating the maximum R_{PU} value. When in a logic high output state, the output impedance of the comparator is very high but there is a finite amount of leakage current that needs to be accounted for. Use I_{OH} from the EC Table and the V_{IH} minimum from the logic device being driven to determine R_{PU} maximum using Equation 4.

$$R_{PU}(max) = \frac{\left(V_{PU} - V_{IH(min)}\right)}{I_{OH}} \tag{4}$$

Next, determine the minimum value for R_{PU} by using the V_{IL} maximum from the logic device being driven. In order for the comparator output to be recognized as a logic low, V_{IL} maximum is used to determine the upper boundary of the comparator's V_{OL}. V_{OL} maximum for the comparator is available in the EC Table for specific sink current levels and can also be found from the V_{OUT} versus I_{SINK} curve in the Typical Application curves. A good design practice is to choose a value for V_{OL} maximum that is 1/2 the value of V_{IL} maximum for the input logic device. The corresponding sink current and V_{OL} maximum value will be needed to calculate the minimum R_{PU}. This method will ensure enough noise margin for the logic low level. With V_{OL} maximum determined and the corresponding I_{SINK} obtained, the minimum R_{PU} value is calculated with Equation 5.

$$R_{PU}(min) = \frac{\left(V_{PU} - V_{OL(max)}\right)}{I_{SINK}} \tag{5}$$

Since the range of possible R_{PU} values is large, a value between 5 kΩ and 100 kΩ is generally recommended. A smaller R_{PU} value provides faster output transition time and better noise immunity, while a larger R_{PU} value consumes less power when in a logic low output state.

8.2.2.2 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 100 nF low equivalent series resistance (ESR) capacitor from (VDD) to (GND).

8.2.2.3 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor from the comparator input (SENSE) to the (GND) for good analog design practice. This capacitor placement reduces device sensitivity to transients.

9 Power Supply Recommendations

The TLV4011 comparator is designed to operate from an input supply from 1.3 V to 6 V. It is recommended to place a 0.1-µF capacitor from the VDD pin to GND.

10 Layout

10.1 Layout Guidelines

TI recommends to place the 0.1-µF decoupling capacitor close to the VDD pin. The VDD trace should be able to carry 6 µA without a significant drop in voltage. Avoid a long trace from the SENSE pin to the resistor divider.

10.2 Layout Examples

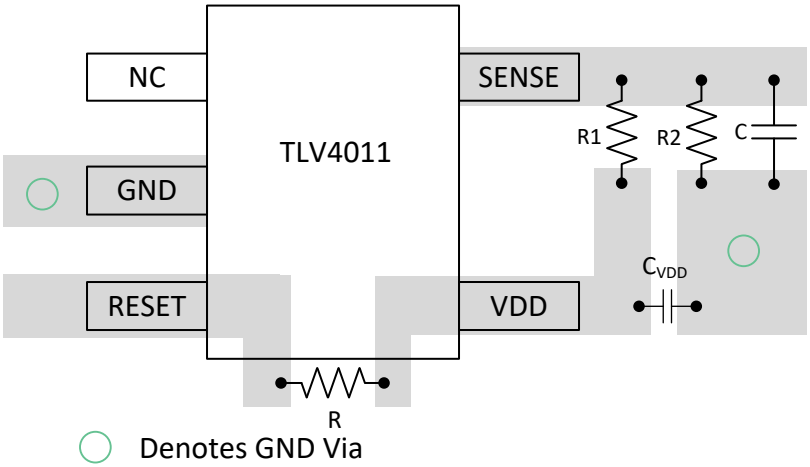


Figure 13. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV4011DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1HK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

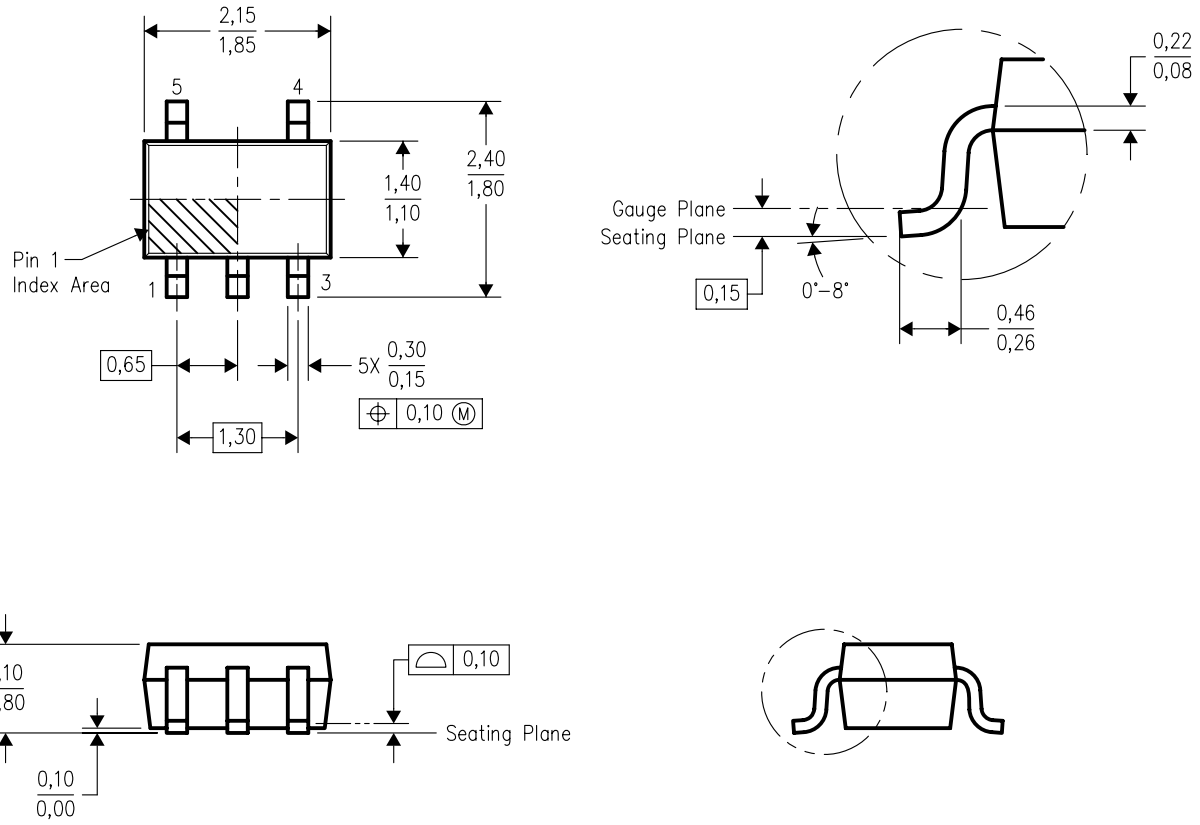
OTHER QUALIFIED VERSIONS OF TLV4011 :

- Automotive: TLV4011-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

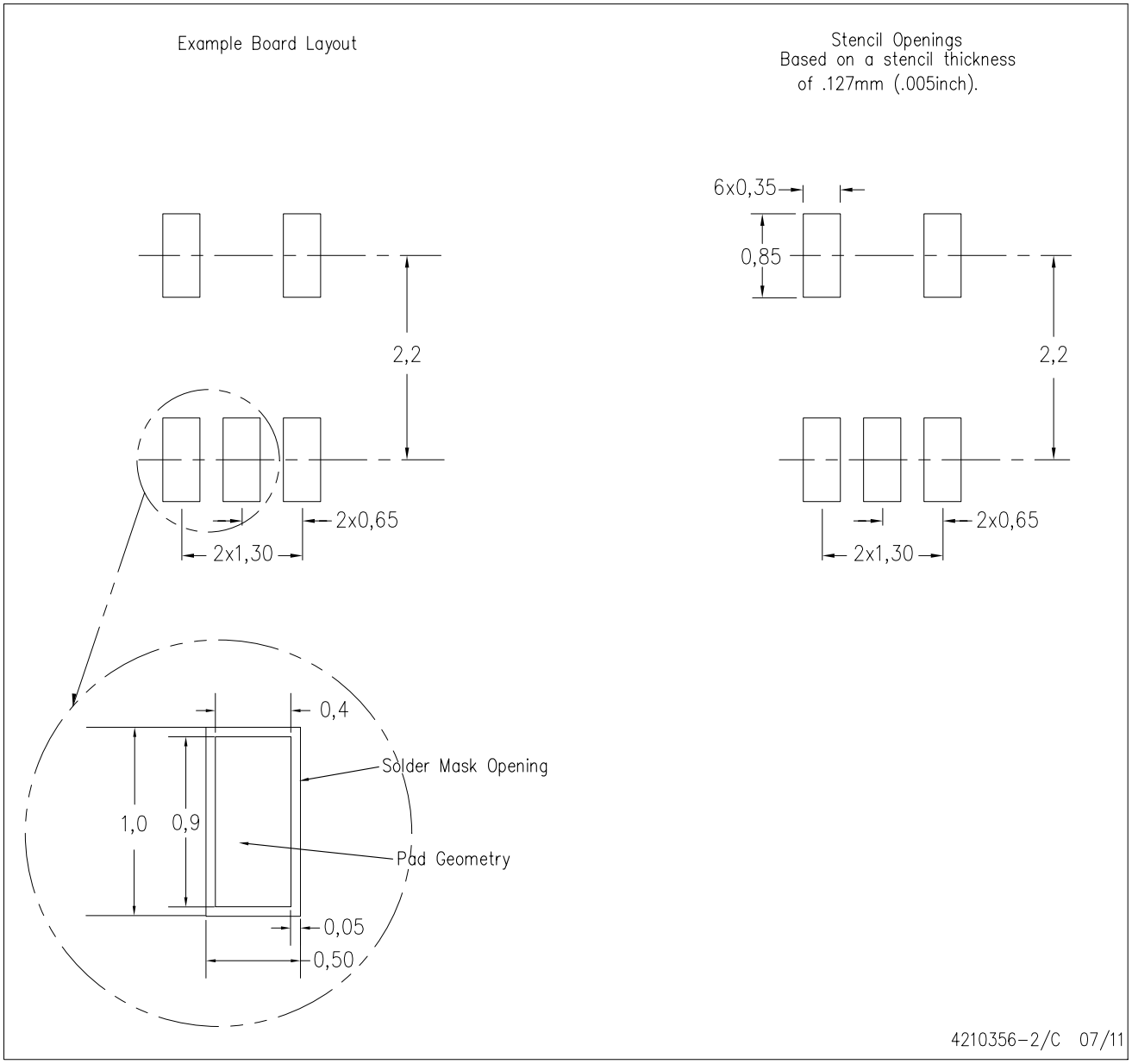
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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