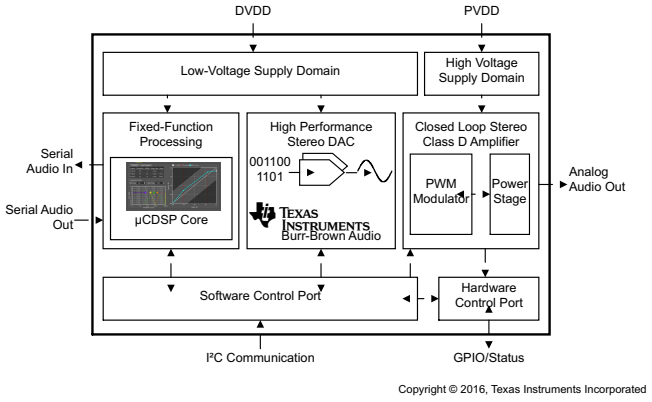
TAS5780M 采用 96kHz 处理架构的数字输入、闭环 D 类放大器

1 特性

- 灵活的音频 I/O 配置
  - 支持 I²S、TDM、LJ 和 RJ 数字输入
  - 支持采样速率
  - 立体声桥接负载 (BTL) 或单声道并行桥接负载 (PBTL) 运行
  - 1SPW 放大器调制
  - 支持三线制数字音频接口（无需 MCLK）
- 高性能闭环架构（PVDD = 12V，R_{SPK} = 8Ω，SPK_GAIN = 20dB）
  - 空闲声道噪声 = 62μVRMS (A-Wtd)
  - 总谐波失真 + 噪声 (THD+N) = 0.2% (1W/1kHz)
  - 信噪比 (SNR) = 100dB A-Wtd（以THD+N = 1% 为基准）
- 固定功能处理 特性
  - 12 个 BiQuad
    - 12 个 BiQuad 实现快速变换的内部存储区切换
  - 双波段高级动态范围压缩 (DRC) + 自动增益限制 (AGL)
  - 动态参数均衡 (DPEQ)
  - 采样速率转换器 (SRC) 支持的频率包括 32kHz、44.1kHz、48kHz、88.2kHz、96kHz
  - 96kHz 处理器采样
- 通信 特性
  - 通过 I²C 端口实现软件模式控制
  - 两个地址选择引脚 – 多达 4 个器件
- 兼具稳定性 和可靠性
  - 时钟误差和短路保护
  - 过热和过流保护

简化框图



2 应用

- 液晶显示屏 (LCD)、发光二极管 (LED) TV 和多用途监视器
- 条形音箱、扩展坞和 PC 音频
- 无线低音炮、蓝牙扬声器和有源扬声器

3 说明

TAS5780M 器件是一款高性能、立体声闭环 D 类放大器，集成采用 96kHz 架构的音频处理器。为实现数模转换，该器件采用了应用 Burr-Brown™技术的高性能数模转换器 (DAC) 该器件仅需两个电源：一个是用于低压电路的 DVDD，另一个是用于高压电路的 PVDD。它采用标准的 I²C 通信软件控制端口实现控制。

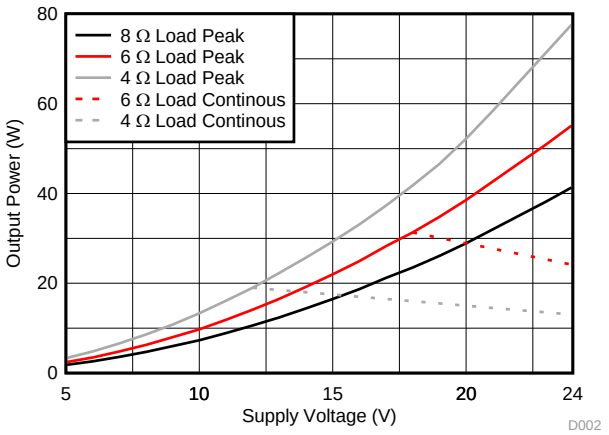
输出金属氧化物半导体场效应晶体管 (MOSFET) 的 90mΩ $r_{DS(on)}$ 兼顾散热性能与器件成本，二者相得益彰。此外，该器件采用耐热增强型 48 引脚薄型小外形尺寸 (TSSOP)，在现代消费类电子器件的较高工作环境温度下展现出优异的性能。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TAS5780M	TSSOP (48)	12.50mm x 6.10mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

10% THD+N 时的功率与 PVDD 间的关系 (1)



(1) 在 TAS5780MEVM 电路板中进行了测试。

目录

4 修订历史记录

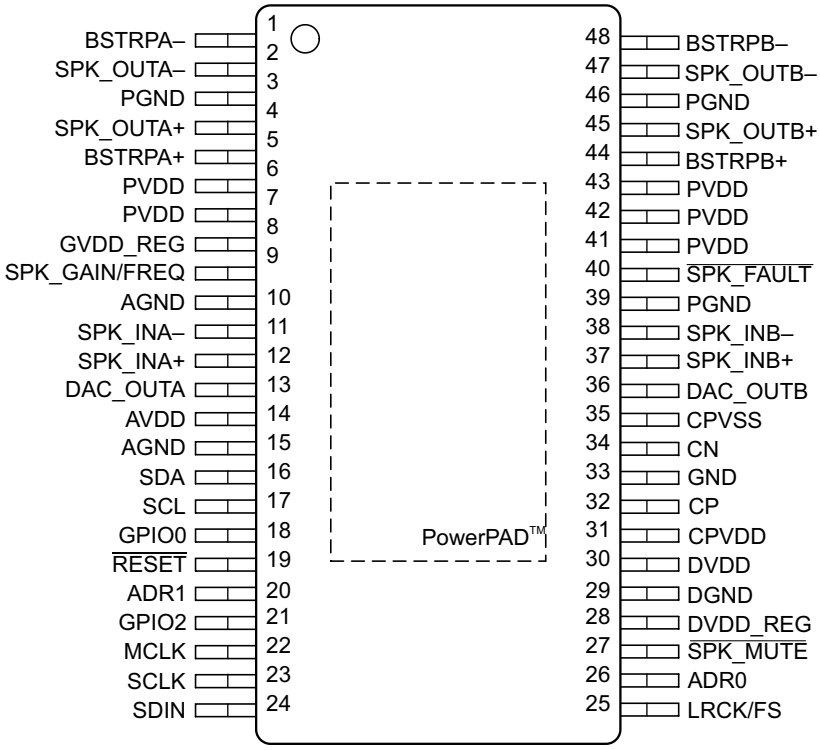
日期	修订版本	注释
2016 年 12 月	*	最初发布。

5 Device Comparison Table

DEVICE NAME	MODULATION STYLE	PROCESSING TYPE
TAS5780MDCA	1SPW (Ternary)	100 MIPs, Fixed-Function (Uses single ROM image of process flow)
TAS5754MDCA	1SPW (Ternary)	50 MIPs, HybridFlow (Uses mixture of RAM and ROM components to create several process flows)
TAS5756MDCA	BD Modulation	50 MIPs, HybridFlow (Uses mixture of RAM and ROM components to create several process flows)

6 Pin Configuration and Functions

DCA Package
48-Pin TSSOP with PowerPAD™
Top View



Pin Functions

PIN		TYPE(1)	INTERNAL TERMINATION	DESCRIPTION
NAME	NO.			
ADR0	26	DI		Sets the LSB of the I^2C address to 0 if pulled to GND, to 1 if pulled to DVDD
ADR1	20	DI		Sets the second LSB of the I^2C address to 0 if pulled to GND, to 1 if pulled to DVDD
AGND	10	G	—	Ground reference for analog circuitry(2)
	15			
AVDD	14	P	Figure 2	Power supply for internal analog circuitry

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0 V)
(2) This pin should be connected to the system ground.

Pin Functions (continued)

PIN		TYPE(1)	INTERNAL TERMINATION	DESCRIPTION
NAME	NO.			
BSTRPA–	1	P	Figure 3	Connection point for the SPK_OUTA– bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTA–
BSTRPA+	5	P		Connection point for the SPK_OUTA+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTA+
BSTRPB–	48	P		Connection point for the SPK_OUTB– bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTB–
BSTRPB+	44	P		Connection point for the SPK_OUTB+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTB+
CN	34	P	Figure 14	Negative pin for capacitor connection used in the line-driver charge pump
CP	32	P	Figure 13	Positive pin for capacitor connection used in the line-driver charge pump
CPVDD	31	P	Figure 2	Power supply for charge pump circuitry
CPVSS	35	P	Figure 14	–3.3-V supply generated by charge pump for the DAC
DAC_OUTA	13	AO	Figure 8	Single-ended output for Channel A of the DAC
DAC_OUTB	36	AO		Single-ended output for Channel B of the DAC
DGND	29	G	—	Ground reference for digital circuitry. Connect this pin to the system ground.
DVDD	30	P	Figure 2	Power supply for the internal digital circuitry
DVDD_REG	28	P	Figure 15	Voltage regulator derived from DVDD supply for use for internal digital circuitry. This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.
GND	33	G	—	Ground pin for device. This pin should be connected to the system ground.
GPIO0	18	DI/O		General purpose input/output pins (GPIOx). Refer to GPIO registers for configuration.
GPIO2	21			
GVDD_REG	8	P	Figure 5	Voltage regulator derived from PVDD supply to generate the voltage required for the gate drive of output MOSFETs. This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.
LRCK/FS	25	DI/O	Figure 11	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ, and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
MCLK	22	DI		Master clock used for internal clock tree and sub-circuit and state machine clocking
PGND	3	G	—	Ground reference for power device circuitry. Connect this pin to the system ground.
	39			
	46			
PVDD	6	P	Figure 1	Power supply for internal power circuitry
	7			
	41			
	42			
	43			
$\overline{\text{RESET}}$	19	DI	Figure 17	Device reset input. Pull down to reset, pull up to activate device.
SCL	17	DI	Figure 10	I^2C serial control port clock
SCLK	23	DI/O	Figure 11	Bit clock for the digital signal that is active on the input data line of the serial data port
SDA	16	DI/O	Figure 9	I^2C serial control port data
SDIN	24	D1	Figure 11	Data line to the serial data port
SPK_INA–	11	AI	Figure 7	Negative pin for differential speaker amplifier input A
SPK_INA+	12	AI		Positive pin for differential speaker amplifier input A
SPK_INB–	38	AI		Negative pin for differential speaker amplifier input B
SPK_INB+	37	AI		Positive pin for differential speaker amplifier input B
$\overline{\text{SPK\_FAULT}}$	40	DO	Figure 16	Fault pin which is pulled low when an overcurrent or overtemperature fault occurs
SPK_GAIN/FREQ	9	AI	Figure 6	Sets the gain and switching frequency of the speaker amplifier, latched in upon start-up of the device.
SPK_OUTA–	2	AO	Figure 4	Negative pin for differential speaker amplifier output A
SPK_OUTA+	4	AO		Positive pin for differential speaker amplifier output A
SPK_OUTB–	47	AO		Negative pin for differential speaker amplifier output B
SPK_OUTB+	45	AO		Positive pin for differential speaker amplifier output B

Pin Functions (continued)

PIN		TYPE(1)	INTERNAL TERMINATION	DESCRIPTION
NAME	NO.			
$\overline{\text{SPK\_MUTE}}$	27	I	Figure 12	Speaker amplifier mute which must be pulled low (connected to DGND) to mute the device and pulled high (connected to DVDD) to unmute the device.
PowerPAD	—	G	—	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it through solder. For proper electrical operation, this ground pad must be connected to the system ground.

6.1 Internal Pin Configurations

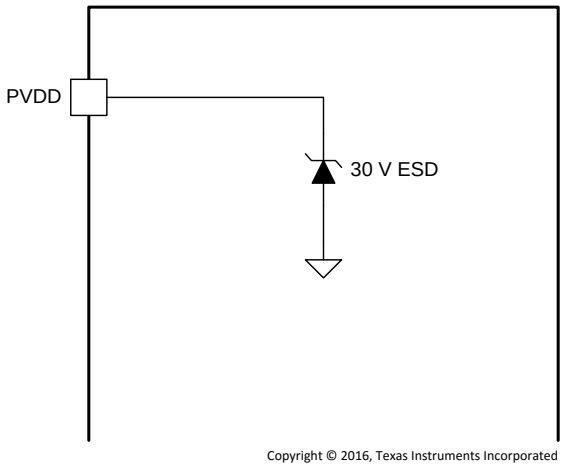


Figure 1. PVDD Pins

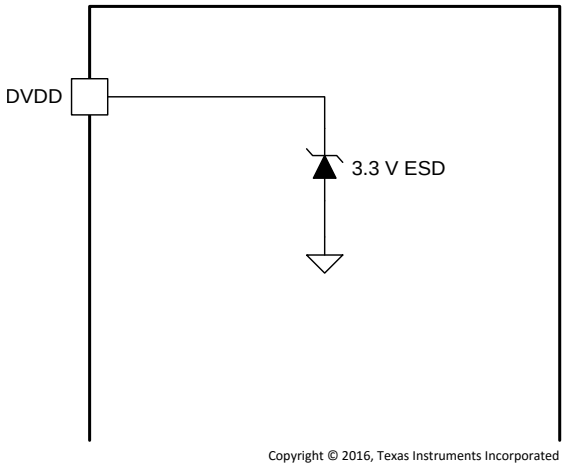


Figure 2. AVDD, DVDD and CPVDD Pins

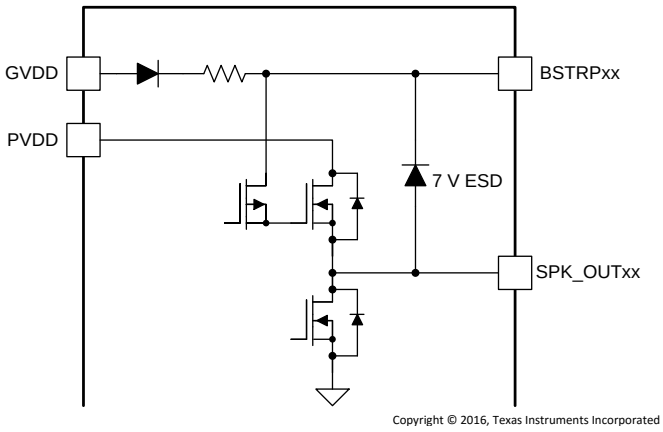


Figure 3. BSTRPxx Pins

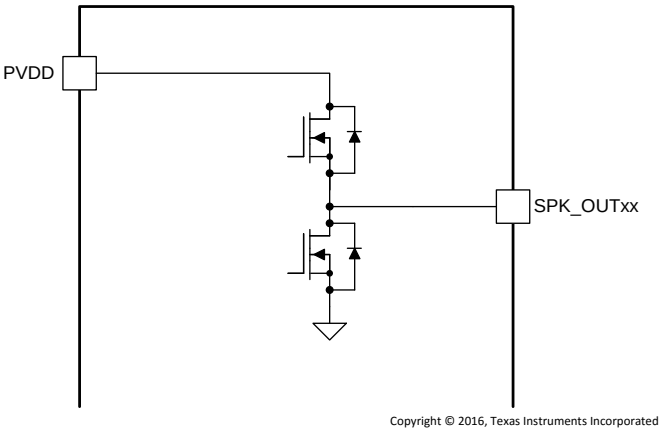


Figure 4. SPK_OUTxx Pins

Internal Pin Configurations (continued)

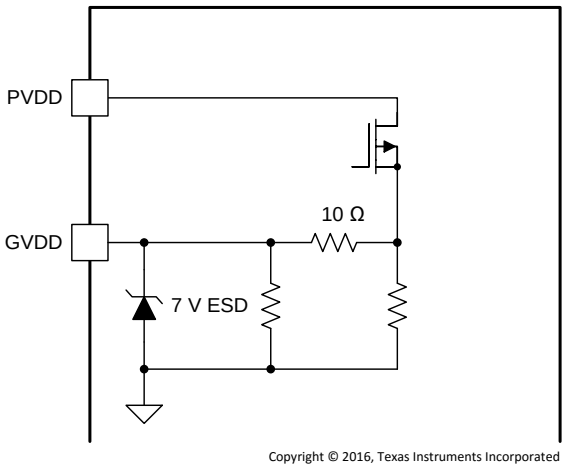


Figure 5. GVDD_REG Pin

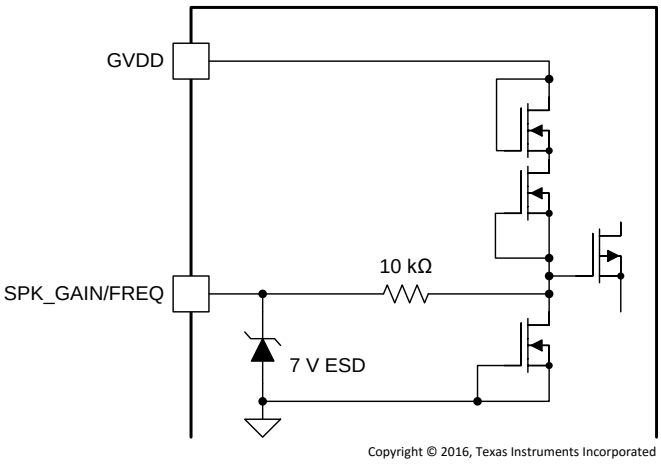


Figure 6. SPK_GAIN/FREQ Pin

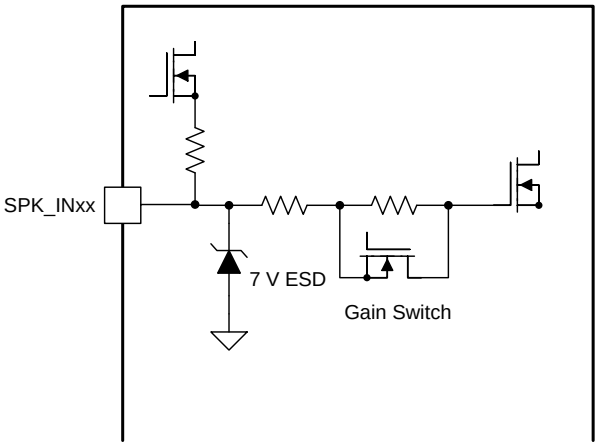


Figure 7. SPK_INxx Pins

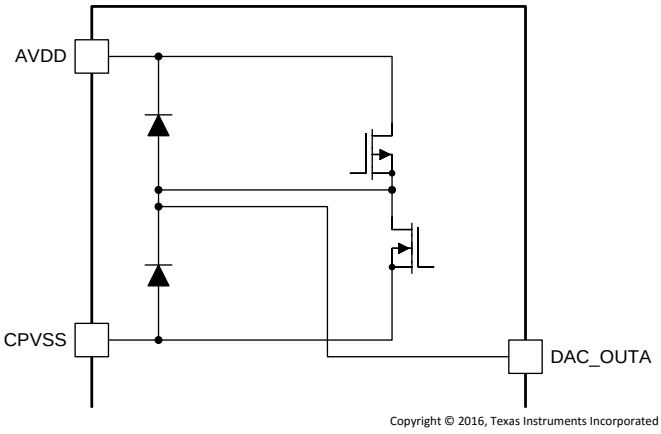


Figure 8. DAC_OUTx Pins

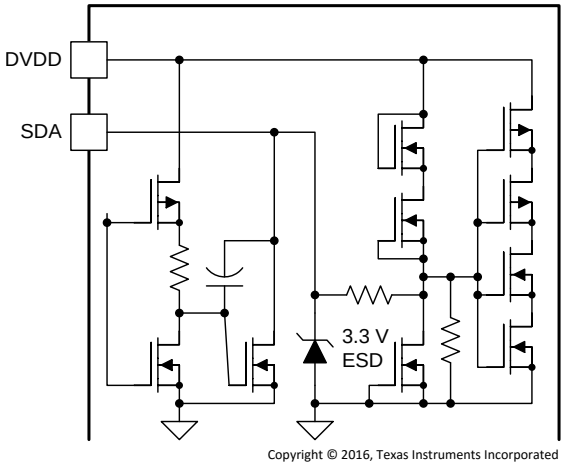


Figure 9. SDA Pin

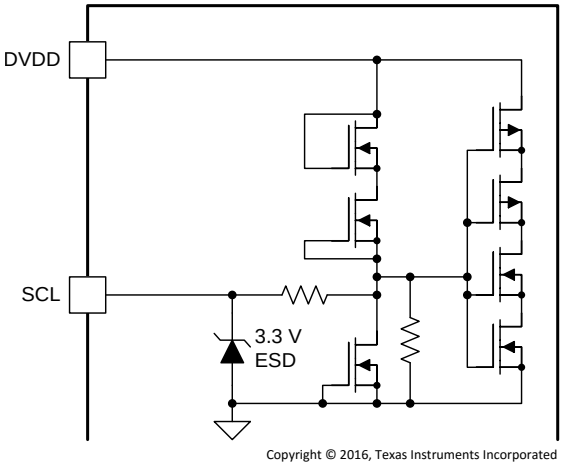


Figure 10. SCL Pin

Internal Pin Configurations (continued)

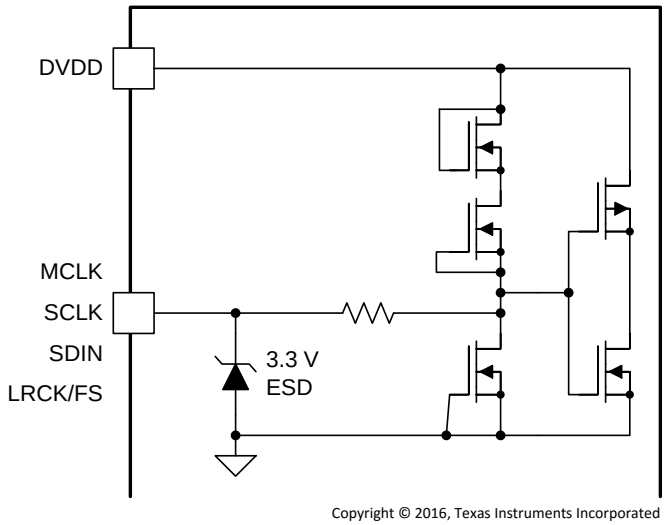


Figure 11. SCLK, BCLK, SDIN, and LRCK/FS Pins

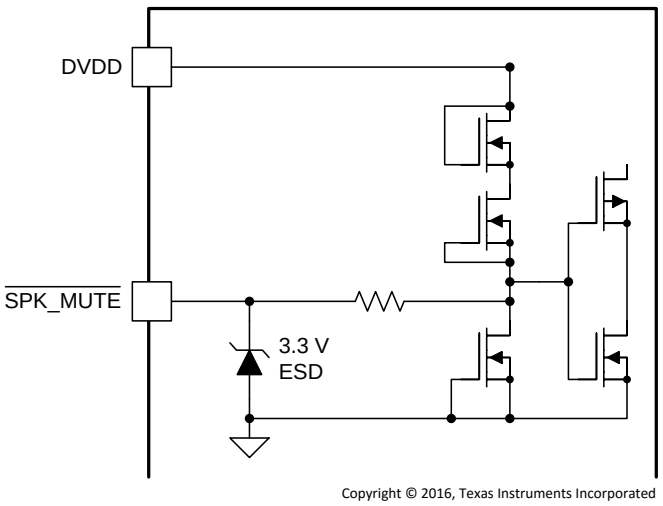


Figure 12. $\overline{\text{SPK\_MUTE}}$ Pin

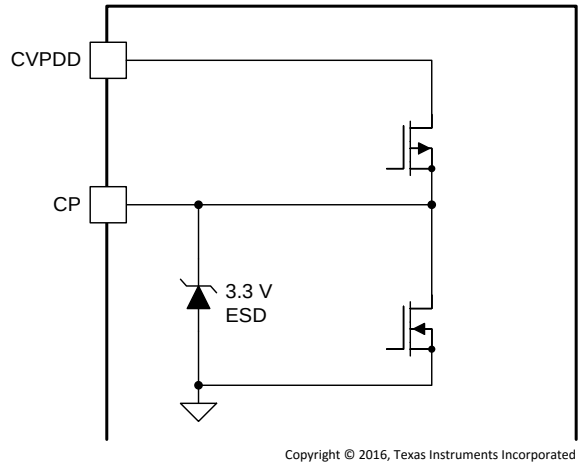


Figure 13. CP Pin

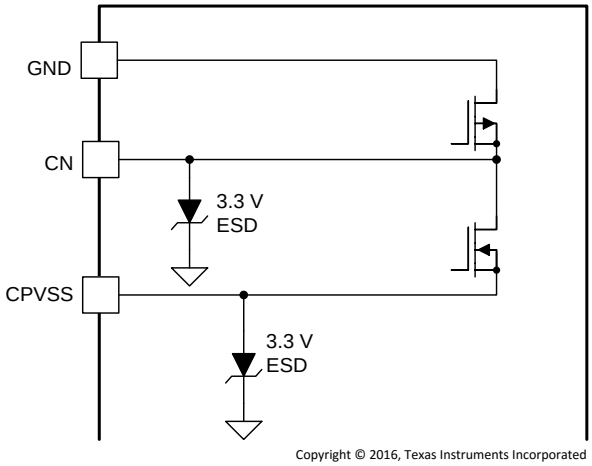


Figure 14. CN and CPVSS Pins

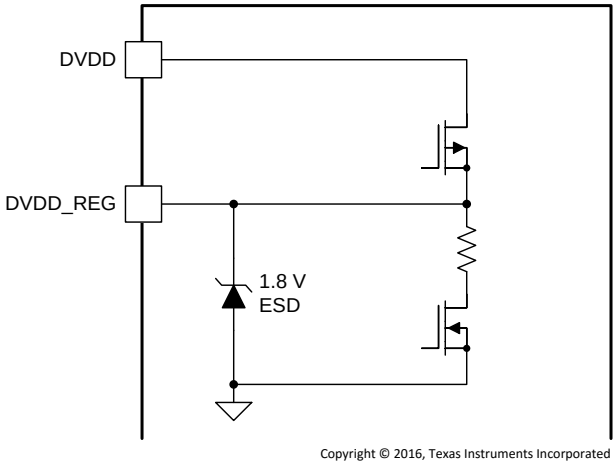


Figure 15. DVDD_REG Pin

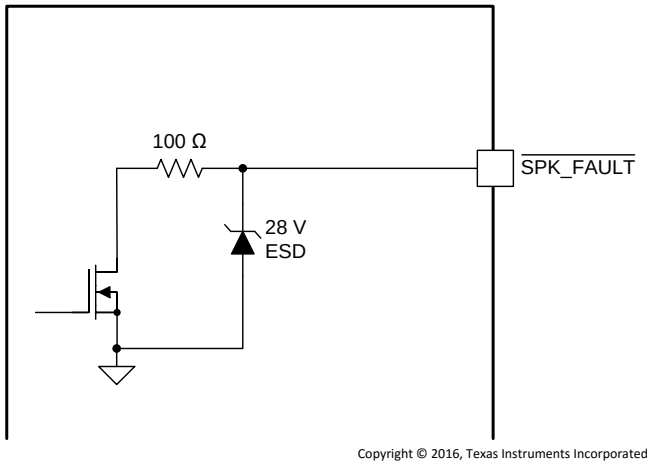


Figure 16. $\overline{\text{SPK\_FAULT}}$ Pin

Internal Pin Configurations (continued)

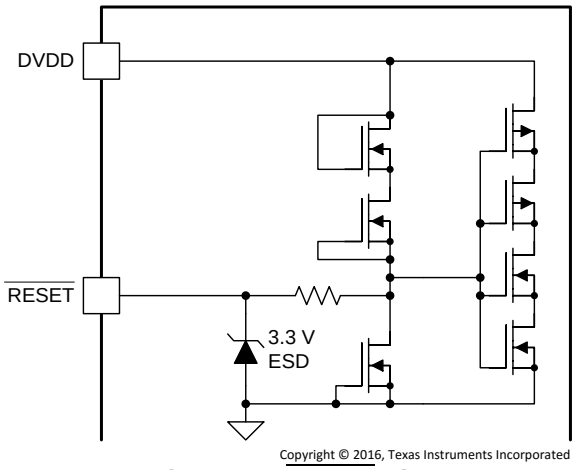


Figure 17. RESET Pin

7 Specifications

7.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
DVDD, AVDD, CPVDD	Low-voltage digital, analog, charge pump supply	–0.3	3.9	V
PVDD	PVDD supply	–0.3	30	V
$V_{I(AmpCtrl)}$	Input voltage for SPK_GAIN/FREQ and $\overline{SPK\_FAULT}$ pins	–0.3	V_{GVDD} + 0.3	V
$V_{I(DigIn)}$	DVDD referenced digital inputs(2)	–0.5	V_{DVDD} + 0.5	V
$V_{I(SPK\_INxx)}$	Analog input into speaker amplifier	–0.3	6.3	V
$V_{I(SPK\_OUTxx)}$	Voltage at speaker output pins	–0.3	32	V
	Ambient operating temperature, T_A	–25	85	°C
T_J	Operating junction temperature, digital die	–40	125	°C
	Operating junction temperature, power die	–40	165	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO2, LRCK/FS, MCLK, $\overline{RESET}$, SCL, SCLK, SDA, SDIN, and $\overline{SPK\_MUTE}$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Free-air room temperature 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	DVDD, AVDD, CPVDD	2.9		3.63	V
		PVDD	4.5		26.4	
R_{SPK}	Minimum speaker load	BTL Mode	3			Ω
		PBTL Mode	2			Ω
$V_{IH(DigIn)}$	Input logic high for DVDD referenced digital inputs(1)(2)		0.9 × V_{DVDD}		V_{DVDD}	V
$V_{IL(DigIn)}$	Input logic low for DVDD referenced digital inputs(1)(3)		V_{DVDD}	0	0.1 × V_{DVDD}	V
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1	4.7		µH

(1) DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO2, LRCK/FS, MCLK, $\overline{\text{RESET}}$, SCL, SCLK, SDA, SDIN, and $\overline{\text{SPK\_MUTE}}$.
(2) The best practice for driving the input pins of the TAS5780M device is to power the drive circuit or pullup resistor from the same supply which provides the DVDD power supply.
(3) The best practice for driving the input pins of the TAS5780M device low is to pull them down, either actively or through pulldown resistors to the system ground.

7.4 Thermal Information

THERMAL METRIC(1)		TAS5780M DCA (TSSOP) 48 PINS			UNIT
		JEDEC STANDARD 2-LAYER PCB	JEDEC STANDARD 4-LAYER PCB	TAS5780MEVM 4-LAYER PCB	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.8	27.6	19.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.4	14.4	14.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	9.4	9.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.6	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.1	9.3	4.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5780MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 40 kHz brickwall filter. The device output PWM frequency was set to 768 kHz unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL I/O						
|IIH|1	Input logic high current level for DVDD referenced digital input pins(1)	$V_{IN(DigIn)} = V_{DVDD}$			10	µA
|IIL|1	Input logic low current level for DVDD referenced digital input pins(1)	$V_{IN(DigIn)}$ = 0 V			–10	µA
V_{IH1}	Input logic high threshold for DVDD referenced digital inputs(1)		70%			V_{DVDD}
V_{IL1}	Input logic low threshold for DVDD referenced digital inputs(1)				30%	V_{DVDD}
$V_{OH(DigOut)}$	Output logic high voltage level(1)	I_{OH} = 4 mA	80%			V_{DVDD}
$V_{OL(DigOut)}$	Output logic low voltage level(1)	I_{OH} = –4 mA			22%	V_{DVDD}
$V_{OL(\overline{SPK\_FAULT})}$	Output logic low voltage level for $\overline{SPK\_FAULT}$	With 100-kΩ pullup resistor			0.8	V
GVDD_REG	GVDD regulator voltage			7		V
I²C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I²C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
V_{NH}	Noise margin at High level for each connected device (including hysteresis)		0.2 × V_{DD}			V
MCLK AND PLL SPECIFICATIONS						
D_{MCLK}	Allowable MCLK duty cycle		40%		60%	
f_{MCLK}	Supported MCLK frequencies	Up to 50 MHz	128		512	f_S(2)
f_{PLL}	PLL input frequency	Clock divider uses fractional divide D > 0, P = 1	6.7		20	MHz
		Clock divider uses integer divide D = 0, P = 1	1		20	
SERIAL AUDIO PORT						
t_{DLY}	Required LRCK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		8		96	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S(2)
f_{SCLK}	SCLK frequency	Either master mode or slave mode			24.576	MHz
SPEAKER AMPLIFIER (ALL OUTPUT CONFIGURATIONS)						
$A_{V(SPK\_AMP)}$	Speaker amplifier gain	SPK_GAIN/FREQ voltage < 3 V, see *Adjustable Amplifier Gain and Switching Frequency Selection*		20		dBV
		SPK_GAIN/FREQ voltage > 3.3 V, see *Adjustable Amplifier Gain and Switching Frequency Selection*		26		
$\Delta A_{V(SPK\_AMP)}$	Typical variation of speaker amplifier gain			±1		dBV

(1) DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO2, LRCK/FS, MCLK,$\overline{RESET}$, SCL, SCLK, SDA, SDIN, and $\overline{SPK\_MUTE}$.
(2) A unit of f_S indicates that the specification is the value listed in the table multiplied by the sample rate of the audio used in the TAS5780M device.

Electrical Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5780MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 40 kHz brickwall filter. The device output PWM frequency was set to 768 kHz unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SPK_AMP}	Switching frequency of the speaker amplifier	Switching frequency depends on voltage presented at SPK_GAIN/FREQ pin and the clocking arrangement, including the incoming sample rate, see *Adjustable Amplifier Gain and Switching Frequency Selection*	176.4		768	kHz
K_{SVR}	Power supply rejection ratio	Injected Noise = 50 Hz to 60 Hz, 200 mV_{P-P}, Gain = 26 dB, input audio signal = digital zero		60		dB
$r_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	V_{PVDD} = 24 V, $I_{(SPK\_OUT)}$ = 500 mA, T_J = 25°C, includes PVDD/PGND pins, leadframe, bondwires and metallization layers.		120		mΩ
		V_{PVDD} = 24 V, $I_{(SPK\_OUT)}$ = 500 mA, T_J = 25°C		90		
OCE_{THRES}	SPK_OUTxx overcurrent error threshold			7.5		A
OTE_{THRES}	Overtemperature error threshold			165		°C
$OCE_{CLRTIME}$	Time required to clear overcurrent error after error condition is removed.			1.3		s
$OTE_{CLRTIME}$	Time required to clear overtemperature error after error condition is removed.			1.3		s
$OVE_{THRES(PVDD)}$	PVDD overvoltage error threshold			27		V
$UVE_{THRES(PVDD)}$	PVDD undervoltage error threshold			4.3		V
SPEAKER AMPLIFIER (STEREO BTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 20 dB gain, V_{PVDD} = 12 V		2		mV
		Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 26 dB gain, V_{PVDD} = 24 V		5	15	
$I_{CN(SPK)}$	Idle channel noise	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, A-Weighted		49		μV_{RMS}
		V_{PVDD} = 15 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, A-Weighted		59		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted		81		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted		82		
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 4 Ω, THD+N = 0.1%		14		W
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, THD+N = 0.1%		8		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, THD+N = 0.1%		23		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, THD+N = 0.1%		13		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, THD+N = 0.1%		34		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, THD+N = 0.1%		20		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, THD+N = 0.1%		40		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, THD+N = 0.1%		33		

Electrical Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5780MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 40 kHz brickwall filter. The device output PWM frequency was set to 768 kHz unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio (referenced to 0 dBFS input signal)	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, A-Weighted, –120 dBFS Input		103		dB
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted, –120 dBFS Input		102		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted, –120 dBFS Input		103		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted, –120 dBFS Input		105		
$THD+N_{SPK}$	Total harmonic distortion and noise	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 4 Ω, P_O = 1 W, f = 1kHz		0.021%		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, P_O = 1 W, f = 1kHz		0.022%		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, P_O = 1 W, f = 1kHz		0.02%		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, P_O = 1 W, f = 1kHz		0.037%		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, P_O = 1 W, f = 1kHz		0021%		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, P_O = 1 W, f = 1kHz		0.028%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, P_O = 1 W, f = 1kHz		0.027%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, P_O = 1 W, f = 1kHz		0.038%		
$X\text{-talk}_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1-kHz Sine, across f(S)		–90		dB
		V_{PVDD} = 15 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1-kHz Sine, across f(S)		–102		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1-kHz Sine, across f(S)		–93		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1-kHz Sine, across f(S)		–93		
SPEAKER AMPLIFIER (MONO PBTL)						
$\lvert V_{OS} \rvert$	Amplifier offset voltage	Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 20 dB gain, V_{PVDD} = 12 V		0.7		mV
		Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 26 dB gain, V_{PVDD} = 24 V		4		
I_{CN}	Idle channel noise	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, A-Weighted		48		μV_{RMS}
		V_{PVDD} = 15 V, SPK_GAIN = 20 dB, RSPK = 8 Ω, A-Weighted		49		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, RSPK = 8 Ω, A-Weighted		83		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted		82		

Electrical Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5780MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 40 kHz brickwall filter. The device output PWM frequency was set to 768 kHz unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (per channel)	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 2 Ω, THD+N = 0.1%, Unless otherwise noted		30		W
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		16		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, THD+N = 0.1%		9		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 2 Ω, THD+N = 0.1%, Unless otherwise noted		44		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		22		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, THD+N = 0.1%		13		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 2 Ω, THD+N = 0.1%, Unless otherwise noted		50		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		36		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, THD+N = 0.1%		20		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 2 Ω, THD+N = 0.1%, Unless otherwise noted		40		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		61		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, THD+N = 0.1%		34		
SNR	Signal-to-noise ratio (referenced to 0 dBFS input signal)	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, A-Weighted, –120 dBFS Input		105		dB
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted, –120 dBFS Input		104		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted, –120 dBFS Input		105		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, A-Weighted, –120 dBFS Input		107		
THD+N	Total harmonic distortion and noise	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 2 Ω, P_O = 1 W, f = 1kHz		0.014%		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 4 Ω, P_O = 1 W, f = 1kHz		0.011%		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 Ω, P_O = 1 W, f = 1kHz		0.014%		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 2 Ω, P_O = 1 W, f = 1kHz		0.015%		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, P_O = 1 W, f = 1kHz		0.013%		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, P_O = 1 W, f = 1kHz		0.015%		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 2 Ω, P_O = 1 W, f = 1kHz		0.018%		
		V, R_{SPK} = 4 Ω, P_O = 1 W, f = 1kHz		0.012%		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, P_O = 1 W, f = 1kHz		0.020%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 2 Ω, P_O = 1 W, f = 1kHz		0.028%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 4 Ω, P_O = 1 W, f = 1kHz		0.02%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 Ω, P_O = 1 W, f = 1kHz		0.027%		

7.6 Power Dissipation Characteristics

Free-air room temperature 25°C (unless otherwise noted)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
7.4	20	384	Idle	4	21.30	59.70	0.355
				6	21.33	59.68	0.355
				8	21.30	59.70	0.355
			Mute	4	21.33	58.82	0.352
				6	21.34	58.81	0.352
				8	21.36	58.81	0.352
			Standby	4	2.08	12.41	0.056
				6	2.11	12.41	0.057
				8	2.17	12.41	0.057
			Powerdown	4	2.03	0.730	0.017
				6	2.04	0.740	0.018
				8	2.06	0.740	0.018
		768	Idle	4	27.48	59.7	0.400
				6	27.49	59.73	0.401
				8	24.46	59.72	0.378
			Mute	4	27.50	58.8	0.398
				6	27.51	58.8	0.398
				8	27.52	58.81	0.398
			Standby	4	2.04	12.41	0.056
				6	2.08	12.41	0.056
				8	2.11	12.41	0.057
			Powerdown	4	2.06	0.73	0.018
				6	2.07	0.74	0.018
				8	2.08	0.74	0.018

(1) Mute: B0-P0-R3-D0,D4 = 1
(2) Standby: B0-P0-R2-D4 = 1
(3) Power down: B0-P0-R2-D0 = 1
(4) I_{PVDD} refers to all current that flows through the PVDD supply for the DUT. Any other current sinks not directly related to the DUT current draw were removed.
(5) I_{DVDD} refers to all current that flows through the DVDD (3.3-V) supply for the DUT. Any other current sinks not directly related to the DUT current draw were removed.

Power Dissipation Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
11.1	20	384	Idle	4	24.33	59.74	0.467
				6	24.32	59.74	0.467
				8	24.36	59.70	0.467
			Mute	4	24.36	58.81	0.464
				6	24.32	58.82	0.464
				8	24.37	58.84	0.465
			Standby	4	3.58	12.40	0.081
				6	3.57	12.41	0.081
				8	3.58	12.42	0.081
			Powerdown	4	3.52	0.74	0.042
				6	3.52	0.74	0.042
				8	3.54	0.74	0.042
		768	Idle	4	30.70	59.70	0.538
				6	30.65	59.72	0.537
				8	30.67	59.71	0.537
			Mute	4	3.072	58.80	0.528
				6	30.69	58.81	0.535
				8	30.69	58.81	0.535
			Standby	4	3.54	12.40	0.080
				6	3.54	12.41	0.080
				8	3.58	12.42	0.081
			Powerdown	4	3.53	0.74	0.042
				6	3.53	0.74	0.042
				8	3.55	0.74	0.042

Power Dissipation Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
12	20	384	Idle	4	25.07	59.72	0.498
				6	25.08	59.73	0.498
				8	25.10	59.71	0.498
			Mute	4	25.12	58.84	0.496
				6	25.08	58.82	0.495
				8	25.11	58.82	0.495
			Standby	4	3.92	12.40	0.088
				6	3.93	12.41	0.088
				8	3.94	12.41	0.088
			Powerdown	4	3.87	0.75	0.049
				6	3.85	0.74	0.049
				8	3.87	0.75	0.049
		768	Idle	4	31.31	59.72	0.573
				6	31.29	59.71	0.573
				8	31.31	59.74	0.573
			Mute	4	31.31	58.80	0.570
				6	31.33	58.81	0.570
				8	31.32	58.81	0.570
			Standby	4	3.88	12.40	0.087
				6	3.90	12.41	0.088
				8	3.91	12.41	0.088
			Powerdown	4	3.89	0.75	0.049
				6	3.91	0.74	0.049
				8	3.88	0.75	0.049

Power Dissipation Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
15	26	384	Idle	4	27.94	59.73	0.616
				6	27.91	59.75	0.616
				8	27.75	59.69	0.613
			Mute	4	27.98	58.84	0.614
				6	27.94	58.87	0.613
				8	27.88	58.85	0.612
			Standby	4	5.09	12.41	0.117
				6	5.12	12.41	0.118
				8	5.19	12.41	0.119
			Powerdown	4	5.02	0.74	0.078
				6	5.06	0.74	0.078
				8	5.14	0.74	0.080
		768	Idle	4	33.05	59.7	0.693
				6	33.03	59.72	0.693
				8	33.08	59.68	0.693
			Mute	4	33.03	58.81	0.690
				6	33.04	58.81	0.690
				8	33.05	58.80	0.690
			Standby	4	5.07	12.41	0.117
				6	5.09	12.41	0.117
				8	5.14	12.41	0.118
			Powerdown	4	5.02	0.74	0.078
				6	5.04	0.74	0.078
				8	5.09	0.74	0.079

Power Dissipation Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
19.6	26	384	Idle	4	32.27	59.77	0.830
				6	32.19	59.76	0.828
				8	32.08	59.75	0.826
			Mute	4	32.27	58.85	0.827
				6	32.24	58.87	0.826
				8	32.22	58.86	0.826
			Standby	4	6.95	12.40	0.177
				6	6.93	12.42	0.177
				8	7.00	12.41	0.178
			Powerdown	4	6.89	0.74	0.137
				6	6.90	0.74	0.138
				8	6.96	0.73	0.139
		768	Idle	4	34.99	59.74	0.883
				6	34.95	59.74	0.882
				8	34.97	59.71	0.882
			Mute	4	34.96	58.85	0.879
				6	34.98	58.83	0.880
				8	34.96	58.81	0.879
			Standby	4	6.93	12.40	0.177
				6	6.93	12.42	0.177
				8	6.98	12.41	0.178
			Powerdown	4	6.84	0.74	0.137
				6	6.89	0.74	0.137
				8	6.90	0.73	0.138

Power Dissipation Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
24	26	384	Idle	4	36.93	59.80	1.084
				6	36.87	59.81	1.082
				8	36.77	59.76	1.080
			Mute	4	36.94	58.91	1.081
				6	36.89	58.89	1.080
				8	36.85	58.90	1.079
			Standby	4	8.73	12.40	0.250
				6	8.72	12.40	0.250
				8	8.71	12.40	0.250
			Powerdown	4	8.64	0.74	0.210
				6	8.66	0.74	0.210
				8	8.69	0.73	0.211
		768	Idle	4	36.84	59.73	1.081
				6	36.86	59.76	1.082
				8	36.83	59.78	1.081
			Mute	4	36.85	58.85	1.079
				6	36.84	58.84	1.078
				8	36.82	58.83	1.078
			Standby	4	8.66	12.40	0.249
				6	8.68	12.40	0.249
				8	8.71	12.40	0.250
			Powerdown	4	8.63	0.74	0.210
				6	8.64	0.74	0.210
				8	8.65	0.73	0.210

7.7 MCLK Timing

See Figure 18.

		MIN	NOM	MAX	UNIT
t_{MCLK}	MCLK period	20		1000	ns
t_{MCLKH}	MCLK pulse width, high	9			ns
t_{MCLKL}	MCLK pulse width, low	9			ns

7.8 Serial Audio Port Timing – Slave Mode

See Figure 19.

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns

7.9 Serial Audio Port Timing – Master Mode

See Figure 20.

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{LRD}	LRCK/FS delay time from to SCLK falling edge	–10		20	ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns

7.10 I^2C Bus Timing – Standard

		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7		µs
t_{LOW}	Low period of the SCL clock	4.7		µs
t_{HI}	High period of the SCL clock	4		µs
t_{RS-SU}	Setup time for (repeated) START condition	4.7		µs
t_{S-HD}	Hold time for (repeated) START condition	4		µs
t_{D-SU}	Data setup time	250		ns
t_{D-HD}	Data hold time	0	900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$	1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$	1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$	1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$	1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$	1000	ns
t_{P-SU}	Setup time for STOP condition	4		µs

7.11 I^2C Bus Timing – Fast

See Figure 21.

		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3		µs
t_{LOW}	Low period of the SCL clock	1.3		µs
t_{HI}	High period of the SCL clock	600		ns
t_{RS-SU}	Setup time for (repeated)START condition	600		ns
t_{RS-HD}	Hold time for (repeated)START condition	600		ns
t_{D-SU}	Data setup time	100		ns
t_{D-HD}	Data hold time	0	900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$	300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$	300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$	300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$	300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$	300	ns
t_{P-SU}	Setup time for STOP condition	600		ns
t_{SP}	Pulse width of spike suppressed		50	ns

7.12 $\overline{\text{SPK\_MUTE}}$ Timing

See Figure 22.

		MIN	MAX	UNIT
t_r	Rise time		20	ns
t_f	Fall time		20	ns

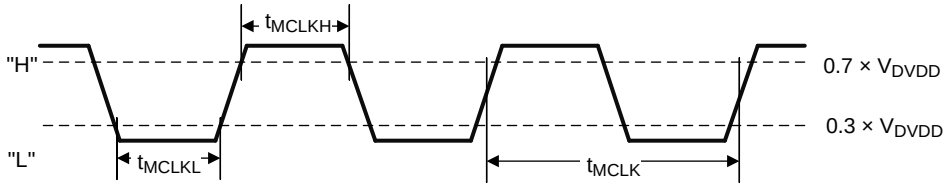


Figure 18. Timing Requirements for MCLK Input

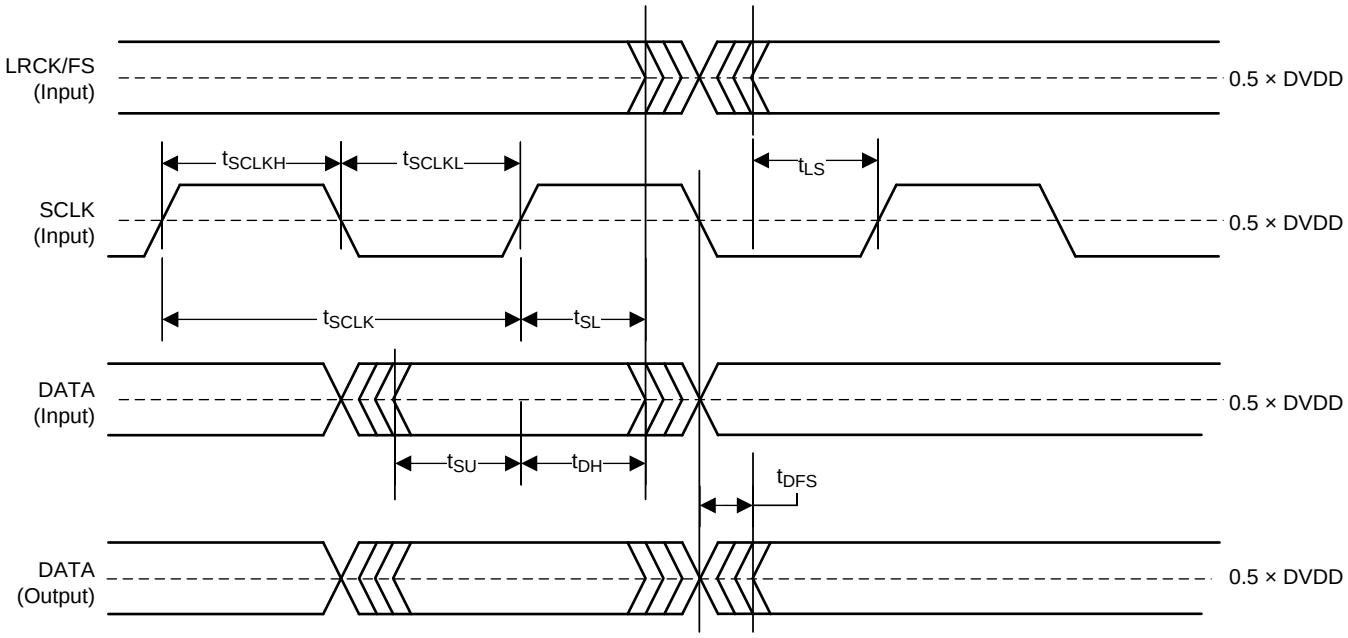


Figure 19. MCLK Timing Diagram in Slave Mode

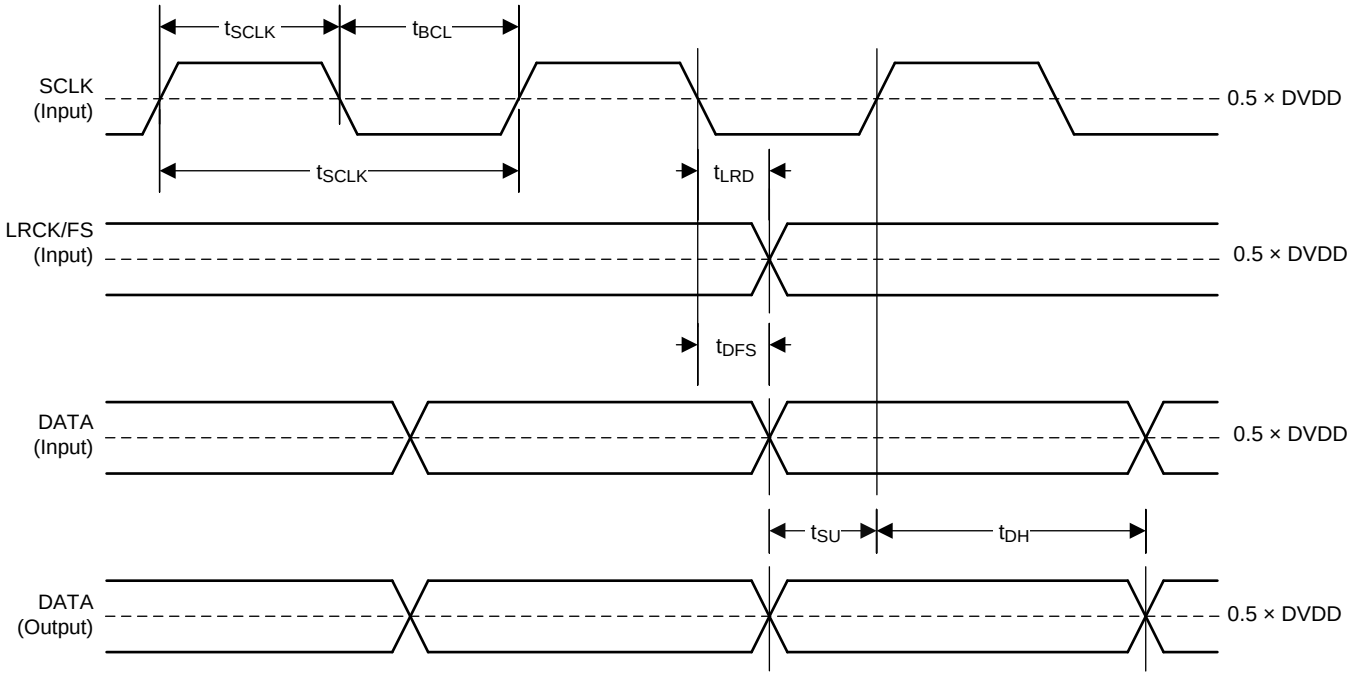


Figure 20. MCLK Timing Diagram in Master Mode

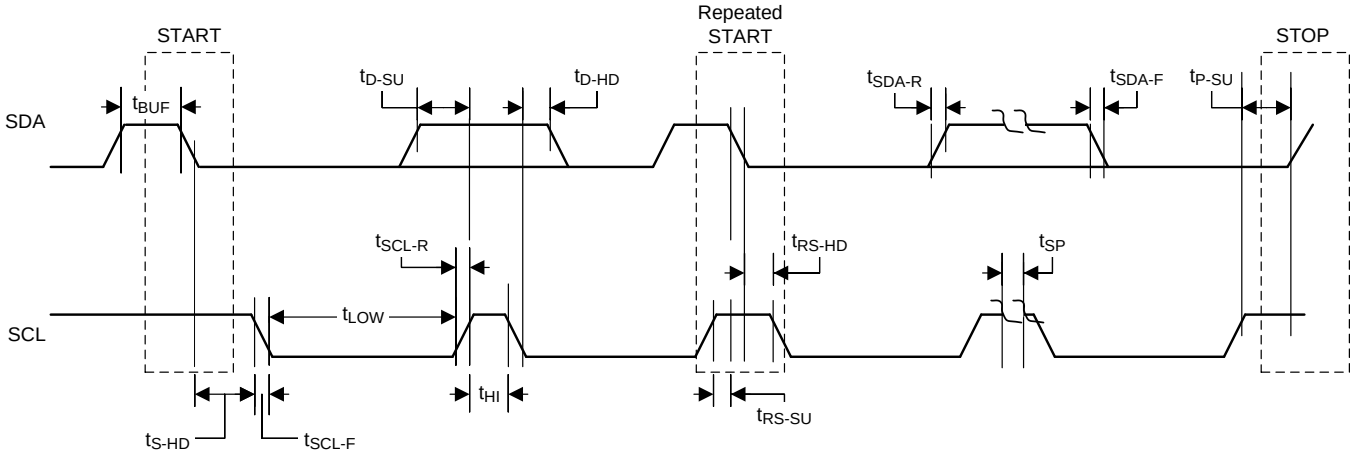


Figure 21. I²C Communication Port Timing Diagram

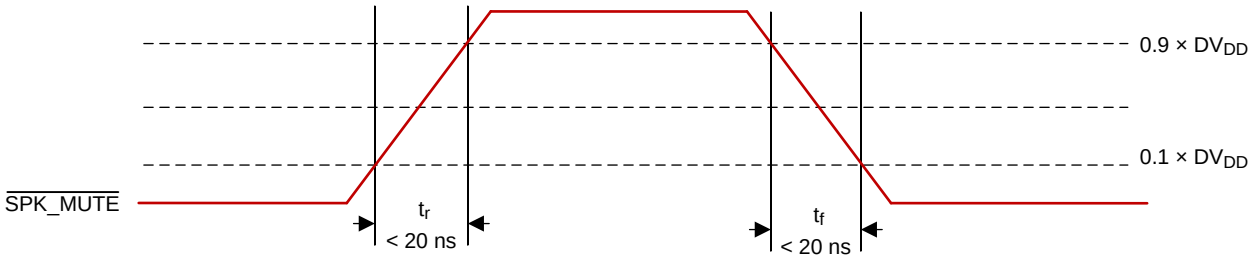


Figure 22. $\overline{\text{SPK\_MUTE}}$ Timing Diagram for Soft Mute Operation via Hardware Pin

7.13 Typical Characteristics

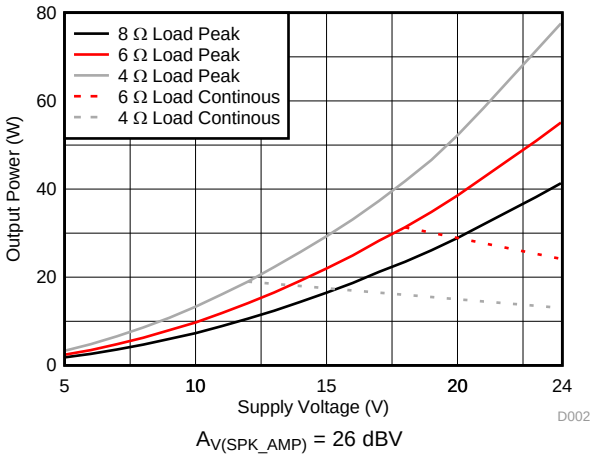
All performance plots were taken using the TAS5780MEVM Board at room temperature, unless otherwise noted. The term "traditional LC filter" refers to the output filter that is present by default on the TAS5780MEVM Board.

Table 1. Quick Reference Table

OUTPUT CONFIGURATIONS	PLOT TITLE	FIGURE NUMBER
Bridge Tied Load (BTL) Configuration Curves	Frequency Response	Figure 34
	Output Power vs PVDD	Figure 23
	THD+N vs Frequency, V_{PVDD} = 12 V	Figure 24
	THD+N vs Frequency, V_{PVDD} = 15 V	Figure 25
	THD+N vs Frequency, V_{PVDD} = 18 V	Figure 26
	THD+N vs Frequency, V_{PVDD} = 24 V	Figure 27
	THD+N vs Power, V_{PVDD} = 12 V	Figure 28
	THD+N vs Power, V_{PVDD} = 15 V	Figure 29
	THD+N vs Power, V_{PVDD} = 18 V	Figure 30
	THD+N vs Power, V_{PVDD} = 24 V	Figure 31
	Idle Channel Noise vs PVDD	Figure 32
	Efficiency vs Output Power	Figure 33
	Efficiency vs Output Power	Figure 34
	Efficiency vs Output Power	Figure 35
	Idle Current Draw (Filterless) vs PVDD	Figure 36
	Crosstalk vs. Frequency	Figure 37
	PVDD PSRR vs Frequency	Figure 38
	DVDD PSRR vs Frequency	Figure 39
	AVDD PSRR vs Frequency	Figure 40
	CPVDD PSRR vs Frequency	Figure 41
Parallel Bridge Tied Load (PBTL) Configuration	Output Power vs PVDD	Figure 43
	THD+N vs Frequency, V_{PVDD} = 12 V	Figure 44
	THD+N vs Frequency, V_{PVDD} = 15 V	Figure 45
	THD+N vs Frequency, V_{PVDD} = 18 V	Figure 46
	THD+N vs Frequency, V_{PVDD} = 24 V	Figure 47
	THD+N vs Power, V_{PVDD} = 12 V	Figure 48
	THD+N vs Power, V_{PVDD} = 15 V	Figure 49
	THD+N vs Power, V_{PVDD} = 18 V	Figure 50
	THD+N vs Power, V_{PVDD} = 24 V	Figure 51
	Idle Channel Noise vs PVDD	Figure 52
	Efficiency vs Output Power	Figure 53

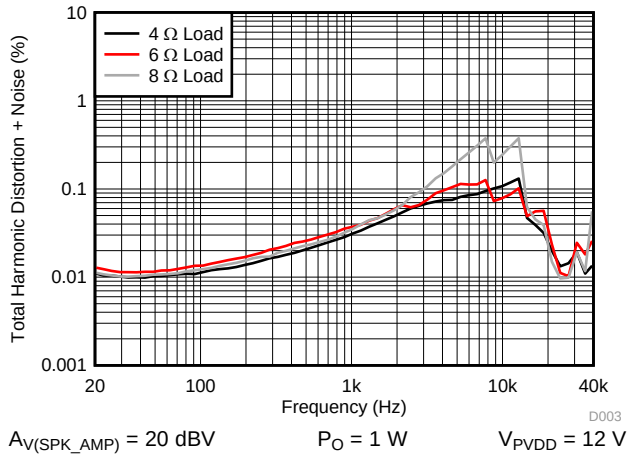
7.13.1 Bridge Tied Load (BTL) Configuration Curves

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5780MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 40-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, unless otherwise noted. For both the BTL plots and the PBTL plots, the LC filter used was 4.7 µH / 0.68 µF. Return to *Quick Reference Table*.



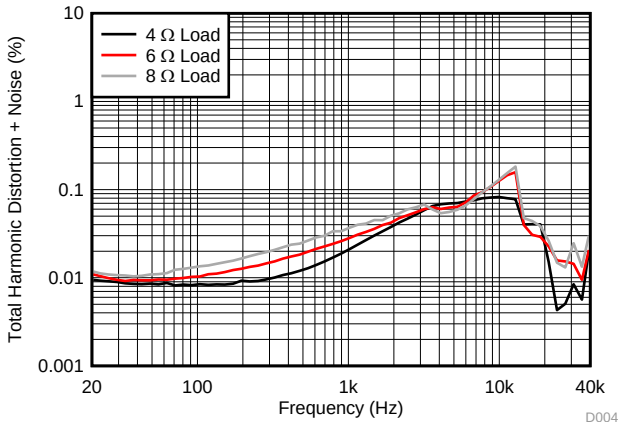
$A_{V(SPK\_AMP)}$ = 26 dBV

Figure 23. Output Power vs PVDD – BTL



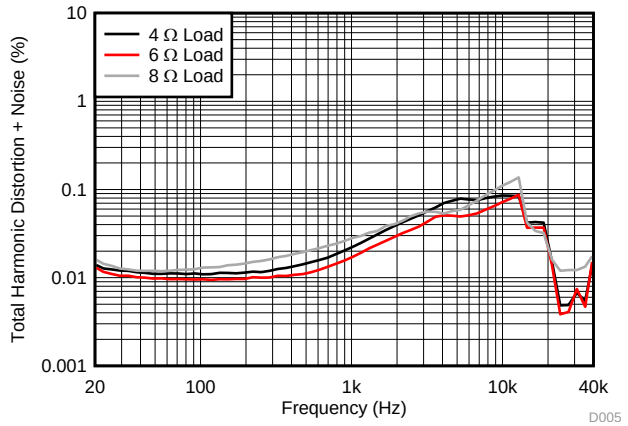
$A_{V(SPK\_AMP)}$ = 20 dBV P_O = 1 W V_{PVDD} = 12 V

Figure 24. THD+N vs Frequency – BTL



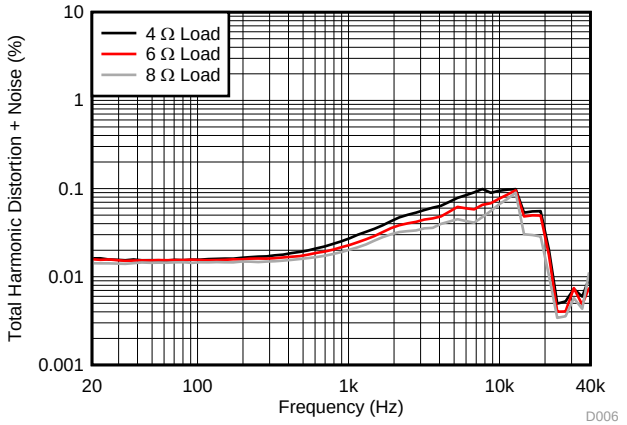
$A_{V(SPK\_AMP)}$ = 20 dBV P_O = 1 W V_{PVDD} = 15 V

Figure 25. THD+N vs Frequency – BTL



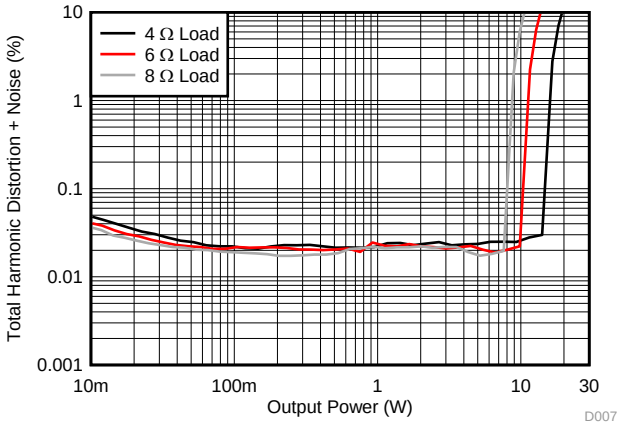
$A_{V(SPK\_AMP)}$ = 26 dBV P_O = 1 W V_{PVDD} = 18 V

Figure 26. THD+N vs Frequency – BTL



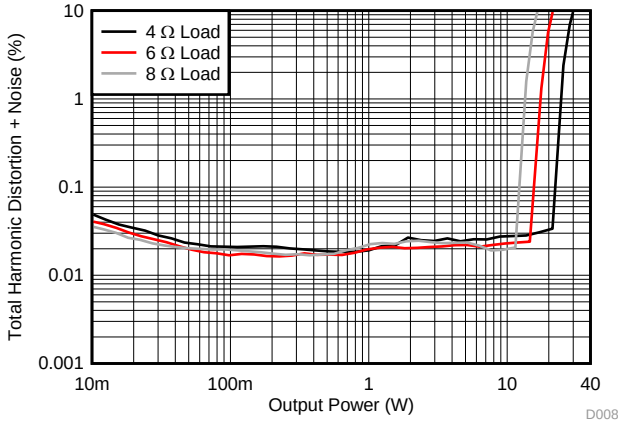
$A_{V(SPK\_AMP)}$ = 26 dBV P_O = 1 W V_{PVDD} = 24 V

Figure 27. THD+N vs Frequency – BTL



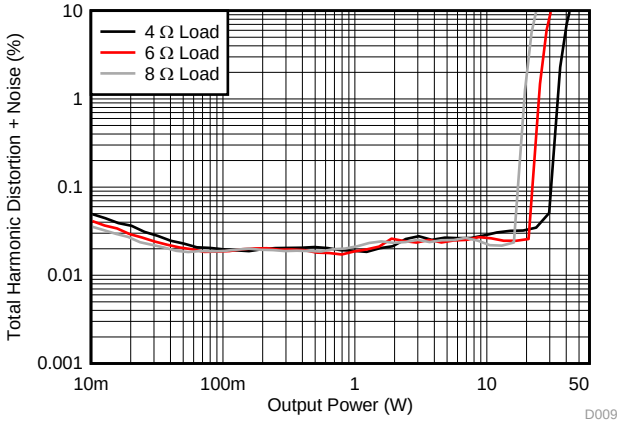
$A_{V(SPK\_AMP)}$ = 20 dBV V_{PVDD} = 12 V

Figure 28. THD+N vs Power – BTL



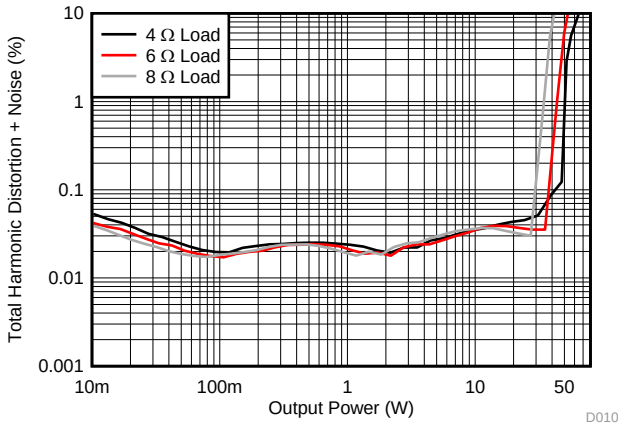
$A_{V(SPK\_AMP)}$ = 20 dBV V_{PVDD} = 15 V

Figure 29. THD+N vs Power – BTL



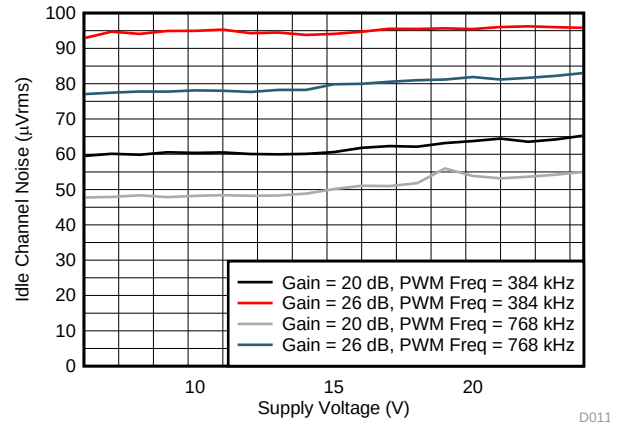
$A_{V(SPK\_AMP)}$ = 26 dBV V_{PVDD} = 18 V

Figure 30. THD+N vs Power – BTL



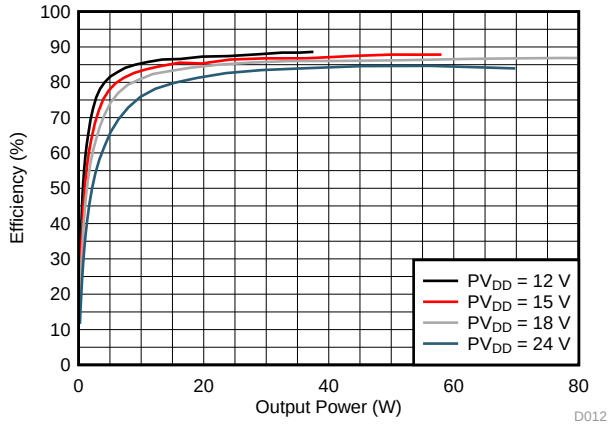
$A_{V(SPK\_AMP)}$ = 26 dBV V_{PVDD} = 24 V

Figure 31. THD+N vs Power – BTL



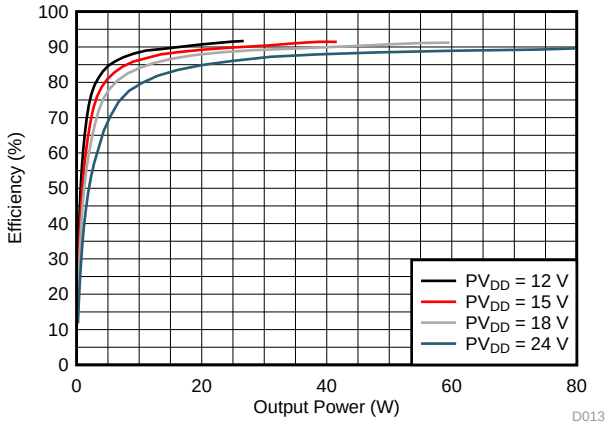
R_{SPK} = 4 Ω

Figure 32. Idle Channel Noise vs PVDD – BTL



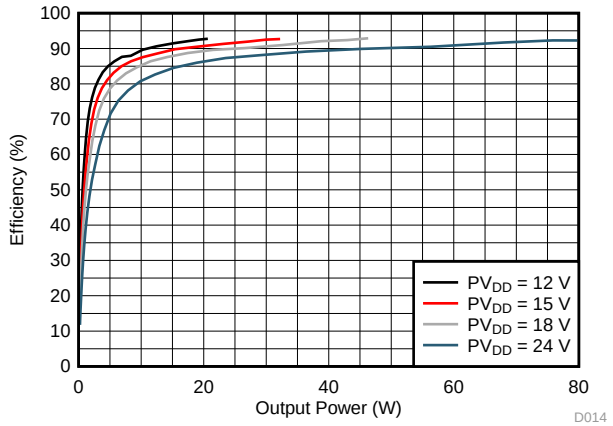
R_{SPK} = 4 Ω

Figure 33. Efficiency vs Output Power – BTL



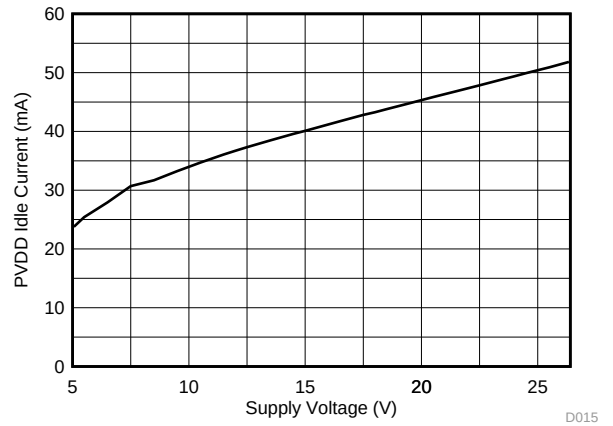
R_{SPK} = 6 Ω

Figure 34. Efficiency vs Output Power – BTL



R_{SPK} = 8 Ω

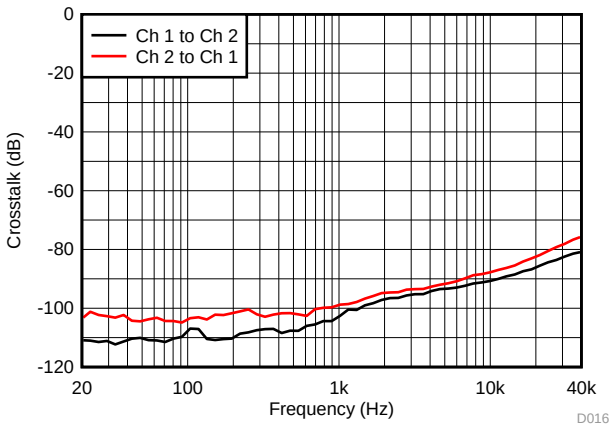
Figure 35. Efficiency vs Output Power – BTL



f_{SPK_AMP} = 768 kHz

R_{SPK} = 8 Ω

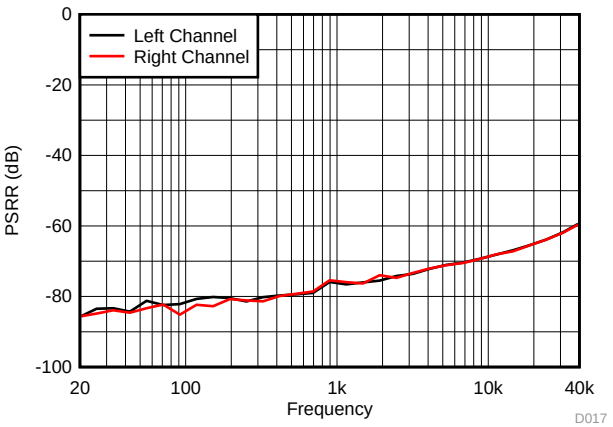
Figure 36. Idle Current Draw (Filterless) vs V_{PVDD} – BTL



$A_{V(SPK\_AMP)}$ = 26 dBV

V_{PVDD} = 24 V

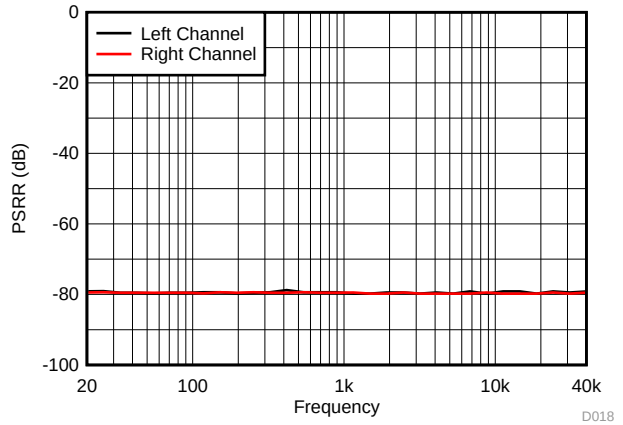
Figure 37. Crosstalk vs Frequency – BTL



$A_{V(SPK\_AMP)}$ = 26 dBV

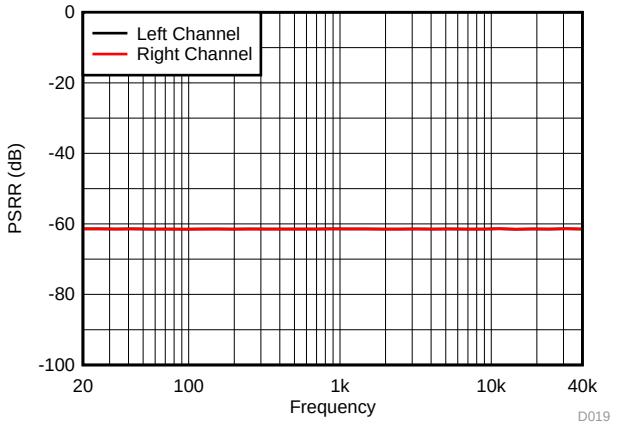
V_{PVDD} = 24 V + 250 mVac

Figure 38. PVDD PSRR vs Frequency – BTL



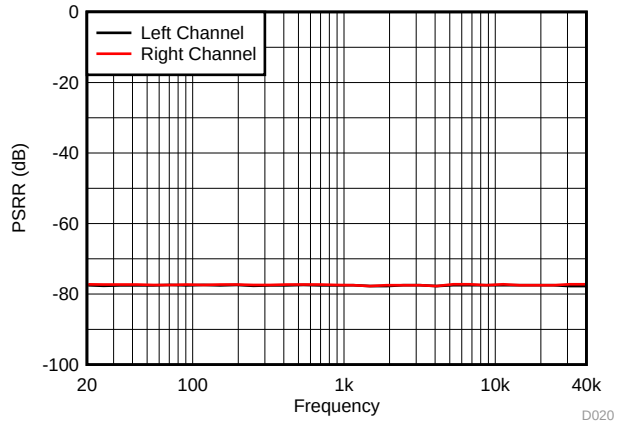
$A_{V(SPK\_AMP)}$ = 26 dBV
V_{PVDD} = 24 V
V_{DVDD} = 3.3 V + 250 mVac

Figure 39. DVDD PSRR vs Frequency – BTL



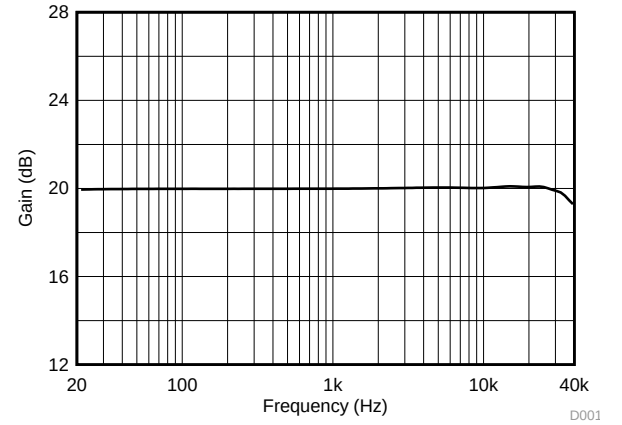
$A_{V(SPK\_AMP)}$ = 26 dBV
V_{PVDD} = 24 V
V_{AVDD} = 3.3 V + 250 mVac

Figure 40. AVDD PSRR vs Frequency – BTL



$A_{V(SPK\_AMP)}$ = 26 dBV
V_{PVDD} = 24 V
V_{CPVDD} = 3.3 V + 250 mVac

Figure 41. CPVDD PSRR vs Frequency – BTL

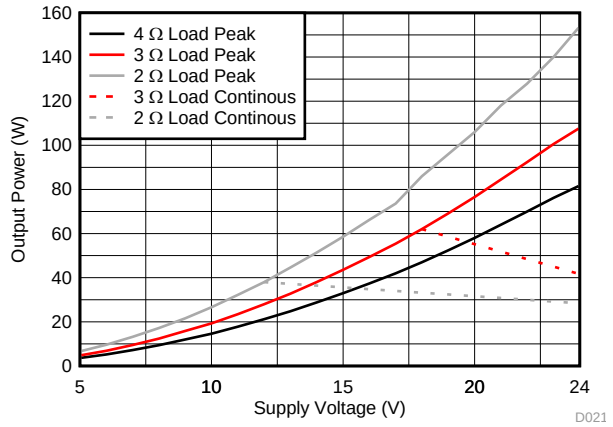


$A_{V(SPK\_AMP)}$ = 20 dB
PVDD = 12 V

Figure 42. Frequency Response

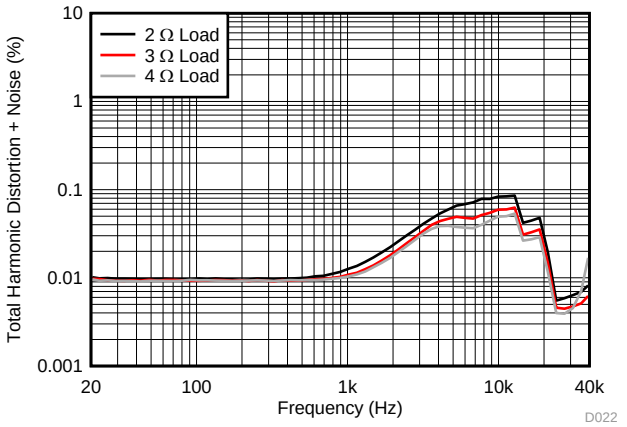
7.13.2 Parallel Bridge Tied Load (PBTL) Configuration

Return to *Quick Reference Table*.



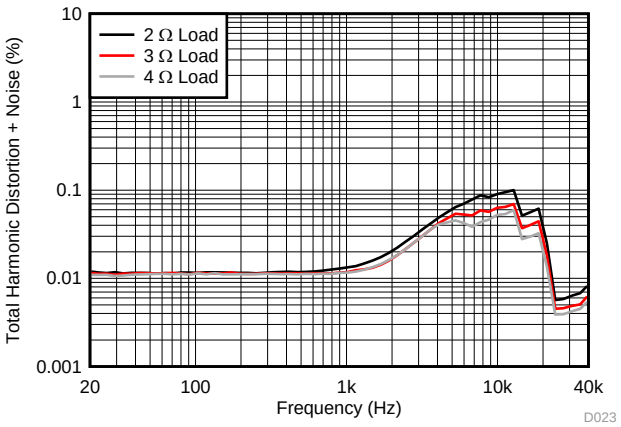
$A_{V(SPK\_AMP)}$ = 26 dBV

Figure 43. Output Power vs PVDD – PBTL



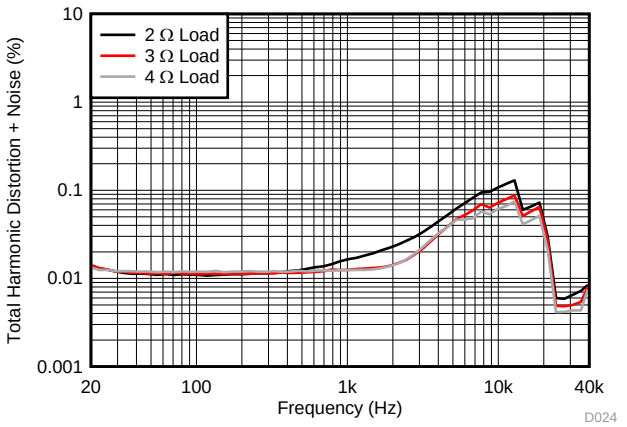
$A_{V(SPK\_AMP)}$ = 20 dBV P_O = 1 W V_{PVDD} = 12 V

Figure 44. THD+N vs Frequency – PBTL



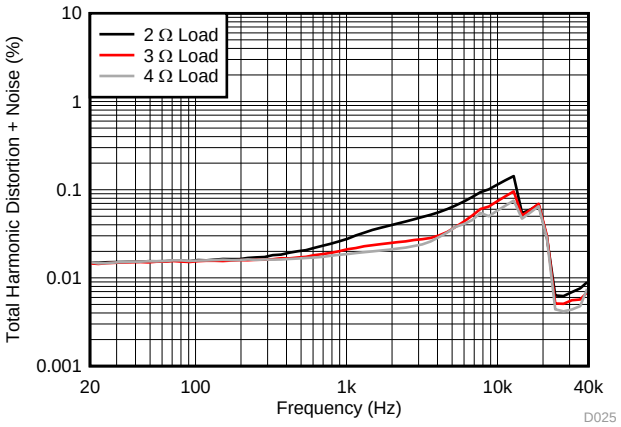
$A_{V(SPK\_AMP)}$ = 20 dBV P_O = 1 W V_{PVDD} = 15 V

Figure 45. THD+N vs Frequency – PBTL



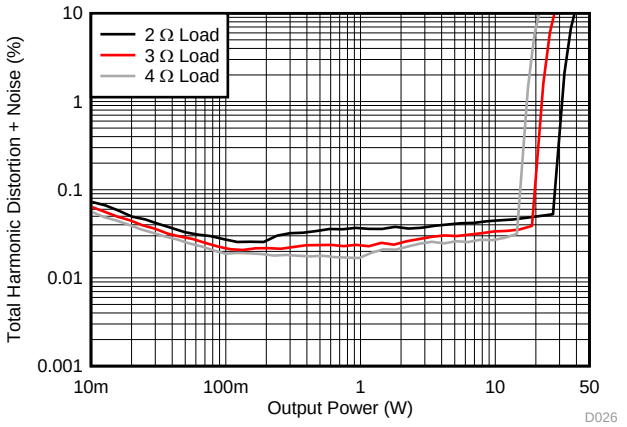
$A_{V(SPK\_AMP)}$ = 26 dBV P_O = 1 W V_{PVDD} = 18 V

Figure 46. THD+N vs Frequency – PBTL



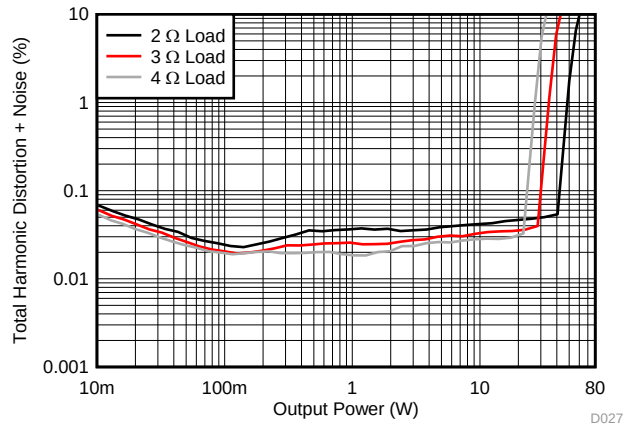
$A_{V(SPK\_AMP)}$ = 26 dBV P_O = 1 W V_{PVDD} = 24 V

Figure 47. THD+N vs Frequency – PBTL



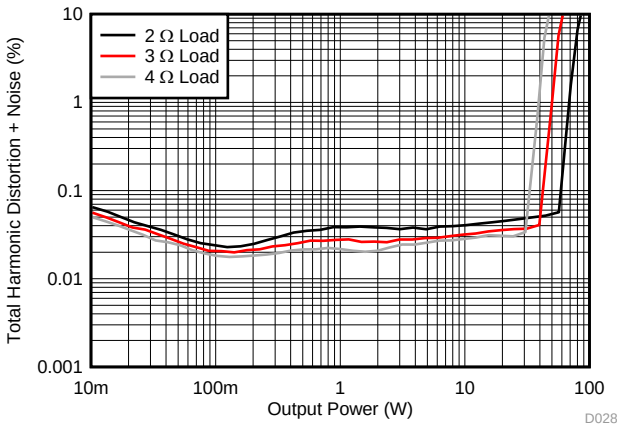
$A_{V(SPK\_AMP)}$ = 20 dBV V_{PVDD} = 12 V

Figure 48. THD+N vs Power – PBTL



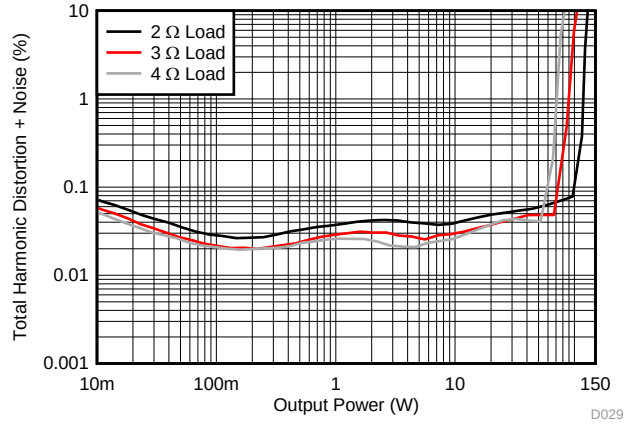
$A_{V(SPK\_AMP)}$ = 20 dBV V_{PVDD} = 15 V

Figure 49. THD+N vs Power – PBTL



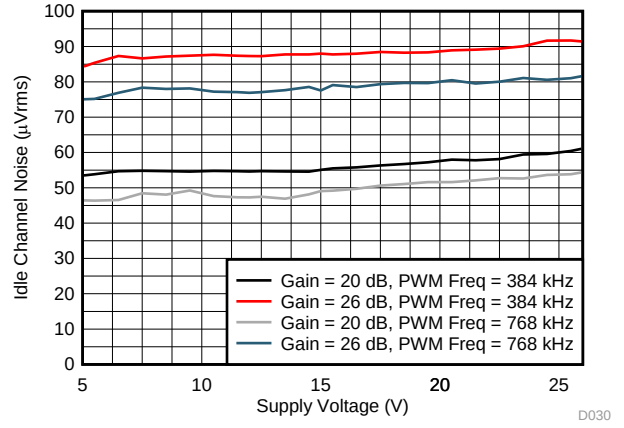
$A_{V(SPK\_AMP)}$ = 26 dBV V_{PVDD} = 18 V

Figure 50. THD+N vs Power – PBTL



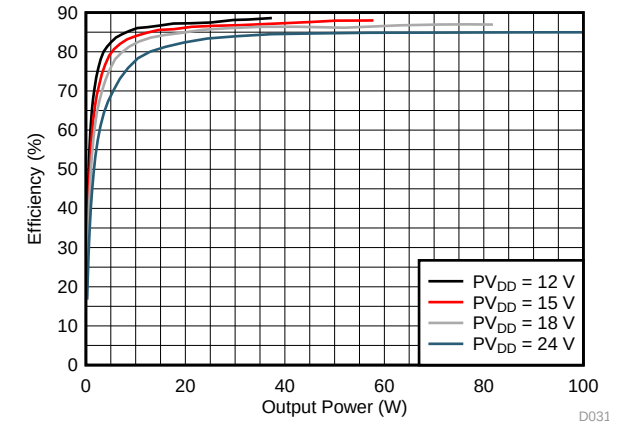
$A_{V(SPK\_AMP)}$ = 20 dBV V_{PVDD} = 24 V

Figure 51. THD+N vs Power – PBTL



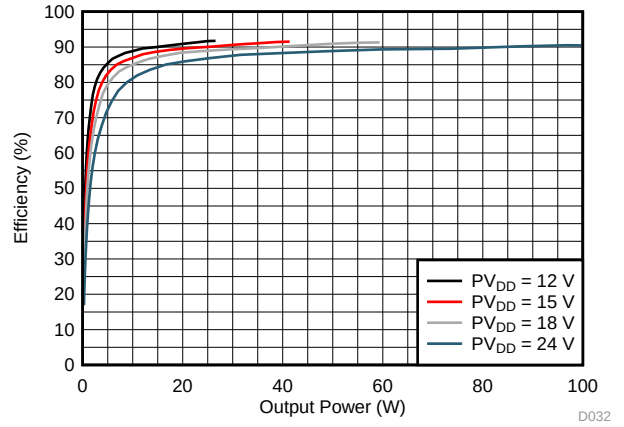
R_{SPK} = 4 Ω

Figure 52. Idle Channel Noise vs PVDD – PBTL



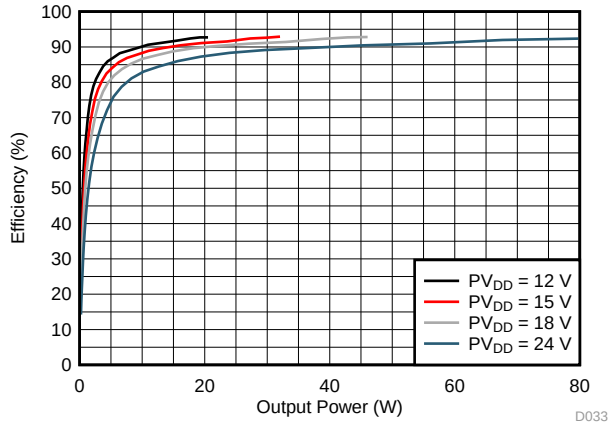
$A_{V(SPK\_AMP)}$ = 26 dBV R_{SPK} = 2 Ω

Figure 53. Efficiency vs Output Power – PBTL



$A_{V(SPK\_AMP)}$ = 20 dBV R_{SPK} = 3 Ω

Figure 54. Efficiency vs Output Power



$A_{V(SPK\_AMP)}$ = 20 dBV

R_{SPK} = 4 Ω

Figure 55. Efficiency vs Output Power

8 Parametric Measurement Information

PARAMETER	FIGURE
Stereo BTL	图 84
Mono PBTL	图 85

9 Detailed Description

9.1 Overview

The TAS5780M device integrates 4 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed below:

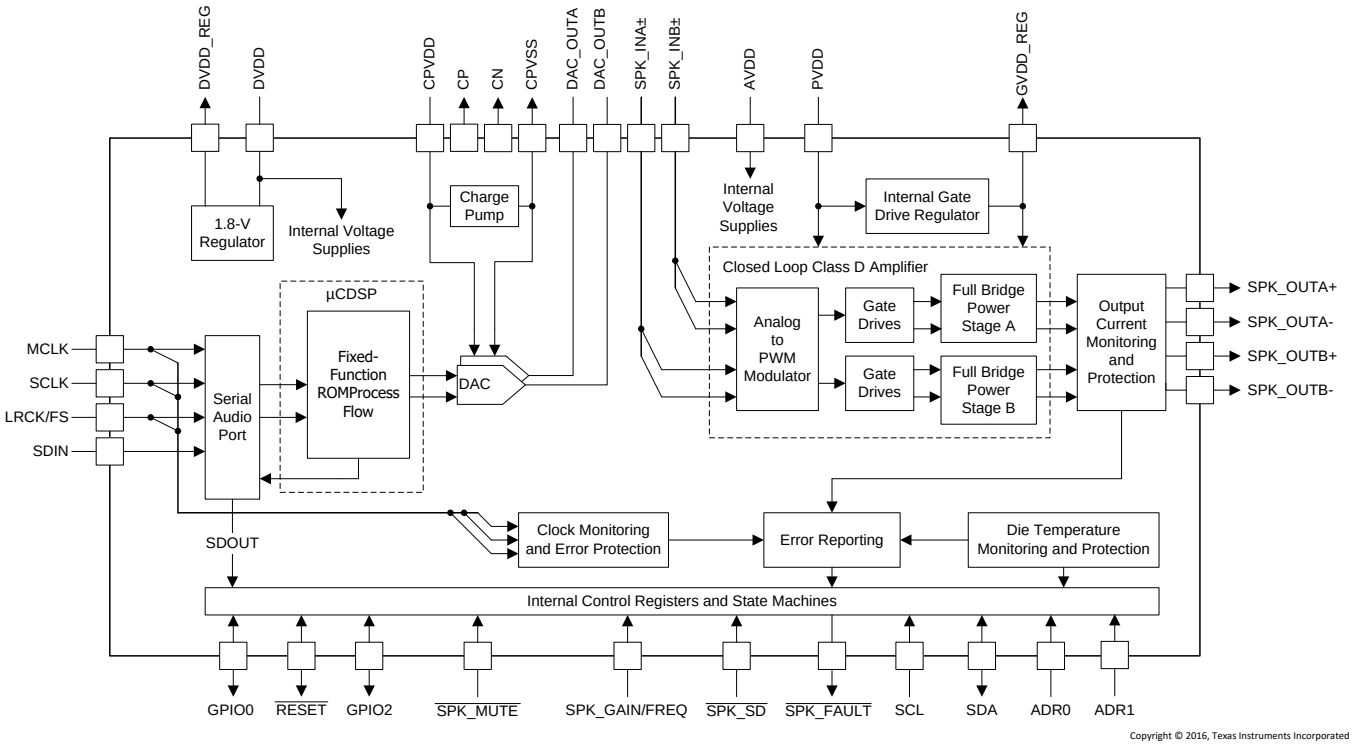
- A stereo audio DAC, boasting a strong Burr-Brown heritage with a highly flexible serial audio port.
- A µCDSP audio processing core, with a pre-programmed ROM image.
- A flexible closed-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
- An I^2C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low-voltage digital and analog circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. The operating range for these supplies is shown in the *Recommended Operating Conditions* table.

Communication with the device is accomplished through the I^2C control port. A speaker amplifier fault line is also provided to notify a system controller of the occurrence of an overtemperature, overcurrent, overvoltage, or undervoltage. Two digital GPIO pins are available for use. In the fixed function ROM image of the TAS5780M, the GPIO2 pin is used as an SDOUT terminal. The other GPIO is unused.

The µCDSP audio processing core is pre-programmed with a configurable DSP program. The RD GUI provides a means by which to manipulate the controls associated with that Process Flow.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-on-Reset (POR) Function

The TAS5780M device has a power-on reset function. The power-on reset feature resets all of the registers to their default configuration as the device is powering up. When the low-voltage power supply used to power DVDD, AVDD, and CPVDD exceeds the POR threshold, the device sets all of the internal registers to their default values and holds them there until the device receives valid MCLK, SCLK, and LRCK/FS toggling for a period of approximately 4 ms. After the toggling period has passed, the internal reset of the registers is removed and the registers can be programmed via the I^2C Control Port.

9.3.2 Device Clocking

The TAS5780M devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface in one form or another.

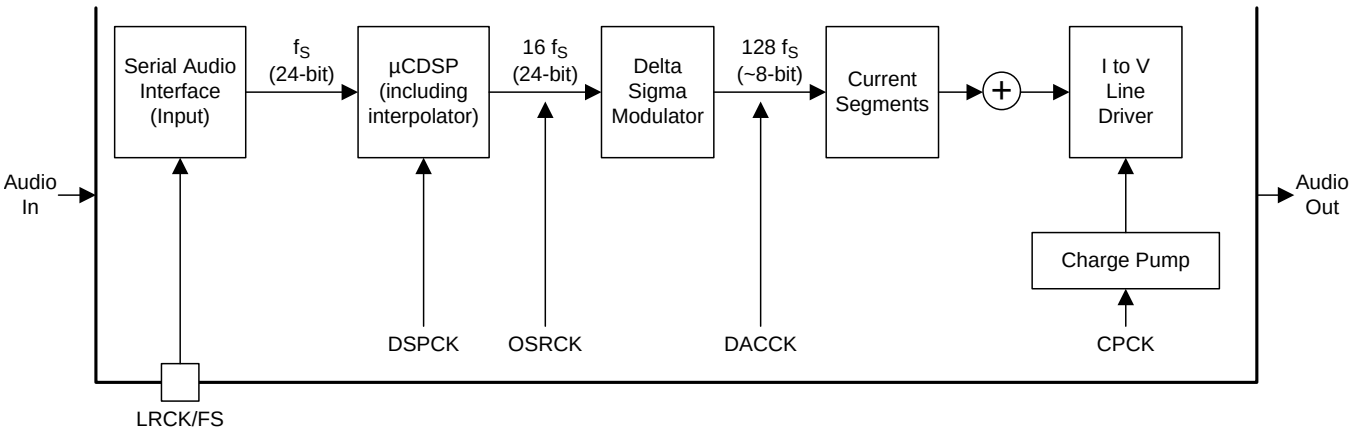


Figure 56. Audio Flow with Respective Clocks

Figure 56 shows the basic data flow at basic sample rate (f_S). When the data is brought into the serial audio interface, the data is processed, interpolated and modulated to 128 × f_S before arriving at the current segments for the final digital to analog conversion.

Figure 57 shows the clock tree.

Feature Description (continued)

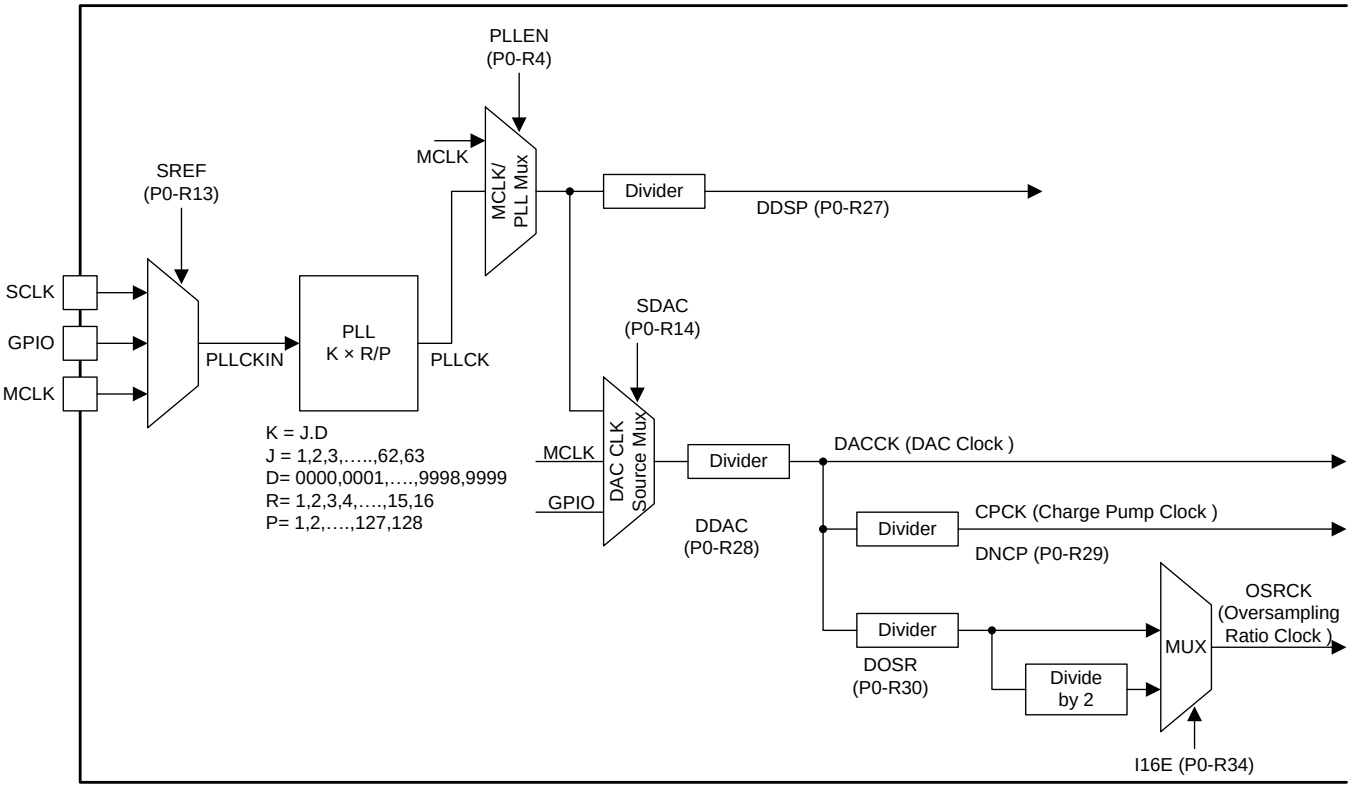


Figure 57. TAS5780M Clock Distribution Tree

The Serial Audio Interface typically has 4 connection pins which are listed as follows:

- MCLK (System Master Clock)
- SCLK (Bit Clock)
- LRCK/FS (Left Right Word Clock and Frame Sync)
- SDIN (Input Data)
- The output data, SDOUT, is presented on one of the GPIO pins.
- See the *GPIO Port and Hardware Control Pins* section)

The device has an internal PLL that is used to take either MCLK or SCLK and create the higher rate clocks required by the DSP and the DAC clock.

In situations where the highest audio performance is required, bringing MCLK to the device along with SCLK and LRCK/FS is recommended. The device should be configured so that the PLL is only providing a clock source to the DSP. All other clocks are then a division of the incoming MCLK. To enable the MCLK as the main source clock, with all others being created as divisions of the incoming MCLK, set the DAC CLK source Mux (SDAC in Figure 57) to use MCLK as a source, rather than the output of the MCLK/PLL Mux.

9.3.3 Serial Audio Port

9.3.3.1 Clock Master Mode from Audio Rate Master Clock

In Master Mode, the device generates bit clock and left-right and frame sync clock and outputs them on the appropriate pins. To configure the device in master mode, first put the device into reset, then use registers SCLKO and LRKO (P0-R9). Then reset the LRCK/FS and SCLK divider counters using bits RSCLK and RLRK (P0-R12). Finally, exit reset.

Figure 58 shows a simplified serial port clock tree for the device in master mode.

Feature Description (continued)

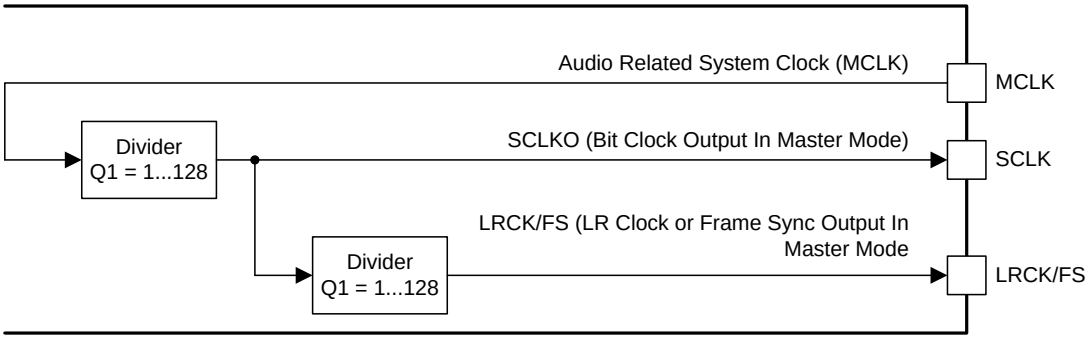


Figure 58. Simplified Clock Tree for MCLK Sourced Master Mode

In master mode, MCLK is an input and SCLK and LRCK/FS are outputs. SCLK and LRCK/FS are integer divisions of MCLK. Master mode with a non-audio rate master clock source requires external GPIO's to use the PLL in standalone mode. The PLL should be configured to ensure that the on-chip processor can be driven at the maximum clock rate. The master mode of operation is described in the *Clock Master from a Non-Audio Rate Master Clock* section.

When used with audio rate master clocks, the register changes that should be done include switching the device into master mode, and setting the divider ratio. An example of the master mode of operations is using 24.576 MHz MCLK as a master clock source and driving the SCLK and LRCK/FS with integer dividers to create 48 kHz sample rate clock output. In master mode, the DAC section of the device is also running from the PLL output. The TAS5780M device is able to meet the specified audio performance while using the internal PLL. However, using the MCLK CMOS oscillator source will have less jitter than the PLL.

To switch the DAC clocks (SDAC in the Figure 57) the following registers should be modified

- Clock Tree Flex Mode (P253-R63 and P253-R64)
- DAC and OSR Source Clock Register (P0-R14). Set to 0x30 (MCLK input, and OSR is set to whatever the DAC source is)
- The DAC clock divider should be 16 f_S.
  - 16 × 48 kHz = 768 kHz
  - 24.576 MHz (MCLK in) / 768 kHz = 32
  - Therefore, the divide ratio for register DDAC (P0-R28) should be set to 32. The register mapping gives 0x00 = 1, therefore 32 must be converter to 0x1F (31dec).

9.3.3.2 Clock Master from a Non-Audio Rate Master Clock

The classic example here is running a 96-kHz sampling system. Given the clock tree for the device (shown in Figure 57), a non-audio clock rate cannot be brought into the MCLK to the PLL in master mode. Therefore, the PLL source must be configured to be a GPIO pin, and the output brought back into another GPIO pin.

Feature Description (continued)

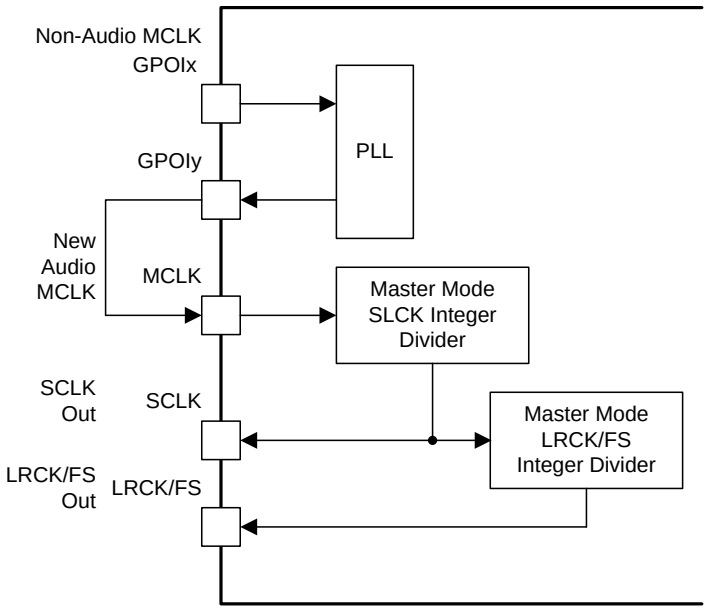


Figure 59. Generating Audio Clocks Using Non-Audio Clock Sources

The clock flow through the system is shown in Figure 59. The newly generated MCLK must be brought out of the device on a GPIO pin, then brought into the MCLK pin for integer division to create SCLK and LRCK/FS outputs.

NOTE

Pull-up resistors should be used on SCLK and LRCK/FS in master mode to ensure the device remains out of sleep mode.

9.3.3.3 Clock Slave Mode with 4-Wire Operation (SCLK, MCLK, LRCK/FS, SDIN)

The TAS5780M device requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the MCLK input and supports up to 50 MHz. The TAS5780M device system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies in the bands of 32 kHz, (44.1 – 48 kHz), (88.2 – 96 kHz) are supported.

NOTE

Values in the parentheses are grouped when detected, for example, 88.2 kHz and 96 kHz are detected as *double rate*, 32 kHz, 44.1 kHz and 48 kHz are detected as *single rate* and so on.

In the presence of a valid bit MCLK, SCLK and LRCK/FS, the device automatically configures the clock tree and PLL to drive the µCDSP as required.

The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 2 shows examples of system clock frequencies for common audio sampling rates.

MCLK rates that are not common to standard audio clocks, between 1 MHz and 50 MHz, are supported by configuring various PLL and clock-divider registers directly. In slave mode, auto clock mode should be disabled using P0-R37. Additionally, the user can be required to ignore clock error detection if external clocks are not available for some time during configuration or if the clocks presented on the pins of the device are invalid. The extended programmability allows the device to operate in an advanced mode in which the device becomes a clock master and drive the host serial port with LRCK/FS and SCLK, from a non-audio related clock (for example, using a setting of 12 MHz to generate 44.1 kHz [LRCK/FS] and 2.8224 MHz [SCLK]).

Feature Description (continued)

Table 2 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise. For MCLK timing requirements, refer to the *Serial Audio Port Timing – Master Mode* section.

Table 2. System Master Clock Inputs for Audio Related Clocks

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{MCLK}) (MHz)					
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S
8 kHz	See(1)	1.024(2)	1.536(2)	2.048	3.072	4.096
16 kHz		2.048(2)	3.072(2)	4.096	6.144	8.192
32 kHz		4.096(2)	6.144(2)	8.192	12.288	16.384
44.1 kHz		5.6488(2)	8.4672(2)	11.2896	16.9344	22.5792
48 kHz		6.144(2)	9.216(2)	12.288	18.432	24.576
88.2 kHz		11.2896(2)	16.9344	22.5792	33.8688	45.1584
96 kHz		12.288(2)	18.432	24.576	36.864	49.152

(1) This system clock rate is not supported for the given sampling frequency.
(2) This system clock rate is supported by PLL mode.

9.3.3.4 Clock Slave Mode with SCLK PLL to Generate Internal Clocks (3-Wire PCM)

9.3.3.4.1 Clock Generation using the PLL

The TAS5780M device supports a wide range of options to generate the required clocks as shown in Figure 57.

The clocks for the PLL require a source reference clock. This clock is sourced as the incoming SCLK or MCLK, a GPIO can also be used.

The source reference clock for the PLL reference clock is selected by programming the SRCREF value on P0-R13, D[6:4]. The TAS5780M device provides several programmable clock dividers to achieve a variety of sampling rates. See Figure 57.

If PLL functionality is not required, set the PLLEN value on P0-R4, D[0] to 0. In this situation, an external master clock is required.

Table 3. PLL Configuration Registers

CLOCK MULTIPLEXER		
REGISTER	FUNCTION	BITS
SREF	PLL Reference	B0-P0-R13-D[6:4]
DDSP	Clock divider	B0-P0-R27-D[6:0]
DSCLK	External SCLK Div	B0-P0-R32-D[6:0]
DLRK	External LRCK/FS Div	B0-P0-R33-D[7:0]

9.3.3.4.2 PLL Calculation

The TAS5780M device has an on-chip PLL with fractional multiplication to generate the clock frequency required by the Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input (PLLCKIN) supports clock frequencies from 1 MHz to 50 MHz and is register programmable to enable generation of required sampling rates with fine precision.

The PLL is enabled by default. The PLL can be enabled by writing to P0-R4, D[0]. When the PLL is enabled, the PLL output clock PLLCK is given by Equation 1:

$$PLLCK = \frac{PLLCKIN \times R \times J.D}{P} \quad \text{or} \quad PLLCK = \frac{PLLCKIN \times R \times K}{P} \tag{1}$$

where

- R = 1, 2, 3,4, ... , 15, 16
- J = 4,5,6, . . . 63, and D = 0000, 0001, 0002, . . . 9999
- K = [J value].[D value]
- P = 1, 2, 3, ... 15

R, J, D, and P are programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

9.3.3.4.2.1 Examples:

- If K = 8.5, then J = 8, D = 5000
- If K = 7.12, then J = 7, D = 1200
- If K = 14.03, then J = 14, D = 0300
- If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, **the following conditions must be satisfied:**

- 1 MHz ≤ (PLLCKIN / P) ≤ 20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 1 ≤ J ≤ 63

When the PLL is enabled and D ≠ 0000, **the following conditions must be satisfied:**

- 6.667 MHz ≤ PLLCLKIN / P ≤ 20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 4 ≤ J ≤ 11
- R = 1

When the PLL is enabled,

- f_S = (PLLCLKIN × K × R) / (2048 × P)
- The value of N is selected so that f_S × N = PLLCLKIN x K x R / P is in the allowable range.

Example: MCLK = 12 MHz and f_S = 44.1 kHz, (N=2048)
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example: MCLK = 12 MHz and f_S = 48.0 kHz, (N=2048)
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

Values are written to the registers in Table 4.

Table 4. PLL Registers

DIVIDER	FUNCTION	BITS
PLLE	PLL enable	P0-R4, D[0]
PPDV	PLL P	P0-R20, D[3:0]
PJDV	PLL J	P0-R21, D[5:0]
PDDV	PLL D	P0-R22, D[5:0]
		P0-R23, D[7:0]
PRDV	PLL R	P0-R24, D[3:0]

Table 5. PLL Configuration Recommendations

EQUATIONS	DESCRIPTION
f_S (kHz)	Sampling frequency
R_{MCLK}	Ratio between sampling frequency and MCLK frequency (MCLK frequency = RMCLK x sampling frequency)
MCLK (MHz)	System master clock frequency at MCLK input (pin 20)
PLL VCO (MHz)	PLL VCO frequency as PLLCK in Figure 57
P	One of the PLL coefficients in Equation 1
PLL REF (MHz)	Internal reference clock frequency which is produced by MCLK / P
M = K × R	The final PLL multiplication factor computed from K and R as described in Equation 1
K = J.D	One of the PLL coefficients in Equation 1
R	One of the PLL coefficients in Equation 1
PLL f_S	Ratio between f_S and PLL VCO frequency (PLL VCO / f_S)
DSP f_S	Ratio between operating clock rate and f_S (PLL f_S / NMAC)
NMAC	The clock divider value in Table 3
DSP CLK (MHz)	The operating frequency as DSPCK in Figure 57
MOD f_S	Ratio between DAC operating clock frequency and f_S (PLL f_S / NDAC)
MOD f (kHz)	DAC operating frequency as DACCK in
NDAC	DAC clock divider value in Table 3
DOSR	OSR clock divider value in Table 3 for generating OSRCK in Figure 57. DOSR must be chosen so that MOD f_S / DOSR = 16 for correct operation.
NCP	NCP (negative charge pump) clock divider value in Table 3
CP f	Negative charge pump clock frequency (f_S × MOD f_S / NCP)
% Error	Percentage of error between PLL VCO / PLL f_S and f_S (mismatch error). • This value is typically zero but can be non-zero especially when K is not an integer (D is not zero). • This value can be non-zero only when the TAS5780M device acts as a master.

The previous equations explain how to calculate all necessary coefficients and controls to configure the PLL. Table 6 provides for easy reference to the recommended clock divider settings for the PLL as a Master Clock.

Table 6. Recommended Clock Divider Settings for PLL as Master Clock

f_S (kHz)	R_{MCLK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
8	128	1.024	98.304	1	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	192	1.536	98.304	1	1.536	64	32	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	256	2.048	98.304	1	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	384	3.072	98.304	3	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	512	4.096	98.304	3	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	768	6.144	98.304	3	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1024	8.192	98.304	3	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1152	9.216	98.304	9	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1536	12.288	98.304	9	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	2048	16.384	98.304	9	1.82	54	54	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	3072	24.576	98.304	9	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
11.025	128	1.4112	90.3168	1	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	192	2.1168	90.3168	3	0.706	128	32	4	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	256	2.8224	90.3168	1	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	384	4.2336	90.3168	3	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	512	5.6448	90.3168	3	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	768	8.4672	90.3168	3	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1024	11.2896	90.3168	3	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1152	12.7008	90.3168	9	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1536	16.9344	90.3168	9	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	2048	22.5792	90.3168	9	2.509	36	36	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	3072	33.8688	90.3168	9	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
16	64	1.024	98.304	1	1.024	96	48	2	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	128	2.048	98.304	1	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	192	3.072	98.304	1	3.072	32	32	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	256	4.096	98.304	1	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	384	6.144	98.304	3	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	512	8.192	98.304	3	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	768	12.288	98.304	3	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1024	16.384	98.304	3	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1152	18.432	98.304	3	6.144	16	16	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1536	24.576	98.304	9	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	2048	32.768	98.304	9	3.641	27	27	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	3072	49.152	98.304	9	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536

Table 6. Recommended Clock Divider Settings for PLL as Master Clock (continued)

f_S (kHz)	R_{MCLK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
22.05	64	1.4112	90.3168	1	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	128	2.8224	90.3168	1	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	192	4.2336	90.3168	3	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	256	5.6448	90.3168	1	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	384	8.4672	90.3168	3	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	512	11.2896	90.3168	3	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	768	16.9344	90.3168	3	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1024	22.5792	90.3168	3	7.526	12	12	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1152	25.4016	90.3168	9	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1536	33.8688	90.3168	9	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	2048	45.1584	90.3168	9	5.018	18	18	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
32	32	1.024	98.304	1	1.024	96	48	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	48	1.536	98.304	1	1.536	64	16	4	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	64	2.048	98.304	1	2.048	48	24	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	128	4.096	98.304	1	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	192	6.144	98.304	3	2.048	48	48	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	256	8.192	98.304	2	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	384	12.288	98.304	3	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	512	16.384	98.304	3	5.461	18	18	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	768	24.576	98.304	3	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1024	32.768	98.304	3	10.923	9	9	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1152	36.864	98.304	9	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1536	49.152	98.304	6	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
44.1	32	1.4112	90.3168	1	1.411	64	32	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	64	2.8224	90.3168	1	2.822	32	16	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	128	5.6448	90.3168	1	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	192	8.4672	90.3168	3	2.822	32	32	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	256	11.2896	90.3168	2	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	384	16.9344	90.3168	3	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	512	22.5792	90.3168	3	7.526	12	12	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	768	33.8688	90.3168	3	11.29	8	8	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	1024	45.1584	90.3168	3	15.053	6	6	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2

Table 6. Recommended Clock Divider Settings for PLL as Master Clock (continued)

f_S (kHz)	R_{MCLK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
48	32	1.536	98.304	1	1.536	64	32	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	64	3.072	98.304	1	3.072	32	16	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	128	6.144	98.304	1	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	192	9.216	98.304	3	3.072	32	32	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	256	12.288	98.304	2	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	384	18.432	98.304	3	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	512	24.576	98.304	3	8.192	12	12	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	768	36.864	98.304	3	12.288	8	8	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	1024	49.152	98.304	3	16.384	6	6	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
96	32	3.072	98.304	1	3.072	32	16	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
	48	4.608	98.304	3	1.536	64	32	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
	64	6.144	98.304	1	6.144	16	8	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
	128	12.288	98.304	2	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	192	18.432	98.304	3	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	256	24.576	98.304	4	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	384	36.864	98.304	6	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	512	49.152	98.304	8	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536

9.3.3.5 Serial Audio Port – Data Formats and Bit Depths

The serial audio interface port is a 3-wire serial port with the signals LRCK/FS (pin 25), SCLK (pin 23), and SDIN (pin 24). SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5780M device on the rising edge of SCLK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Table 7. TAS5780M Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCK/FS FREQUENCY (kHz)	MCLK RATE (f_S)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	Up to 96	128 to 3072 (≤ 50 MHz)	64, 48, 32
TDM	32, 24, 20, 16	Up to 48	128 to 3072	125, 256
		96	128 to 512	125, 256

The TAS5780M device requires the synchronization of LRCK/FS and system clock, but does not require a specific phase relation between LRCK/FS and system clock.

If the relationship between LRCK/FS and system clock changes more than ±5 MCLK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until re-synchronization between LRCK/FS and system clock is completed.

If the relationship between LRCK/FS and SCLK are invalid more than 4 LRCK/FS periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until re-synchronization between LRCK/FS and SCLK is completed.

9.3.3.5.1 Data Formats and Master/Slave Modes of Operation

The TAS5780M device supports industry-standard audio data formats, including standard I^2S and left-justified. Data formats are selected via Register (P0-R40). All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. The data formats are detailed in Figure 60 through Figure 65.

The TAS5780M device also supports right-justified, and TDM data. I^2S, LJ, RJ, and TDM are selected using Register (P0-R40). All formats require binary 2s complement, MSB-first audio data. Up to 32 bits are accepted. Default setting is I^2S and 24 bit word length. The I^2S slave timing is shown in Figure 20.

shows a detailed timing diagram for the serial audio interface.

In addition to acting as a I^2S slave, the TAS5780M device can act as an I^2S master, by generating SCLK and LRCK/FS as outputs from the MCLK input. Table 8 lists the registers used to place the device into Master or Slave mode. Please refer to the *Serial Audio Port Timing – Master Mode* section for serial audio Interface timing requirements in Master Mode. For Slave Mode timing, please refer to the *Serial Audio Port Timing – Slave Mode* section.

Table 8. I^2S Master Mode Registers

REGISTER	FUNCTION
P0-R9-B0, B4, and B5	I^2S Master mode select
P0-R32-D[6:0]	SCLK divider and LRCK/FS divider
P0-R33-D[7:0]	

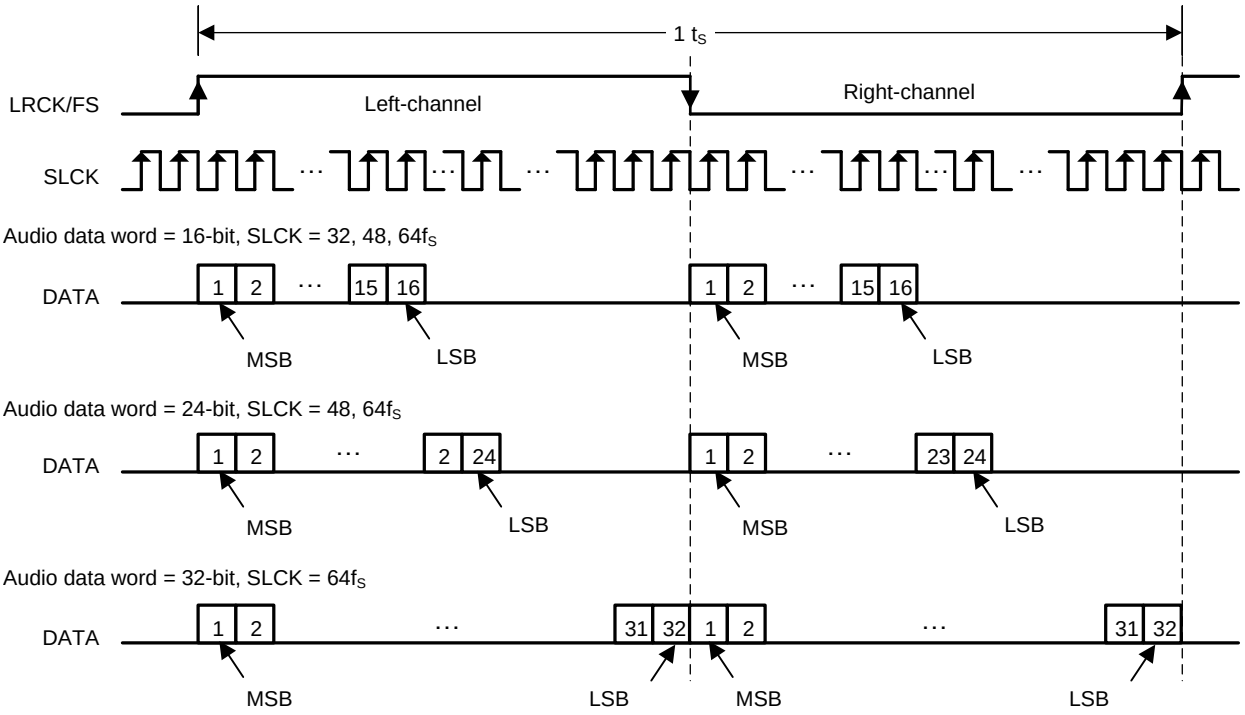
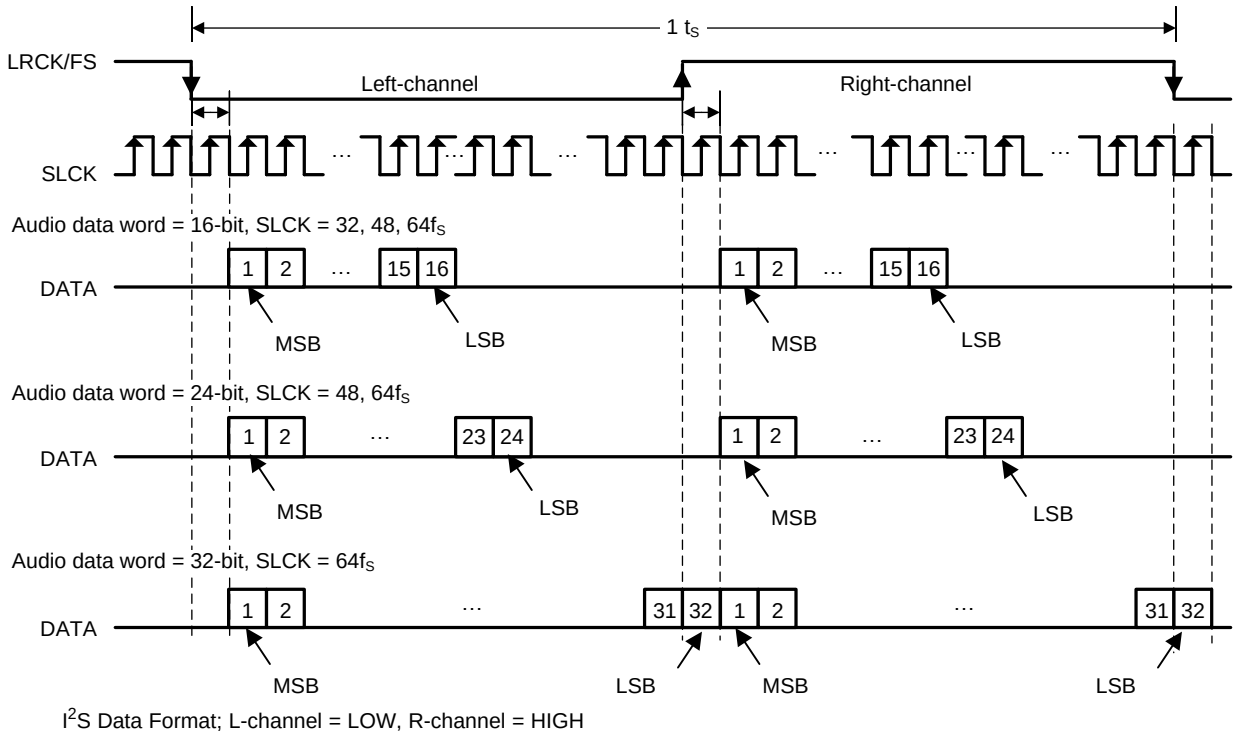


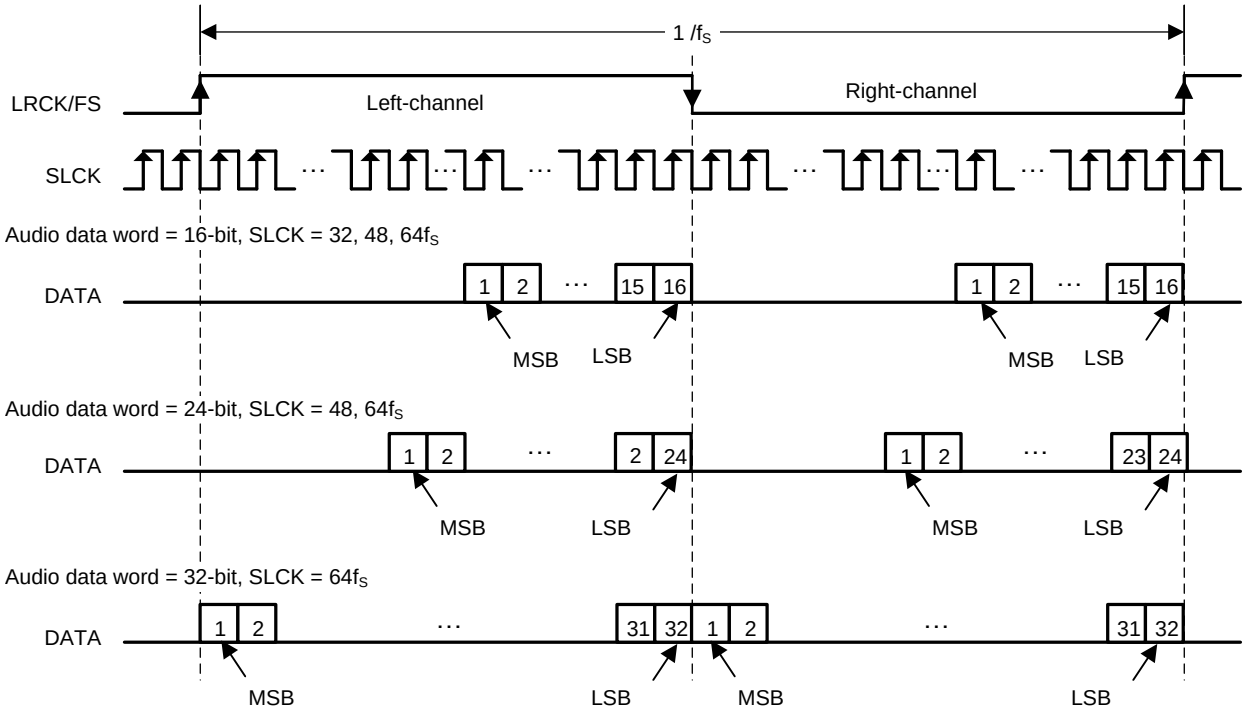
Figure 60. Left Justified Audio Data Format



I^2S Data Format; L-channel = LOW, R-channel = HIGH

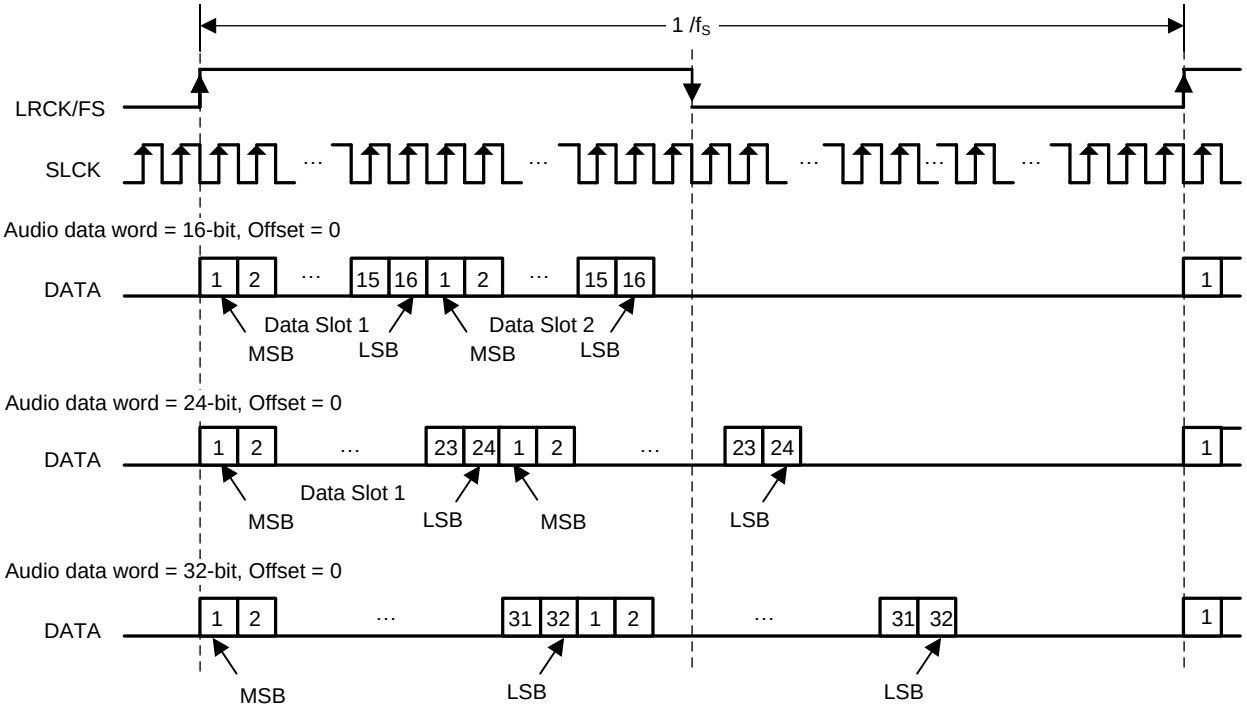
Figure 61. I^2S Audio Data Format

The following data formats are only available in software mode.



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

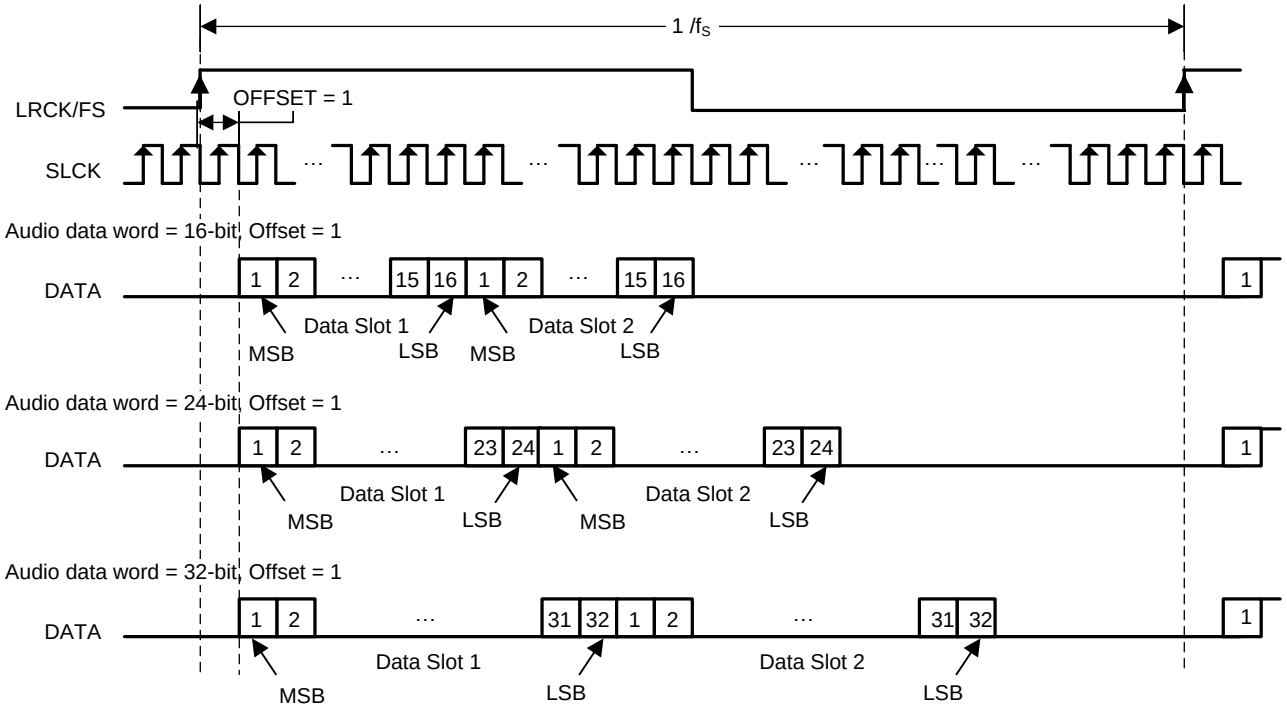
Figure 62. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

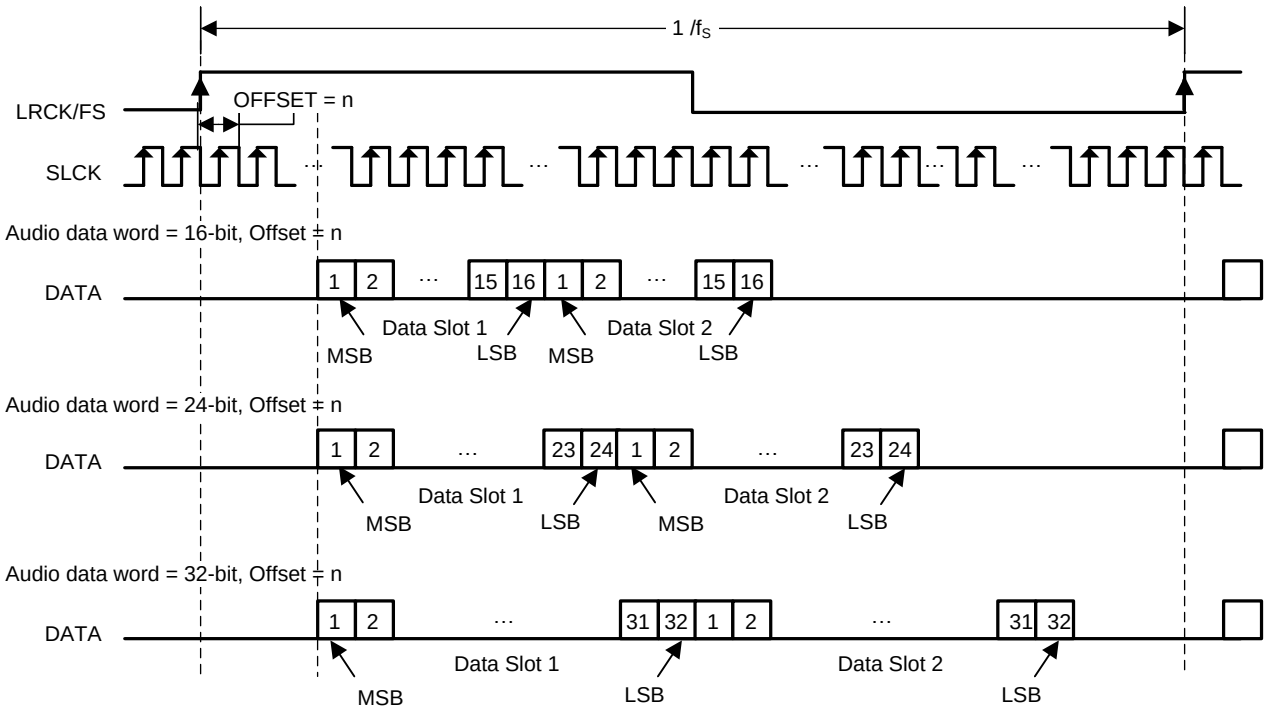
Figure 63. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 64. TDM 2 Audio Data Format



TDM Data Format with OFFSET = N

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 65. TDM 3 Audio Data Format

9.3.3.6 Input Signal Sensing (Power-Save Mode)

The TAS5780M device has a zero-detect function. The zero-detect function can be applied to both channels of data as an AND function or an OR function, via controls provided in the control port in P0-R65-D[2:1].Continuous Zero data cycles are counted by LRCK/FS, and the threshold of decision for analog mute can be set by P0-R59, D[6:4] for the data which is clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal and P0-R59, D[2:0] for the data which is clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal as shown in Table 10. Default values are 0 for both channels.

In Hardware mode, the device uses default values.

Table 9. Zero Detection Mode

ATMUTECTL	VALUE	FUNCTION
Bit : 2	0	Zero data triggers for the two channels for zero detection are ORed together.
	1 (Default)	Zero data triggers for the two channels for zero detection are ANDed together.
Bit : 1	0	Zero detection and analog mute are disabled for the data clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal.
	1 (Default)	Zero detection analog mute are enabled for the data clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal.
Bit : 0	0	Zero detection analog mute are disabled for the data clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal.
	1 (Default)	Zero detection analog mute are enabled for the data clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal.

Table 10. Zero Data Detection Time

ATMUTETIML OR ATMA	NUMBER OF LRCK/FS CYCLES	TIME at 48 kHz
0 0 0	1024	21 ms
0 0 1	5120	106 ms
0 1 0	10240	213 ms
0 1 1	25600	533 ms
1 0 0	51200	1.066 secs
1 0 1	102400	2.133 secs
1 1 0	256000	5.333 secs
1 1 1	512000	10.66 secs

9.3.4 Enable Device

To play audio after the device is powered up or reset the device must be enabled by writing book 0x00, page 0x00, register 0x02 to 0x00.

9.3.4.1 Example

The following is a sample script for enabling the device:

```
#Enable DUT
w 90 00 00 #Go to page 0
w 90 7f 00 #Go to book 0
w 90 02 00 #Enable device
```

9.3.5 Volume Control

9.3.5.1 DAC Digital Gain Control

A basic DAC digital gain control with range between 24 dB and –103 dB and mute is available on each channels by P0-R61-D[7:0] for SPK_OUTB± and P0-R62-D[7:0] for SPK_OUTA±. These volume controls all have 0.5 dB step programmability over most gain and attenuation ranges. Table 11 lists the detailed gain versus programmed setting for the basic volume control. Volume can be changed for both SPK_OUTB± and SPK_OUTA± at the same time or independently by P0-R61-D[1:0] . When D[1:0] set 00 (default), independent control is selected. When D[1:0] set 01, SPK_OUTA± accords with SPK_OUTB± volume. When D[1:0] set 10, SPK_OUTA± volume controls the volume for both channels. To set D[1:0] to 11 is prohibited.

Table 11. DAC Digital Gain Control Settings

GAIN SETTING	BINARY DATA	GAIN (dB)	COMMENTS
0	0000-0000	24.0	Positive maximum
1	0000-0001	23.5	
. . .	. . .	. . .	
46	0010-1110	1.0	
47	0010-1111	0.5	
48	0011-0000	0.0	No attenuation (default)
49	0011-0001	–0.5	
50	0011-0010	–1.0	
51	0011-0011	–1.5	
. . .	. . .	. . .	
253	1111-1101	–102.5	
254	1111-1110	–103	Negative maximum
255	1111-1111	– ∞	Negative infinite (Mute)

Ramp-up frequency and ramp-down frequency can be controlled by P0-R63, D[7:6] and D[3:2] as shown in Table 12. Also ramp-up step and ramp-down step can be controlled by P0-R63, D[5:4] and D[1:0] as shown in Table 13.

Table 12. Ramp Up or Down Frequency

RAMP UP SPEED	EVERY N f_S	COMMENTS	RAMP DOWN FREQUENCY	EVERY N f_S	COMMENTS
00	1	Default	00	1	Default
01	2		01	2	
10	4		10	4	
11	Direct change		11	Direct change	

Table 13. Ramp Up or Down Step

RAMP UP STEP	STEP dB	COMMENTS	RAMP DOWN STEP	STEP dB	COMMENTS
00	4.0		00	–4.0	
01	2.0		01	–2.0	
10	1.0	Default	10	–1.0	Default
11	0.5		11	–0.5	

9.3.5.1.1 Emergency Volume Ramp Down

Emergency ramp down of the volume is provided for situations such as I^2S clock error and power supply failure. Ramp-down speed is controlled by P0-R64-D[7:6]. Ramp-down step can be controlled by P0-R64-D[5:4]. Default is ramp-down by every f_S cycle with –4dB step.

9.3.6 Adjustable Amplifier Gain and Switching Frequency Selection

The voltage divider between the GVDD_REG pin and the SPK_GAIN/FREQ pin is used to set the gain and switching frequency of the amplifier. Upon start-up of the device, the voltage presented on the SPK_GAIN/FREQ pin is digitized and then decoded into a 3-bit word which is interpreted inside the TAS5780M device to correspond to a given gain and switching frequency. In order to change the SPK_GAIN or switching frequency of the amplifier, the PVDD must be cycled off and on while the new voltage level is present on the SPK_GAIN/FREQ pin.

Because the amplifier adds gain to both the signal and the noise present in the audio signal, the lowest gain setting that can meet voltage-limited output power targets should be used. Using the lowest gain setting ensures that the power target can be reached while minimizing the idle channel noise of the system. The switching frequency selection affects three important operating characteristics of the device. The three affected characteristics are the power dissipation in the device, the power dissipation in the inductor, and the target output filter for the application.

Higher switching frequencies typically result in slightly higher power dissipation in the TAS5780M device and lower dissipation in the inductor in the system, due to decreased ripple current through the inductor and increased charging and discharging current in device and parasitic capacitances. Switching at the higher of the available switching frequencies will result in lower overall dissipation in the system and lower operating temperature of the inductors. However, the thermally limited power output of the device can be decreased in this situation, because some of the TAS5780M device thermal headroom will be absorbed by the higher switching frequency. Conversely inductor heating can be reduced by using the higher switching frequency to reduce the ripple current.

Another advantage of increasing the switching frequency is that the higher frequency carrier signal can be filtered by an L-C filter with a higher corner frequency, leading to physically smaller components. Use the highest switching frequency that continues to meet the thermally limited power targets for the application. If thermal constraints require heat reduction in the TAS5780M device, use a lower switching rate.

The switching frequency of the speaker amplifier is dependent on an internal synchronizing signal, (f_{SYNC}), which is synchronous with the sample rate. The rate of the synchronizing signal is also dependent on the sample rate. Refer to Table 14 below for details regarding how the sample rates correlate to the synchronizing signal.

Table 14. Sample Rates vs Synchronization Signal

SAMPLE RATE [kHz]	f_{SYNC} [kHz]
8	96
16	
32	
48	
96	
192	
11.025	88.2
22.05	
44.1	
88.2	

Table 15 summarizes the de-code of the voltage presented to the SPK_GAIN/FREQ pin. The voltage presented to the SPK_GAIN/FREQ pin is latched in upon startup of the device. Subsequent changes require power cycling the device. A gain setting of 20 dB is recommended for nominal supply voltages of 13 V and lower, while a gain of 26 dB is recommended for supply voltages up to 26.4 V. Table 15 shows the voltage required at the SPK_GAIN/FREQ pin for various gain and switching scenarios as well some example resistor values for meeting the voltage range requirements.

Table 15. Amplifier Switching Mode vs. SPK_GAIN/FREQ Voltage

$V_{SPK\_GAIN/FREQ}$ (V)		RESISTOR EXAMPLES	GAIN MODE	AMPLIFIER SWITCHING FREQUENCY MODE
MIN	MAX	R100 (kΩ): RESISTOR TO GROUND R101 (kΩ): RESISTOR TO GVDD_REG		
6.61	7	Reserved	Reserved	Reserved
5.44	6.6	R100 = 750 R101 = 150	26 dBV	8 × f_{SYNC}
4.67	5.43	R100 = 390 R101 = 150		6 × f_{SYNC}
3.89	4.66	R100 = 220 R101 = 150		5 × f_{SYNC}
3.11	3.88	R100 = 150 R101 = 150		4 × f_{SYNC}
2.33	3.1	R100 = 100 R101 = 150	20 dBV	8 × f_{SYNC}
1.56	2.32	R100 = 56 R101 = 150		6 × f_{SYNC}
0.78	1.55	R100 = 33 R101 = 150		5 × f_{SYNC}
0	0.77	R100 = 8.2 R101 = 150		4 × f_{SYNC}

9.3.7 Error Handling and Protection Suite

9.3.7.1 Device Overtemperature Protection

The TAS5780M device continuously monitors die temperature to ensure the temperature does not exceed the OTE_{THRES} level specified in the *Recommended Operating Conditions* table. If an OTE event occurs, the SPK_FAULT line is pulled low and the SPK_OUTxx outputs transition to high impedance, signifying a fault. This is a non-latched error and the device will attempt to self clear after $OTE_{CLRTIME}$ has passed.

9.3.7.2 SPK_OUTxx Overcurrent Protection

The TAS5780M device continuously monitors the output current of each amplifier output to ensure the output current does not exceed the OCE_{THRES} level specified in the *Recommended Operating Conditions* table. If an OCE event occurs, the SPK_FAULT line is pulled low and the SPK_OUTxx outputs transition to high impedance, signifying a fault. This is a non-latched error and the device will attempt to self clear after $OCE_{CLRTIME}$ has passed.

9.3.7.3 Internal V_{AVDD} Undervoltage-Error Protection

The TAS5780M device internally monitors the AVDD net to protect against the AVDD supply dropping unexpectedly. To enable this feature, P1-R5-B0 is used.

9.3.7.4 Internal V_{PVDD} Undervoltage-Error Protection

If the voltage presented on the PVDD supply drops below the $UVE_{THRES(PVDD)}$ value listed in the *Recommended Operating Conditions* table, the SPK_OUTxx outputs transition to high impedance. This is a self-clearing error, which means that once the PVDD level drops below the level listed in the *Recommended Operating Conditions* table, the device resumes normal operation.

9.3.7.5 Internal V_{PVDD} Overvoltage-Error Protection

If the voltage presented on the PVDD supply exceeds the $OVE_{THRES(PVDD)}$ value listed in the *Recommended Operating Conditions* table, the SPK_OUTxx outputs will transition to high impedance. This is a self-clearing error, which means that once the PVDD level drops below the level listed in the *Recommended Operating Conditions* table, the device will resume normal operation.

NOTE

The voltage presented on the PVDD supply only protects up to the level described in the *Recommended Operating Conditions* table for the PVDD voltage. Exceeding the absolute maximum rating may cause damage and possible device failure, because the levels exceed that which can be protected by the OVE protection circuit.

9.3.7.6 External Undervoltage-Error Protection

The $\overline{\text{SPK\_MUTE}}$ pin can also be used to monitor a system voltage, such as a LCD TV backlight, a battery pack in portable device, by using a voltage divider created with two resistors (see Figure 66).

- If the $\overline{\text{SPK\_MUTE}}$ pin makes a transition from 1 to 0 over 6 ms or more, the device switches into external undervoltage protection mode, which uses two trigger levels.
- When the $\overline{\text{SPK\_MUTE}}$ pin level reaches 2 V, soft mute process begins.
- When the $\overline{\text{SPK\_MUTE}}$ pin level reaches 1.2 V, analog output mute engages, regardless of digital audio level, and analog output shutdown begins.

Figure 67 shows a timing diagram for external undervoltage error protection.

NOTE

The $\overline{\text{SPK\_MUTE}}$ input pin voltage range is provided in the *Recommended Operating Conditions* table. The ratio of external resistors must produce a voltage within the provided input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the $\overline{\text{SPK\_MUTE}}$ pin higher than the level specified in the *Recommended Operating Conditions* table, potentially causing damage to or failure of the device. Therefore, any monitored voltage (including all ripple, power supply variation, resistor divider variation, transient spikes, and others) must be scaled by the resistor divider network to never drive the voltage on the $\overline{\text{SPK\_MUTE}}$ pin higher than the maximum level specified in the *Recommended Operating Conditions* table.

When the divider is set correctly, any DC voltage can be monitored. Figure 66 shows a 12-V example of how the $\overline{\text{SPK\_MUTE}}$ is used for external undervoltage error protection.

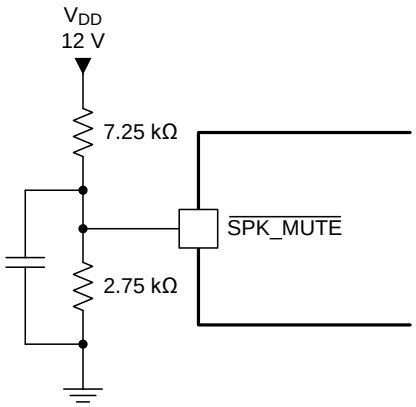


Figure 66. $\overline{\text{SPK\_MUTE}}$ Used in External Undervoltage Error Protection

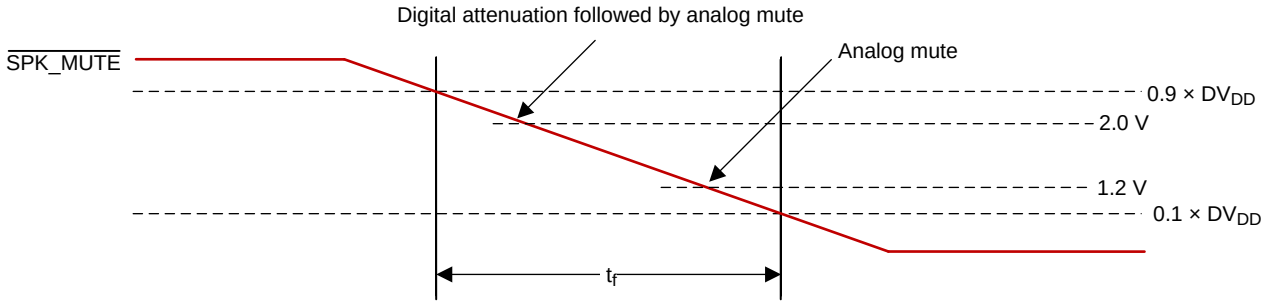


Figure 67. $\overline{\text{SPK\_MUTE}}$ Timing for External Undervoltage Error Protection

9.3.7.7 Internal Clock Error Notification (CLKE)

When a clock error is detected on the incoming data clock, the TAS5780M device switches to an internal oscillator and continues to the drive the DAC, while attenuating the data from the last known value. Once this process is complete, the DAC outputs will be hard muted to the ground and the class D PWM output will stop switching. The clock error can be monitored at B0-P0-R94 and R95. The clock error status bits are non-latching, except for MCLK halted B0-P0-R95-D[4] and CERF B0-P0-R95-D[0] which are cleared when read.

9.3.8 GPIO Port and Hardware Control Pins

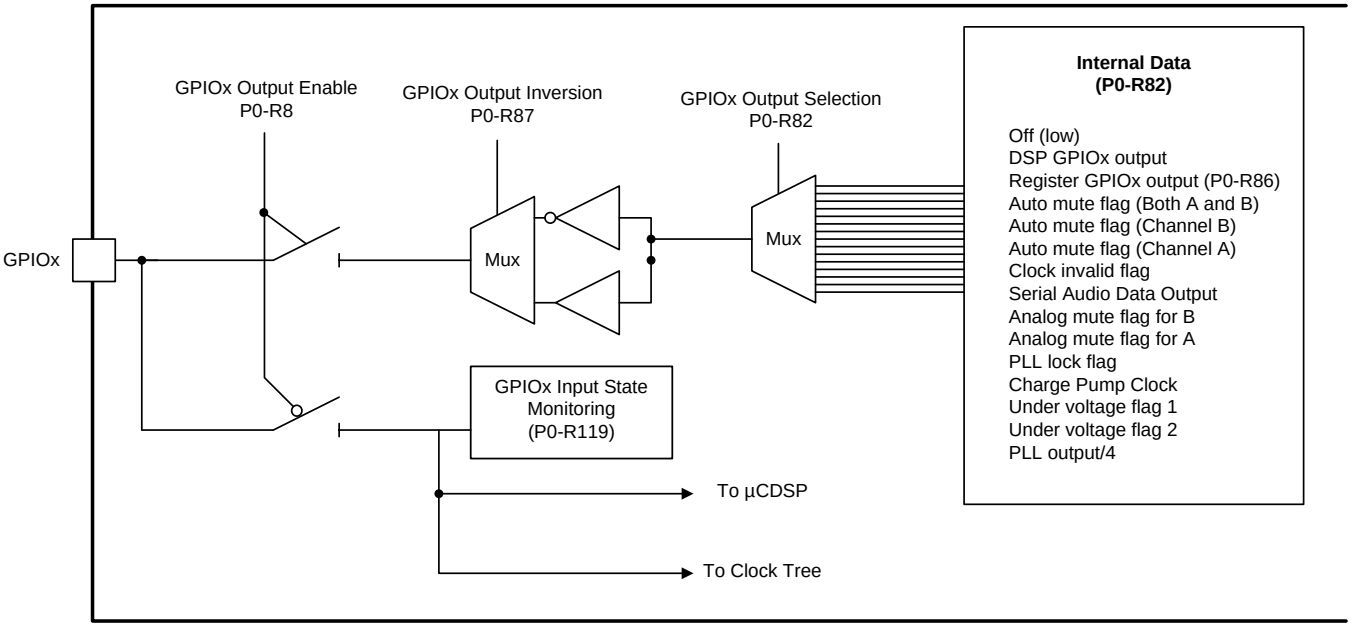


Figure 68. GPIO Port

9.3.9 I²C Communication Port

The TAS5780M device supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device. Because the TAS5780M register map spans several books and pages, the user must select the correct book and page before writing individual register bits or bytes. Changing from book to book is accomplished by first changing to page 0x00 by writing 0x00 to register 0x00 and then writing the book number to register 0x7f of page 0. Changing from page to page is accomplished via register 0x00 on each page. The register value selects the register page, from 0 to 255.

9.3.9.1 Slave Address

Table 16. I²C Slave Address

MSB							LSB
1	0	0	1	1	ADR2	ADR1	R/ $\overline{W}$

The TAS5780M device has 7 bits for the slave address. The first five bits (MSBs) of the slave address are factory preset to 10011 (0x9x). The next two bits of the address byte are the device select bits which can be user-defined by the ADR1 and ADR0 terminals. A maximum of four devices can be connected on the same bus at one time, which gives a range of 0x90, 0x92, 0x94 and 0x96, as detailed in Table 17. Each TAS5780M device responds when it receives the slave address.

Table 17. I²C Address Configuration via ADR0 and ADR1 Pins

ADR1	ADR0	I²C SLAVE ADDRESS [R/$\overline{W}$]
0	0	0x90
0	1	0x92
1	0	0x94
1	1	0x96

9.3.9.2 Register Address Auto-Increment Mode

Auto-increment mode allows multiple sequential register locations to be written to or read back in a single operation, and is especially useful for block write and read operations. The TAS5780M device supports auto-increment mode automatically. Auto-increment stops at page boundaries.

9.3.9.3 Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The TAS5780M device supports only slave receivers and slave transmitters.

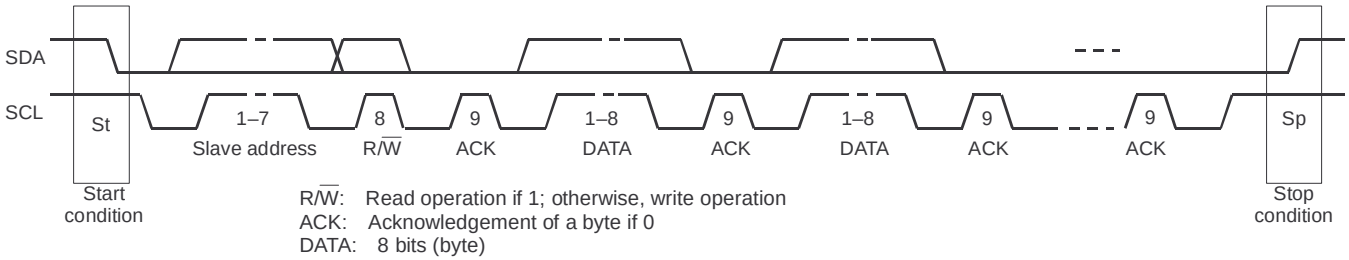


Figure 69. Packet Protocol

Table 18. Write Operation - Basic I²C Framework

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK		ACK	Sp

Table 19. Read Operation - Basic I²C Framework

Transmitter	*M*	*M*	*M*	*S*	*S*	*M*	*S*	*M*		*M*	*M*
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK		NACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition

9.3.9.4 Write Register

A master can write to any TAS5780M device registers using single or multiple accesses. The master sends a TAS5780M device slave address with a write bit, a register address, and the data. If auto-increment is enabled, the address is that of the starting register, followed by the data to be transferred. When the data is received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 20 shows the write operation.

Table 20. Write Operation

Transmitter	*M*	*M*	*M*	*S*	*M*		*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	write data 1	ACK	write data 2	ACK		ACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition; W = Write; ACK = Acknowledge

9.3.9.5 Read Register

A master can read the TAS5780M device register. The value of the register address is stored in an indirect index register in advance. The master sends a TAS5780M device slave address with a read bit after storing the register address. Then the TAS5780M device transfers the data which the index register points to. When auto-increment is enabled, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 21 lists the read operation.

Table 21. Read Operation

Transmitter	*M*	*M*	*M*	*S*	*M*		*S*	*M*	*M*	*M*	*S*	*S*	*M*		*M*	*M*
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	Sr	slave addr	R	ACK	data	ACK		NACK	Sp

M = Master Device; S = Slave Device; St = Start Condition; Sr = Repeated start condition; Sp = Stop Condition; W = Write; R = Read; NACK = Not acknowledge

9.3.9.6 DSP Book, Page, and Register Update

The DSP memory is arranged in books, pages, and registers. Each book has several pages and each page has several registers.

9.3.9.6.1 Book and Page Change

To change the book, the user must be on page 0x00. In register 0x7f on page 0x00 you can change the book. On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

9.3.9.6.2 Swap Flag

The swap flag is used to copy the audio coefficient from the host memory to the DSP memory. The swap flag feature is important to maintain the stability of the BQs. A BQ is a closed-loop system with 5 coefficients. To avoid instability in the BQ in an update transition between two different filters, update all five parameters within one audio sample. The internal swap flag insures all 5 coefficients for each filter are transferred from host memory to DSP memory occurs within an audio sample. The swap flag stays high until the full host buffer is transferred to DSP memory. Updates to the Host buffer should not be made while the swap flag is high.

All writes to book 0x8C from page 0x1B and register 0x58 through page 0x22 and register 0x1C require the swap flag. The swap flag is located in book 0x8C, page 0x01, and register 0x10 and must be set to 0x00 00 00 01 for a swap.

9.3.9.6.3 Example Use

The following is a sample script for using the DSP host memory to change the fine volume on the device on I^2C slave address 0x90 to the default value of 0 dB:

```
w 90 00 00 #Go to page 0
w 90 7f 8C #Change the book to 0x8C
w 90 00 21 #Go to page 0x21
w 90 21 48 00 00 00 #Fine volume Left
w 90 21 4C 00 00 00 #Fine volume Right
#Run the swap flag for the DSP to work on the new coefficients
w 90 00 00 #Go to page 0
w 90 7f 8C #Change the book to 0x8C
w 90 00 01 #Go to page 0x01
w 90 10 00 00 00 01 #Swap flag
```

9.4 Device Functional Modes

Because the TAS5780M device is a highly configurable device, numerous modes of operation can exist for the device. For the sake of succinct documentation, these modes are divided into two modes:

- Fundamental operating modes
- Secondary usage modes

Fundamental operating modes are the primary modes of operation that affect the major operational characteristics of the device, which are the most basic configurations that are chosen to ensure compatibility with the intended application or the other components that interact with the device in the final system. Some examples of the operating modes are the communication protocol used by the control port, the output configuration of the amplifier, or the Master/Slave clocking configuration.

The fundamental operating modes are described starting in the *Serial Audio Port Operating Modes* section.

Secondary usage modes are best described as modes of operation that are used after the fundamental operating modes are chosen to fine tune how the device operates within a given system. These secondary usage modes can include selecting between left justified and right justified Serial Audio Port data formats, or enabling some slight gain/attenuation within the DAC path. Secondary usage modes are accomplished through manipulation of the registers and controls in the I^2C control port. Those modes of operation are described in their respective register/bit descriptions and, to avoid redundancy, are not included in this section.

9.4.1 Serial Audio Port Operating Modes

The serial audio port in the TAS5780M device supports industry-standard audio data formats, including I^2S, Time Division Multiplexing (TDM), Left-Justified (LJ), and Right-Justified (RJ) formats. To select the data format that will be used with the device, controls are provided on P0-R40. The timing diagrams for the serial audio port are shown in the *Serial Audio Port Timing – Slave Mode* section, and the data formats are shown in the *Serial Audio Port – Data Formats and Bit Depths* section.

9.4.2 Communication Port Operating Modes

The TAS5780M device is configured via an I^2C communication port. The device does not support a hardware only mode of operation, nor Serial Peripheral Interface (SPI) communication. The I^2C Communication Protocol is detailed in the *I^2C Communication Port* section. The I^2C timing requirements are described in the *I^2C Bus Timing – Standard* and *I^2C Bus Timing – Fast* sections.

9.4.3 Speaker Amplifier Operating Modes

The TAS5780M device can be used in two different amplifier configurations:

- Stereo Mode
- Mono Mode

9.4.3.1 Stereo Mode

The familiar stereo mode of operation uses the TAS5780M device to amplify two independent signals, which represent the left and right portions of a stereo signal. These amplified left and right audio signals are presented on differential output pairs shown as SPK_OUTA± and SPK_OUTB±. The routing of the audio data which is presented on the SPK_OUTxx outputs can be changed according to the Audio Process Flow which is used and the configuration of registers P0-R42-D[5:4] and P0-R42-D[1:0]. The familiar stereo mode of operation is shown in .

By default, the TAS5780M device is configured to output the Right frame of a I^2S input on the Channel A output and the left frame on the Channel B output.

9.4.3.2 Mono Mode

The mono mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the audio output channel. This is also known as Parallel Bridge Tied Load (PBTL).

Device Functional Modes (continued)

On the output side of the TAS5780M device, the summation of the devices can be done before the filter in a configuration called Pre-Filter PBTL. However, the two outputs may be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. This process is called *Post-Filter PBTL*. Both variants of mono operation are shown in Figure 70 and Figure 71.

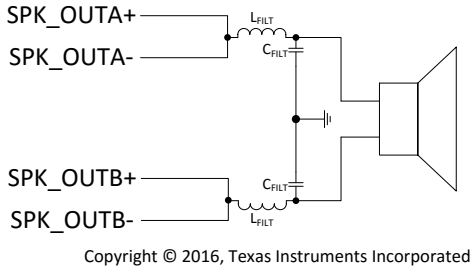


Figure 70. Pre-Filter PBTL

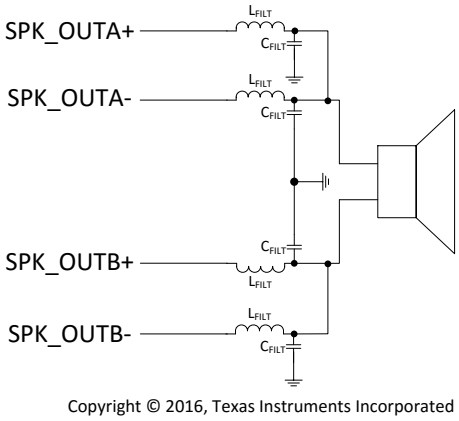


Figure 71. Post-Filter PBTL

On the input side of the TAS5780M device, the input signal to the mono amplifier can be selected from the any slot in a TDM stream or the left or right frame from an I²S, LJ, or RJ signal. The TAS5780M device can also be configured to amplify some mixture of two signals, as in the case of a subwoofer channel which mixes the left and right channel together and sends the mixture through a low-pass filter to create a mono, low-frequency signal.

The mono mode of operation is shown in the *Mono (PBTL) Systems* section.

9.4.3.3 Master and Slave Mode Clocking for Digital Serial Audio Port

The digital audio serial port in the TAS5780M device can be configured to receive clocks from another device as a serial audio slave device. The slave mode of operation is described in the *Clock Slave Mode with SCLK PLL to Generate Internal Clocks (3-Wire PCM)* section. If no system processor is available to provide the audio clocks, the TAS5780M device can be placed into Master Mode. In master mode, the TAS5780M device provides the clocks to the other audio devices in the system. For more details regarding the Master and Slave mode operation within the TAS5780M device, see the *Serial Audio Port Operating Modes* section.

9.5 Programming

9.5.1 Audio Processing Features

The TAS5780M device includes audio processing to optimize the audio performance of the audio system into which they are integrated. The TAS5780M device has 12 Biquad Filters for speaker response tuning, One dual band DPEQ to dynamically adjust the equalization curve that is applied to low-level signal and the curve that is applied to high level signals. A 2-band advanced DRC + AGL structure limits the output power of the amplifier for two regions while controlling the peaking that can occur in the crossover region during compression. A fine volume control is provided to finely adjust the output level of the amplifier based upon the system level considerations faced by the product development engineer.

The TAS5780M device has two signal monitoring options available, the level meter and the serial data out signal. The level meter monitors the signal level through an alpha filter and presents the signal in an I²C register. The level meter signal is taken before the 4x interpolation which occurs before the digital-to-analog conversion.

The SDOUT signal can be presented on any one of the GPIOx pins. Customarily, as is the case in all of the TI evaluation hardware for the TAS5780M device, GPIO2 is used.

The details of the audio processing flow, including the I²C control port registers associated with each block, are shown in .

Programming (continued)

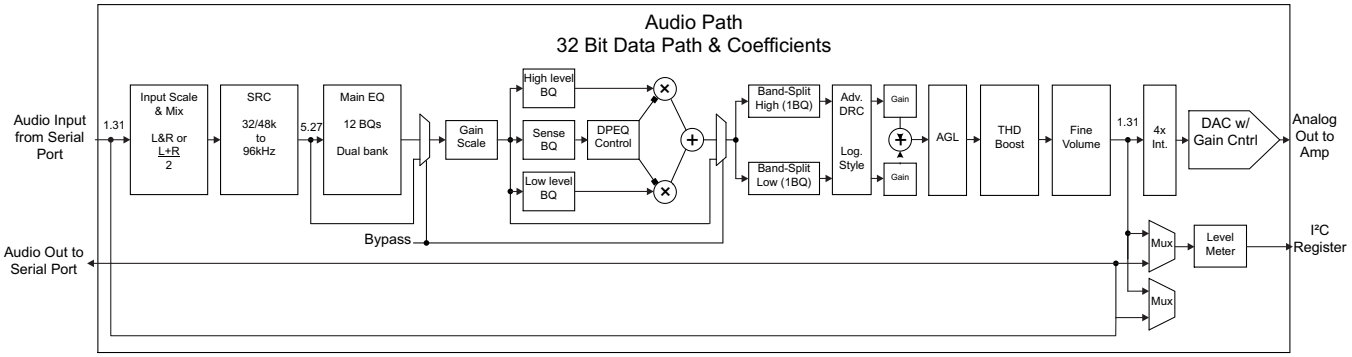


Figure 72. Fixed-Function Process Flow found in the TAS5780M

9.5.2 Processing Block Description

The processing block shown in the above is comprised of the following major blocks:

- Input scale and mixer
- Sample Rate Converter (SRC)
- Parametric Equalizers (PEQs)
- BQs Gain Scale
- Dynamic Parametric Equalizer (DPEQ)
- Two-Band Dynamic Ranger Control (DRC)
- Automatic Gain Limiter (AGL)
- Fine Volume
- Level Meter
- THD Management

9.5.2.1 Input Scale and Mixer

The input mixer can be used to mix the left and right channel input signals as shown in Figure 73. The input mixer has four coefficients, which control the mixing and gains of the input signals. When mixing and scaling the input signals, ensure that at maximum input level the input mixer outputs don't exceed 0 dBFS, which will overdrive the SRC inputs.

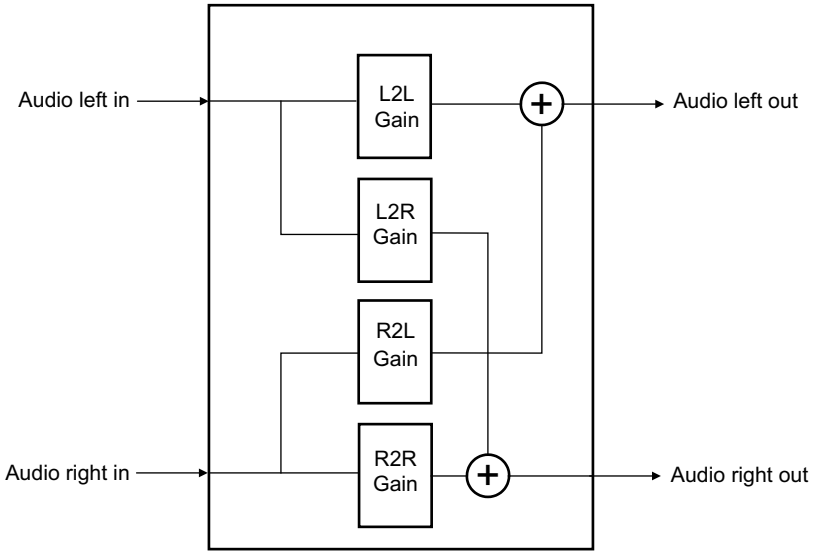


Figure 73. Input Scale and Mixer

Programming (continued)

9.5.2.1.1 Example

The following is a sample script for setting up the both left and right channels for (½L + ½R) or (L + R) / 2:

```
w 90 00 00 # Go to page 0
w 90 7f 8C #Change the book to 0x8C
w 90 00 21 #Go to page 0x21
w 90 50 00 40 26 E7 #Input mixer left in to left out gain
w 90 54 00 40 26 E7 #Input mixer right in to left out gain
w 90 58 00 40 26 E7 #Input mixer left in to right out gain
w 90 5C 00 40 26 E7 #Input mixer right in to right out gain
#Run the swap flag for the DSP to work on the new coefficients
w 90 00 00 #Go to page 0
w 90 7f 8C #Change the book to 0x8C
w 90 00 01 #Go to page 0x05
w 90 10 00 00 00 01 #Swap flag
```

9.5.2.2 Sample Rate Converter

The sample rate converter supports 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz and 96 kHz input sample rates. These input sample rates are converted to 88.2 or 96 kHz sample rate. The sample rate detection doesn't distinguish between sample rates from 32 to 48 kHz. These sample rates are treated as 48 kHz by the sample rate converter. The detected sample rate can be read at book 0x78 page 0x0C register 0x5C. The input sample rate is 88.2 or 96 kHz at register 0x5C which reads 0x00 00 00 01. The input sample rate is 32 to 48 kHz at register 0x5C which reads 0x00 00 00 02. Input sample rate 32 kHz requires changing the interpolation setting from 2x to 3x by writing B0-P0-R37-D7 to 1. The device must be placed in standby mode for this change to take effect.

Table 22. Sample Rate Detection

SAMPLING RATE (KHZ)	B0-P0-R91-D[6:4]
8	001
16	010
32 – 48	011
88.2 – 96	100

Even though the sample rate converter supports 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz and 96 kHz input sample rates, the TAS5780M device supports all input sample rates shown in Table 22 in 1x interpolation mode, base rate processing.

The SRC input should not be overdriven. Making the maximum signal level into the SRC –0.5dBFs is recommended to prevent overdriving the SRC and causing audio artifacts. The input scale and mixer can be used to attenuate or boost the maximum input signal to –0.5dBFs. The processing block has several blocks after the SRC where the signal can be compensate for any gain attenuation done in the input mixer and scale block to prevent over driving the SRC.

9.5.2.3 Parametric Equalizers (PEQ)

The device supports 12 individual tuned PEQs for left channel and 12 individual tuned PEQs for the right channel. The PEQs are implemented using cascaded "direct form 1" BQs structures as shown in Figure 74.

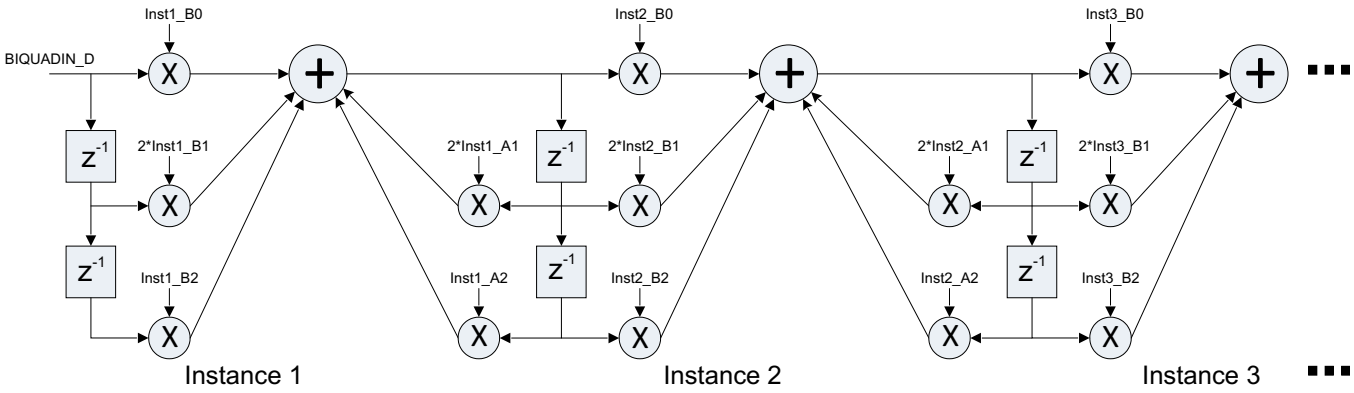


Figure 74. Cascaded BQ Structure

$$H(z) = \frac{b_0 + b_1 Z^{-1} + b_2 Z^{-2}}{a_0 + a_1 Z^{-1} + a_2 Z^{-2}} \quad (2)$$

All BQ coefficients are normalized with a0 to insure that a0 is equal to 1. The structure requires 5 BQ coefficients as shown in Table x. Any BQ with coefficients greater than 1 undergoes gain scaling as described in *BQ Gain Scale*.

Table 23. BQ Coefficients Normalization

BQ COEFFICIENT FOR TAS5780M	COEFFICIENT CALCULATION
B0_DSP	b0 / a0
B1_DSP	b1 / (a0 × 2)
B2_DSP	b2 / a0
A1_DSP	–a1 / (a0 × 2)
A2_DSP	–a2 / a0

9.5.2.4 BQ Gain Scale

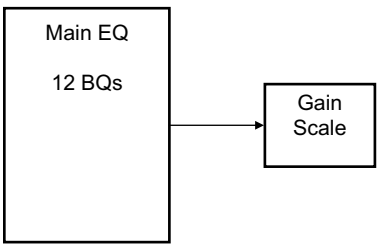


Figure 75. PEQs and BQs Gain Scale Block

The BQ coefficients format is as follows: The first BQ has B0 = 5.x, B1 = 6.x, B2 = 5.x, A1 = 2.x, and A2 = 1.x. The rest of the BQ have this format: B0 = 1.x, B1 = 2.x, B2 = 1.x, A1 = 2.x, and A2 = 1.x. This formatting maintains the highest possible resolution and noise performance. The 1.31 format restricts the ability to do high gains within the BQs and as a result requires gain compensation for the restriction. When generating BQ coefficients, ensure none of the BQ coefficients is greater than 1 by implementing gain compensation. The Gain compensation reduces the BQ coefficients gain to ensure all BQ coefficients are less than 1. The reduced gain is then reapplied in the subsequent gain scale block.

Gain compensation takes the maximum value of B0_DSP, B1_DSP, and B2_DSP after the BQ normalization shown in Table 23 is implemented. All the B coefficients are divided by maximum B coefficient value then multiplied by 0.999999999534339 (the nearest two's complement 32-bit number to 1). The following calculations are done for each BQ in the PEQ block:

$$Max\_k = \max(B0\_DSP, B1\_DSP, B2\_DSP) \quad (3)$$

$$k\_BQX = Max\_k \quad (4)$$

$$B0\_DSP = \frac{B0\_DSP}{k\_BQX} \quad (5)$$

$$B1\_DSP = \frac{B1\_DSP}{k\_BQX} \quad (6)$$

$$B2\_DSP = \frac{B2\_DSP}{k\_BQX} \quad (7)$$

The calculations above insure all DSP BQ coefficients are in a 1.31 format. The reduced gains in the BQ 1.31 format is compensation for in the gain scale block. The following calculation is done for each channel.

k_BQ = k_BQ1 × k_BQ2 × k_BQ3 × k_BQ4 × k_BQ5 × k_BQ6 × k_BQ7 × k_BQ8 × k_BQ9 × k_BQ10 × k_BQ11 × k_BQ12 (8)

The calculated k_BQ compensation value is then applied to the BQ gain scale in an 8.24 format. The BQ gain scale can also be used for volume control before the DRCs. The block can be considered as *BQ gain scale and volume gain block*. When the BQ gain scale block is used for volume control the coefficient value must be calculated as follows:

$$Gain\_BQ\_V = 10^{\frac{Volume}{20}} \times k\_BQ \quad (9)$$

where

- Volume is in dB

The BQ gain scale coefficients are located in book 0x8C, page 0x1F register 0x58 for left and register 0x5C for right.

The Bypass EQ Mux allows the user to bypass all processing. The Bypass EQ mux is at Page 0x21, Register 0x64. The Gang Left / Right mux forces the left processing to be the same as the right processing. The Gang Left / Right Mux is located at Page 0x21, Register 0x68.

9.5.2.5 Dynamic Parametric Equalizer (DPEQ)

The dynamic parametric equalizer mixes the audio signals routed through two paths containing one BQ each based upon the signal level detected by the sense path, as shown in Figure 76. The sense path contains one BQ, which can be used to focus the DPEQ sensing on a specific frequency bandwidth. An alpha filter structure is used to sense the energy in the sense path and setting the dynamic mixing ratios.

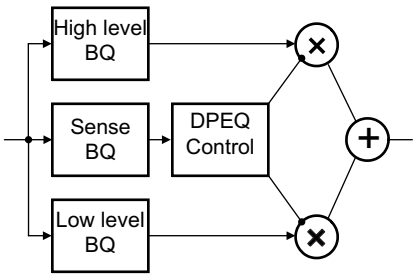


Figure 76. DPEQ Signal Path

The dynamic mixing is controlled by offset, gain, and alpha coefficients in a 1.31 format. The alpha coefficient controls the average time constant in ms of the signal data in the sense path. The offset and gain coefficients control the dynamic mixing thresholds shown in Figure 77.

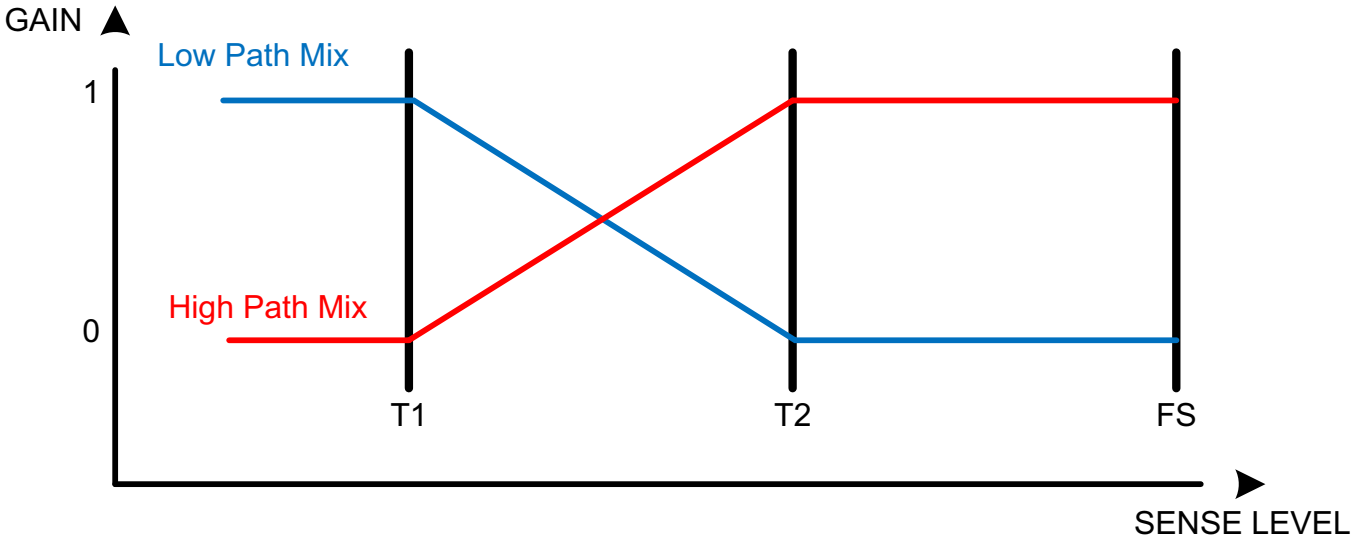


Figure 77. Dynamic Mixing

The offset, gain and alpha coefficients are calculated as follows:

$$T1\_Linear = 10^{\frac{T1}{20}} \quad (10)$$

$$T2\_Linear = 10^{\frac{T2-6}{20}}$$

where

- T2 ≥ –20 dB

$$T2\_Linear = 10^{\frac{T2}{20}} \quad (11)$$

where

- T2 < –20 dB

$$Offset = -T1\_Linear \quad (12)$$

$$Gain = \frac{1}{32(T2\_Linear - T1\_Linear)} \quad (13)$$

$$Alpha = 1 - e^{\frac{-1000}{time\ constant \times Fs}} \quad (14)$$

where

- T1 and T2 are in dB
- The time constant is in ms (15)

The DPEQ control coefficients are located in book 0x8C, page0x20. Register 0x58 is alpha coefficient, register 0x5C is gain coefficient and register 0x60 is offset coefficient.

The high level path BQ, low level path BQ, and sense path BQ coefficients use a 1.31 format as shown in Table 25. The DPEQ BQs don't have a gain scale to compensate for any BQ gain reduction due to the requirements of the 1.31 format. During tuning, the reduced gain can be compensated by using the BQ gain scale or the DRC offset coefficient.

The DPEQ sense gain scale is located in the sensing path. The DPEQ sense gain scale can be used to shift the dynamic mixing thresholds by changing the signal level in the sensing path. A positive dB gain shifts the dynamic mixing thresholds down by the gain amount and a negative dB gain shifts the dynamic mixing thresholds up by the gain amount.

9.5.2.6 Two-Band Dynamic Range Control

The Dynamic Range Control (DRC) is a feed-forward mechanism that can be used to automatically control the audio signal amplitude or the dynamic range within specified limits. The dynamic range control is done by sensing the audio signal level using an estimate of the alpha filter energy then adjusting the gain based on the region and slope parameters that are defined. The Dynamic Range Control is shown in Figure 78.

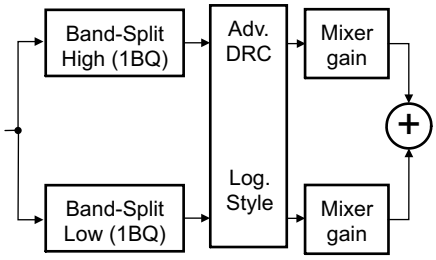


Figure 78. Dynamic Range Control

The DRCs have seven programmable transfer function parameters each: k0, k1, k2, T1, T2, OFF1, and OFF2. The T1 and T2 parameters specify thresholds or boundaries of the three compression or expansion regions in terms of input level. The Parameters k0, k1, and k2 define the gains or slopes of curves for each of the three regions. The parameters OFF1 and OFF2 specify the offset shift relative 1:1 transfer function curve at the thresholds T1 and T2 respectively shown in Figure 79.

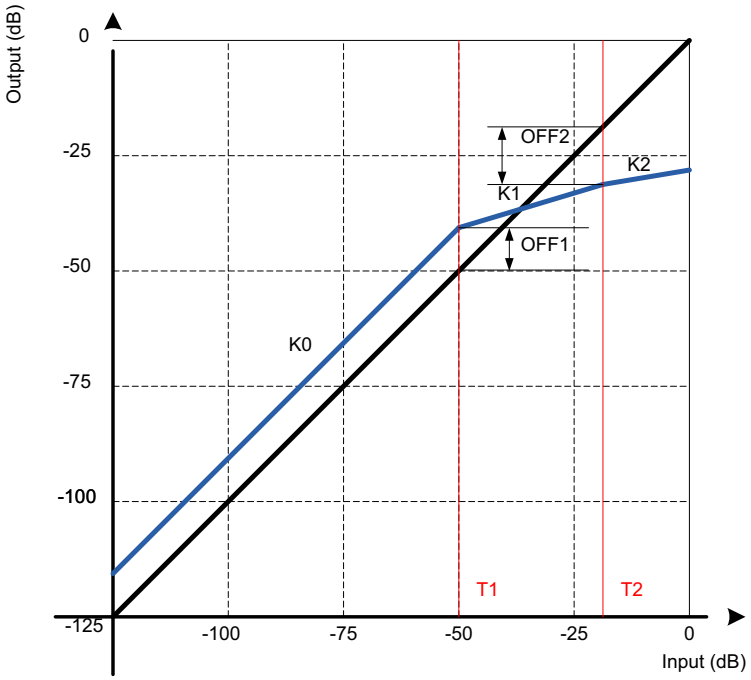


Figure 79. DRC Transfer Function Example Plot

The two-band dynamic range control is comprised of two DRCs that can be spilt into two bands using the BQ at the input of each band. The frequency where the two bands are spilt is referred to as the crossover frequency. The crossover frequency is the cut off frequency for the low pass filter used to create the low band and the cut off frequency for the high pass filter used to create the high band.

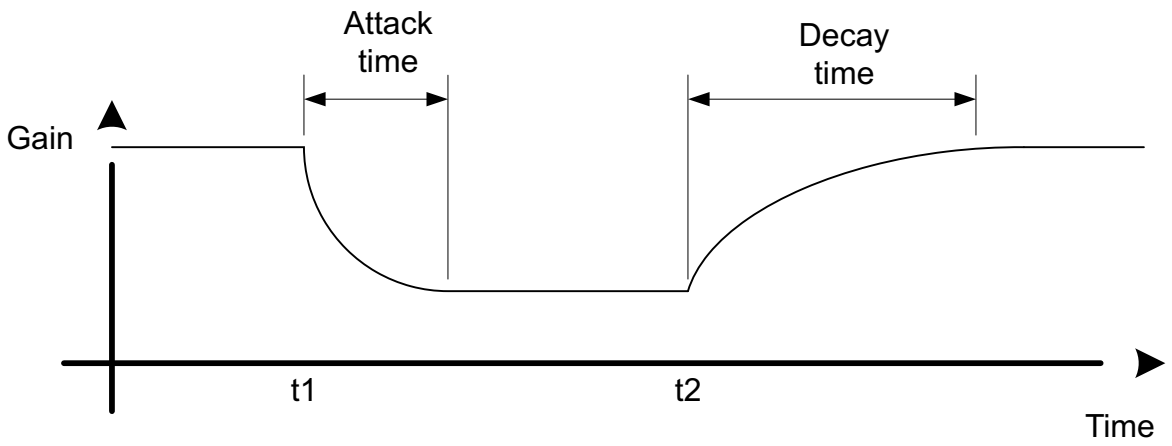


Figure 80. DRC Attack and Decay

The DRC in each band is equipped with individual energy, attack, and decay time constants. The DRC time constants control the transition time of changes and decisions in the DRC gain during compression or expansion. The energy, attack, and decay time constants affect the sensitivity level of the DRC. The shorter the time constant, the more aggressive the DRC response and vice versa.

9.5.2.7 Automatic Gain Limiter

The Automatic Gain Limiter (AGL) is a feedback mechanism that can be used to automatically control the audio signal amplitude or dynamic range within specified limits. The automatic gain limiting is done by sensing the audio signal level using an alpha filter energy structure shown in Figure 82 at the output of the AGL then adjusting the gain based on the whether the signal level is above or below the defined threshold. Three decisions made by the AGL are engage, disengage, or do nothing. The rate at which the AGL engages or disengages depends on the attack and release settings, respectively.

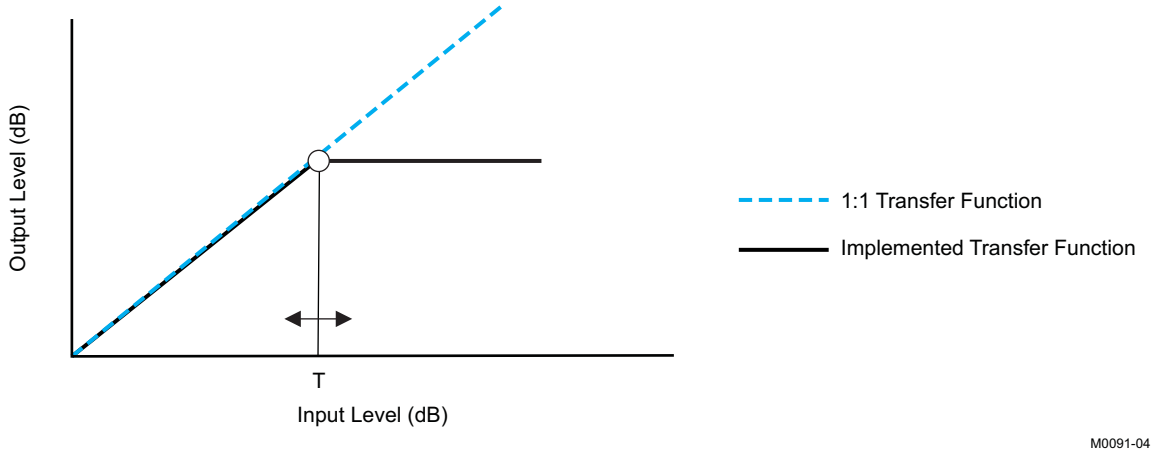


Figure 81. AGL Transfer Function Example Plot

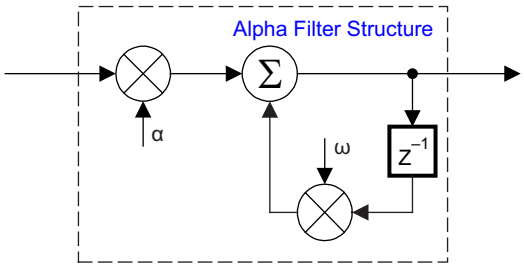


Figure 82. AGL Alpha Filter Structure

9.5.2.7.1 Softening Filter Alpha (AEA)

- $AEA = 1 - e^{-1000 / (fs \times User\_AE)}$
- e ≈ 2.718281828
- Fs = sampling frequency
- User_AE = user input step size

9.5.2.7.2 Softening Filter Omega (AEO)

- AEO = 1 – AEA

9.5.2.7.3 Attack Rate

- Attack rate = 2 (AA + Release rate)
- AA = 1000 × User_Ad / Fs
- User_Ad = user input attack step size

9.5.2.7.4 Release Rate

- Release rate = 1000 × User_Rd / Fs
- User_Rd = user input release step size

NOTE

The release duration (User_Rd) should be longer than the attack duration (User_Ad).

9.5.2.7.5 Attack Threshold

- Attack Threshold = user input level in dB

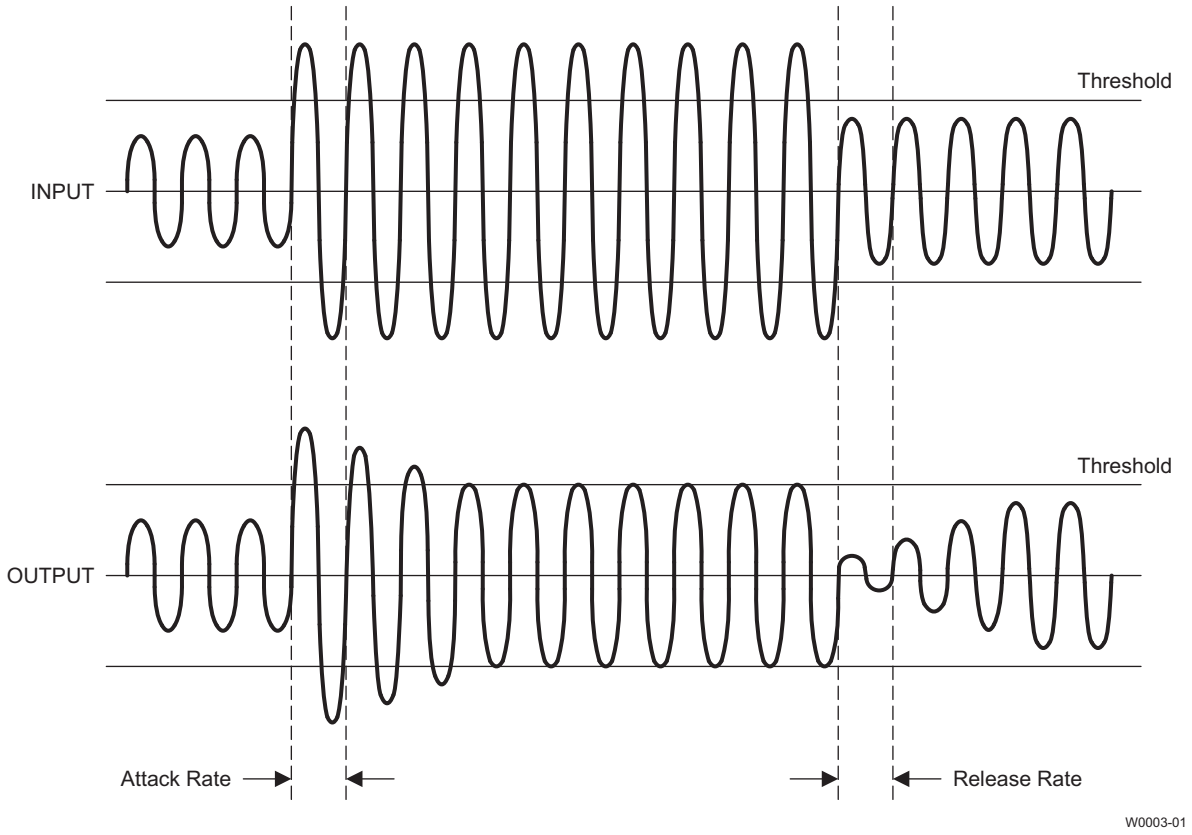


Figure 83. AGL Attack and Release

The Attack Threshold AGL coefficients are shown in .

9.5.2.8 Fine Volume

The fine volume block after the AGL can be used to provide additional fine volume steps from –192 dB to 6 dB in a 2.30 format. The Fine Coefficients are shown in .

9.5.2.9 THD Boost

A boost scalar and fine volume together can be used for clipping. The THD boost block allows the user to programmatically increase the THD by clipping at an operating point earlier than that defined by the supply rails.

9.5.2.10 Level Meter

The level meter uses an energy estimator with a programmable time constant to adjust the sensitivity level based on signal frequency and desired accuracy level. The level meter outputs of both left and right channels are written to a 32-bit sub address location in a 1.31 format as shown in . The BypassToLevelMeter Bit in Book 8C, Page 0x21, Register 0x70 can be used to switch the input to the Level Meter from the audio before processing to audio post-processing.

9.5.3 Other Processing Block Features

9.5.3.1 Number Format

The data processing path is 32 bits with 32-bit coefficients. The coefficients use the two's complement digital number format.

Table 24. Two's Complement Format

BITS	TWO'S COMPLEMENT VALUE
0111 1111	127
0111 1110	126
0000 0010	2
0000 0001	1
0000 0000	0
1111 1111	–1
1111 1110	–2
1000 0010	–126
1000 0001	–127
1000 0000	–128

9.5.3.1.1 Coefficient Format Conversion

The device uses 32 bit two's complement number formats. The calculated 4 byte register values are shown below in an 8 digit hex value.

Table 25. Sample Calculations for 1.31 Format

dB	Linear	Decimal	Hex (1.31 Format)
0	1	2147483648	7FFFFFFF
–6	0.5	1073741824	40000000
–20	0.1	214748364	0CCCCCCC
x	$L = 10^{(x/20)}$	$D = 2^{31} \times L, D < 2^{31}$ $D = 2^{31}, D \geq 2^{31}$	Dec2Hex(D, 8) (1)

(1) Dec2Hex(D, 8), where 8 represents 8 nibbles or 38 bits.

Please note that for a 1.31 format the linear value cannot be greater than 1 or decimal value 232.

Table 26. Sample Calculations for B.A Format

dB	Linear	Decimal	Hex (1.31 Format)
x	$L = 10^{(x/20)}$	$D = 2^{A} \times L, D < 2^{(B + A - 1)}$ $D = 2^{(B + A - 1)}, D \geq 2^{(B + A - 1)}$	Dec2Hex(D, 8)

9.5.4 Checksum

The TAS5780M device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Both checksums work on every register write, except for *book switch register* and *page switching register*, 0x7F and 0x00, respectively. Register reads do not change checksum, but writes to even nonexistent registers will change the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

9.5.4.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, $(1 + x^1 + x^2 + x^8)$. A major advantage of the CRC checksum is that it is input order sensitive.

The CRC supports all I^2C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on any page of book 0x00 (B0_Page x_Reg 126). If the book isn't Book 0, the CRC checksum is only valid on page 0x00 register 0x7E (Page 0_Reg 126). The CRC checksum can be reset by writing 0x00 00 00 00 to the same register locations where the CRC checksum is valid.

9.5.4.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only YMEM, which is located in Book 0x8C and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B140_Page 0_Reg 125). The XOR Checksum can be reset by writing 0x00 00 00 00 to the same register location where it is read.

Table 27. XOR Truth Table

INPUT		OUTPUT
A	B	
0	0	0
0	1	1
1	0	1
1	1	0

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5780M device into the larger system.

10.1.1 External Component Selection Criteria

The *Supporting Component Requirements* table in each application description section lists the details of the supporting required components in each of the *System Application Schematics*.

Where possible, the supporting component requirements have been consolidated to minimize the number of unique components which are used in the design. Component list consolidation is a method to reduce the number of unique part numbers in a design, to ease inventory management, and to reduce the manufacturing steps during board assembly. For this reason, some capacitors are specified at a higher voltage than what would normally be required. An example of this is a 50-V capacitor may be used for decoupling of a 3.3-V power supply net.

In this example, a higher voltage capacitor can be used even on the lower voltage net to consolidate all caps of that value into a single component type. Similarly, several unique resistors that have all the same size and value but different power ratings can be consolidated by using the highest rated power resistor for each instance of that resistor value.

While this consolidation can seem excessive, the benefits of having fewer components in the design can far outweigh the trivial cost of a higher voltage capacitor. If lower voltage capacitors are already available elsewhere in the design, they can be used instead of the higher voltage capacitors. In all situations, the voltage rating of the capacitors must be at least 1.45 times the voltage of the voltage which appears across them. The power rating of the capacitors should be 1.5 times to 1.75 times the power dissipated in it during normal use case.

10.1.2 Component Selection Impact on Board Layout, Component Placement, and Trace Routing

Because the layout is important to the overall performance of the circuit, the package size of the components shown in the component list was intentionally chosen to allow for proper board layout, component placement, and trace routing. In some cases, traces are passed in between two surface mount pads or ground plane extensions from the TAS5780M device and into to the surrounding copper for increased heat-sinking of the device. While components may be offered in smaller or larger package sizes, it is highly recommended that the package size remain identical to the size used in the application circuit as shown. This consistency ensures that the layout and routing can be matched very closely, which optimizes thermal, electromagnetic, and audio performance of the TAS5780M device in circuit in the final system.

10.1.3 Amplifier Output Filtering

The TAS5780M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the *L-C Filter*, due to the presence of an inductive element *L* and a capacitive element *C* to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the traditional large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report *Class-D LC Filter Design* (SLOA119) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.

Application Information (接下页)

10.1.4 Programming the TAS5780M

The TAS5780M device includes an I^2C compatible control port to configure the internal registers of the TAS5780M device. The control console software provided by TI is required to configure the device. More details regarding programming steps, and a few important notes are available below and also in the design examples that follow.

10.1.4.1 Resetting the TAS5780M Registers and Modules

The TAS5780M device has several methods by which the device can reset the register, interpolation filters, and DAC modules. The registers offer the flexibility to do these in or out of shutdown as well as in or out of standby. However, there can be issues if the reset bits are toggled in certain illegal operation modes.

Any of the following routines can be used with no issue:

- Reset Routine 1
  - Place device in Standby
  - Reset modules
- Reset Routine 2
  - Place device in Standby + Power Down
  - Reset registers
- Reset Routine 3
  - Place device in Power Down
  - Reset registers
- Reset Routine 4
  - Place device in Standby
  - Reset registers
- Reset Routine 5
  - Place device in Standby + Power Down
  - Reset modules + Reset registers
- Reset Routine 6
  - Place device in Power Down
  - Reset modules + Reset registers
- Reset Routine 7
  - Place device in Standby
  - Reset modules + Reset registers

Two reset routines are not supported and should be avoided. If used, they can cause the device to become unresponsive. These unsupported routines are shown below.

- Unsupported Reset Routine 1 (do not use)
  - Place device in Standby + Power Down
  - Reset modules
- Unsupported Reset Routine 2 (do not use)
  - Place device in Power Down
  - Reset modules

10.2 Typical Applications

10.2.1 2.0 (Stereo BTL) System

For the stereo (BTL) PCB layout, see 图 89.

A 2.0 system refers to a system in which there are two full range speakers without a separate amplifier path for the speakers which reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a *stereo pair*, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

图 84 shows the 2.0 (Stereo BTL) system application.

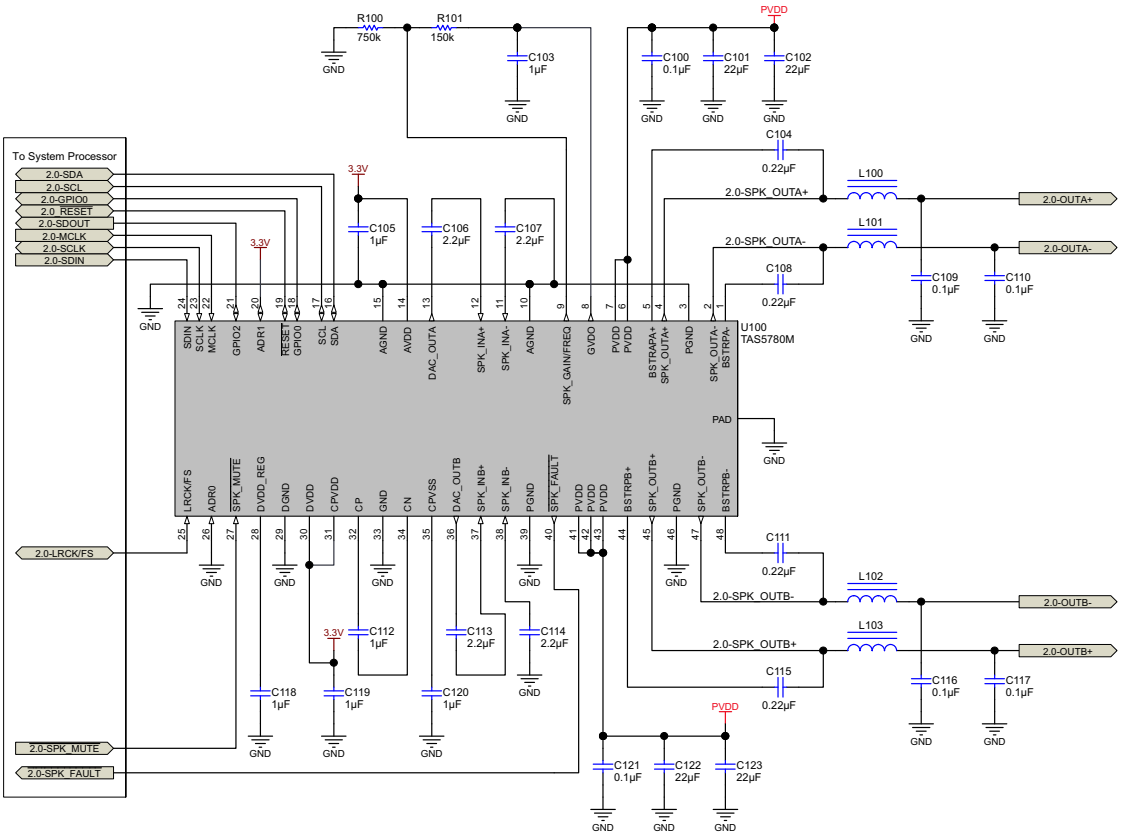


图 84. 2.0 (Stereo BTL) System Application Schematic

10.2.1.1 Design Requirements

- Power supplies:
  - 3.3-V supply
  - 5-V to 24-V supply
- Communication: host processor serving as I^2C compliant master
- External memory (such as EEPROM and flash) used for coefficients

The requirements for the supporting components for the TAS5780M device in a Stereo 2.0 (BTL) system is provided in 表 28.

表 28. Supporting Component Requirements for Stereo 2.0 (BTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
U100	TAS5780M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier
R100	See the *Adjustable Amplifier Gain and Switching Frequency Selection* section	0402	1%, 0.063 W
R101		0402	1%, 0.063 W
L100, L101, L102, L103	See the *Amplifier Output Filtering* section		
C100, C121	0.1 µF	0402	Ceramic, 0.1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C104, C108, C111, C115	0.22 µF	0603	Ceramic, 0.22 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C109, C110, C116, C117	0.68 µF	0805	Ceramic, 0.68 µF, ±10%, X7R Voltage rating must be > 1.8 × V_{PVDD}
C103	1 µF	0603 (this body size chosen to aid in trace routing)	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 16 V
C105, C118, C119, C120	1 µF	0402	Ceramic, 1 µF, 6.3V, ±10%, X5R
C106, C107, C113, C114	2.2 µF	0402	Ceramic, 2.2 µF, ±10%, X5R At a minimum, voltage rating must be > 10V, however higher voltage caps have been shown to have better stability under DC bias. Refer to the guidance provided in the TAS5780M for suggested values.
C101, C102, C122, C123	22 µF	0805	Ceramic, 22 µF, ±20%, X5R Voltage rating must be > 1.45 × V_{PVDD}

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Step One: Hardware Integration

- Using the *Typical Application Schematic* as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they are given precedent as design trade-offs are made is recommended.
  - For questions and support go to the E2E forums (e2e.ti.com). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

10.2.1.2.2 Step Two: System Level Tuning

- Use the TAS5780MEVM evaluation module and the PPC3 app to configure the desired device settings.
- Tune the end equipment by following the instructions in SLAU694

10.2.1.2.3 Step Three: Software Integration

- Use the End System Integration feature of the PPC3 app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

10.2.1.3 Application Curves

表 29 shows the application specific performance plots for Stereo 2.0 (BTL) systems.

表 29. Relevant Performance Plots

PLOT TITLE	FIGURE NUMBER
Output Power vs PVDD	Figure 23
THD+N vs Frequency, V_{PVDD} = 12 V	Figure 24
THD+N vs Frequency, V_{PVDD} = 15 V	Figure 25
THD+N vs Frequency, V_{PVDD} = 18 V	Figure 26
THD+N vs Frequency, V_{PVDD} = 24 V	Figure 27
THD+N vs Power, V_{PVDD} = 12 V	Figure 28
THD+N vs Power, V_{PVDD} = 15 V	Figure 29
THD+N vs Power, V_{PVDD} = 18 V	Figure 30
THD+N vs Power, V_{PVDD} = 24 V	Figure 31
Idle Channel Noise vs PVDD	Figure 32
Efficiency vs Output Power	Figure 33
DVDD PSRR vs. Frequency	Figure 39
AVDD PSRR vs. Frequency	Figure 40
C_{PVDD} PSRR vs. Frequency	Figure 41

10.2.2 Mono (PBTL) Systems

For the mono (PBTL) PCB layout, see 图 91.

A mono system refers to a system in which the amplifier is used to drive a single loudspeaker. Parallel Bridge Tied Load (PBTL) indicates that the two full-bridge channels of the device are placed in parallel and drive the loudspeaker simultaneously using an identical audio signal. The primary benefit of operating the TAS5780M device in PBTL operation is to reduce the power dissipation and increase the current sourcing capabilities of the amplifier output. In this mode of operation, the current limit of the audio amplifier is approximately doubled while the on-resistance is approximately halved.

The loudspeaker can be a full-range transducer or one that only reproduces the low-frequency content of an audio signal, as in the case of a powered subwoofer. Often in this use case, two stereo signals are mixed together and sent through a low-pass filter to create a single audio signal which contains the low frequency information of the two channels. Conversely, advanced digital signal processing can create a low-frequency signal for a multichannel system, with audio processing which is specifically targeted on low-frequency effects.

Because low-frequency signals are not perceived as having a direction (at least to the extent of high-frequency signals) it is common to reproduce the low-frequency content of a stereo signal that is sent to two separate channels. This configuration pairs one device in Mono PBTL configuration and another device in Stereo BTL configuration in a single system called a 2.1 system. The Mono PBTL configuration is detailed in the *2.1 (Stereo BTL + External Mono Amplifier) Systems* section. shows the Mono (PBTL) system application

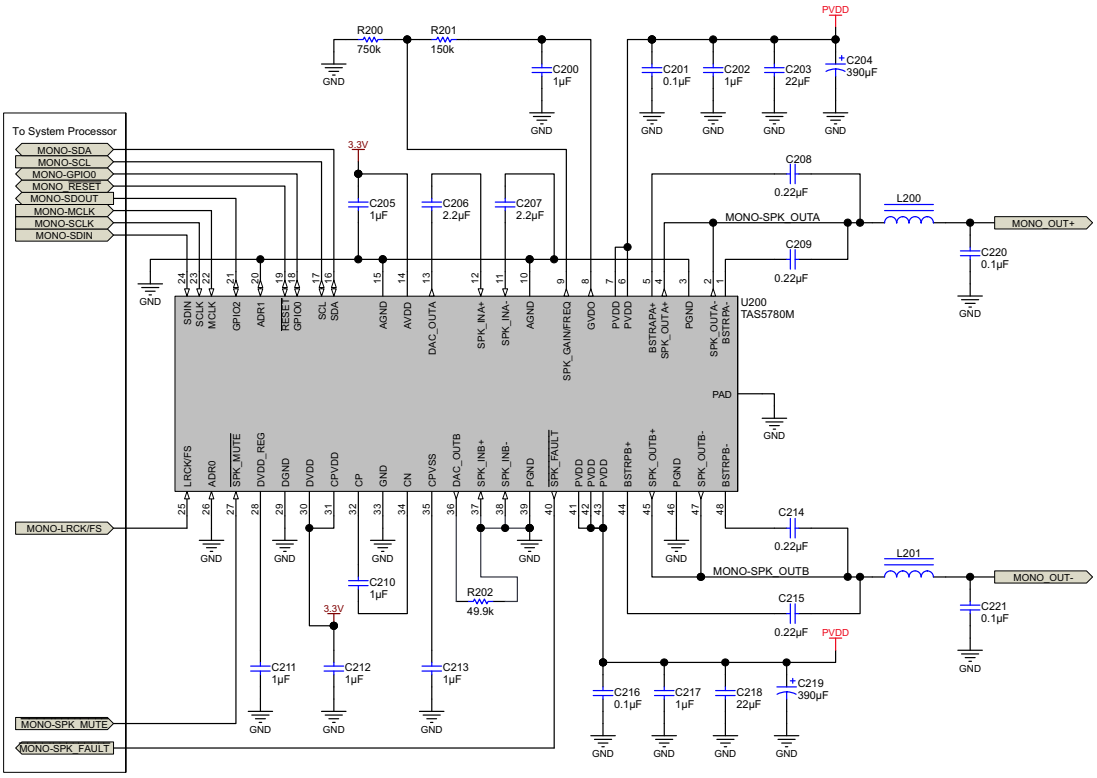


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图 85. Mono (PBTL) System Application Schematic

10.2.2.1 Design Requirements

- Power supplies:
  - 3.3-V supply
  - 5-V to 24-V supply
- Communication: Host processor serving as I^2C compliant master
- External memory (EEPROM, flash, and others) used for coefficients.

The requirements for the supporting components for the TAS5780M device in a Mono (PBTL) system is provided in 表 30.

表 30. Supporting Component Requirements for Mono (PBTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
U200	TAS5780M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier with 96kHz processing
R200	See the *Adjustable Amplifier Gain and Switching Frequency Selection* section	0402	1%, 0.063 W
R201		0402	1%, 0.063 W
R202		0402	1%, 0.063 W
L200, L201	See the *Amplifier Output Filtering* section		
C216, C201	0.1 µF	0402	Ceramic, 0.1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C208, C209, C214, C215	0.22 µF	0603	Ceramic, 0.22 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C220, C221	0.68 µF	0805	Ceramic, 0.68 µF, ±10%, X7R Voltage rating must be > 1.8 × V_{PVDD}

表 30. Supporting Component Requirements for Mono (PBTL) Systems (接下页)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C200	1 µF	0603 (this body size chosen to aid in trace routing)	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 16 V
C205, C211, C213, C212	1 µF	0402	Ceramic, 1 µF, 6.3 V, ±10%, X5R
C202, C217, C352, C367	1 µF	0805 (this body size chosen to aid in trace routing)	Ceramic, 1 µF, ±10%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C206, C207	2.2 µF	0402	Ceramic, 2.2 µF, ±10%, X5R At a minimum, voltage rating must be > 10V, however higher voltage caps have been shown to have better stability under DC bias please follow the guidance provided in the TAS5780M for suggested values.
C203, C218	22 µF	0805	Ceramic, 22 µF, ±20%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C204, C219	390 µF	10 × 10	Aluminum, 390 µF, ±20%, 0.08-Ω Voltage rating must be > 1.45 × V_{PVDD} Anticipating that this application circuit would be followed for higher power subwoofer applications, these capacitors are added to provide local current sources for low-frequency content. These capacitors can be reduced or even removed based upon final system testing, including critical listening tests when evaluating low-frequency designs.

10.2.2.2 Detailed Design Procedure

10.2.2.2.1 Step One: Hardware Integration

- Using the *Typical Application Schematic* as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they are given precedent as design trade-offs are made is recommended.
  - For questions and support go to the E2E forums (e2e.ti.com). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

10.2.2.2.2 Step Two: System Level Tuning

- Use the TAS5780MEVM evaluation module and the PPC3 app to configure the desired device settings.

10.2.2.2.3 Step Three: Software Integration

- Use the End System Integration feature of the PPC3 app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

10.2.2.3 Application Specific Performance Plots for Mono (PBTL) Systems

表 31 shows the application specific performance plots for Mono (PBTL) Systems

表 31. Relevant Performance Plots

PLOT TITLE	FIGURE NUMBER
Output Power vs PVDD	Figure 43
THD+N vs Frequency, V_{PVDD} = 12 V	Figure 44
THD+N vs Frequency, V_{PVDD} = 15 V	Figure 45
THD+N vs Frequency, V_{PVDD} = 18 V	Figure 46
THD+N vs Frequency, V_{PVDD} = 24 V	Figure 47
THD+N vs Power, V_{PVDD} = 12 V	Figure 48
THD+N vs Power, V_{PVDD} = 15 V	Figure 49
THD+N vs Power, V_{PVDD} = 18 V	Figure 50
THD+N vs Power, V_{PVDD} = 24 V	Figure 51
Idle Channel Noise vs PVDD	Figure 52
Efficiency vs Output Power	Figure 53

10.2.3 2.1 (Stereo BTL + External Mono Amplifier) Systems

图 93 shows the PCB Layout for the 2.1 System.

To increase the low-frequency output capabilities of an audio system, a single subwoofer can be added to the system. Because the spatial clues for audio are predominately higher frequency than that reproduced by the subwoofer, often a single subwoofer can be used to reproduce the low frequency content of several other channels in the system. This is frequently referred to as a *dot one* system. A stereo system with a subwoofer is referred to as a 2.1 (two-dot-one), a 3 channel system with subwoofer is referred to as a 3.1 (three-dot-one), a popular surround system with five speakers and one subwoofer is referred to as a 5.1, and so on.

10.2.3.1 Advanced 2.1 System (Two TAS5780M devices)

In higher performance systems, the subwoofer output can be enhanced using digital audio processing as was done in the high-frequency channels. To accomplish this, two TAS5780M devices are used — one for the high frequency left and right speakers and one for the mono subwoofer speaker. In this system, the audio signal can be sent from the TAS5780M device through the SDOUT pin. Alternatively, the subwoofer amplifier can accept the same digital input as the stereo, which might come from a central systems processor. 图 86 shows the 2.1 (Stereo BTL + External Mono Amplifier) system application.

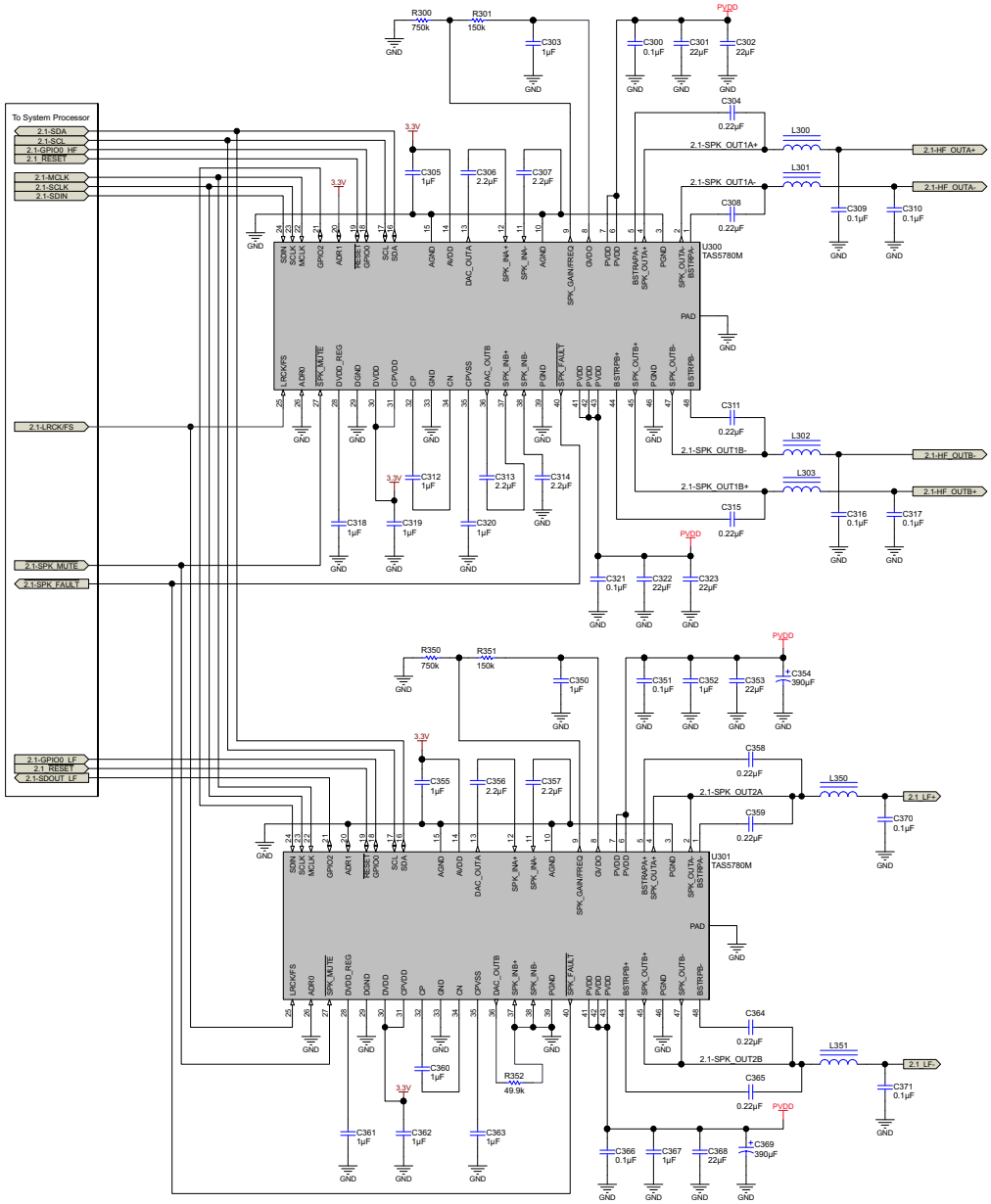

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图 86. 2.1 (Stereo BTL + External Mono Amplifier) Application Schematic

10.2.3.2 Design Requirements

- Power supplies:
  - 3.3-V supply
  - 5-V to 24-V supply
- Communication: Host processor serving as I^2C compliant master
- External memory (EEPROM, flash, and others) used for coefficients.

The requirements for the supporting components for the TAS5780M device in a 2.1 (Stereo BTL + External Mono Amplifier) system is provided in 表 32.

表 32. Supporting Component Requirements for 2.1 (Stereo BTL + External Mono Amplifier) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
U300	TAS5780M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier 96kHz Processing
R300, R350	See the *Adjustable Amplifier Gain and Switching Frequency Selection* section	0402	1%, 0.063 W
R301, R351		0402	1%, 0.063 W
R352		0402	1%, 0.063 W
L300, L301, L302, L303	See the *Amplifier Output Filtering* section		
L350, L351			
C394, C395, C396, C397, C398, C399	0.01 µF	0603	Ceramic, 0.01 µF, 50 V, +/-10%, X7R
C300, C321, C351, C366	0.1 µF	0402	Ceramic, 0.1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C304, C308, C311, C315, C358, C359, C364, C365	0.22 µF	0603	Ceramic, 0.22 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C309, C310, C316, C317, C370, C371	0.68 µF	0805	Ceramic, 0.68 µF, ±10%, X7R Voltage rating must be > 1.8 × V_{PVDD}
C303, C350, C312, C360	1 µF	0603	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C305, C318, C319, C320, C355, C361, C363, C312, C362	1 µF	0402	Ceramic, 1 µF, 6.3V, ±10%, X5R
C352, C367	1 µF	0805	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C306, C307, C313, C314, C356, C357,	2.2 µF	0402	Ceramic, 2.2 µF, ±10%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C301, C302, C322, C323, C353, C368	22 µF	0805	Ceramic, 22 µF, ±20%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C354, C369	390 µF	10 × 10	Aluminum, 390 µF, ±20%, 0.08 Ω Voltage rating must be > 1.45 × V_{PVDD}

10.2.3.3 Application Specific Performance Plots for 2.1 (Stereo BTL + External Mono Amplifier) Systems

表 33 shows the application specific performance plots for 2.1 (Stereo BTL + External Mono Amplifier) Systems

表 33. Relevant Performance Plots

DEVICE	PLOT TITLE	FIGURE NUMBER
U300	Output Power vs PVDD	Figure 23
	THD+N vs Frequency, V_{PVDD} = 12 V	Figure 24
	THD+N vs Frequency, V_{PVDD} = 15 V	Figure 25
	THD+N vs Frequency, V_{PVDD} = 18 V	Figure 26
	THD+N vs Frequency, V_{PVDD} = 24 V	Figure 27
	THD+N vs Power, V_{PVDD} = 12 V	Figure 28
	THD+N vs Power, V_{PVDD} = 15 V	Figure 29
	THD+N vs Power, V_{PVDD} = 18 V	Figure 30
	THD+N vs Power, V_{PVDD} = 24 V	Figure 31
	Idle Channel Noise vs PVDD	Figure 32
	Efficiency vs Output Power	Figure 33
U301	PVDD PSRR vs Frequency	Figure 38
	Output Power vs PVDD	Figure 43
	THD+N vs Frequency, V_{PVDD} = 12 V	Figure 44
	THD+N vs Frequency, V_{PVDD} = 15 V	Figure 45
	THD+N vs Frequency, V_{PVDD} = 18 V	Figure 46
	THD+N vs Frequency, V_{PVDD} = 24 V	Figure 47
	THD+N vs Power, V_{PVDD} = 12 V	Figure 48
	THD+N vs Power, V_{PVDD} = 15 V	Figure 49
	THD+N vs Power, V_{PVDD} = 18 V	Figure 50
	THD+N vs Power, V_{PVDD} = 24 V	Figure 51
	Idle Channel Noise vs PVDD	Figure 52
	Efficiency vs Output Power	Figure 53
U300 and U301	DVDD PSRR vs. Frequency	Figure 39
	AVDD PSRR vs. Frequency	Figure 40
	C_{PVDD} PSRR vs. Frequency	Figure 41
	Powerdown Current Draw vs. PVDD	Figure 43

11 Power Supply Recommendations

11.1 Power Supplies

The TAS5780M device requires two power supplies for proper operation. A *high-voltage* supply called PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one *low-voltage* power supply which is called DVDD is required to power the various low-power portions of the device. The allowable voltage range for both the PVDD and the DVDD supply are listed in the *Recommended Operating Conditions* table. The two power supplies do not have a required powerup sequence. The power supplies can be powered on in any order. TI recommends waiting 100 ms to 240 ms for the DVDD power supplies to stabilize before starting I^2C communication and providing stable I^2S clock before enabling the device outputs.

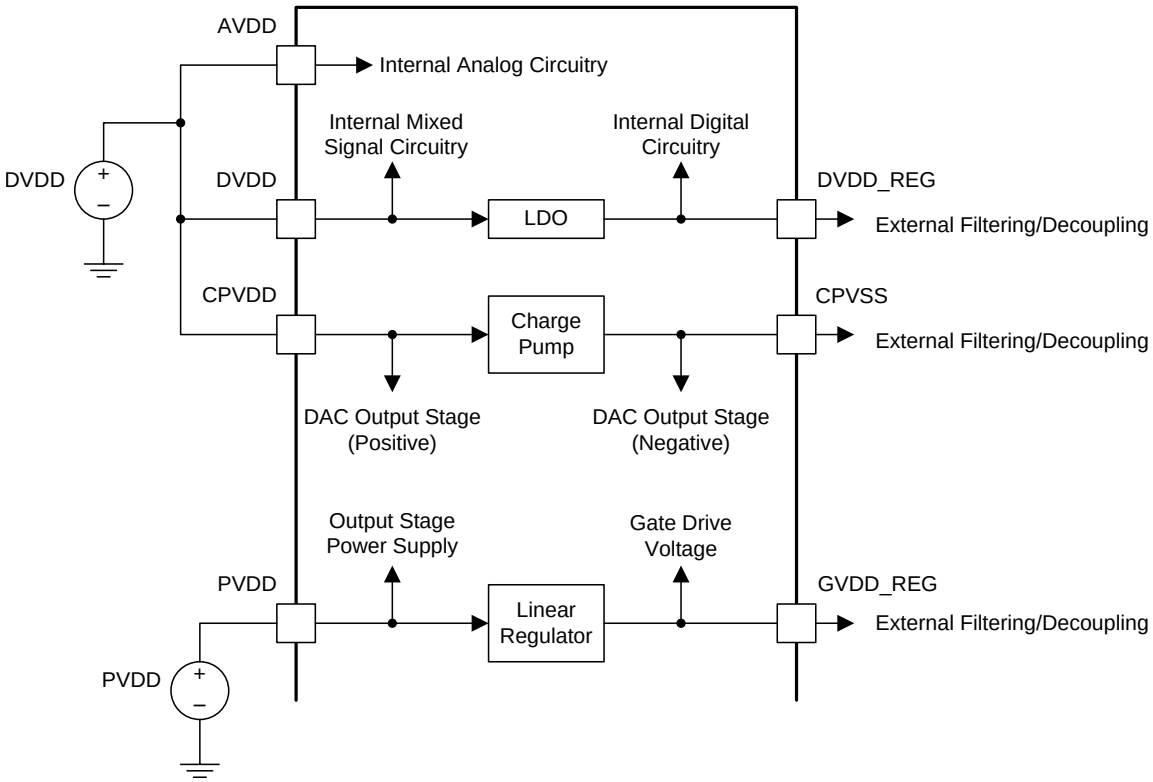


图 87. Power Supply Functional Block Diagram

11.1.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in *图 87*, it provides power to the DVDD pin, the CPVDD pin, and the AVDD pin. Proper connection, routing, and decoupling techniques are highlighted in the *Application and Implementation* section and the *Layout Example* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TAS5780M device *Application and Implementation* section can result in reduced performance, errant functionality, or even damage to the TAS5780M device.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5780M device includes an integrated low-dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Power Supplies (接下页)

The outputs of the high-performance DACs used in the TAS5780M device are ground centered, requiring both a positive low-voltage supply and a negative low-voltage supply. The positive power supply for the DAC output stage is taken from the AVDD pin, which is connected to the DVDD supply provided by the system. A charge pump is integrated in the TAS5780M device to generate the negative low-voltage supply. The power supply input for the charge pump is the CPVDD pin. The CPVSS pin is provided to allow the connection of a filter capacitor on the negative low-voltage supply. As is the case with the other supplies, the component selection, placement, and routing of the external components for these low voltage supplies are shown in the TAS5780M and should be followed as closely as possible to ensure proper operation of the device.

11.1.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5780MEVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5780M deviceApplication and Implementation . Lack of proper decoupling, like that shown in the Application and Implementation , results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD_REG pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

12 Layout

12.1 Layout Guidelines

12.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in Layout Example. These examples represent exemplary *baseline* balance of the engineering trade-offs involved with laying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper near the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the *Layout Example* section and work with TI field application engineers or through the E2E community to modify it based upon the application specific goals.

12.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, CPVDD, and PVDD. However, the capacitors on the PVDD net for the TAS5780M device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only does placing these devices far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5780M device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Example* section

12.1.3 Optimizing Thermal Performance

Follow the layout examples shown in the *Layout Example* section of this document to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

12.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5780M device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5780M device away from the edge of the PCB when possible to ensure that heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5780M device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5780M device.

Layout Guidelines (接下页)

- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

12.1.3.2 Stencil Pattern

The recommended drawings for the TAS5780M device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperatures or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system.

注

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

12.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a *symbol* or *land pattern*) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5780M device will be soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD of the TAS5780M device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5780M device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in the *Layout Example* section, this interface can benefit from improved thermal performance.

注

Vias can obstruct heat flow if they are not constructed properly.

More notes on the construction and placement of vias as as follows:

- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drull must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the *Layout Example* section.
- Ensure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5780M device to open up the current path to and from the device.

12.1.3.2.1.1 Solder Stencil

During the PCB assembly process, a piece of metal called a *stencil* on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself.

Layout Guidelines (接下页)

However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste would lead to manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Layout Example* section. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

12.2 Layout Example

12.2.1 2.0 (Stereo BTL) System

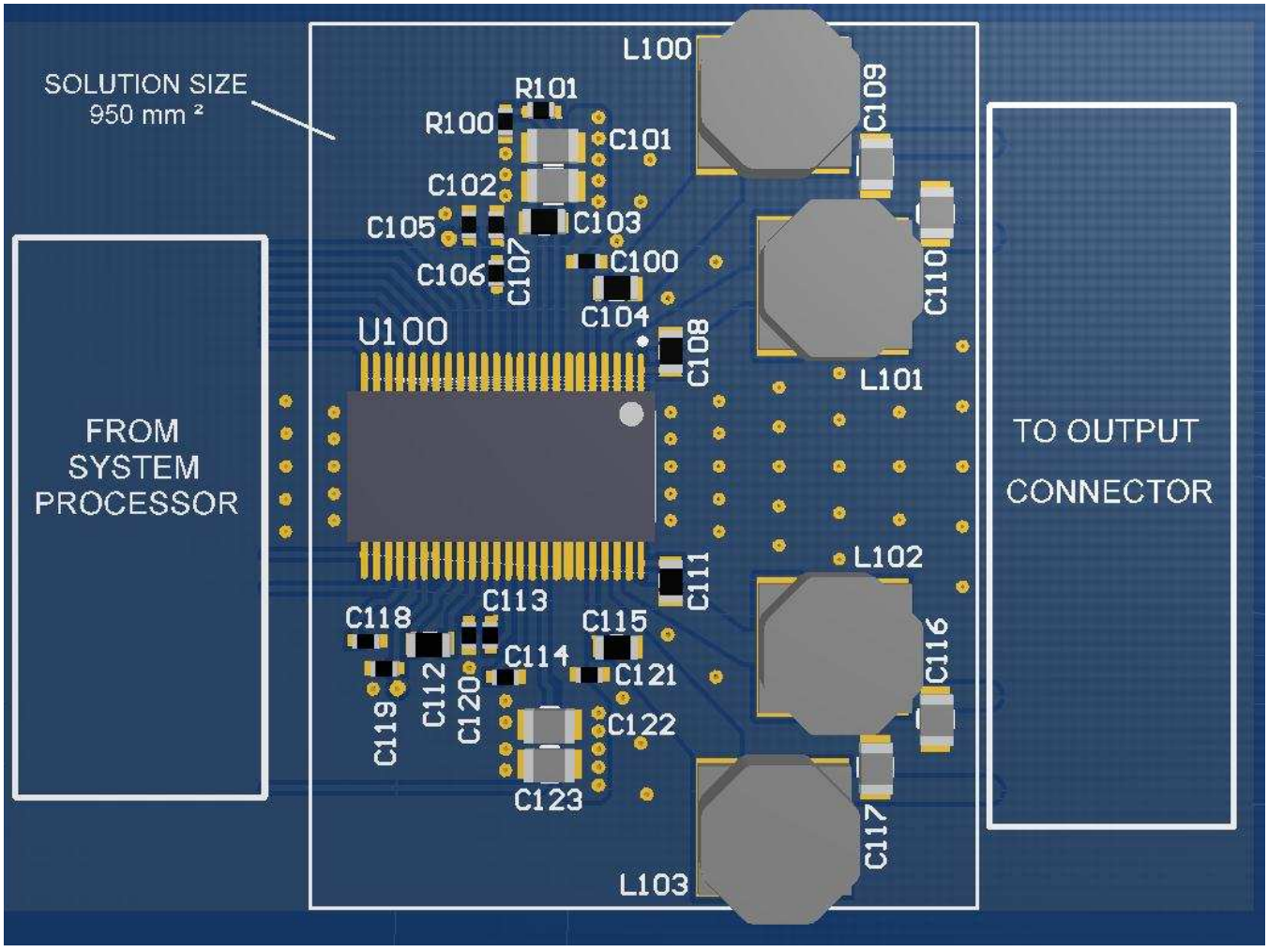


图 88. 2.0 (Stereo BTL) 3-D View

Layout Example (接下页)

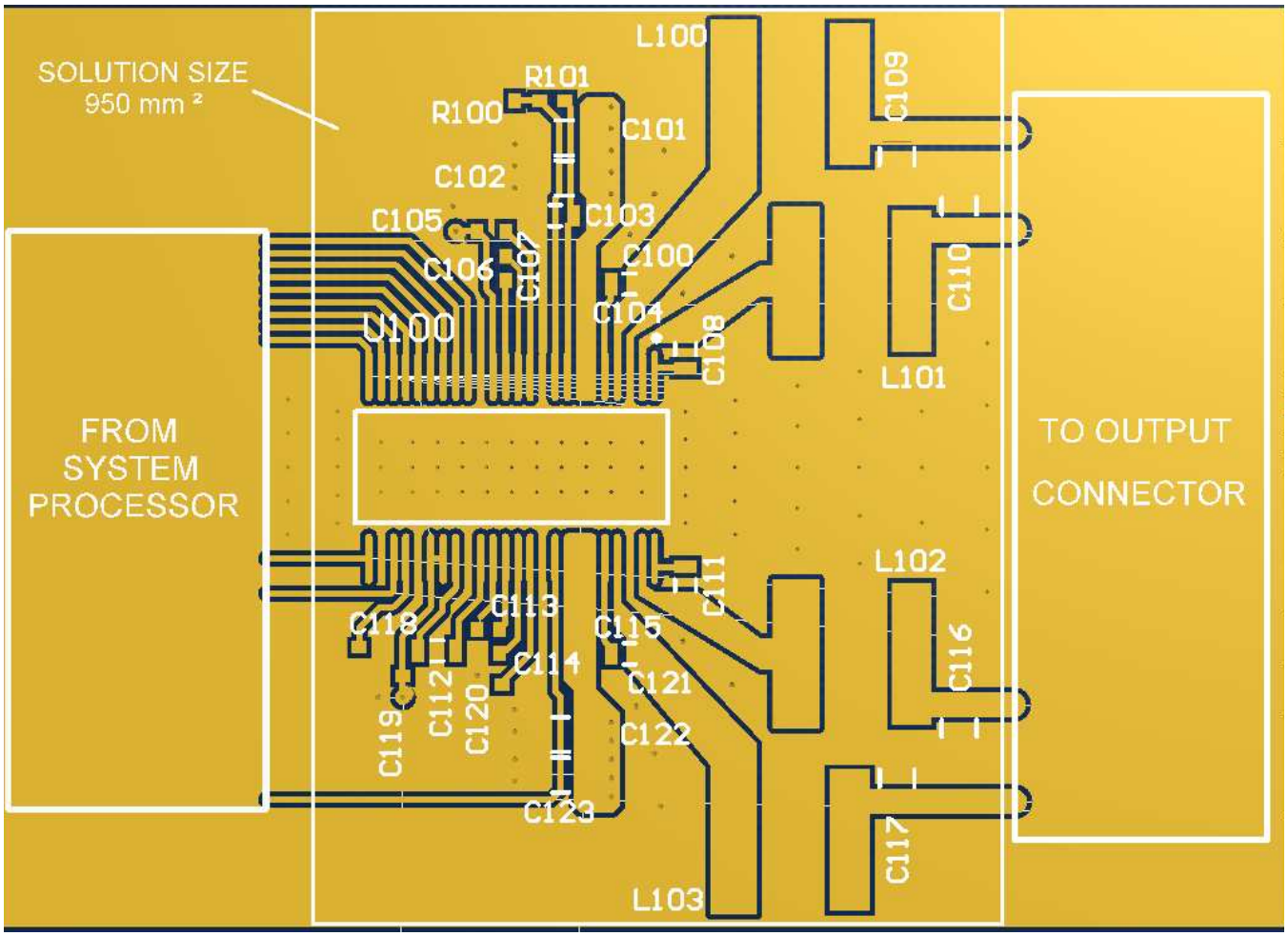


图 89. 2.0 (Stereo BTL) Top Copper View

Layout Example (接下页)

12.2.2 Mono (PBTL) System

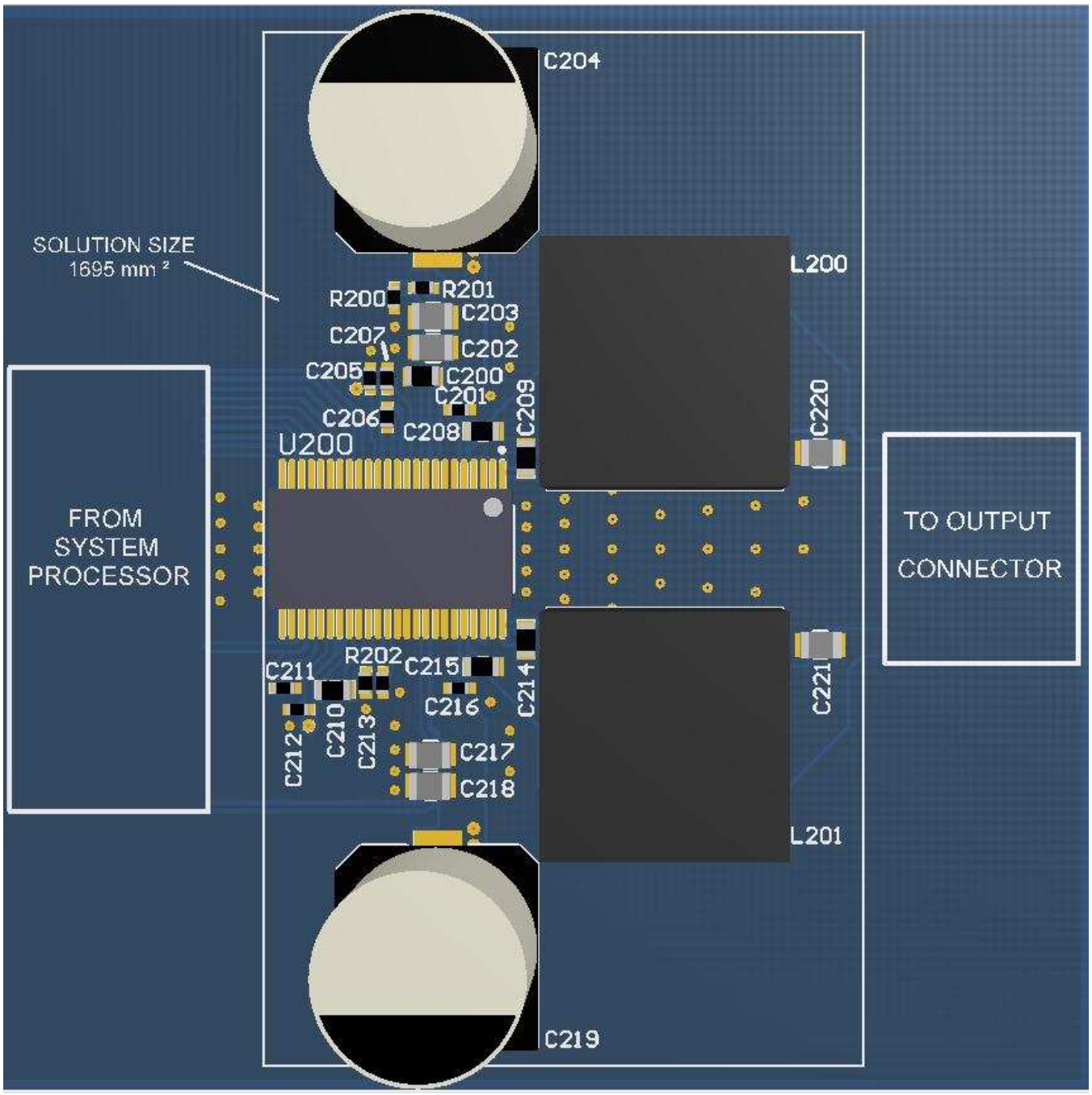


图 90. Mono (PBTL) 3-D View

Layout Example (接下页)

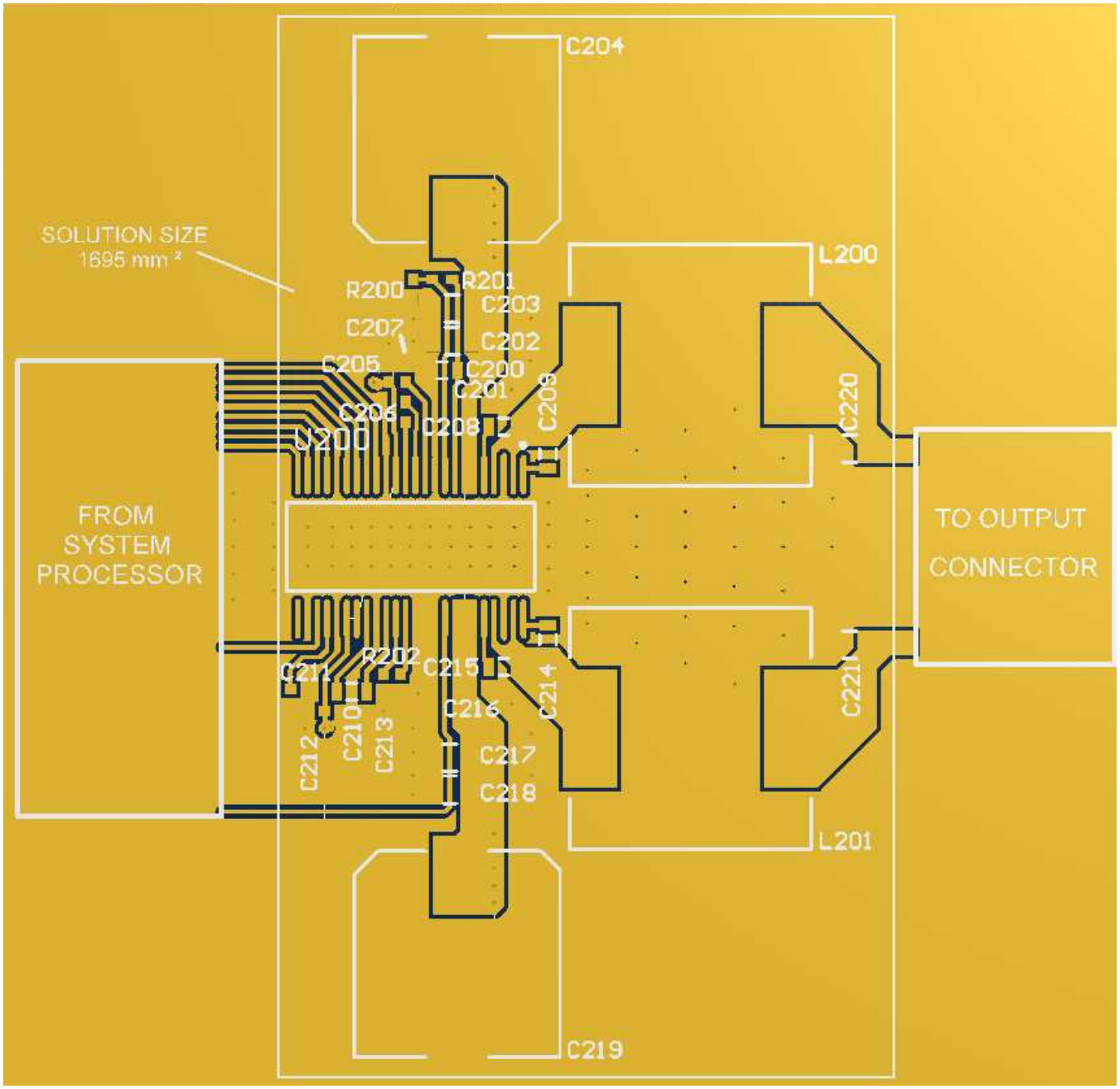


图 91. Mono (PBTL) Top Copper View

Layout Example (接下页)

12.2.3 2.1 (Stereo BTL + Mono PBTL) Systems

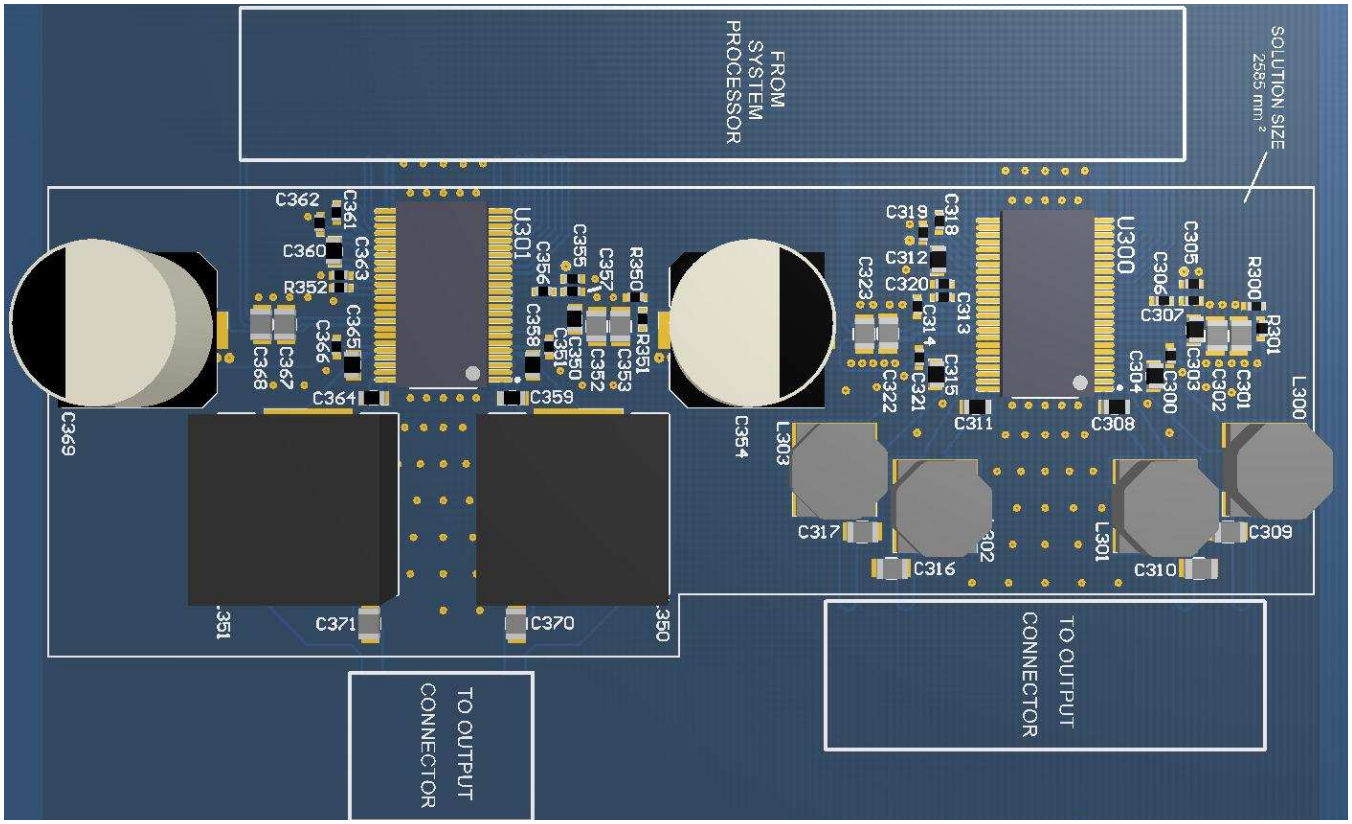


图 92. 2.1 (Stereo BTL + Mono PBTL) 3-D View

Layout Example (接下页)

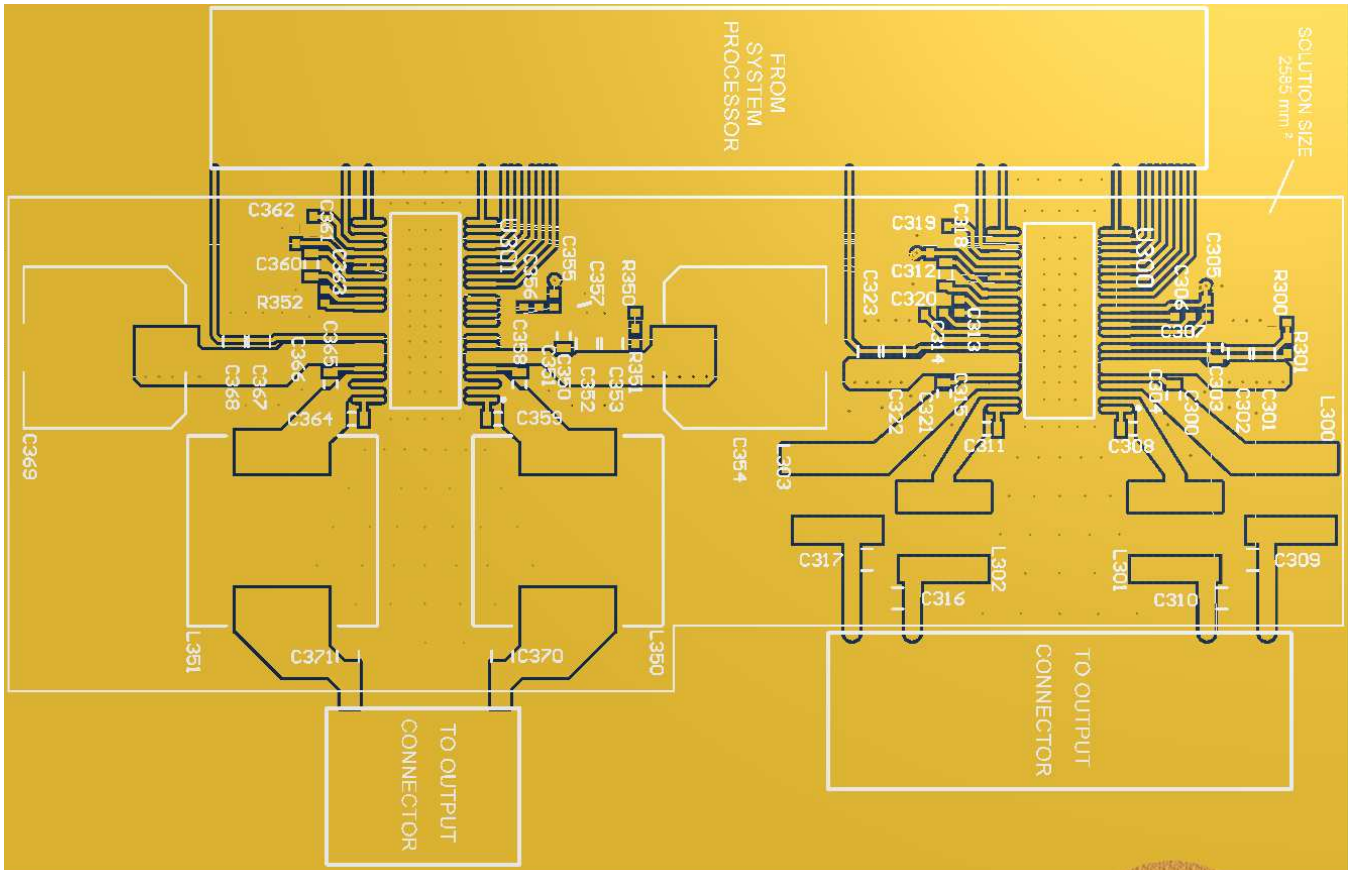


图 93. 2.1 (Stereo BTL + Mono PBTL) Top Copper View

13 Register Maps

13.1 Registers - Page 0

13.1.1 Register 1 (0x01)

Figure 94. Register 1 (0x01)

7	6	5	4	3	2	1	0
Reserved			RSTM	Reserved			RSTR
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Register 1 (0x01) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved			Reserved
4	RSTM	R/W	0	Reset Modules – This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in standby mode. 0: Normal 1: Reset modules
3-1	Reserved			Reserved
0	RSTR	R/W	0	Reset Registers – This bit resets the mode registers back to their initial values. The RAM content is not cleared, but the execution source will be back to ROM. This bit is auto cleared and must be set only when the DAC is in standby mode (resetting registers when the DAC is running is prohibited and not supported). 0: Normal 1: Reset mode registers

13.1.2 Register 2 (0x02)

Figure 95. Register 2 (0x02)

7	6	5	4	3	2	1	0
DSPR	Reserved		RQST	Reserved			RQPD
R/W	R/W		R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Register 2 (0x02) Field Descriptions

Bit	Field	Type	Reset	Description
7	DSPR	R/W	1	DSP reset – When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are (ASI,MCLK,PLLCLK) are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
6-5	Reserved	R/W		Reserved
4	RQST	R/W	0	Standby Request – When this bit is set, the DAC will be forced into a system standby mode, which is also the mode the system enters in the case of clock errors. In this mode, most subsystems will be powered down but the charge pump and digital power supply. 0: Normal operation 1: Standby mode
3-1	Reserved	R/W		Reserved

Table 35. Register 2 (0x02) Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RQPD	R/W	0	Powerdown Request – When this bit is set, the DAC will be forced into powerdown mode, in which the power consumption would be minimum as the charge pump is also powered down. However, it will take longer to restart from this mode. This mode has higher precedence than the standby mode, i.e. setting this bit along with bit 4 for standby mode will result in the DAC going into powerdown mode. 0: Normal operation 1: Powerdown mode

13.1.3 Register 3 (0x03)

Figure 96. Register 3 (0x03)

7	6	5	4	3	2	1	0
SYNC	SDZE	SDZS	RQML	Reserved			RQMR
RO	RO	RO	R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. Register 3 (0x03) Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC	RO		sync_sig_to_dig – This is the clock signal to BackEnd. The clock frequency when device is running is 98.304 Mhz/1024 = 96 ksps
6	SDZE	RO		sdz_oe_to_dig – Backend IO buffer tristate signal. Will be asserted when LDO input and LDO output PORs are both detected 0: SYNC and SDZ buffers are tristated 1: SYNC and SDZ buffers are enabled
5	SDZS	RO		sdz_sig_to_dig – Backend Power up signal. Will be asserted when AVDD & CPVDD PORs are detected and Line amplifiers are unmuted 0: BackEnd is shutdown 1: BackEnd is powered up
4	RQML	R/W	0	Mute Left Channel – This bit issues soft mute request for the left channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
3-1	Reserved	R/W		Reserved
0	RQMR	R/W	0	Mute Right Channel – This bit issues soft mute request for the right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute

13.1.4 Register 4 (0x04)

Figure 97. Register 4 (0x04)

7	6	5	4	3	2	1	0
Reserved			PLCK	Reserved			PLLE
R/W			R	R/W			R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. Register 4 (0x04) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4	PLCK	R	0	PLL Lock Flag – This bit indicates whether the PLL is locked or not. When the PLL is disabled this bit always shows that the PLL is not locked. 0: The PLL is locked 1: The PLL is not locked

Table 37. Register 4 (0x04) Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	Reserved	R/W		Reserved
0	PLLE	R	1	PLL Enable – This bit enables or disables the internal PLL. When PLL is disabled, the master clock will be switched to the MCLK. 0: Disable PLL 1: Enable PLL

13.1.5 Register 5 (0x05)

Figure 98. Register 5 (0x05)

7	6	5	4	3	2	1	0
Reserved		OSSL	OSPD	Reserved			OSAD
R/W		RO	RO	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. Register 5 (0x05) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W		Reserved
5	OSSL	RO		Oscillator Clock Selected – This bit, when set, indicates that the internal oscillator is being selected as the master clock and that the system is in emergency state where the normal system clock is not available/reliable. 0: Oscillator clock is not selected 1: Oscillator clock is being selected
4	OSPD	RO		Oscillator Powerdown Status – This bit, when set, indicates that the oscillator is being powered down, as a result of setting the oscillator to auto disable mode and the oscillator clock is not needed/selected. 0: Oscillator is active 1: Oscillator is powered down
3-1	Reserved	R/W		Reserved
0	OSAD	R/W	1	Oscillator Auto Disable – This bit sets the oscillator to auto disable mode, in which the oscillator is powered down when it is not needed anymore. By disabling the oscillator, both power consumption and potential interference is reduced. 0: Oscillator is always active 1: Oscillator is auto disabled (Powered down when not in use)

13.1.6 Register 6 (0x06)

Figure 99. Register 6 (0x06)

7	6	5	4	3	2	1	0
Reserved			OI2C	DBPG	FRMD	FSMI	Reserved
R/W			R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. Register 6 (0x06) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved			Reserved
4	OI2C	R/W	0	old_i2c_mode_reg_r – In Hans, I2C is always in auto increment mode. In old device MSB during control word decides whether is auto-increment mode or not. Writing this bit as 1 enables the older mode. 0: Register Auto increment enabled by default 1: Register auto increment mode enabled based on the MSB value sent during address portion of I2C protocol

Table 39. Register 6 (0x06) Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DBPG	R/W	0	Page auto increment disable – Disable page auto increment mode. for non -zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2	FRMD	R/W	0	SPI register read frame delay – When reading non-zero memory locations there is 1 frame delay between address and actual data. Which is read. By making this bit even for book0 register read there will be 1 frame delay to make it consistent across all books 0: No frame delay for SPI read for Book0 registers. 1: 1 frame delay for SPI read for Book0 registers.
1	FSMI	R/W	0	SPI MISO function sel: 00: SPI_MISO 01: GPIO3 Others: Reserved (Do not set)
0	Reserved	R/W	0	These bits select the function of the SPI_MISO pin when in SPI mode. If the pin is set as GPIO, register readout via SPI is not possible.

13.1.7 Register 7 (0x07)

Figure 100. Register 7 (0x07)

7	6	5	4	3	2	1	0
Reserved			DEMP	Reserved			SDSL
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. Register 7 (0x07) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4	DEMP	R/W	0	De-Emphasis Enable – This bit enables or disables the de-emphasis filter. The default coefficients are for 44.1 kHz sampling rate, but can be changed by reprogramming the appropriate coeffients in RAM. 0: De-emphasis filter is disabled 1: De-emphasis filter is enabled
3-1	Reserved	R/W		Reserved
0	SDSL	R/W	0	SDOUT Select – This bit selects what is being output as SDOUT via GPIO pins. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

13.1.8 Register 8 (0x08)

Figure 101. Register 8 (0x08)

7	6	5	4	3	2	1	0
Reserved		G2OE	MUTEOE	G0OE	Reserved		
R/W		R/W	R/W	R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. Register 8 (0x08) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W		Reserved
5	G2OE	R/W	0	GPIO2 Output Enable – This bit sets the direction of the GPIO2 pin 0: GPIO2 is input 1: GPIO2 is output
4	MUTEOE	R/W	0	MUTE Control Enable – This bit sets an enable of MUTE control from PCM to TPA 0: MUTE control disable 1: MUTE control enable
3	G0OE	R/W	0	GPIO0 Output Enable – This bit sets the direction of the GPIO0 pin 0: GPIO0 is input 1: GPIO0 is output
2	Reserved	R/W	0	Reserved
1-0	Reserved	R/W	0	Reserved

13.1.9 Register 9 (0x09)

Figure 102. Register 9 (0x09)

7	6	5	4	3	2	1	0
Reserved		SCLKP	SCLKO	Reserved			LRCLKFSO
R/W		R/W	R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. Register 9 (0x09) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved			Reserved
5	SCLKP	R/W	0	SCLK Polarity – This bit sets the inverted SCLK mode. In inverted SCLK mode, the DAC assumes that the LRCLK and DIN edges are aligned to the rising edge of the SCLK. Normally they are assumed to be aligned to the falling edge of the SCLK. 0: Normal SCLK mode 1: Inverted SCLK mode
4	SCLKO	R/W	0	SCLK Output Enable – This bit sets the SCLK pin direction to output for I2S master mode operation. In I2S master mode the PCM51xx outputs the reference SCLK and LRCLK, and the external source device provides the DIN according to these clocks. Use P0-R32 to program the division factor of the MCLK to yield the desired SCLK rate (normally 64 FS) 0: SCLK is input (I2S slave mode) 1: SCLK is output (I2S master mode)
3-1	Reserved			Reserved
0	LRKO	R/W	0	LRCLK Output Enable – This bit sets the LRCLK pin direction to output for I2S master mode operation. In I2S master mode the PCM51xx outputs the reference SCLK and LRCLK, and the external source device provides the DIN according to these clocks. Use P0-R33 to program the division factor of the SCLK to yield 1 FS for LRCLK. 0: LRCLK is input (I2S slave mode) 1: LRCLK is output (I2S master mode)

13.1.10 Register 10 (0x0A)

Figure 103. Register 10 (0x0A)

7	6	5	4	3	2	1	0
DSPG	Reserved						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. Register 10 (0x0A) Field Descriptions

Bit	Field	Type	Reset	Description
7	DSPG	R/W	0	DSP GPIO Input – this 8 bit bus reaches the DSP input port. DSP s/w can access these bits for getting any direct control/input from host ny means of this register write
6-0	Reserved	R/W	0	Reserved

13.1.11 Register 12 (0x0C)

Figure 104. Register 12 (0x0C)

7	6	5	4	3	2	1	0
Reserved	RDSP	RDAC	RNCP	ROSR	RSYN	RSCLK	RLRK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. Register 12 (0x0C) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6	RDSP	R/W	1	$\overline{\text{RST}}$ uCDSP clock – This bit, when set to 0 will reset the DSP clock divider and thus, halt the DSP clock. 0: DSP clock divider is reset 1: DSP clock divider is functional
5	RDAC	R/W	1	$\overline{\text{RST}}$ DAC clock – This bit, when set to 0 will reset the DAC clock divider and thus, halt the DAC clock and its derivatives. 0: DAC clock divider is reset 1: DAC clock divider is functional
4	RNCP	R/W	1	$\overline{\text{RST}}$ NCP clock – This bit, when set to 0 will reset the OSR clock divider and thus, halt the OSR clock. 0: OSR clock divider is reset 1: OSR clock divider is functional
3	ROSR	R/W	1	$\overline{\text{RST}}$OSR clock – This bit, when set to 0 will reset the clock synchronizer and thus, halt the DAC clock and its derivatives. When this bit is set to 1, the dividers un-reset will take place synchronized to the beginning of audio frame. 0: DAC clock and its derivatives are stopped asynchronously 1: DAC clock and its derivatives started synchronized to the beginning of audio frame
2	RSYN	R/W	1	$\overline{\text{RST}}$ clock sync – This bit, when set to 0 will reset the clock synchronizer and thus, halt the DAC clock and its derivatives. When this bit is set to 1, the dividers un-reset will take place synchronized to the beginning of audio frame. 0: DAC clock and its derivatives are stopped asynchronously 1: DAC clock and its derivatives started synchronized to the beginning of audio frame
1	RSCLK	R/W	0	Master Mode SCLK Divider Reset – This bit, when set to 0, will reset the MCLK divider to generate SCLK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly. 0: Master mode SCLK clock divider is reset 1: Master mode SCLK clock divider is functional
0	RLRK	R/W	1	Master Mode LRCLK Divider Reset – This bit, when set to 0, will reset the SCLK divider to generate LRCLK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly. 0: Master mode LRCLK clock divider is reset 1: Master mode LRCLK clock divider is functional

13.1.12 Register 13 (0x0D)

Figure 105. Register 13 (0x0D)

7	6	5	4	3	2	1	0
Reserved	SREF		SREF	Reserved	SDSP		
R/W	R/W		R/W	R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 45. Register 13 (0x0D) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6-5	SREF	R/W	0	PLL Reference:
4	SREF	R/W	0	DSP clock source – This bit select the source clock for internal PLL. This bit is ignored and overriden in clock auto set mode. 0: The PLL reference clock is MCLK 1: The PLL reference clock is SCLK 010: The PLL reference clock is oscillator clock 011: The PLL reference clock is GPIO (selected using P0-R18) Others: Reserved (PLL reference is muted)
3	Reserved	R/W		Reserved
2-0	SDSP	R/W	0	DAC clock source – These bits select the source clock for DSP clock divider. 000: Master clock (PLL/MCLK and OSC auto-select) 001: PLL clock 010: OSC clock 011: MCLK clock 100: SCLK clock 101: GPIO (selected using P0-R16) Others: Reserved (muted)

13.1.13 Register 14 (0x0E)

Figure 106. Register 14 (0x0E)

7	6	5	4	3	2	1	0
Reserved	SDAC			Reserved	SOSR		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 46. Register 14 (0x0E) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	SDAC	R/W	0	DAC clock source – These bits select the source clock for DAC clock divider. 000: Master clock (PLL/MCLK and OSC auto-select) 001: PLL clock 010: OSC clock 011: MCLK clock 100: SCLK clock 101: GPIO (selected using P0-R16) Others: Reserved (muted)
3	Reserved	R/W	0	Reserved
2-0	SOSR	R/W	0	OSR clock source – These bits select the source clock for OSR clock divider. 000: DAC clock 001: Master clock (PLL/MCLK and OSC auto-select) 010: PLL clock 011: OSC clock 100: MCLK clock 101: SCLK clock 110: GPIO (selected using P0-R17) Others: Reserved (muted)

13.1.14 Register 15 (0x0F)

Figure 107. Register 15 (0x0F)

7	6	5	4	3	2	1	0
Reserved					SNCP		
R/W					R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 47. Register 15 (0x0F) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W		Reserved
2-0	SNCP	R/W	0	NCP clock source – These bits select the source clock for CP clock divider. 000: DAC clock 001: Master clock (PLL/MCLK and OSC auto-select) 010: PLL clock 011: OSC clock 100: MCLK clock 101: SCLK clock 110: GPIO (selected using P0-R17) Others: Reserved (muted)

13.1.15 Register 16 (0x10)

Figure 108. Register 16 (0x10)

7	6	5	4	3	2	1	0
Reserved	GDSP			Reserved	GDAC		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 48. Register 16 (0x10) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	GDSP	R/W	0	GPIO Source for uCDSP clk – These bits select the GPIO pins as clock input source when GPIO is selected as DSP clock divider source. 000: N/A 001: N/A 010: N/A 011: GPIO0 100: N/A 101: GPIO2 Others: Reserved (muted)
3	Reserved	R/W	0	Reserved
2-0	GDAC	R/W	0	GPIO Source for DAC clk – These bits select the GPIO pins as clock input source when GPIO is selected as DAC clock divider source. 000: N/A 001: N/A 010: N/A 011: GPIO0 100: N/A 101: GPIO2 Others: Reserved (muted)

13.1.16 Register 17 (0x11)

Figure 109. Register 17 (0x11)

7	6	5	4	3	2	1	0
Reserved	GNCP			Reserved	GOSR		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 49. Register 17 (0x11) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	GNCP	R/W	0	GPIO Source for NCP clk – These bits select the GPIO pins as clock input source when GPIO is selected as CP clock divider source 000: N/A 001: N/A 010: Reserved 011: GPIO0 100: N/A 101: GPIO2 Others: Reserved (muted)
3	Reserved	R/W	0	Reserved
2-0	GOSR	R/W	0	GPIO Source for OSR clk – These bits select the GPIO pins as clock input source when GPIO is selected as OSR clock divider source. 000: N/A 001: N/A 010: Reserved 011: GPIO0 100: N/A 101: GPIO2 Others: Reserved (muted)

13.1.17 Register 18 (0x12)

Figure 110. Register 18 (0x12)

7	6	5	4	3	2	1	0
Reserved					GREF		
R/W					R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 50. Register 18 (0x12) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W	0	Reserved
2-0	GREF	R/W	0	GPIO Source for PLL reference clk – These bits select the GPIO pins as clock input source when GPIO is selected as the PLL reference clock source. 000: N/A 001: N/A 010: Reserved 011: GPIO0 100: N/A 101: GPIO2 Others: Reserved (muted)

13.1.18 Register 19 (0x13)

Figure 111. Register 19 (0x13)

7	6	5	4	3	2	1	0
Reserved			AREN	Reserved			RQSY
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. Register 19 (0x13) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4	AREN	R/W	1	Auto resync enable – This bits enables or disables the DAC/CP clock auto resynchronization with the beginning of audio frame. When enabled, the resynchronization is carried out just before the DAC transitions from standby mode to normal operation mode. 0: Auto resynchronization is disabled 1: Auto resynchronization is enabled
3-1	Reserved	R/W		Reserved
0	RQSY	R/W	0	This bit, when set to 1 will issue the clock resynchronization by synchronously resets the DAC, CP and OSR clocks. The actual clock resynchronization takes place when this bit is set back to 0, where the DAC, CP and OSR clocks are resumed at the beginning of the audio frame. 0: Resume DAC, CP and OSR clocks synchronized to the beginning of audio frame 1: Halt DAC, CP and OSR clocks as the beginning of resynchronization process

13.1.19 Register 20 (0x14)

Figure 112. Register 20 (0x14)

7	6	5	4	3	2	1	0
Reserved	PPDV				Reserved		
R/W	R/W				R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 52. Register 20 (0x14) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-3	PPDV	R/W	0	PLL P – These bits set the PLL divider P factor. These bits are ignored in clock auto set mode. 0000: P=1 0001: P=2 ... 1110: P=15 1111: Prohibited (do not set this value)
2-1	Reserved	R/W	0	Reserved
0	Reserved	R/W	1	Reserved

13.1.20 Register 21 (0x15)

Figure 113. Register 21 (0x15)

7	6	5	4	3	2	1	0
Reserved		PJDV		Reserved			Reserved
R/W		R/W		R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 53. Register 21 (0x15) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved		0	Reserved
5-4	PJDV	P/W	0	PLL J – These bits set the J part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 000000: Prohibited (do not set this value) 000001: J=1 000010: J=2 ... 111111: J=63
3		P/W	1	Reserved
2-0		P/W	0	Reserved

13.1.21 Register 22 (0x16)

Figure 114. Register 22 (0x16)

7	6	5	4	3	2	1	0
Reserved		PDDV					
R/W		R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 54. Register 22 (0x16) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W		Reserved
5-0	PDDV	R/W	0	PLL D (MSB) – These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 0 (in decimal): D=0000 1 (in decimal): D=0001 ... 9999 (in decimal): D=9999 Others: Prohibited (do not set)

13.1.22 Register 23 (0x17)

Figure 115. Register 23 (0x17)

7	6	5	4	3	2	1	0
PDDV							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 55. Register 23 (0x17) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PDDV	R/W	0	PLL D (LSB) – These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 0 (in decimal): D=0000 1 (in decimal): D=0001 ... 9999 (in decimal): D=9999 Others: Prohibited (do not set)

13.1.23 Register 24 (0x18)

Figure 116. Register 24 (0x18)

7	6	5	4	3	2	1	0
Reserved				PRDV			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 56. Register 24 (0x18) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W		Reserved
3-0	PRDV	R/W	0	PLL R – These bits set the R part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 0000: R=1 0001: R=2 ... 1111: R=16

13.1.24 Register 25 (0x19)

Figure 117. Register 25 (0x19)

7	6	5	4	3	2	1	0
PLCT							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 57. Register 25 (0x19) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLCT	R/W	0	PLL Lock Count – These bits set the number of consecutive PLL lock flags counted by the feedback clock before PLL is declared locked. The count value is updated when addr 26 is written, so it is recommended to update addr 25 first and then addr 26.

13.1.25 Register 26 (0x1A)

Figure 118. Register 26 (0x1A)

7	6	5	4	3	2	1	0
PLCT							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 58. Register 26 (0x1A) Field Descriptions

Bit	Field	Type	Reset	Description
7	PLCT	R/W	1	PLL Lock Count – These bits set the number of consecutive PLL lock flags counted by the feedback clock before PLL is declared locked. The count value is updated when addr 26 is written, so it is recommended to update addr 25 first and then addr 26.
6-0		R/W	0	

13.1.26 Register 27 (0x1B)

Figure 119. Register 27 (0x1B)

7	6	5	4	3	2	1	0
Reserved	DDSP						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 59. Register 27 (0x1B) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6-0	DDSP	R/W	0	DSP Clock Divider – These bits set the source clock divider value for the DSP clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

13.1.27 Register 28 (0x1C)

Figure 120. Register 28 (0x1C)

7	6	5	4	3	2	1	0
Reserved	DDAC						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 60. Register 28 (0x1C) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Reserved
6-4	DDAC	R/W	0	DAC Clock Divider – These bits set the source clock divider value for the DAC clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128
3-0		R/W	1	

13.1.28 Register 29 (0x1D)

Figure 121. Register 29 (0x1D)

7	6	5	4	3	2	1	0
Reserved	DNCP						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 61. Register 29 (0x1D) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Reserved
6-2	DNCP	R/W	0	NCP Clock Divider – These bits set the source clock divider value for the CP clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128
1-0		R/W	1	

13.1.29 Register 30 (0x1E)

Figure 122. Register 30 (0x1E)

7	6	5	4	3	2	1	0
Reserved	DOSR						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 62. Register 30 (0x1E) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Reserved
6-4	DOSR	R/W	0	OSR Clock Divider – These bits set the source clock divider value for the OSR clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128
5-0		R/W	1	

13.1.30 Register 31 (0x1F)

Figure 123. Register 31 (0x1F)

7	6	5	4	3	2	1	0
Reserved	DOFS						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 63. Register 31 (0x1F) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Reserved
6-3	DOFS	R/W	0	Offset calibrator clock div – These bits set the source clock divider value for the offset calibrator 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128
2		R/W	1	
1-0		R/W	0	

13.1.31 Register 32 (0x20)

Figure 124. Register 32 (0x20)

7	6	5	4	3	2	1	0
Reserved	DSCLK						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 64. Register 32 (0x20) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6-0	DSCLK	R/W	0	Master Mode SCLK Divider – These bits set the MCLK divider value to generate I2S master SCLK clock. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

13.1.32 Register 33 (0x21)

Figure 125. Register 33 (0x21)

7	6	5	4	3	2	1	0
DLRK							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 65. Register 33 (0x21) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLRK	R/W	0	Master Mode LRCLK Divider – These bits set the I2S master SCLK clock divider value to generate I2S master LRCLK clock 00000000: Divide by 1 00000001: Divide by 2 ... 11111111: Divide by 256

13.1.33 Register 34 (0x22)

Figure 126. Register 34 (0x22)

7	6	5	4	3	2	1	0
Reserved			I16E	Reserved	FSSP	FSSP	
R/W			R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 66. Register 34 (0x22) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4	I16E	R/W	0	16x Interpolation – This bit enables or disables the 16x interpolation mode 0: 8x interpolation 1: 16x interpolation
3	Reserved	R/W		Reserved
2	FSSP	R/W	1	FS Speed Mode – These bits select the FS operation mode, which must be set according to the current audio sampling rate. These bits are ignored in clock auto set mode. 000: Reserved 001: Reserved 010: Reserved 011: 48 kHz 100: 88.2-96 kHz 101: Reserved 110: Reserved 111: 32kHz
1-0		R/W	0	

13.1.34 Register 35 (0x23)

Figure 127. Register 35 (0x23)

7	6	5	4	3	2	1	0
Reserved							INTFLAG
R/W							R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 67. Register 35 (0x23) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0		R	0	Pin interrupt sticky flag – Sticky flag that reflects the pin interrupt value. Once read pin interrupt and this register will automatically reset to 0. To mask which all faults/errors can generate this interrupt use B0_P0_R45. 0: interrupt de-asserted 1: interrupt asserted

13.1.35 Register 37 (0x25)

Figure 128. Register 37 (0x25)

7	6	5	4	3	2	1	0
Reserved	IDFS	IDBK	IDSK	IDCH	IDCM	DCAS	IPLK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 68. Register 37 (0x25) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6	IDFS	R/W	0	Ignore FS Detection – This bit controls whether to ignore the FS detection. When ignored, FS error will not cause a clock error. 0: Regard FS detection 1: Ignore FS detection
5	IDBK	R/W	0	Ignore SCLK Detection – This bit controls whether to ignore the SCLK detection against LRCLK. The SCLK must be stable between 32 FS and 256 FS inclusive or an error will be reported. When ignored, a SCLK error will not cause a clock error. 0: Regard SCLK detection 1: Ignore SCLK detection
4	IDSK	R/W	0	Ignore MCLK Detection – This bit controls whether to ignore the MCLK detection against LRCLK. Only some certain MCLK ratios within some error margin are allowed. When ignored, an MCLK error will not cause a clock error. 0: Regard MCLK detection 1: Ignore MCLK detection
3	IDCH	R/W	0	Ignore Clock Halt Detection – This bit controls whether to ignore the MCLK halt (static or frequency is lower than acceptable) detection. When ignored an MCLK halt will not cause a clock error. 0: Regard MCLK halt detection 1: Ignore MCLK halt detection
2	IDCM	R/W	0	Ignore LRCLK/SCLK Missing Detection – This bit controls whether to ignore the LRCLK/SCLK missing detection. The LRCLK/SCLK need to be in low state (not only static) to be deemed missing. When ignored an LRCLK/SCLK missing will not cause the DAC go into powerdown mode. 0: Regard LRCLK/SCLK missing detection 1: Ignore LRCLK/SCLK missing detection
1	DCAS	R/W	0	Disable Clock Divider Autoset – This bit enables or disables the clock auto set mode. When dealing with uncommon audio clock configuration, the auto set mode must be disabled and all clock dividers must be set manually. Addtionally, some clock detectors might also need to be disabled. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled and the clock dividers must be set manually. 0: Enable clock auto set 1: Disable clock auto set
0	IPLK	R/W	0	Ignore PLL Lock Detection – This bit controls whether to ignore the PLL lock detection. When ignored, PLL unlocks will not cause a clock error. The PLL lock flag at P0-R4, bit 4 is always correct regardless of this bit. 0: PLL unlocks raise clock error 1: PLL unlocks are ignored

13.1.36 Register 38 (0x26)

Figure 129. Register 38 (0x26)

7	6	5	4	3	2	1	0
BKCG				BKCB			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 69. Register 38 (0x26) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BKCG	R/W	1	BCLK count to good – These bits specify the number of consecutive valid SCLK counts in LRCLK until the SCLK is deemed good. To be valid, the SCLK counts in LRCLK should be between 32 and 256 inclusive and match the count at previous audio frame. 0000: One consecutive LRCLK 0001: Two consecutive LRCLKs ... 1111: 16 consecutive LRCLKs
3-2	BKCB	R/W	0	BCLK count to bad – These bits specify the number of consecutive invalid SCLK counts in LRCLK until the SCLK is deemed bad. To be valid, the SCLK counts in LRCLK should be between 32 and 256 inclusive and match the count at previous audio frame. 0000: One consecutive LRCLK 0001: Two consecutive LRCLKs ... 1111: 16 consecutive LRCLKs
1-0		R/W	1	

13.1.37 Register 39 (0x27)

Figure 130. Register 39 (0x27)

7	6	5	4	3	2	1	0
Reserved			MCLKT				
R/W			R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 70. Register 39 (0x27) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4-3	MCLKT	R/W	0	MCLK tolerance – These bits specify the tolerance for MCLK counts in LRCLK. When the MCLK count in LRCLK matches any valid ratio within this tolerance, it will be deemed good 00000: tolerate ± 0 count 00001: tolerate ± 1 count … 11111: tolerate ± 31 counts
2		R/W	1	
1-0		R/W	0	

13.1.38 Register 40 (0x28)

Figure 131. Register 40 (0x28)

7	6	5	4	3	2	1	0
Reserved		AFMT		Reserved		ALEN	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 71. Register 40 (0x28) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	–			
5-4	AFMT	R/W	0	I2S Data Format – These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: DSP 10: RTJ 11: LTJ
3-2	Reserved	R/W		Reserved
1	ALEN	R/W	1	I2S Word Length – These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits
0		R/W	0	

13.1.39 Register 41 (0x29)

Figure 132. Register 41 (0x29)

7	6	5	4	3	2	1	0
AOFS							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 72. Register 41 (0x29) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AOFS	R/W	0	I2S Shift – These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. 00000000: offset = 0 SCLK (no offset) 00000001: ofsset = 1 SCLK 00000010: offset = 2 SCLKs … 11111111: offset = 256 SCLKs

13.1.40 Register 42 (0x2A)

Figure 133. Register 42 (0x2A)

7	6	5	4	3	2	1	0
Reserved		AUPL		Reserved		AUPR	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 73. Register 42 (0x2A) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W		Reserved
5	AUPL	R/W	0	Left DAC Data Path – These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
4		R/W	1	
3-2	Reserved	R/W		Reserved
1	AUPR	R/W	0	Right DAC Data Path – These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)
0		R/W	1	

13.1.41 Register 43 (0x2B)

Figure 134. Register 43 (0x2B)

7	6	5	4	3	2	1	0
Reserved				PSEL			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 74. Register 43 (0x2B) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4-1	PSEL	R/W	0	DSP Program Selection – These bits select the DSP program to use for audio processing. 00000: Reserved 00001: Rom Mode 1 00010: Reserved 00011: Reserved
0		R/W	1	

13.1.42 Register 44 (0x2C)

Figure 135. Register 44 (0x2C)

7	6	5	4	3	2	1	0
Reserved				CLKM	CMDP		
R/W				R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 75. Register 44 (0x2C) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved			Reserved
3	CLKM	R/W	1	clk_missing_mode_hans_reg_r – Fallback option to change clock missing detection to older PCM device. In Hans clock missing is detected whenever either BCLK or LRCLK go missing. In older PCM device clock missing is detected whenever LRCLK or BCLK are stuck to 1. 0 : Old mode of ASI clock missing detection 1: Hans mode of ASI clock missing detect
2-0	CMDP	R/W	0	Clock Missing Detection Period – These bits set how long both SCLK and LRCLK keep low before the audio clocks deemed missing and the DAC transitions to powerdown mode. 000: about 1 second 001: about 2 seconds 010: about 3 seconds ... 111: about 8 seconds

13.1.43 Register 45 (0x2D)

Figure 136. Register 45 (0x2D)

7	6	5	4	3	2	1	0
MSKP							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 76. Register 45 (0x2D) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MSKP	R/W	1	Mask for Pin interrupt generated by device (?) To mask and selectively use the required faults alone to generate the interrupt 0 : No interrupt generated 1 : Allow interrupt to be generated 1 : No interrupt generated 1 : Allow interrupt to be generated 2 : No interrupt generated 1 : Allow interrupt to be generated 3 : No interrupt generated 1 : Allow interrupt to be generated 4 : No interrupt generated 1 : Allow interrupt to be generated 5 : No interrupt generated 1 : Allow interrupt to be generated Mask for Pin interrupt generated by device (short-flag) 6 : No interrupt generated 1 : Allow interrupt to be generated Mask for Pin interrupt generated by device (dsp_interrupt) 7 : No interrupt generated 1 : Allow interrupt to be generated

13.1.44 Register 46 (0x2E)

Figure 137. Register 46 (0x2E)

7	6	5	4	3	2	1	0
Reserved							SDZF
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 77. Register 46 (0x2E) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W		Reserved
0	SDZF	R/W	1	Disable Force shutdown of Backend – This controls the Backed device shutdown signal. When it is programmed 0 backend devi ce will be shutdown. 0 : Force shutdown of Backend 1 : Disable force shutdown of Backend

13.1.45 Register 47 (0x2F)

Figure 138. Register 47 (0x2F)

7	6	5	4	3	2	1	0
Reserved		DLSH	Reserved				
R/W		R/W	R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 78. Register 47 (0x2F) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W		Reserved
5	DLSH	R/W	0	Disable Last Sample Hold – This bit controls whether to hold the last sample at audio interface in the event of clock error. The last known good sample is held to prevent errorneous samples to flow through the DAC. 0: Enable last sample hold 1: Disable last sample hold
4-0	Reserved	R/W		Reserved

13.1.46 Register 48 (0x30)

Figure 139. Register 48 (0x30)

7	6	5	4	3	2	1	0
Reserved	EDINT	INTSTAT	INTGPIO			DBCLK	
R/W	R/W	R/W	R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 79. Register 48 (0x30) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Reserved
6	EDINT	R/W	1	Edge detection of pin interrupt input – this bit controls whether to detect a positive edge and send interrupt to dsp or reflect the pin value at the dsp_interrupt port 0: disable positive edge detect 1: enable positive edge detect
5	INTSTAT	R/W	0	Enable active low for input pin interrupt – This controls whether input pin interrupt is active low or active high. 0 : input pin interrupt is active high 1 : input pin interrupt is active low
4-2	INTGPIO	R/W	0	GPIO for input pin interrupt – these bits control which GPIO to be used as the input pin interrupt 000: pin interrupt disabled 001: pin interrupt = Input from RESERVED 010: pin interrupt = Input from RESERVED 011: Reserved 100: pin interrupt = Input from GPIO0 101: pin interrupt = Input from RESERVED 110: pin interrupt = Input from GPIO2 111: reserved
1-0	DBCLK	R/W	0	Pin debounce clock select – selects the clk frequency to be used for deboucing glitches on pin before detecting a flip on the pin (debouncing is done for 4 clock cycles of this selected clock) 00: approx 1 ms clk used for debouncing 01: approx 500 µs clk used for debouncing 10: approx 125 µs clk used for debouncing 11: oscillator clk used for debouncing

13.1.47 Register 49 (0x31)

Figure 140. Register 49 (0x31)

7	6	5	4	3	2	1	0
Reserved	GSPGPI2	Reserved	GSPGPI0	GSPGPI1		Reserved	
R/W	R/W	R/W	R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 80. Register 49 (0x31) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6	GSPGPI2	R/W	0	Enable GPIO2 value to propagate to DSP – Each bit when set high allows the corresponding GPIO pin value to propagate to DSP as an input port bus 0 : GPIO2 value will not propagate to DSP 1 : GPIO2 value is allowed to propagate to DSP
5	Reserved	R/W		Reserved
4	GSPGPI0	R/W	0	Enable GPIO0 value to propagate to DSP – Each bit when set high allows the corresponding GPIO pin value to propagate to DSP as an input port bus 0 : GPIO0 value will not propagate to DSP 1 : GPIO0 value is allowed to propagate to DSP

Table 80. Register 49 (0x31) Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	Reserved	R/W		Reserved

13.1.48 Register 50 (0x32)

Figure 141. Register 50 (0x32)

7	6	5	4	3	2	1	0
Reserved						DSPMEM	DSPCOEF
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 81. Register 50 (0x32) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1	DSPMEM	R/W	0	DSP boots from IRAM – When set DSP will boot from IRAM instead of IROM 0: boot DSP from IROM 1: boot DSP from IRAM
0	DSPCOEF	R/W		Use default coefficients from ZROM – This bit controls whether to use default coefficients from ZROM or use the non-default coefficients downloaded to device by the Host 0 : don't use default coefficients from ZROM 1 : use default coefficents from ZROM

13.1.49 Register 51 (0x33)

Figure 142. Register 51 (0x33)

7	6	5	4	3	2	1	0
Reserved							DSPINT
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 82. Register 51 (0x33) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W		Reserved
0	DSPINT	R/W		Interrupt DSP – This bit can be set to generate an interrupt to DSP. Once the DSP acknowledges this interrupt this bit will be automatically cleared 0: normal 1 : generate interrupt to DSP

13.1.50 Register 52 (0x34)

Figure 143. Register 52 (0x34)

7	6	5	4	3	2	1	0
Reserved				DSPRMEM	MEMCRYP	MEMCRC	
R/W				R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 83. (Register 52 (0x34) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0	Reserved
3	DSPRMEM	R/W	0	Enable read from IRAM,IROM,ZROM – This bit controls whether to allow reads to IRAM, IROM and ZROM . When this bit is zero , read request to these memories will give out a 0 0 : dis-allow read from IRAM,IROM and ZROM 1 : all reads from IRAM, IROM and ZROM
2	MEMCRYP	R/W	0	Disable decryption – This bit controls whether to disable or enable decryption on the content that is downloaded by Host into IRAM 0 : enable decryption 1 : disable decryption
1-0	MEMCRC	R/W	0	CRC seed selection for Decryption – These bits control which seed to use for CRC based decryption logic. 00 : use A5 hex as seed 01 : use B6 hex as seed 10 : use 94 hex as seed 11 : use E2 hex as seed

13.1.51 Register 53 (0x35)

Figure 144. Register 53 (0x35)

7	6	5	4	3	2	1	0
Reserved							RSTD
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 84. Register 53 (0x35) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W		Reserved
0	RSTD	WO	0	Reset decryption block – Setting this bit to '1' resets the decryption block and reinitializes the CRC with the CRC seed. It is a self clearing bit. '1' -> reset the decryption block '0' -> decryption block is not reset

13.1.52 Register 59 (0x3B)

Figure 145. Register 59 (0x3B)

7	6	5	4	3	2	1	0
Reserved	AMTL			Reserved	AMTR		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 85. Register 59 (0x3B) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6-4	AMTL	R/W	0	Auto Mute Time for Left Channel – These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	Reserved	R/W		Reserved
2-0	AMTR	R/W	0	Auto Mute Time for Right Channel – These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

13.1.53 Register 60 (0x3C)

Figure 146. Register 60 (0x3C)

7	6	5	4	3	2	1	0
Reserved						PCTL	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 86. Register 60 (0x3C) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1-0	PCTL	R/W	0	Digital Volume Control – These bits control the behavior of the digital volume. 00: The volume for Left and right channels are independent 01: Right channel volume follows left channel setting

13.1.54 Register 61 (0x3D)

Figure 147. Register 61 (0x3D)

7	6	5	4	3	2	1	0
VOLL							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 87. Register 61 (0x3D) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOLL	R/W	00010000	Left Digital Volume – These bits control the left channel digital volume. The digital volume is 24 dB to –103 dB in –0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB … 00101111: +0.5 dB 00110000: 0.0 dB 00110001: –0.5 dB ... 11111110: –103 dB 11111111: Mute

13.1.55 Register 62 (0x3E)

Figure 148. Register 62 (0x3E)

7	6	5	4	3	2	1	0
VOLR							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 88. Register 62 (0x3E) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOLR	R/W	00110000	Right Digital Volume – These bits control the right channel digital volume. The digital volume is 24 dB to –103 dB in –0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB … 00101111: +0.5 dB 00110000: 0.0 dB 00110001: –0.5 dB ... 11111110: –103 dB 11111111: Mute

13.1.56 Register 63 (0x3F)

Figure 149. Register 63 (0x3F)

7	6	5	4	3	2	1	0
VNDF		VNDS		VNUF		VNUS	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 89. Register 63 (0x3F) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VNDF	R/W	0	Digital Volume Normal Ramp Down Frequency – These bits control the frequency of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or P0-R3. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VNDS	R/W	1	Digital Volume Normal Ramp Down Step – These bits control the step of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or P0-R3. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-2	VNUF	R/W	0	Digital Volume Normal Ramp Up Frequency – These bits control the frequency of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by XSMUTE pin or P0-R3. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	VNUS	R/W	1	Digital Volume Normal Ramp Up Step – These bits control the step of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by XSMUTE pin or P0-R3. 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

13.1.57 Register 64 (0x40)

Figure 150. Register 64 (0x40)

7	6	5	4	3	2	1	0
VEDF		VEDS		Reserved			
R/W		R/W		R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 90. Register 64 (0x40) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VEDF	R/W	0	Digital Volume Emergency Ramp Down Frequency – These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VEDS	R/W	1	Digital Volume Emergency Ramp Down Step – These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-0	Reserved	R/W		Reserved

13.1.58 Register 65 (0x41)

Figure 151. Register 65 (0x41)

7	6	5	4	3	2	1	0
Reserved					ACTL	AMLE	AMRE
R/W					R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 91. Register 65 (0x41) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W		Reserved
2	ACTL	R/W	1	Auto Mute Control**NOBUS** – This bit controls the behavior of the auto mute upon zero sample detection. The time length for zero detection is set with P0-R59. 0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted.
1	AMLE	R/W	1	Auto Mute Left Channel**NOBUS** – This bit enables or disables auto mute on right channel. Note that when right channel auto mute is disabled and the P0-R65, bit 2 is set to 1, the left channel will also never be auto muted. 0: Disable right channel auto mute 1: Enable right channel auto mute
0	AMRE	R/W	1	Auto Mute Right Channel**NOBUS** – This bit enables or disables auto mute on left channel. Note that when left channel auto mute is disabled and the P0-R65, bit 2 is set to 1, the right channel will also never be auto muted. 0: Disable left channel auto mute 1: Enable left channel auto mute

13.1.59 Register 66 (0x42)

Figure 152. Register 66 (0x42)

7	6	5	4	3	2	1	0
ADLY							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 92. Register 66 (0x42) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADLY	R/W	00011001	AMUTE Delay – These bits control the delay before the complete digital mute to the assertion of analog mute. This is to allow the non-mute audio samples to completely flow out through analog parts before the assertion of the analog mute. 00000000: No delay 00000001: 1 LRCLK delay 00000010: 2 LRCLK delay … 11111111: 255 LRCLK delay

13.1.60 Register 67 (0x43)

Figure 153. Register 67 (0x43)

7	6	5	4	3	2	1	0
DLPA		DRPA		DLPM		DRPM	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 93. Register 67 (0x43) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DLPA	R/W	0	Left DAC primary AC dither gain – These bits control the AC dither gain for left channel primary DAC modulator. 00: AC dither gain = 0.125 01: AC dither gain = 0.25
5-4	DRPA	R/W	0	Right DAC primary AC dither gain – These bits control the AC dither gain for right channel primary DAC modulator. 00: AC dither gain = 0.125 01: AC dither gain = 0.25
3-2	DLPM	R/W	0	Left DAC primary DEM dither gain – These bits control the dither gain for left channel primary Galton DEM. 00: DEM dither gain = 0.5 01: DEM dither gain = 1.0 Others: Reserved (do not set)
1-0	DRPM	R/W	0	Right DAC primary DEM dither gain – These bits control the dither gain for right channel primary Galton DEM. 00: DEM dither gain = 0.5 01: DEM dither gain = 1.0 Others: Reserved (do not set)

13.1.61 Register 68 (0x44)

Figure 154. Register 68 (0x44)

7	6	5	4	3	2	1	0
Reserved						DLPD	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 94. Register 68 (0x44) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W		Reserved
2-0	DLPD	R/W	0	Left DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

13.1.62 Register 69 (0x45)

Figure 155. Register 69 (0x45)

7	6	5	4	3	2	1	0
DLPD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 95. Register 69 (0x45) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLPD	R/W	0	Left DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

13.1.63 Register 70 (0x46)

Figure 156. Register 70 (0x46)

7	6	5	4	3	2	1	0
DRPD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 96. Register 70 (0x46) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRPD	R/W	0	Right DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

13.1.64 Register 71 (0x47)

Figure 157. Register 71 (0x47)

7	6	5	4	3	2	1	0
DRPD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 97. Register 71 (0x47) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRPD	R/W	0	Right DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

13.1.65 Register 72 (0x48)

Figure 158. Register 72 (0x48)

7	6	5	4	3	2	1	0
DLSA		DRSA		DLSM		RSM	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 98. Register 72 (0x48) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DLSA	R/W	01	Left DAC secondary AC dither gain – These bits control the AC dither gain for left channel secondary DAC. 00: AC dither gain = 0.125 01: AC dither gain = 0.25
5-4	DRSA	R/W	01	Right DAC secondary AC dither gain – These bits control the AC dither gain for right channel secondary DAC modulator. 00: AC dither gain = 0.125 01: AC dither gain = 0.25 10: AC dither gain = 0.5 11: no AC dither
3-2	DLSM	R/W	01	Left DAC secondary DEM dither gain – These bits control the dither gain for left channel secondary Galton DEM. 00: DEM dither gain = 0.5 01: DEM dither gain = 1.0 Others: Reserved (do not set)
1-0	DRSM	R/W	01	Right DAC secondary DEM dither gain – These bits control the dither gain for right channel secondary Galton DEM. 00: DEM dither gain = 0.5 01: DEM dither gain = 1.0 Others: Reserved (do not set)

13.1.66 Register 73 (0x49)

Figure 159. Register 73 (0x49)

7	6	5	4	3	2	1	0
DLSD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 99. Register 73 (0x49) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLSD	R/W	0	Left DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

13.1.67 Register 74 (0x4A)

Figure 160. Register 74 (0x4A)

7	6	5	4	3	2	1	0
DLSD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 100. Register 74 (0x4A) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLSD	R/W	0	Left DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

13.1.68 Register 75 (0x4B)

Figure 161. Register 75 (0x4B)

7	6	5	4	3	2	1	0
DRSD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 101. Register 75 (0x4B) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRSD	R/W	00000000	Right DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

13.1.69 Register 76 (0x4C)

Figure 162. Register 76 (0x4C)

7	6	5	4	3	2	1	0
DRSD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 102. Register 76 (0x4C) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRSD	R/W	00000000	Right DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

13.1.70 Register 78 (0x4E)

Figure 163. Register 78 (0x4E)

7	6	5	4	3	2	1	0
OLOF							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 103. Register 78 (0x4E) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OLOF	R/W	00000000	Left OFSCAL offset – These bits controls the amount of manual DC offset to be added to the left channel DAC output. The additional offset would be approximately the negative of the decimal value of this register divided by 4 in mV. 01111111 : –31.75 mV 01111110 : –31.50 mV … 00000010 : –0.50 mV 00000001 : –0.25 mV 00000000 : 0.0 mV 11111111 : +0.25 mV 11111110 : +0.50 mV … 10000000 : +32.0 mV

13.1.71 Register 79 (0x4F)

Figure 164. Register 79 (0x4F)

7	6	5	4	3	2	1	0
OROF							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 104. Register 79 (0x4F) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OROF	R/W	0	Right OFSCAL offset – These bits controls the amount of manual DC offset to be added to the right channel DAC output. The additional offset would be approximately the negative of the decimal value of this register divided by 4 in mV. 01111111 : –31.75 mV 01111110 : –31.50 mV … 00000010 : –0.50 mV 00000001 : –0.25 mV 00000000 : 0.0 mV 11111111 : +0.25 mV 11111110 : +0.50 mV … 10000000 : +32.0 mV

13.1.72 Register 80 (0x50)

Figure 165. Register 80 (0x50)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 105. Register 80 (0x50) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.1.73 Register 81 (0x51)

Figure 166. Register 81 (0x51)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 106. Register 81 (0x51) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.1.74 Register 82 (0x52)

Figure 167. Register 82 (0x52)

7	6	5	4	3	2	1	0
Reserved				G1SL			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 107. Register 82 (0x52) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W		Reserved

13.1.75 Register 83 (0x53)

Figure 168. Register 83 (0x53)

7	6	5	4	3	2	1	0
Reserved				G0SL			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 108. Register 83 (0x53) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4-0	G0SL	R/W	0	GPIO0 Output Selection – These bits select the signal to output to GPIO0. To actually output the selected signal, the GPIO0 must be set to output mode at P0-R8. 0110: Clock invalid flag (clock error or clock changing or clock missing) 0111: Serial audio interface data output (SDOUT) 1000: Analog mute flag for left channel (low active) 1001: Analog mute flag for right channel (low active) 1010: PLL lock flag 1011: Charge pump clock 1100: Reserved 1101: Reserved 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD ** INTERNAL ** 1100: Short detection flag for left channel 1101: Short detection flag for right channel 10000: PLL clock/4 10001: Oscillator clock/4 10010: Impedance sense flag for left channel 10011: Impedance sense flag for right channel 10100: Internal UVP flag, becomes low when VDD falls below roughly 2.7V 10101: Offset calibration flag, asserted when the system is offset calibrating itself. 10110: Clock error flag 10111: Clock changing flag 11000: Clock missing flag 11001: Clock halt detection flag 11010: DSP boot done flag 11011: Charge pump voltage output valid flag (low active) Others: N/A (zero)

13.1.76 Register 84 (0x54)

Figure 169. Register 84 (0x54)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 109. Register 84 (0x54) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.1.77 Register 85 (0x55)

Figure 170. Register 85 (0x55)

7	6	5	4	3	2	1	0
Reserved			G2SL				
R/W			R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 110. Register 85 (0x55) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4-0	G2SL	R/W	0	GPIO2 Output Selection – These bits select the signal to output to GPIO2. To actually output the selected signal, the GPIO2 must be set to output mode at P0-R8. 0000: off (low) 0001: DSP GPIO2 output 0010: Register GPIO2 output (P0-R86, bit 5) 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock changing or clock missing) 0111: Serial audio interface data output (SDOUT) 1000: Analog mute flag for left channel (low active) 1001: Analog mute flag for right channel (low active) 1010: PLL lock flag 1011: Charge pump clock 1100: Reserved 1101: Reserved 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD ** INTERNAL ** 1100: Short detection flag for left channel 1101: Short detection flag for right channel 10000: PLL clock/4 10001: Oscillator clock/4 10010: Impedance sense flag for left channel 10011: Impedance sense flag for right channel 10100: Internal UVP flag, becomes low when VDD falls below roughly 2.7V 10101: Offset calibration flag, asserted when the system is offset calibrating itself. 10110: Clock error flag 10111: Clock changing flag 11000: Clock missing flag 11001: Clock halt detection flag 11010: DSP boot done flag 11011: Charge pump voltage output valid flag (low active) Others: N/A (zero)

13.1.78 Register 86 (0x56)

Figure 171. Register 86 (0x56)

7	6	5	4	3	2	1	0
Reserved		GOUT2	MUTE	GOUT0	Reserved	Reserved	
R/W		R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 111. Register 86 (0x56) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GOUT2	R/W	0	GPIO Output Control – This bit controls the GPIO2 output when the selection at P0-R85 is set to 0010 (register output) 0: Output low 1: Output high
4	MUTE	R/W	0	This bit controls the MUTE output when the selection at P0-R84 is set to 0010 (register output). 0: Output low 1: Output high
3	GOUT0	R/W	0	This bit controls the GPIO0 output when the selection at P0-R83 is set to 0010 (register output) 0: Output low 1: Output high
2-0	Reserved	R/W	0	Reserved

13.1.79 Register 87 (0x57)

Figure 172. Register 87 (0x57)

7	6	5	4	3	2	1	0
Reserved		GINV2	MUTE	GINV0	Reserved	Reserved	
R/W		R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 112. Register 87 (0x57) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GINV2	R/W	0	GPIO Output Inversion – This bit controls the polarity of GPIO2 output. When set to 1, the output will be inverted for any signal being selected. 0: Non-inverted 1: Inverted
4	MUTE	R/W	0	This bit controls the polarity of MUTE output. When set to 1, the output will be inverted for any signal being selected. 0: Non-inverted 1: Inverted
3	GINV0	R/W	0	This bit controls the polarity of GPIO0 output. When set to 1, the output will be inverted for any signal being selected. 0: Non-inverted 1: Inverted
2-0	Reserved	R/W	0	Reserved

13.1.80 Register 88 (0x58)

Figure 173. Register 88 (0x58)

7	6	5	4	3	2	1	0
DIEI							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 113. Register 88 (0x58) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIEI	RO	0x84	Die ID, Device ID = 0x84

13.1.81 Register 89 (0x59)

Figure 174. Register 89 (0x59)

7	6	5	4	3	2	1	0
Reserved		VSTL	VENTL	Reserved		VSTR	VENR
R/W		R	R	R/W		R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 114. Register 89 (0x59) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	VSTL	R	0	Left Digital Volume Status – This bit indicates the status of the left channel digital volume. 0: Digital volume is not changing 1: Digital volume is changing
4	VENTL	R	0	Left Digital Volume Complete Flag – This bit indicates whether the left channel digital volume has reached its target volume. 0: The digital volume has not reached the target volume 1: The digital volume has reached the target volume
3-2	Reserved	R/W	0	Reserved
1	VSTR	R	0	Right Digital Volume Status – This bit indicates the status of the right channel digital volume. 0: Digital volume is not changing 1: Digital volume is changing
0	VENR	R	0	Right Digital Volume Complete Flag – This bit indicates whether the right channel digital volume has reached its target volume. 0: The digital volume has not reached the target volume 1: The digital volume has reached the target volume

13.1.82 Register 91 (0x5B)

Figure 175. Register 91 (0x5B)

7	6	5	4	3	2	1	0
Reserved	DTFS			DTSR			
R/W	R			R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 115. Register 91 (0x5B) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	DTFS	R	0	Detected FS – These bits indicate the currently detected audio sampling rate. 000: Error (Out of valid range) 001: 8 kHz 010: 16 kHz 011: 32-48 kHz 100: 88.2-96 kHz 101: 176.4-192 kHz 110: 384 kHz
3-0	DTSR	R	0	Detected MCLK Ratio – These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz. 0000: Ratio error (The MCLK ratio is not allowed) 0001: MCLK = 32 FS 0010: MCLK = 48 FS 0011: MCLK = 64 FS 0100: MCLK = 128 FS 0101: MCLK = 192 FS 0110: MCLK = 256 FS 0111: MCLK = 384 FS 1000: MCLK = 512 FS 1001: MCLK = 768 FS 1010: MCLK = 1024 FS 1011: MCLK = 1152 FS 1100: MCLK = 1536 FS 1101: MCLK = 2048 FS 1110: MCLK = 3072 FS

13.1.83 Register 92 (0x5C)

Figure 176. Register 92 (0x5C)

7	6	5	4	3	2	1	0
Reserved						DTBR	
R/W						R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 116. Register 92 (0x5C) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
1	DTBR	R	0	Detected SCLK Ratio (MSB)

13.1.84 Register 93 (0x5D)

Figure 177. Register 93 (0x5D)

7	6	5	4	3	2	1	0
DTBR	Reserved						
R	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 117. Register 93 (0x5D) Field Descriptions

Bit	Field	Type	Reset	Description
7	DTBR	R		Detected SCLK Ratio (LSB) – These bits indicate the currently detected SCLK ratio, i.e. the number of SCLK clocks in one audio frame. Note that for extreme case of SCLK = 1 FS (which is not usable anyway), the detected ratio will be unreliable
6-0	Reserved	R/W	0	Reserved

13.1.85 Register 94 (0x5E)

Figure 178. Register 94 (0x5E)

7	6	5	4	3	2	1	0
Reserved	CDST6	CDST5	CDST4	CDST3	CDST2	CDST1	CDST0
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 118. Register 94 (0x5E) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6	CDST6	R		Clock Detector Status – This bit indicates whether the MCLK clock is present or not. 0: MCLK is present 1: MCLK is missing (halted)
5	CDST5	R		This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. 0: PLL is locked 1: PLL is unlocked
4	CDST4	R		This bit indicates whether the both LRCLK and SCLK are missing (tied low) or not. 0: LRCLK and/or SCLK is present 1: LRCLK and SCLK are missing
3	CDST3	R		This bit indicates whether the combination of current sampling rate and MCLK ratio is valid for clock auto set. 0: The combination of FS/MCLK ratio is valid 1: Error (clock auto set is not possible)
2	CDST2	R		This bit indicates whether the MCLK is valid or not. The MCLK ratio must be detectable to be valid. There is a limitation with this flag, that is, when the low period of LRCLK is less than or equal to five SCLKs, this flag will be asserted (MCLK invalid reported). 0: MCLK is valid 1: MCLK is invalid
1	CDST1	R		This bit indicates whether the SCLK is valid or not. The SCLK ratio must be stable and in the range of 32-256FS to be valid. 0: SCLK is valid 1: SCLK is invalid
0	CDST0	R		This bit indicated whether the audio sampling rate is valid or not. The sampling rate must be detectable to be valid. There is a limitation with this flag, that is when this flag is asserted and P0-R37 is set to ignore all asserted error flags such that the DAC recovers, this flag will be de-asserted (sampling rate invalid not reported anymore). 0: Sampling rate is valid 1: Sampling rate is invalid

13.1.86 Register 95 (0x5F)

Figure 179. Register 95 (0x5F)

7	6	5	4	3	2	1	0
Reserved			LTSH	Reserved	CKMF	CSRF	CERF
R/W			R	R/W	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 119. Register 95 (0x5F) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	LTSH	R		Latched Clock Halt – This bit indicates whether MCLK halt has occurred. The bit is cleared when read. 0: MCLK halt has not occurred 1: MCLK halt has occurred since last read
3	Reserved	R/W	0	Reserved
2	CKMF	R		Clock Missing – This bit indicates whether the LRCLK and SCLK are missing (tied low). 0: LRCLK and/or SCLK is present 1: LRCLK and SCLK are missing
1	CSRF	R		Clock Resync Request – This bit indicates whether the clock resynchronization is in progress. 0: Not resynchronizing 1: Clock resynchronization is in progress
0	CERF	R		Clock Error – This bit indicates whether a clock error has occurred. The bit is cleared when read 0: Clock error has not occurred 1: Clock error has occurred.

13.1.87 Register 96 (0x60)

Figure 180. Register 96 (0x60)

7	6	5	4	3	2	1	0
Reserved	PDPM						
R/W	R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 120. Register 96 (0x60) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-0	PDPM	RO		PLL P Monitor – These bits indicate the actually used value for PLL divider P. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 0000000: P = 1 0000001: P = 2 ... 1111111: P = 128

13.1.88 Register 97 (0x61)

Figure 181. Register 97 (0x61)

7	6	5	4	3	2	1	0
Reserved		PDJM					
R/W		R					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 121. Register 97 (0x61) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5-0	PDJM	R		PLL J Monitor – These bits indicate the actually used value for PLL multiplication factor J of the overall J.D × R. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 000000: Error 000001: J = 1 000010: J = 2 ... 111111: J = 63

13.1.89 Register 98 (0x62)

Figure 182. Register 98 (0x62)

7	6	5	4	3	2	1	0
Reserved		PDDM					
R/W		R					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 122. Register 98 (0x62) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5-0	PDDM	R		PLL D Monitor (MSB) – These bits indicate the actually used value for PLL multiplication factor D of the overall J.D × R. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 0 (in decimal): D=0000 1 (in decimal): D=0001 .... 9999 (in decimal): D=9999 Others: Error

13.1.90 Register 99 (0x63)

Figure 183. Register 99 (0x63)

7	6	5	4	3	2	1	0
Reserved		PDDM					
R/W		R					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 123. Register 99 (0x63) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	PDDM	R		PLL D Monitor (LSB) – These bits indicate the actually used value for PLL multiplication factor D of the overall J.D × R. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 0 (in decimal): D=0000 1 (in decimal): D=0001 .... 9999 (in decimal): D=9999 Others: Error

13.1.91 Register 100 (0x64)

Figure 184. Register 100 (0x64)

7	6	5	4	3	2	1	0
Reserved				PDRM			
R/W				R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 124. Register 100 (0x64)Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0	Reserved
3-0	PDRM	R		PLL R Monitor – These bits indicate the actually used value for PLL multiplication factor R of the overall J.D × R. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 0000: R = 1 0001: R = 2 ... 1111: R = 16

13.1.92 Register 101 (0x65)

Figure 185. Register 101 (0x65)

7	6	5	4	3	2	1	0
Reserved	DDSM						
R/W	R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 125. Register 101 (0x65) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-0	DDSM	R		DSP clock divider monitor – These bits indicate the actually used value of the DSP clock divider ratio. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

13.1.93 Register 102 (0x66)

Figure 186. Register 102 (0x66)

7	6	5	4	3	2	1	0
Reserved	DDAM						
R/W	R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 126. Register 102 (0x66) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-0	DDAM	R		DAC clock divider monitor – These bits indicate the actually used value of the DAC clock divider ratio. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

13.1.94 Register 103 (0x67)

Figure 187. Register 103 (0x67)

7	6	5	4	3	2	1	0
Reserved	DCPM						
R/W	R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 127. Register 103 (0x67) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-0	DCPM	R		NCP clock divider monitor – These bits indicate the actually used value of the CP clock divider ratio. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

13.1.95 Register 104 (0x68)

Figure 188. Register 104 (0x68)

7	6	5	4	3	2	1	0
Reserved	DOSM						
R/W	R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 128. Register 104 (0x68) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-0	DOSM	R		OSR clock divider monitor – These bits indicate the actually used value of the OSR clock divider ratio. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

13.1.96 Register 105 (0x69)

Figure 189. Register 105 (0x69)

7	6	5	4	3	2	1	0
Reserved			PENM	Reserved	PRFM		
R/W			R	R/W	R		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 129. Register 105 (0x69) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4	PENM	R		PLL enable monitor – This bit indicates whether the PLL is currently enabled. 0: PLL is disabled 1: PLL is enabled
3	Reserved	R/W		Reserved
2-0	PRFM	R		PLL Reference Monitor – These bits indicate the actual source for the PLL. The source is auto set when clock auto set is active and register set when clock auto set is disabled. 000: MCLK 001: SCLK 010: OSC 011: GPIO Others: Reserved (mute)

13.1.97 Register 106 (0x6A)

Figure 190. Register 106 (0x6A)

7	6	5	4	3	2	1	0
CPPM	RFPM	LDPM	LBPM	LCPM	LOPM	ROPM	DAPM
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 130. Register 106 (0x6A) Field Descriptions

Bit	Field	Type	Reset	Description
7	CPPM	R		CP $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for CP powerdown status. 0: Powered down 1: Active
6	RFPM	R		REF $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for analog reference powerdown status. 0: Powered down 1: Active
5	LDPM	R		Line Driver $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for line driver powerdown status. 0: Powered down 1: Active
4	LBPM	R		Line Bias $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for line bias powerdown status. 0: Powered down 1: Active
3	LCPM	R		Line CMFB2 $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for line common feedback powerdown status. 0: Powered down 1: Active
2	LOPM	R		L Output Stage $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for left channel output stage powerdown status. 0: Powered down 1: Active

Table 130. Register 106 (0x6A) Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ROPM	R		R Output Stage $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for right channel output stage powerdown status.. 0: Powered down 1: Active
0	DAPM	R		DAC $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for DAC powerdown status. 0: Powered down 1: Active

13.1.98 Register 107 (0x6B)

Figure 191. Register 107 (0x6B)

7	6	5	4	3	2	1	0
OFPM	SSPM	ISPM	IWPM	LSPM	RSPM	DSRM	DERM
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 131. Register 107 (0x6B) Field Descriptions

Bit	Field	Type	Reset	Description
7	OFPM	R		OFSCOMP $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for offset compensator powerdown status. 0: Powered down 1: Active
6	SSPM	R		Short Protection $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for short protector powerdown status. 0: Powered down 1: Active
5	ISPM	R		IMP sense $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for impedance sensor powerdown status. 0: Powered down 1: Active
4	IWPM	R		IMP whole $\overline{\text{PWRDN}}$ monitor – This bit is a monitor for whole impedance sensor circuitry powerdown status. 0: Powered down 1: Active
3	LSPM	R		L Short Protection $\overline{\text{RST}}$ monitor – This bit is a monitor for left channel short protector reset status. 0: Reset 1: Active
2	RSPM	R		R Short Protection $\overline{\text{RST}}$ monitor – This bit is a monitor for right channel short protector reset status. 0: Reset 1: Active
1	DSRM	R		DSM $\overline{\text{RST}}$ monitor – This bit is a monitor for DAC modulator reset status. 0: Reset 1: Active
0	DERM	R		DEM $\overline{\text{RST}}$ monitor – This bit is a monitor for DAC DEM reset status. 0: Reset 1: Active

13.1.99 Register 108 (0x6C)

Figure 192. Register 108 (0x6C)

7	6	5	4	3	2	1	0
Reserved		ADLM	ADRM	Reserved		AMLM	AMRM
R/W		R	R	R/W		R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 132. Register 108 (0x6C) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	ADLM	R		$\overline{\text{AMUTE}}$ dummy left monitor – This bit is a monitor for left channel dummy output analog mute status. 0: Mute 1: Unmute
4	ADRM	R		$\overline{\text{AMUTE}}$ dummy right monitor – This bit is a monitor for right channel dummy output analog mute status. 0: Mute 1: Unmute
3-2	Reserved	R/W	0	Reserved
1	AMLM	R		Left Analog Mute Monitor – This bit is a monitor for left channel analog mute status. 0: Mute 1: Unmute
0	AMRM	R		Right Analog Mute Monitor – This bit is a monitor for right channel analog mute status. 0: Mute 1: Unmute

13.1.100 Register 109 (0x6D)

Figure 193. Register 109 (0x6D)

7	6	5	4	3	2	1	0
Reserved			SDTM	Reserved			SHTM
R/W			R	R/W			R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 133. Register 109 (0x6D) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	SDTM	R		Short detect monitor – This bit indicates whether line output short is occuring. 0: Normal (No short) 1: Line output is being shorted
3-1	Reserved	R/W	0	Reserved
0	SHTM	R		Short detected monitor – This bit indicates whether line output short has occurred since last read. This bit is sticky and is cleared when read. 0: No short 1: Line output short occurred

13.1.101 Register 110 (0x6E)

Figure 194. Register 110 (0x6E)

7	6	5	4	3	2	1	0
DLCM							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 134. Register 110 (0x6E) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLCM	R		Left DIFF control monitor – These bits indicate the final control value of the left channel differential offset compensator. The value approximates the magnitude of the original offset before calibration. 0000000: 0 mV 0000001: 0.25 mV 0000010: 0.50 mV 0000011: 0.75 mV … 1111111: 63.75 mV

13.1.102 Register 111 (0x6F)

Figure 195. Register 111 (0x6F)

7	6	5	4	3	2	1	0
DRCM							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 135. Register 111 (0x6F) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRCM	R		Right DIFF control monitor – These bits indicate the final control value of the right channel differential offset compensator. The value approximates the magnitude of the original offset before calibration. 0000000: 0 mV 0000001: 0.25 mV 0000010: 0.50 mV 0000011: 0.75 mV … 1111111: 63.75 mV

13.1.103 Register 112 (0x70)

Figure 196. Register 112 (0x70)

7	6	5	4	3	2	1	0
DLCS	Reserved				CLCM		
R	R/W				R		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 136. Register 112 (0x70) Field Descriptions

Bit	Field	Type	Reset	Description
7	DLCS	R		Left DIFF control sign – This bit indicates the polarity of DC offset at left channel before calibration (the magnitude is indicated in R0/P110). 0: Negative 1: Positive
6-5	Reserved	R/W	0	Reserved
4-0	CLCM	R		Left CMFB control monitor – These bits indicate the final control value of the left channel common feedback offset compensator. The value approximates the magnitude of the original offset before calibration. 00000: 0 mV 00001: 0.25 mV 00010: 0.50 mV … 11111: 7.75 mV

13.1.104 Register 113 (0x71)

Figure 197. Register 113 (0x71)

7	6	5	4	3	2	1	0
DRCS	Reserved				CRCM		
R	R/W				R		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 137. Register 113 (0x71) Field Descriptions

Bit	Field	Type	Reset	Description
7	DRCS	R		Right DIFF control sign – This bit indicates the polarity of DC offset at right channel before calibration (the magnitude is indicated in R0-P111) 0: Negative 1: Positive
6-5	Reserved	R/W	0	Reserved
4-0	CRCM	R		Right CMFB control monitor – These bits indicate the final control value of the right channel common feedback offset compensator. The value approximates the magnitude of the original offset before calibration. 00000: 0 mV 00001: 0.25 mV 00010: 0.50 mV … 11111: 7.75 mV

13.1.105 Register 114 (0x72)

Figure 198. Register 114 (0x72)

7	6	5	4	3	2	1	0
Reserved						MTST	
R/W						R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 138. Register 114 (0x72) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1-0	MTST	R		$\overline{\text{MUTE}}$ status – These bits indicate the output of the XSMUTE level decoder for monitoring purpose. 11: 0.7 VDD ≤ XSMUTE 01: 0.3 VDD ≤ XSMUTE < 0.7 VDD 00: 0.3 VDD > XSMUTE

13.1.106 Register 115 (0x73)

Figure 199. Register 115 (0x73)

7	6	5	4	3	2	1	0
Reserved						FSMM	
R/W						R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 139. Register 115 (0x73) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W	0	Reserved
2-0	FSMM	R		FS Speed Mode Monitor – These bits indicate the actual FS operation mode being used. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled. **In Auto set,** 000: error 001: 8 kHz 010: 16 kHz 011: 32-48 kHz 100: 88.2-96 kHz 101: 176.4-192 kHz 110: 384 kHz 111: reserved **In register set mode,** 000: reserved 001: 8 kHz 010: 16 kHz 011: 48 kHz 100: 88.2-96 kHz 101: 176.4-192 kHz 110: 384 kHz 111: 32 kHz

13.1.107 Register 118 (0x76)

Figure 200. Register 118 (0x76)

7	6	5	4	3	2	1	0
BOTM	Reserved			PSTM			
R	R/W			R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 140. Register 118 (0x76) Field Descriptions

Bit	Field	Type	Reset	Description
7	BOTM	R		DSP Boot Done Flag – This bit indicates whether the DSP boot is completed. 0: DSP is booting 1: DSP boot completed
6-4	Reserved	R/W		Reserved
3-0	PSTM	R		Power State – These bits indicate the current power state of the DAC. 000: Powerdown 0001: Wait for CP voltage valid 0010: Common feedback offset calibration 0011: Differential mode offset calibration 0100: Volume ramp up 0101: Run (Playing) 0110: Line output short and Low impedance 0111: Volume ramp down 1000: Standby

13.1.108 Register 119 (0x77)

Figure 201. Register 119 (0x77)

7	6	5	4	3	2	1	0
Reserved		GPIN2	MUTE	GPIN0	Reserved	Reserved	Reserved
R/W		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 141. Register 119 (0x77) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GPIN2	RO		GPIO Input States – This bit indicates the logic level at GPIO2 pin. 0: Low 1: High
4	MUTE	RO		This bit indicates the logic level at MUTE pin. 0: Low 1: High
3	GPIN0	RO		This bit indicates the logic level at GPIO0 pin. 0: Low 1: High
2		RO		N/A 0: Low 1: High
1		RO		N/A 0: Low 1: High
0		RO		N/A 0: Low 1: High

13.1.109 Register 120 (0x78)

Figure 202. Register 120 (0x78)

7	6	5	4	3	2	1	0
Reserved			AMFL	Reserved			AMFR
R/W			R	R/W			R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 142. Register 120 (0x78) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	AMFL	R		Auto Mute Flag for Left Channel – This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted
3-1	Reserved	R/W	0	Reserved
0	AMFR	R		Auto Mute Flag for Right Channel – This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted

13.1.110 Register 121 (0x79)

Figure 203. Register 121 (0x79)

7	6	5	4	3	2	1	0
Reserved			DWAO	Reserved		DAMD	
R/W			R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 143. Register 121 (0x79) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	DWAO	R/W	0	DWA off – This bit controls the DWA rotation. 0: DWA is active (Rotation active) 1: DWA is disabled (No rotation)
3-2	Reserved	R/W	0	Reserved
1-0	DAMD	R/W	0	DAC Mode – This bit controls the DAC mode. 0: Mode1 1: Mode2 ** INTERNAL ** (Mode1: Cascaded Galton, Mode2: Cascaded DWA) 10: Non-cascaded Galton 11: Non-cascaded DWA

13.2 Registers - Page 1

13.2.1 Register 1 (0x01)

Figure 204. Register 1 (0x01)

7	6	5	4	3	2	1	0
Reserved			REXT	Reserved			OSEL
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 144. Register 1 (0x01) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	REXT	R/W	0	REF BG Ext - This bit controls what is output from the VCOM pin 0: AVDD divided voltage 1: Bandgap reference voltage
3-1	Reserved	R/W	0	Reserved
0	OSEL	R/W	0	Output Amplitude Type - This bit selects the output amplitude type. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled via P0-R37 and the clock dividers must be set manually. 0: VREF mode (Constant output amplitude against AVDD variation) 1: VCOM mode (Output amplitude is proportional to AVDD variation)

13.2.2 Register 2 (0x02)

Figure 205. Register 2 (0x02)

7	6	5	4	3	2	1	0
Reserved			LAGN	Reserved			RAGN
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 145. Register 2 (0x02) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	LAGN	R/W	0	Analog Gain Control for Left Channel - This bit controls the left channel analog gain. 0: 0 dB 1: -6 dB
3-1	Reserved	R/W	0	Reserved
0	RAGN	R/W	0	Analog Gain Control for Right Channel - This bit controls the right channel analog gain. 0: 0 dB 1: -6 dB

13.2.3 Register 3 (0x03)

Figure 206. Register 3 (0x03)

7	6	5	4	3	2	1	0
Reserved						CPDY	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 146. Register 3 (0x03) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W	0	Reserved
2-0	CPDY	R/W	0	CP Delay -These bits control the delay of charge pump clock. 000: 65 ns 001: 90 ns 010: 115 ns 011: 140 ns 100: 165 ns 101: 190 ns 110: 215 ns 111: 240 ns

13.2.4 Register 4 (0x04)

Figure 207. Register 4 (0x04)

7	6	5	4	3	2	1	0
Reserved						OPWR	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 147. Register 4 (0x04) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1-0	OPWR	R/W	1	Output Power - These bits control the power of output driver. 00: Normal power 01: Increased power 10: More increased power 11: Maximum power

13.2.5 Register 5 (0x05)

Figure 208. Register 5 (0x05)

7	6	5	4	3	2	1	0
Reserved						UEPD	UIPD
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 148. Register 5 (0x05) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1	UEPD	R/W	0	External UVP Control - This bit enables or disables detection of power supply drop via XSMUTE pin (External Under Voltage Protection). 0: Enabled 1: Disabled
0	UIPD	R/W	0	Internal UVP Control - This bit enables or disables internal detection of AVDD voltage drop (Internal Under Voltage Protection). 0: Enabled 1: Disabled

13.2.6 Register 6 (0x06)

Figure 209. Register 6 (0x06)

7	6	5	4	3	2	1	0
Reserved							AMCT
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 149. Register 6 (0x06) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	AMCT	R/W	1	Analog Mute Control -This bit enables or disables analog mute following digital mute. 0: Disabled 1: Enabled

13.2.7 Register 7 (0x07)

Figure 210. Register 7 (0x07)

7	6	5	4	3	2	1	0
Reserved			AGBL	Reserved			AGBR
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 150. Register 7 (0x07) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	AGBL	R/W	0	Analog +10% Gain for Left Channel - This bit enables or disables amplitude boost mode for left channel. 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude
3-1	Reserved	R/W	0	Reserved
0	AGBR	R/W	1	Analog +10% Gain for Right Channel - This bit enables or disables amplitude boost mode for right channel. 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude

13.2.8 Register 8 (0x08)

Figure 211. Register 8 (0x08)

7	6	5	4	3	2	1	0
Reserved			RBGF	Reserved			RCMF
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 151. Register 8 (0x08) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	RBGF	R/W	0	REF BG Fast - This bit controls the bandgap voltage ramp up speed. 0: Normal ramp up, ~50 ms with external capacitance = 1 µF 1: Fast ramp up, ~1 ms with external capacitance = 1 µF
3-1	Reserved	R/W	0	Reserved
0	RCMF	R/W	1	VCOM Reference Ramp Up - This bit controls the VCOM voltage ramp up speed. 0: Normal ramp up, ~600 ms with external capacitance = 1 µF 1: Fast ramp up, ~3 ms with external capacitance = 1 µF

13.2.9 Register 9 (0x09)

Figure 212. Register 9 (0x09)

7	6	5	4	3	2	1	0
Reserved						DEME	VCPD
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 152. Register 9 (0x09) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1	DEME	R/W	0	VCOM Pin as De-emphasis Control - This bit controls whether to use the DEEMP/VCOM pin as De-emphasis control. 0: Disabled (DEEMP/VCOM is not used to control De-emphasis) 1: Enabled (DEEMP/VCOM is used to control De-emphasis)
0	VCPD	R/W	1	Power down control for VCOM - This bit controls VCOM powerdown switch. 0: VCOM is powered on 1: VCOM is powered down

13.2.10 Register 10 (0x0A)

Figure 213. Register 10 (0x0A)

7	6	5	4	3	2	1	0
Reserved		LBBG		Reserved		LBVC	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 153. Register 10 (0x0A) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5-4	LBBG	R/W	1	Line 1st stage bias ctrl<1> at BG mode - Applied when LSB of 0x01 at Page1=0 0: low 1: high
3-2	Reserved	R/W	0	Reserved
1-0	LBVC	R/W	1	Line 1st stage bias ctrl<1> at COM mode - Applied when LSB of 0x01 at Page1=1 0: low 1: high

13.2.11 Register 11 (0x0B)

Figure 214. Register 11 (0x0B)

7	6	5	4	3	2	1	0
Reserved		CBBG		Reserved		CBVC	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 154. Register 11 (0x0B) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5-4	CBBG	R/W	1	CMFB bias ctrl<1> at BG mode - Applied when LSB of 0x01 at Page1=0 0: low 1: high
3-2	Reserved	R/W	0	Reserved
1-0	CBVC	R/W	0	CMFB bias ctrl<1> at COM mode - Applied when LSB of 0x01 at Page1=1 0: low 1: high

13.2.12 Register 12 (0x0C)

Figure 215. Register 12 (0x0C)

7	6	5	4	3	2	1	0
Reserved		SSBG		Reserved		SSVC	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 155. Register 12 (0x0C) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5-4	SSBG	R/W	0	Short protection sink ref current ctrl<1> at BG mode - Applied when LSB of 0x01at Page1=0 0: low 1: high
3-2	Reserved	R/W	0	Reserved
1-0	SSVC	R/W	0	Short protection sink ref current ctrl<1> at COM mode - Applied when LSB of 0x01 at Page1=1 0: low 1: high

13.2.13 Register 13 (0x0D)

Figure 216. Register 13 (0x0D)

7	6	5	4	3	2	1	0
Reserved		SRBG				SRVC	
R/W		R/W				R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 156. Register 13 (0x0D) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	SRBG	R/W	0	Short protection source ref current ctrl<1> at BG mode - Applied when LSB of 0x01 at Page1=0 0: low 1: high
4-2		R/W	1	
1	SRVC	R/W	0	Short protection source ref current ctrl<1> at COM mode - Applied when LSB of 0x01 at Page1=1 0: low 1: high
0		R/W	1	

13.2.14 Register 14 (0x0E)

Figure 217. Register 14 (0x0E)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 157. Register 14 (0x0E) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.2.15 Register 15 (0x0F)

Figure 218. Register 15 (0x0F)

7	6	5	4	3	2	1	0
Reserved							CPCP
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 158. Register 15 (0x0F) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	CPCP	R/W	1	NCP clock digital delay control - This bit controls the CP clock phase delay against the DAC clock. 0: 0 degree (no delay) 1: 180 degree delay

13.3 Registers - Page 253

13.3.1 Register 1 (0x01)

Figure 219. Register 1 (0x01)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 159. Register 1 (0x01) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.2 Register 2 (0x02)

Figure 220. Register 2 (0x02)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 160. Register 2 (0x02) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.3 Register 3 (0x03)

Figure 221. Register 3 (0x03)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 161. Register 3 (0x03 Field Descriptions)

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.4 Register 4 (0x04)

Figure 222. Register 4 (0x04)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 162. Register 4 (0x04) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.5 Register 5 (0x05)

Figure 223. Register 5 (0x05)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 163. Register 5 (0x05) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.6 Register 6 (0x06)

Figure 224. Register 6 (0x06)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 164. Register 6 (0x06) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.7 Register 7 (0x07)

Figure 225. Register 7 (0x07)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 165. Register 7 (0x07) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.8 Register 8 (0x08)

Figure 226. Register 8 (0x08)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 166. Register 8 (0x8) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.9 Register 9 (0x09)

Figure 227. Register 9 (0x09)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 167. Register 9 (0x9) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.10 Register 10 (0x0A)

Figure 228. Register 10 (0x0A)

7	6	5	4	3	2	1	0
DRSV	Reserved						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 168. Register 10 (0xA) Field Descriptions

Bit	Field	Type	Reset	Description
7	DRSV	R/W	0	Dither Reserved - Performance adjustment dither setting when "RESERVED" bond option is selected
6-0	Reserved	R/W	0	Reserved

13.3.11 Register 11 (0x0B)

Figure 229. Register 11 (0x0B)

7	6	5	4	3	2	1	0
D100	Reserved		OFSCAL0	OFSCAL1	OFSCAL2	OFSCAL3	OFSCAL4
R/W	R/W		R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 169. Register 11 (0xB) Field Descriptions

Bit	Field	Type	Reset	Description
7	D100	R/W	0	Dither Reserved - Performance adjustment dither setting when "RESERVED" bond option is selected
6-5	Reserved	R/W	0	Reserved
4	OFSCAL0	R/W	0	Ofscal Bypass Filter - Select whether to bypass the front-end filter. 0: Front-end filter used. 1: Front-end filter bypassed.
3	OFSCAL1	R/W	0	Ofscal Full Span - Select whether to activate front-end filter half period (good for majority type) or full period (good for averaging type). 0: Front-end filter is active last half of control period. 1: Front-end filter is active the whole control period.
2	OFSCAL2	R/W	0	Ofscal Average Filtering - Select the type of front-end filter. 0: Front-end filter is majority decision type 1: Front-end filter is averaging type
1	OFSCAL3	R/W	0	Ofscal Disable Fine Calibration - Select whether to do fine calibration. 0: Do 64-step coarse calibration followed by 32-step fine calibration. 1: Do 96-step coarse calibration only (no fine calibration).
0	OFSCAL4	R/W	0	Ofscal Disable Post Averaging - Select whether to use post-averaging on the integrator output. 0: Final calibration control source is post-averaging result. 1: Final calibration control source is integrator output.

13.3.12 Register 12 (0x0C)

Figure 230. Register 12 (0x0C)

7	6	5	4	3	2	1	0
D105	Reserved						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 170. Register 12 (0x0C) Field Descriptions

Bit	Field	Type	Reset	Description
7	D105	R/W	0	Dither 105 dB - Performance adjustment dither setting when "105dB" bond option is selected
6-0	Reserved	R/W	0	Reserved

13.3.13 Register 13 (0x0D)

Figure 231. Register 13 (0x0D)

7	6	5	4	3	2	1	0
D110	Reserved						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 171. Register 13 (0x0D) Field Descriptions

Bit	Field	Type	Reset	Description
7	D110	R/W	0	Dither 115 dB - Performance adjustment dither setting when "110dB" bond option is selected
6-0	Reserved	R/W	0	Reserved

13.3.14 Register 14 (0x0E)

Figure 232. Register 14 (0x0E)

7	6	5	4	3	2	1	0
Reserved			SUMD	Reserved			SUAS
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 172. Register 14 (0x0E) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	SUMD	R/W	0	SpeedUp CLK missing detection
3-1	Reserved	R/W	0	Reserved
0	SUAS	R/W	0	SpeedUp Analog Sequence

13.3.15 Register 15 (0x0F)

Figure 233. Register 15 (0x0F)

7	6	5	4	3	2	1	0
Reserved			SDEN	Reserved			DSOC
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 173. Register 15 (0x0F) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	SDEN	R/W	1	Short Detection Enable 0: Short detection enable 1: Short detection disable
3-1	Reserved	R/W	0	Reserved
0	DSOC	R/W	0	Disable Subsequent Offset Cancellation

13.3.16 Register 16 (0x10)

Figure 234. Register 16 (0x10)

7	6	5	4	3	2	1	0
Reserved		SWDA		Reserved			DPOL
R/W		R/W		R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 174. Register 16 (0x10) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved		0	Reserved
5	SDWA	R/W	1	Shuffle DWA of Galton - Shuffle DWA Outputs of Galton DEM 0,3: No shuffle
4		R/W	0	1: Shuffle Internally 2: Global Shuffle
3-1	Reserved		0	Reserved
0	DPOL	R/W	0	Select DC dither polarity for the secandary DAC. Select DC dither polarity +4.0% or -4.0% for the secondary DAC.

13.3.17 Register 17 (0x11)

Figure 235. Register 17 (0x11)

7	6	5	4	3	2	1	0
DLSC	Reserved			DRSC	Reserved		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 175. Register 17 (0x11) Field Descriptions

Bit	Field	Type	Reset	Description
7	DLSC	R/W	0	Left DAC Primary/Secondary Scale - Secondary to Primary scaling factor for left DAC
6-4	Reserved	R/W	0	Reserved
3	DRSC	R/W	0	Right DAC Primary/Secondary Scale - See DAC digital design spec
2-0	Reserved	R/W	0	Reserved

13.3.18 Register 18 (0x12)

Figure 236. Register 18 (0x12)

7	6	5	4	3	2	1	0
LPA0	LPB1	LPB2	LPB3	RPA0	RPB1	RPB2	RPB3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 176. Register 18 (0x12) Field Descriptions

Bit	Field	Type	Reset	Description
7	LPA0	R/W	0	Left DAC primary a0 zero - Left DAC primary modulator coeff tweaks. 0: normal 1: zero
6	LPB1	R/W	0	Left DAC primary b1 zero 0: normal 1: zero
5	LPB2	R/W	0	Left DAC primary b2 zero 0: normal 1: zero
4	LPB3	R/W	0	Left DAC primary b3 zero 0: normal 1: zero
3	RPA0	R/W	0	Right DAC primary a0 zero - Right DAC primary modulator coeff tweaks 0: normal 1: zero
2	RPB1	R/W	0	Right DAC primary b1 zero 0: normal 1: zero
1	RPB2	R/W	0	Right DAC primary b2 zero 0: normal 1: zero
0	RPB3	R/W	0	Right DAC primary b3 zero 0: normal 1: zero

13.3.19 Register 19 (0x13)

Figure 237. Register 19 (0x13)

7	6	5	4	3	2	1	0
LPG1	Reserved	LPUB	Reserved	RPG1	Reserved	RPUB	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 177. Register 19 (0x13) Field Descriptions

Bit	Field	Type	Reset	Description
7	LPG1	R/W	0	Left DAC primary g1 gain. Left DAC primary local loop gain
6	Reserved	R/W	0	Reserved
5	LPUB	R/W	0	Left DAC primary upper bits. Number of left DAC primary upper bits
4	Reserved	R/W	0	Reserved
3	RPG1	R/W	0	Right DAC primary g1 gain. Right DAC primary local loop gain
2	Reserved	R/W	0	Reserved
1	RPUB	R/W	0	Right DAC primary upper bits. Number of right DAC primary upper bits
0	Reserved	R/W	0	Reserved

13.3.20 Register 20 (0x14)

Figure 238. Register 20 (0x14)

7	6	5	4	3	2	1	0
LSA0	LSB1	LSB2	LSB3	RSA0	RSB1	RSB2	RSB3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 178. Register 20 (0x14) Field Descriptions

Bit	Field	Type	Reset	Description
7	LSA0	R/W	0	Left DAC secondary a0 zero. Left DAC secondary modulator coeff tweaks. 0: normal 1: zero
6	LSB1	R/W	0	Left DAC secondary b1 zero 0: normal 1: zero
5	LSB2	R/W	0	Left DAC secondary b2 zero 0: normal 1: zero
4	LSB3	R/W	0	Left DAC secondary b3 zero 0: normal 1: zero
3	RSA0	R/W	0	Right DAC secondary a0 zero. Right DAC seconday modulator coeff tweaks. 0: normal 1: zero
2	RSB1	R/W	0	Right DAC secondary b1 zero 0: normal 1: zero
1	RSB2	R/W	0	Right DAC secondary b2 zero 0: normal 1: zero
0	RSB3	R/W	0	Right DAC secondary b3 zero 0: normal 1: zero

13.3.21 Register 21 (0x15)

Figure 239. Register 21 (0x15)

7	6	5	4	3	2	1	0
LSG1	Reserved	LSUB	Reserved	RSG1	Reserved	RSUB	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 179. Register 21 (0x15) Field Descriptions

Bit	Field	Type	Reset	Description
7	LSG1	R/W	0	Left DAC secondary g1 gain. Left DAC secondary local loop gain
6	Reserved	R/W	0	Reserved
5	LSUB	R/W	0	Left DAC secondary upper bits. Number of left DAC secondary upper bits
4	Reserved	R/W	0	Reserved
3	RSG1	R/W	0	Right DAC secondary g1 gain. Right DAC secondary local loop gain
2	Reserved	R/W	0	Reserved
1	RSUB	R/W	0	Right DAC secondary upper bits. Number of right DAC secondary upper bits
0	Reserved	R/W	0	Reserved

13.3.22 Register 2 (0x16)

Figure 240. Register 22 (0x16)

7	6	5	4	3	2	1	0
Reserved						CPHY	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 180. Register 22 (0x16) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1-0	CPHY	R/W	1	CP Hysterisis - Hysterisis control of VNEG Detector

13.3.23 Register 23 (0x17)

Figure 241. Register 23 (0x17)

7	6	5	4	3	2	1	0
Reserved						CPHY	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 181. Register 23 (0x17) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1-0	CPHY	R/W	1	CP Hysterisis - Hysterisis control of VNEG Detector

13.3.24 Register 24 (0x18)

Figure 242. Register 24 (0x18)

7	6	5	4	3	2	1	0
Reserved						OT33	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 182. Register 24 (0x18) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W	0	Reserved
2	OT33	R/W	1	Bias current trimming for internal 3.3V oscillator. Bias current 00-111: ?-?uA
1		R/W	0	
0		R/W	0	

13.3.25 Register 25 (0x19)

Figure 243. Register 25 (0x19)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 183. Register 25 (0x19) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.26 Register 26 (0x1A)

Figure 244. Register 26 (0x1A)

7	6	5	4	3	2	1	0
RBTR				RCTR			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 184. Register 26 (0x1A) Field Descriptions

Bit	Field	Type	Reset	Description
7	RBTR	R/W	0	REF BTrim. Trimming of bandgap reference voltage.
6		R/W	1	
5		R/W	0	
4		R/W	0	
3-0	RCTR	R/W	0	REF CTrim. Trimming of common voltage dividing AVDD.

13.3.27 Register 27 (0x1B)

Figure 245. Register 27 (0x1B)

7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 185. Register 27 (0x1B) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.28 Register 28 (0x1C)

Figure 246. Register 28 (0x1C)

7	6	5	4	3	2	1	0
Reserved			PLLR	Reserved		PTST	PVC1
R/W			R/W	R/W		R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 186. Register 28 (0x1C) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	PLLR	R/W	1	PLL $\overline{\text{RST}}$ - Reset counter of all divider. 0: Reset 1: Normal operation
3-2	Reserved	R/W	0	Reserved
1	PTST	R/W	0	PLL IREF TEST. IREF test mode enable/disable. 0: normal 1: test mode
0	PVCI	R/W	0	PLL VCIC. 0: Normal operation 1: Brings higher free-running frequency

13.3.29 Register 29 (0x1D)

Figure 247. Register 29 (0x1D)

7	6	5	4	3	2	1	0
PLL IREF							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 187. Register 29 (0x1D) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL IREF	R/W	0	Reference current control on test-mode. 00000000-11111111: ?? -??A

13.3.30 Register 30 (0x1E)

Figure 248. Register 30 (0x1E)

7	6	5	4	3	2	1	0
Reserved							PLLT
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 188. Register 30 (0x1E) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	PLLT	R/W	0	PLL TEST - Power up/down control for PFD in PLL at test mode. 0: Power up 1: Power down

13.3.31 Register 31 (0x1F)

Figure 249. Register 31 (0x1F)

7	6	5	4	3	2	1	0
Reserved			LSFG	Reserved			LSPD
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 189. Register 31 (0x1F) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	LSFG	R/W	0	LDO_SCPZ - LDO short flag. 0: Short state 1: Not short state
3-1	Reserved	R/W	0	Reserved
0	LSPD	R/W	0	LDO SCPD - LDO power down behavior at short condition. 0: LDO is automatically power down if short state detects 1: Disable

13.3.32 Register 32 (0x20)

Figure 250. Register 32 (0x20)

7	6	5	4	3	2	1	0
Reserved						UTM1	UTM2
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 190. Register 32 (0x20) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1	UTM1	R/W		UVP TEST mode 1 - Change external threshold voltage. 0: VH=0.7xDVDD, VL=0.3xDVDD 1: VH=0.67xDVDD, VL=0.33xDVDD
0	UTM2	R/W	0	UVP TEST mode 2 - Change reference source for internal AVDD detection. 0: Divided LDO_1p8 by resistor 1: Bandgap reference of UVP

13.3.33 Register 33 (0x21)

Figure 251. Register 33 (0x21)

7	6	5	4	3	2	1	0
Reserved				TST1	TST2	TST3	TST4
R/W				R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 191. Register 33 (0x21) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0	Reserved
3	TST1	R/W	0	Analog test mode 1 - Line first stage load ctrl <0> 0: Disable 1: Enable
2	TST2	R/W	0	Analog test mode 2 - Line first stage load ctrl <1>0: Disable 1: Enable
1	TST3	R/W	1	Analog test mode 3 - Line slew rate ctrl <0> 0: Disable 1: Enable
0	TST4	R/W	1	Analog test mode 4 - Line slew rate ctrl <1> 0: Disable 1: Enable

13.3.34 Register 34 (0x22)

Figure 252. Register 34 (0x22)

7	6	5	4	3	2	1	0
Reserved		RFPO	DLPO	LLPO	BLPO	CLPO	OLPO
R/W		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 192. Register 34 (0x22) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	RFPO	R/W	0	REF $\overline{\text{PWRDN}}$ override. Power up/down control for whole bias current. 0: normal 1: override
4	DLPO	R/W	0	Lch DAC $\overline{\text{PWRDN}}$ override. Power up/down control for Lch current DAC. 0: normal 1: override
3	LLPO	R/W	0	Lch Line Driver $\overline{\text{PWRDN}}$ override. Power up/down control for Lch line driver 0: normal 1: override
2	BLPO	R/W	0	Lch Line Bias $\overline{\text{PWRDN}}$ override. Power up/down control for bais block of Lch line driver 0: normal 1: override
1	CLPO	R/W	0	Lch Line CMFB2 $\overline{\text{PWRDN}}$ override. Power up/down control for CMFB of Lch line driver 0: normal 1: override
0	OLPO	R/W	0	Lch Output Stage $\overline{\text{PWRDN}}$ override. Power up/down control for output stage of Lch line driver 0: normal 1: override

13.3.35 Register 35 (0x23)

Figure 253. Register 35 (0x23)

7	6	5	4	3	2	1	0
GLPO	ALPO	ULPO	CPPO	FLPO	SLPO	ILPO	WLPO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 193. Register 35 (0x23) Field Descriptions

Bit	Field	Type	Reset	Description
7	GLPO	R/W	0	Lch Gain control $\overline{\text{PWRDN}}$ override. Power up/down control for Lch gain control 0: normal 1: override
6	ALPO	R/W	0	Lch $\overline{\text{AMUTE}}$ override. Lch Analog Mute control. 0: normal 1: override
5	ULPO	R/W	0	Lch $\overline{\text{AMUTE}}$ dummy override. Lch Analog Mute control. 0: normal 1: override
4	CPPO	R/W	0	CP $\overline{\text{PWRDN}}$ override. Power up/down control for negative charge pump. 0: normal 1: override
3	FLPO	R/W	0	Lch OFSCOMP $\overline{\text{PWRDN}}$ override. Power up/down control for offset calibration block for Lch line driver. 0: normal 1: override
2	SLPO	R/W	0	Lch Short Protection $\overline{\text{PWRDN}}$ override. Power up/down control for short protection of Lch line driver. 0: normal 1: override
1	ILPO	R/W	0	Lch IMP sense $\overline{\text{PWRDN}}$ override. Power up/down control for impedance sensing circuit of Lch line driver. 0: normal 1: override
0	WLPO	R/W	0	Lch IMP whole $\overline{\text{PWRDN}}$ override. Power up/down control for impedance sensing circuit of Lch line driver at whole analog power down. 0: normal 1: override

13.3.36 Register 36 (0x24)

Figure 254. Register 36 (0x24)

7	6	5	4	3	2	1	0
Reserved		RFPS	DLPS	LLPS	BLPS	CLPS	OLPS
R/W		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 194. Register 36 (0x24) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	RFPS	R/W	0	REF $\overline{\text{PWRDN}}$ state. Power up/down control for whole bias current. 0: Power down 1: Power up
4	DLPS	R/W	0	Lch DAC $\overline{\text{PWRDN}}$ state. Power up/down control for Lch current DAC. 0: Power down 1: Power up
3	LLPS	R/W	0	Lch Line Driver $\overline{\text{PWRDN}}$ state. Power up/down control for Lch line driver. 0: Power down 1: Power up
2	BLPS	R/W	0	Lch Line Bias $\overline{\text{PWRDN}}$ state .Power up/down control for bais block of Lch line driver. 0: Power down 1: Power up
1	CLPS	R/W	0	Lch Line CMFB2 $\overline{\text{PWRDN}}$ state. Power up/down control for CMFB of Lch line driver. 0: Power down 1: Power up
0	OLPS	R/W	0	Lch Output Stage $\overline{\text{PWRDN}}$ state. Power up/down control for output stage of Lch line driver. 0: Power down 1: Power up

13.3.37 Register 37 (0x25)

Figure 255. Register 37 (0x25)

7	6	5	4	3	2	1	0
GLPS	ALPS	ULPS	CPPS	FLPS	SLPS	ILPS	WLPS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 195. Register 37 (0x25) Field Descriptions

Bit	Field	Type	Reset	Description
7	GLPS	R/W	0	Lch Gain control $\overline{\text{PWRDN}}$ state. Power up/down control for Lch gain control. 0: Power down 1: Power up
6	ALPS	R/W	0	Lch $\overline{\text{AMUTE}}$ state. Lch Analog Mute control. 0: Power down 1: Power up
5	ULPS	R/W	0	Lch $\overline{\text{AMUTE}}$ dummy state. Lch Analog Mute control. 0: Power down 1: Power up
4	CPPS	R/W	0	CP $\overline{\text{PWRDN}}$ state. Power up/down control for negative charge pump. 0: Power down 1: Power up
3	FLPS	R/W	0	Lch OFSCOMP $\overline{\text{PWRDN}}$ state. Power up/down control for offset calibration block for Lch line driver. 0: Power down 1: Power up
2	SLPS	R/W	0	Lch Short Protection $\overline{\text{PWRDN}}$ state. Power up/down control for short protection of Lch line driver. 0: Power down 1: Power up
1	ILPS	R/W	0	Lch IMP sense $\overline{\text{PWRDN}}$ state. Power up/down control for impedance sensing circuit of Lch line driver. 0: Power down 1: Power up
0	WLPS	R/W	0	Lch IMP whole $\overline{\text{PWRDN}}$ state. Power up/down control for impedance sensing circuit of Lch line driver at whole analog power down. 0: Power down 1: Power up

13.3.38 Register 38 (0x26)

Figure 256. Register 38 (0x26)

7	6	5	4	3	2	1	0
Reserved			DRPO	LRPO	BRPO	CRPO	ORPO
R/W			R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 196. Register 38 (0x26) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	DRPO	R/W	0	Rch DAC $\overline{\text{PWRDN}}$ override. Power up/down control for Rch current DAC. 0: normal 1: override
3	LRPO	R/W	0	Rch Line Driver $\overline{\text{PWRDN}}$ override. Power up/down control for Rch line driver. 0: normal 1: override
2	BRPO	R/W	0	Rch Line Bias $\overline{\text{PWRDN}}$ override. Power up/down control for bais block of Rch line driver. 0: normal 1: override
1	CRPO	R/W	0	Rch Line CMFB2 $\overline{\text{PWRDN}}$ override. Power up/down control for CMFB of Rch line driver. 0: normal 1: override
0	ORPO	R/W	0	Rch Output Stage $\overline{\text{PWRDN}}$ override. Power up/down control for output stage of Rch line driver. 0: normal 1: override

13.3.39 Register 39 (0x27)

Figure 257. Register 39 (0x27)

7	6	5	4	3	2	1	0
GRPO	ARPO	URPO	Reserved	FRPO	SRPO	IRPO	WRPO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 197. Register 39 (0x27) Field Descriptions

Bit	Field	Type	Reset	Description
7	GRPO	R/W	0	Rch Gain control $\overline{\text{PWRDN}}$ override. Power up/down control for Rch gain control. 0: normal 1: override
6	ARPO	R/W	0	Rch $\overline{\text{AMUTE}}$ override. Rch Analog Mute control. 0: normal 1: override
5	URPO	R/W	0	Rch $\overline{\text{AMUTE}}$ dummy override. Rch Analog Mute control. 0: normal 1: override
4	Reserved	R/W	0	Reserved
3	FRPO	R/W	0	Rch OFSCOMP $\overline{\text{PWRDN}}$ override. Power up/down control for offset calibration block for Rch line driver. 0: normal 1: override
2	SRPO	R/W	0	Rch Short Protection $\overline{\text{PWRDN}}$ override. Power up/down control for short protection of Rch line driver. 0: normal 1: override
1	IRPO	R/W	0	Rch IMP sense $\overline{\text{PWRDN}}$ override. Power up/down control for impedance sensing circuit of Rch line driver. 0: normal 1: override
0	WRPO	R/W	0	Rch IMP whole $\overline{\text{PWRDN}}$ override. Power up/down control for Rch impedance sensing circuit of Rch line driver at whole analog power down. 0: normal 1: override

13.3.40 Register 40 (0x28)

Figure 258. Register 40 (0x28)

7	6	5	4	3	2	1	0
Reserved			DRPS	LRPS	BRPS	CRPS	ORPS
R/W			R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 198. Register 40 (0x28) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	DRPS	R/W	0	Rch DAC $\overline{\text{PWRDN}}$ state. Power up/down control for Rch current DAC. 0: Power down 1: Power up
3	LRPS	R/W	0	Rch Line Driver $\overline{\text{PWRDN}}$ state. Power up/down control for Rch line driver. 0: Power down 1: Power up
2	BRPS	R/W	0	Rch Line Bias $\overline{\text{PWRDN}}$ state. Power up/down control for bais block of Rch line driver. 0: Power down 1: Power up
1	CRPS	R/W	0	Rch Line CMFB2 $\overline{\text{PWRDN}}$ state. Power up/down control for CMFB of Rch line driver. 0: Power down 1: Power up
0	ORPS	R/W	0	Rch Output Stage $\overline{\text{PWRDN}}$ state. Power up/down control for output stage of Rch line driver. 0: Power down 1: Power up

13.3.41 Register 41 (0x29)

Figure 259. Register 41 (0x29)

7	6	5	4	3	2	1	0
GRPS	ARPS	URPS	Reserved	FRPS	SRPS	IRPS	WRPS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 199. Register 41 (0x29) Field Descriptions

Bit	Field	Type	Reset	Description
7	GRPS	R/W	0	Rch Gain control $\overline{\text{PWRDN}}$ state. Power up/down control for Rch gain control. 0: Power down 1: Power up
6	ARPS	R/W	0	Rch $\overline{\text{AMUTE}}$ state. Rch Analog Mute control. 0: Power down 1: Power up
5	URPS	R/W	0	Rch $\overline{\text{AMUTE}}$ dummy state. Rch Analog Mute control. 0: Power down 1: Power up
4	Reserved	R/W	0	Reserved
3	FRPS	R/W	0	Rch OFSCOMP $\overline{\text{PWRDN}}$ state. Power up/down control for offset calibration block for Rch line driver. 0: Power down 1: Power up
2	SRPS	R/W	0	Rch Short Protection $\overline{\text{PWRDN}}$ state. Power up/down control for short protection of Rch line driver. 0: Power down 1: Power up
1	IRPS	R/W	0	Rch IMP sense $\overline{\text{PWRDN}}$ state. Power up/down control for impedance sensing circuit of Rch line driver. 0: Power down 1: Power up
0	WRPS	R/W	0	Rch IMP whole $\overline{\text{PWRDN}}$ state. Power up/down control for Rch impedance sensing circuit of Rch line driver at whole analog power down. 0: Power down 1: Power up

13.3.42 Register 42 (0x2A)

Figure 260. Register 42 (0x2A)

7	6	5	4	3	2	1	0
Reserved			CMEN	Reserved			CMSL
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 200. Register 42 (0x2A) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	CMEN	R/W	0	CP operation mode control enable. Enable/Disable for charge pump mode select. 0: Disable 1: Enable
3-1	Reserved	R/W	0	Reserved
0	CMSL	R/W	1	CP operation mode select. Charge pump mode select by register. 0: Normal operation 1: Constant current mode

13.3.43 Register 43 (0x2B)

Figure 261. Register 43 (0x2B)

7	6	5	4	3	2	1	0
Reserved			CHDP	Reserved		CHI4	HDEN
R/W			R/W	R/W		R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 201. Register 43 (0x2B) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	CHDP	R/W	1	CHD power up/down control. Power up/down control for clock halt detector. 0: Power down 1: Power up
3-2	Reserved	R/W	0	Reserved
1	CHI4	R/W	0	CHD current control override. x4 current control for clock halt detector. 0: Normal operation 1: x4 current operation
0	HDEN	R/W	0	CHD detector enable/disable control. Enable/disable control for clock halt detector. At 'disable', output shows "1". 0: Enable 1: Disable

13.3.44 Register 44 (0x2C)

Figure 262. Register 44 (0x2C)

7	6	5	4	3	2	1	0
Reserved							LBPD
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 202. Register 44 (0x2C) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	LBPD	R/W	0	LDO bandgap power up/down control. LDO bandgap power/up down control on Test mode. 0: Power down 1: Power up

13.3.45 Register 63 (0x3F)

Figure 263. Register 63 (0x3F)

7	6	5	4	3	2	1	0
PWD1							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 203. Register 63 (0x3F) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWD1	R/W	0	Password1 First word of password. Both words of password must be correctly set in order to unlock test registers. When locked, writing to test registers are inhibited and reading them will return 0.

13.3.46 Register 64 (0x40)

Figure 264. Register 64 (0x40)

7	6	5	4	3	2	1	0
PWD2							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 204. Register 64 (0x40) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWD2	R/W	0	Password2 First word of password. Both words of password must be correctly set in order to unlock test registers. When locked, writing to test registers are inhibited and reading them will return 0.

13.3.47 Register 65 (0x41)

Figure 265. Register 65 (0x41)

7	6	5	4	3	1	0
Reserved					TSEL	
R/W					R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 205. Register 65 (0x41) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0	Reserved
3-0	TSEL	R/W	0	Test Mode Selection (No longer need) 0: Normal 1:SCAN 2:IDDQ 3:VOH 4:VOL 5: VIL 6:VIH 7:HI-Z

13.3.48 Register 70 (0x46)

Figure 266. Register 70 (0x46)

7	6	5	4	3	1	0
Left Channel DIFF Manual Offset (Q5.2)						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 206. Register 70 (0x46) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Left Channel DIFF Manual Offset (Q5.2)	R/W	0	Add manual offset to the left channel DIFF offset compensator. Observed offset delta: 0111111 : -15.75 mV 0111110 : -15.50 mV 0111101 : -15.25 mV … 0000001 : -0.25 mV 0000000 : 0.0 mV 1111111 : 0.25 mV … 1000010 : 15.50 mV 1000001 : 15.75 mV 1000000 : 16.0 mV

13.3.49 Register 71 (0x47)

Figure 267. Register 71 (0x47)

7	6	5	4	3	1	0
Left Channel CMFB Manual Offset (Q6.2)						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 207. Register 71 (0x47) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Left Channel CMFB Manual Offset (Q6.2)	R/W	0	Add manual offset to the left channel CMFB offset compensator. Observed offset delta: 0111111 : -31.75 mV 0111110 : -31.50 mV 0111101 : -31.25 mV … 0000001 : -0.25 mV 0000000 : 0.0 mV 1111111 : 0.25 mV … 1000010 : 31.50 mV 1000001 : 31.75 mV 1000000 : 32.0 mV

13.3.50 Register 72 (0x48)

Figure 268. Register 72 (0x48)

7	6	5	4	3	1	0
Right Channel DIFF Manual Offset (Q5.2)						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 208. Register 72 (0x48) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Right Channel DIFF Manual Offset (Q5.2)	R/W	0	Add manual offset to the right channel DIFF offset compensator. Observed offset delta: 0111111 : -15.75 mV 0111110 : -15.50 mV 0111101 : -15.25 mV … 0000001 : -0.25 mV 0000000 : 0.0 mV 1111111 : 0.25 mV … 1000010 : 15.50 mV 1000001 : 15.75 mV 1000000 : 16.0 mV

13.3.51 Register 73 (0x49)

Figure 269. Register 73 (0x49)

7	6	5	4	3	1	0
Right Channel CMFB Manual Offset (Q6.2)						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 209. Register 73 (0x49) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Right Channel CMFB Manual Offset (Q6.2)	R/W	0	Add manual offset to the right channel CMFB offset compensator. Observed offset delta: 0111111 : -31.75 mV 0111110 : -31.50 mV 0111101 : -31.25 mV … 0000001 : -0.25 mV 0000000 : 0.0 mV 1111111 : 0.25 mV … 1000010 : 31.50 mV 1000001 : 31.75 mV 1000000 : 32.0 mV

13.3.52 Register 74 (0x4A)

Figure 270. Register 74 (0x4A)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 210. Register 74 (0x4A) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.53 Register 75 (0x4B)

Figure 271. Register 75 (0x4B)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 211. Register 75 (0x4B) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.54 Register 76 (0x4C)

Figure 272. Register 76 (0x4C)

7	6	5	4	3	1	0
Reserved						Left Channel DIFF Monitor(8)
R/W						R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 212. Register 76 (0x4C) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	Left Channel DIFF Monitor(8)	R		This register shows the approximation of original / compensated left channel DIFF offset. Observed offset delta: 0111111 : 63.75 mV 0111110 : 63.50 mV 0111101 : 63.25 mV … 0000001 : 0.25 mV 0000000 : 0.0 mV 1111111 : -0.25 mV … 1000010 : -63.50 mV 1000001 : -63.75 mV 1000000 : -64.0 mV

13.3.55 Register 77 (0x4D)

Figure 273. Register 77 (0x4D)

7	6	5	4	3	1	0
Left Channel DIFF Monitor(7:0)						
R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 213. Register 77 (0x4D) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Left Channel DIFF Monitor(7:0)	R		This register shows the approximation of original / compensated left channel DIFF offset. Observed offset delta: 0111111 : 63.75 mV 0111110 : 63.50 mV 0111101 : 63.25 mV … 0000001 : 0.25 mV 0000000 : 0.0 mV 1111111 : -0.25 mV … 1000010 : -63.50 mV 1000001 : -63.75 mV 1000000 : -64.0 mV

13.3.56 Register 78 (0x4E)

Figure 274. Register 78 (0x4E)

7	6	5	4	3	1	0
Reserved				I048		
R/W				RW		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 214. Register 78 (0x4E) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4-0	I048	R/W	0	FS Det 48 kHz Min Range . Minimum OSC count in LRCLK for 48 kHz detection. Decimal Value 863.

13.3.57 Register 79 (0x4F)

Figure 275. Register 79 (0x4F)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 215. Register 79 (0x4F) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.58 Register 80 (0x50)

Figure 276. Register 80 (0x50)

7	6	5	4	3	1	0
Reserved				X048		
R/W				RW		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 216. Register 80 (0x50) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4-0	X048	R/W	0	FS Det 48 kHz Max Range. Minimum OSC count in LRCLK for 48 kHz detection. Decimal Value 2479.

13.3.59 Register 81 (0x51)

Figure 277. Register 81 (0x51)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 217. Register 81 (0x51) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.60 Register 82 (0x52)

Figure 278. Register 82 (0x52)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 218. Register 82 (0x52) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.61 Register 83 (0x53)

Figure 279. Register 83 (0x53)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 219. Register 83 (0x53) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.62 Register 84 (0x54)

Figure 280. Register 84 (0x54)

7	6	5	4	3	1	0
Reserved						Left Channel CMFB Monitor (8)
R/W						R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 220. Register 84 (0x54) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	Left Channel CMFB Monitor(8)	R		This register shows the approximation of original / compensated left channel CMFB offset. Observed offset delta: 0111111 : 63.75 mV 0111110 : 63.50 mV 0111101 : 63.25 mV … 0000001 : 0.25 mV 0000000 : 0.0 mV 1111111 : -0.25 mV … 1000010 : -63.50 mV 1000001 : -63.75 mV 1000000 : -64.0 mV

13.3.63 Register 85 (0x55)

Figure 281. Register 85 (0x55)

7	6	5	4	3	1	0
Left Channel CMFB Monitor (7:0)						
R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 221. Register 85 (0x55) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Left Channel CMFB Monitor (7:0)	R		This register shows the approximation of original / compensated left channel CMFB offset. Observed offset delta: 0111111 : 63.75 mV 0111110 : 63.50 mV 0111101 : 63.25 mV … 0000001 : 0.25 mV 0000000 : 0.0 mV 1111111 : –0.25 mV … 1000010 : –63.50 mV 1000001 : –63.75 mV 1000000 : –64.0 mV

13.3.64 Register 86 (0x56)

Figure 282. Register 86 (0x56)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 222. Register 86 (0x56) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.65 Register 87 (0x57)

Figure 283. Register 87 (0x57)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 223. Register 87 (0x57) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.66 Register 88 (0x58)

Figure 284. Register 88 (0x58)

7	6	5	4	3	1	0
Reserved						Right Channel DIFF Monitor (8)
R/W						R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 224. Register 88 (0x58) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	Right Channel DIFF Monitor (8)	R		This register shows the approximation of original / compensated right channel DIFF offset. Observed offset delta: 0111111 : 63.75 mV 0111110 : 63.50 mV 0111101 : 63.25 mV … 0000001 : 0.25 mV 0000000 : 0.0 mV 1111111 : -0.25 mV … 1000010 : -63.50 mV 1000001 : -63.75 mV 1000000 : -64.0 mV

13.3.67 Register 89 (0x59)

Figure 285. Register 89 (0x59)

7	6	5	4	3	1	0
Right Channel DIFF Monitor (7:0)						
R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 225. Register 89 (0x59) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Right Channel DIFF Monitor (7:0)	R		This register shows the approximation of original / compensated right channel DIFF offset. Observed offset delta: 0111111 : 63.75 mV 0111110 : 63.50 mV 0111101 : 63.25 mV … 0000001 : 0.25 mV 0000000 : 0.0 mV 1111111 : -0.25 mV … 1000010 : -63.50 mV 1000001 : -63.75 mV 1000000 : -64.0 mV

13.3.68 Register 90 (0x5A)

Figure 286. Register 90 (0x5A)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 226. Register 90 (0x5A) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.69 Register 91 (0x5B)

Figure 287. Register 91 (0x5B)

7	6	5	4	3	1	0
Reserved						
R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 227. Register 91 (0x5B) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R/W	0	Reserved

13.3.70 Register 92 (0x5C)

Figure 288. Register 92 (0x5C)

7	6	5	4	3	1	0
Reserved						Right Channel CMFB Monitor (8)
R/W						R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 228. Register 92 (0x5C) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	Right Channel CMFB Monitor(8)	R		This register shows the approximation of original / compensated right channel CMFB offset. Observed offset delta: 0111111 : 63.75 mV 0111110 : 63.50 mV 0111101 : 63.25 mV … 0000001 : 0.25 mV 0000000 : 0.0 mV 1111111 : –0.25 mV … 1000010 : –63.50 mV 1000001 : –63.75 mV 1000000 : –64.0 mV

13.3.71 Register 93 (0x5D)

Figure 289. Register 93 (0x5D)

7	6	5	4	3	1	0
Right Channel CMFB Monito r(7:0)						
R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 229. Register 93 (0x5D) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Right Channel CMFB Monitor (7:0)	R		This register shows the approximation of original / compensated right channel CMFB offset. Observed offset delta: 0111111 : 63.75 mV 0111110 : 63.50 mV 0111101 : 63.25 mV … 0000001 : 0.25 mV 0000000 : 0.0 mV 1111111 : –0.25 mV … 1000010 : –63.50 mV 1000001 : –63.75 mV 1000000 : –64.0 mV

13.4 DSP Memory Map

Table 230. Memory Map — Book 0x78 (120)(1)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
LEVEL METER					
0x54	0x0C	Level Meter Left Output	4 / 1.31	0x000000--	Level Meter Left Output
0x58	0x0C	Level Meter Right Output	4 / 1.31	0x000000--	Level Meter Right Output
SECONDARY EQ LEFT 12 BQS					
0x08	0x15	CH-L BQ 1 B0	4 / 5.27	0x7FFFFFFF	Left BQ coefficient
0x0C	0x15	CH-L BQ 1 B1	4 / 6.26	0x00000000	Left BQ coefficient
0x10	0x15	CH-L BQ 1 B2	4 / 5.27	0x00000000	Left BQ coefficient
0x14	0x15	CH-L BQ 1 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x18	0x15	CH-L BQ 1 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x1C	0x15	CH-L BQ 2 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x20	0x15	CH-L BQ 2 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x24	0x15	CH-L BQ 2 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x28	0x15	CH-L BQ 2 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x2C	0x15	CH-L BQ 2 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x30	0x15	CH-L BQ 3 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x34	0x15	CH-L BQ 3 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x38	0x15	CH-L BQ 3 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x3C	0x15	CH-L BQ 3 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x40	0x15	CH-L BQ 3 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x44	0x15	CH-L BQ 4 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x48	0x15	CH-L BQ 4 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x4C	0x15	CH-L BQ 4 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x50	0x15	CH-L BQ 4 A1	4 / 2.30	0x00000000	Left BQ coefficient

(1) The registers in this table do not require the swap flag to work

DSP Memory Map (continued)

Table 230. Memory Map — Book 0x78 (120)[1] (continued)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
0x54	0x15	CH-L BQ 4 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x58	0x15	CH-L BQ 5 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x5C	0x15	CH-L BQ 5 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x60	0x15	CH-L BQ 5 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x64	0x15	CH-L BQ 5 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x68	0x15	CH-L BQ 5 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x6C	0x15	CH-L BQ 6 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x70	0x15	CH-L BQ 6 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x74	0x15	CH-L BQ 6 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x78	0x15	CH-L BQ 6 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x7C	0x15	CH-L BQ 6 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x08	0x16	CH-L BQ 7 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x0C	0x16	CH-L BQ 7 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x10	0x16	CH-L BQ 7 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x14	0x16	CH-L BQ 7 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x18	0x16	CH-L BQ 7 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x1C	0x16	CH-L BQ 8 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x20	0x16	CH-L BQ 8 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x24	0x16	CH-L BQ 8 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x28	0x16	CH-L BQ 8 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x2C	0x16	CH-L BQ 8 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x30	0x16	CH-L BQ 9 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x34	0x16	CH-L BQ 9 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x38	0x16	CH-L BQ 9 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x3C	0x16	CH-L BQ 9 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x40	0x16	CH-L BQ 9 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x44	0x16	CH-L BQ 10 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x48	0x16	CH-L BQ 10 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x4C	0x16	CH-L BQ 10 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x50	0x16	CH-L BQ 10 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x54	0x16	CH-L BQ 10 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x58	0x16	CH-L BQ 11 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x5C	0x16	CH-L BQ 11 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x60	0x16	CH-L BQ 11 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x64	0x16	CH-L BQ 11 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x68	0x16	CH-L BQ 11 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x6C	0x16	CH-L BQ 12 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x70	0x16	CH-L BQ 12 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x74	0x16	CH-L BQ 12 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x78	0x16	CH-L BQ 12 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x7C	0x16	CH-L BQ 12 A2	4 / 1.31	0x00000000	Left BQ coefficient
SECONDARY EQ RIGHT 12 BQS					
0x08	0x17	CH-R BQ 1 B0	4 / 5.27	0x7FFFFFFF	Right BQ coefficient
0x0C	0x17	CH-R BQ 1 B1	4 / 6.26	0x00000000	Right BQ coefficient
0x10	0x17	CH-R BQ 1 B2	4 / 5.27	0x00000000	Right BQ coefficient

DSP Memory Map (continued)

Table 230. Memory Map — Book 0x78 (120)[1] (continued)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
0x14	0x17	CH-R BQ 1 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x18	0x17	CH-R BQ 1 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x1C	0x17	CH-R BQ 2 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x20	0x17	CH-R BQ 2 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x24	0x17	CH-R BQ 2 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x28	0x17	CH-R BQ 2 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x2C	0x17	CH-R BQ 2 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x30	0x17	CH-R BQ 3 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x34	0x17	CH-R BQ 3 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x38	0x17	CH-R BQ 3 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x3C	0x17	CH-R BQ 3 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x40	0x17	CH-R BQ 3 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x44	0x17	CH-R BQ 4 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x48	0x17	CH-R BQ 4 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x4C	0x17	CH-R BQ 4 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x50	0x17	CH-R BQ 4 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x54	0x17	CH-R BQ 4 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x58	0x17	CH-R BQ 5 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x5C	0x17	CH-R BQ 5 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x60	0x17	CH-R BQ 5 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x64	0x17	CH-R BQ 5 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x68	0x17	CH-R BQ 5 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x6C	0x17	CH-R BQ 6 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x70	0x17	CH-R BQ 6 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x74	0x17	CH-R BQ 6 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x78	0x17	CH-R BQ 6 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x7C	0x17	CH-R BQ 6 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x08	0x18	CH-R BQ 7 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x0C	0x18	CH-R BQ 7 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x10	0x18	CH-R BQ 7 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x14	0x18	CH-R BQ 7 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x18	0x18	CH-R BQ 7 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x1C	0x18	CH-R BQ 8 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x20	0x18	CH-R BQ 8 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x24	0x18	CH-R BQ 8 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x28	0x18	CH-R BQ 8 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x2C	0x18	CH-R BQ 8 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x30	0x18	CH-R BQ 9 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x34	0x18	CH-R BQ 9 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x38	0x18	CH-R BQ 9 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x3C	0x18	CH-R BQ 9 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x40	0x18	CH-R BQ 9 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x44	0x18	CH-R BQ 10 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x48	0x18	CH-R BQ 10 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x4C	0x18	CH-R BQ 10 B2	4 / 1.31	0x00000000	Right BQ coefficient

DSP Memory Map (continued)

Table 230. Memory Map — Book 0x78 (120)[1] (continued)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
0x50	0x18	CH-R BQ 10 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x54	0x18	CH-R BQ 10 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x58	0x18	CH-R BQ 11 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x5C	0x18	CH-R BQ 11 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x60	0x18	CH-R BQ 11 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x64	0x18	CH-R BQ 11 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x68	0x18	CH-R BQ 11 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x6C	0x18	CH-R BQ 12 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x70	0x18	CH-R BQ 12 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x74	0x18	CH-R BQ 12 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x78	0x18	CH-R BQ 12 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x7C	0x18	CH-R BQ 12 A2	4 / 1.31	0x00000000	Right BQ coefficient
SECONDARY BQ GAIN SCALE AND VOLUME					
0x08	0x19	Left Gain	4 / 8.24		Gain
0x0C	0x19	Right Gain	4 / 8.24		Gain
BANK SWITCH					
0x08	0x14	Left Gain	4 / 32.0	0x00000000	Needs swap flag to run -

Table 231. Memory Map — Book 0x8C (140)[1]

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
DSP MEMORY UPDATE					
0x10	0x01	DSP Memory Swap Flag	4 / 32.0	0x00000000	DSP Memory Swap Flag
MAIN EQ LEFT 12 BQS					
0x58	0x1B	CH-L BQ 1 B0	4 / 5.27	0x7FFFFFFF	Left BQ coefficient
0x5C	0x1B	CH-L BQ 1 B1	4 / 6.26	0x00000000	Left BQ coefficient
0x60	0x1B	CH-L BQ 1 B2	4 / 5.27	0x00000000	Left BQ coefficient
0x64	0x1B	CH-L BQ 1 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x68	0x1B	CH-L BQ 1 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x6C	0x1B	CH-L BQ 2 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x70	0x1B	CH-L BQ 2 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x74	0x1B	CH-L BQ 2 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x78	0x1B	CH-L BQ 2 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x7C	0x1B	CH-L BQ 2 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x08	0x1C	CH-L BQ 3 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x0C	0x1C	CH-L BQ 3 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x10	0x1C	CH-L BQ 3 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x14	0x1C	CH-L BQ 3 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x18	0x1C	CH-L BQ 3 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x1C	0x1C	CH-L BQ 4 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x20	0x1C	CH-L BQ 4 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x24	0x1C	CH-L BQ 4 B2	4 / 1.31	0x00000000	Left BQ coefficient

(1) Will be set to default anytime a DSP reset, CP error or device standby occurs. Clock errors and frequency changes cause DSP reset. The clocks should be stable when using these mux in non-default state. Always poll muxes status and set muxes prior to use in application. TI recommends that these muxes are repeatedly polled and refreshed during application in the event a DSP reset occurred that cleared the muxes.

Table 231. Memory Map — Book 0x8C (140)[1] (continued)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
0x28	0x1C	CH-L BQ 4 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x2C	0x1C	CH-L BQ 4 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x30	0x1C	CH-L BQ 5 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x34	0x1C	CH-L BQ 5 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x38	0x1C	CH-L BQ 5 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x3C	0x1C	CH-L BQ 5 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x40	0x1C	CH-L BQ 5 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x44	0x1C	CH-L BQ 6 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x48	0x1C	CH-L BQ 6 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x4C	0x1C	CH-L BQ 6 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x50	0x1C	CH-L BQ 6 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x54	0x1C	CH-L BQ 6 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x58	0x1C	CH-L BQ 7 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x5C	0x1C	CH-L BQ 7 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x60	0x1C	CH-L BQ 7 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x64	0x1C	CH-L BQ 7 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x68	0x1C	CH-L BQ 7 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x6C	0x1C	CH-L BQ 8 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x70	0x1C	CH-L BQ 8 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x74	0x1C	CH-L BQ 8 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x78	0x1C	CH-L BQ 8 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x7C	0x1C	CH-L BQ 8 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x08	0x1D	CH-L BQ 9 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x0C	0x1D	CH-L BQ 9 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x10	0x1D	CH-L BQ 9 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x14	0x1D	CH-L BQ 9 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x18	0x1D	CH-L BQ 9 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x1C	0x1D	CH-L BQ 10 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x20	0x1D	CH-L BQ 10 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x24	0x1D	CH-L BQ 10 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x28	0x1D	CH-L BQ 10 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x2C	0x1D	CH-L BQ 10 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x30	0x1D	CH-L BQ 11 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x34	0x1D	CH-L BQ 11 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x38	0x1D	CH-L BQ 11 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x3C	0x1D	CH-L BQ 11 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x40	0x1D	CH-L BQ 11 A2	4 / 1.31	0x00000000	Left BQ coefficient
0x44	0x1D	CH-L BQ 12 B0	4 / 1.31	0x7FFFFFFF	Left BQ coefficient
0x48	0x1D	CH-L BQ 12 B1	4 / 2.30	0x00000000	Left BQ coefficient
0x4C	0x1D	CH-L BQ 12 B2	4 / 1.31	0x00000000	Left BQ coefficient
0x50	0x1D	CH-L BQ 12 A1	4 / 2.30	0x00000000	Left BQ coefficient
0x54	0x1D	CH-L BQ 12 A2	4 / 1.31	0x00000000	Left BQ coefficient
MAIN EQ RIGHT 12 BQS					
0x58	0x1D	CH-R BQ 1 B0	4 / 5.27	0x7FFFFFFF	Right BQ coefficient
0x5C	0x1D	CH-R BQ 1 B1	4 / 6.26	0x00000000	Right BQ coefficient
0x60	0x1D	CH-R BQ 1 B2	4 / 5.27	0x00000000	Right BQ coefficient
0x64	0x1D	CH-R BQ 1 A1	4 / 2.30	0x00000000	Right BQ coefficient

Table 231. Memory Map — Book 0x8C (140)[1] (continued)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
0x68	0x1D	CH-R BQ 1 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x6C	0x1D	CH-R BQ 2 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x70	0x1D	CH-R BQ 2 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x74	0x1D	CH-R BQ 2 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x78	0x1D	CH-R BQ 2 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x7C	0x1D	CH-R BQ 2 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x08	0x1E	CH-R BQ 3 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x8C	0x1E	CH-R BQ 3 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x10	0x1E	CH-R BQ 3 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x14	0x1E	CH-R BQ 3 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x18	0x1E	CH-R BQ 3 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x1C	0x1E	CH-R BQ 4 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x20	0x1E	CH-R BQ 4 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x24	0x1E	CH-R BQ 4 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x28	0x1E	CH-R BQ 4 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x2C	0x1E	CH-R BQ 4 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x30	0x1E	CH-R BQ 5 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x34	0x1E	CH-R BQ 5 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x38	0x1E	CH-R BQ 5 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x3C	0x1E	CH-R BQ 5 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x40	0x1E	CH-R BQ 5 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x44	0x1E	CH-R BQ 6 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x48	0x1E	CH-R BQ 6 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x4C	0x1E	CH-R BQ 6 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x50	0x1E	CH-R BQ 6 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x54	0x1E	CH-R BQ 6 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x58	0x1E	CH-R BQ 7 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x5C	0x1E	CH-R BQ 7 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x60	0x1E	CH-R BQ 7 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x64	0x1E	CH-R BQ 7 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x68	0x1E	CH-R BQ 7 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x6C	0x1E	CH-R BQ 8 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x70	0x1E	CH-R BQ 8 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x74	0x1E	CH-R BQ 8 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x78	0x1E	CH-R BQ 8 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x7C	0x1E	CH-R BQ 8 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x08	0x1F	CH-R BQ 9 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x0C	0x1F	CH-R BQ 9 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x10	0x1F	CH-R BQ 9 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x14	0x1F	CH-R BQ 9 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x18	0x1F	CH-R BQ 9 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x1C	0x1F	CH-R BQ 10 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x20	0x1F	CH-R BQ 10 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x24	0x1F	CH-R BQ 10 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x28	0x1F	CH-R BQ 10 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x2C	0x1F	CH-R BQ 10 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x30	0x1F	CH-R BQ 11 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient

Table 231. Memory Map — Book 0x8C (140)[1] (continued)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
0x34	0x1F	CH-R BQ 11 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x38	0x1F	CH-R BQ 11 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x3C	0x1F	CH-R BQ 11 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x40	0x1F	CH-R BQ 11 A2	4 / 1.31	0x00000000	Right BQ coefficient
0x44	0x1F	CH-R BQ 12 B0	4 / 1.31	0x7FFFFFFF	Right BQ coefficient
0x48	0x1F	CH-R BQ 12 B1	4 / 2.30	0x00000000	Right BQ coefficient
0x4C	0x1F	CH-R BQ 12 B2	4 / 1.31	0x00000000	Right BQ coefficient
0x50	0x1F	CH-R BQ 12 A1	4 / 2.30	0x00000000	Right BQ coefficient
0x54	0x1F	CH-R BQ 12 A2	4 / 1.31	0x00000000	Right BQ coefficient
MAIN BQ GAIN SCALE AND VOLUME					
0x58	0x1F	Left Gain	4 / 8.24	0x01000000	Gain
0x5C	0x1F	Right Gain	4 / 8.24	0x01000000	Gain
DPEQ SENSE BQ					
0x6C	0x1F	BQ B0	4 / 1.31	0x7FFFFFFF	DPEQ sense BQ coefficient
0x70	0x1F	BQ B1	4 / 1.31	0x00000000	DPEQ sense BQ coefficient
0x74	0x1F	BQ B2	4 / 1.31	0x00000000	DPEQ sense BQ coefficient
0x78	0x1F	BQ A1	4 / 1.31	0x00000000	DPEQ sense BQ coefficient
0x7C	0x1F	BQ A2	4 / 1.31	0x00000000	DPEQ sense BQ coefficient
DPEQ HIGH LEVEL PATH BQ					
0x08	0x20	BQ B0	4 / 1.31	0x7FFFFFFF	DPEQ high BQ coefficient
0x0C	0x20	BQ B1	4 / 1.31	0x00000000	DPEQ high BQ coefficient
0x10	0x20	BQ B2	4 / 1.31	0x00000000	DPEQ high BQ coefficient
0x14	0x20	BQ A1	4 / 1.31	0x00000000	DPEQ high BQ coefficient
0x18	0x20	BQ A2	4 / 1.31	0x00000000	DPEQ high BQ coefficient
DPEQ LOW LEVEL PATH BQ					
0x1C	0x20	BQ B0	4 / 1.31	0x7FFFFFFF	DPEQ low BQ coefficient
0x20	0x20	BQ B1	4 / 1.31	0x00000000	DPEQ low BQ coefficient
0x24	0x20	BQ B2	4 / 1.31	0x00000000	DPEQ low BQ coefficient
0x28	0x20	BQ A1	4 / 1.31	0x00000000	DPEQ low BQ coefficient
0x2C	0x20	BQ A2	4 / 1.31	0x00000000	DPEQ low BQ coefficient
DRC 1 BQ					
0x30	0x20	BQ B0	4 / 1.31	0x9D8E8900	DRC 1 BQ coefficient
0x34	0x20	BQ B1	4 / 1.31	0x007BFC00	DRC 1 BQ coefficient
0x38	0x20	BQ B2	4 / 1.31	0x007BFC00	DRC 1 BQ coefficient
0x3C	0x20	BQ A1	4 / 1.31	0x7040C300	DRC 1 BQ coefficient
0x40	0x20	BQ A2	4 / 1.31	0x9D8E8900	DRC 1 BQ coefficient

Table 231. Memory Map — Book 0x8C (140)[1] (continued)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
DRC 2 BQ					
0x44	0x20	BQ B0	4 / 1.31	0x70BCBF00	DRC 2 BQ coefficient
0x48	0x20	BQ B1	4 / 1.31	0x007BFC00	DRC 2 BQ coefficient
0x4C	0x20	BQ B2	4 / 1.31	0x007BFC00	DRC 2 BQ coefficient
0x50	0x20	BQ A1	4 / 1.31	0x7040C300	DRC 2 BQ coefficient
0x54	0x20	BQ A2	4 / 1.31	0x9D8E8900	DRC 2 BQ coefficient
DPEQ CONTROL					
0x58	0x20	Alpha	4 / 1.31	0x02DEAD00	DPEQ Sense Energy Time constant
0x5C	0x20	Gain	4 / 1.31	0x74013901	DPEQ Threshold Gain
0x60	0x20	Offset	4 / 1.31	0x0020C49B	DPEQ Threshold Offset
LEVER METER					
0x64	0x20	Level Meter Alpha	4 / 1.31	0x00A7264A	Level meter Energy Time constant
DRC SUM					
0x68	0x20	DRC 1 sum	4 / 1.31	0x7FFFFFFF	DRC1 Mixer Gain
0x6C	0x20	DRC 2 sum	4 / 1.31	0x00000000	DRC2 Mixer Gain
DRC 1					
0x70	0x20	DRC1 Energy	4 / 1.31	0x7FFFFFFF	DRC1 Energy Time constant
0x74	0x20	DRC1 Attack	4 / 1.31	0x7FFFFFFF	DRC1 Attack Time constant
0x78	0x20	DRC1 Decay	4 / 1.31	0x7FFFFFFF	DRC1 Decay Time constant
0x7C	0x20	K0_1	4 / 9.23	0x00000000	DRC1 Region 1 Slope (comp/Exp)
0x08	0x21	K1_1	4 / 9.23	0x00000000	DRC1 Region 2 Slope (comp/Exp)
0x0C	0x21	K2_1	4 / 9.23	0x00000000	DRC1 Region 3 Slope (comp/Exp)
0x10	0x21	T1_1	4 / 9.23	0xE7000000	DRC1 Threshold 1
0x14	0x21	T2_1	4 / 9.23	0xFE800000	DRC1 Threshold 2
0x18	0x21	Offset 1	4 / 9.23	0x00000000	DRC1 Offset 1
0x1C	0x21	Offset 2	4 / 9.23	0x00000000	DRC1 Offset 2
DRC 2					
0x20	0x21	DRC2 Energy	4 / 1.31	0x7FFFFFFF	DRC2 Energy Time constant
0x24	0x21	DRC2 Attack	4 / 1.31	0x7FFFFFFF	DRC2 Attack Time constant
0x28	0x21	DRC2 Decay	4 / 1.31	0x7FFFFFFF	DRC2 Decay Time constant
0x2C	0x21	K0_1	4 / 9.23	0x00000000	DRC2 Region 1 Slope (comp/Exp)
0x30	0x21	K1_1	4 / 9.23	0x00000000	DRC2 Region 2 Slope (comp/Exp)
0x34	0x21	K2_1	4 / 9.23	0x00000000	DRC2 Region 3 Slope (comp/Exp)
0x38	0x21	T1_1	4 / 9.23	0xE7000000	DRC2 Threshold 1
0x3C	0x21	T2_1	4 / 9.23	0xFE800000	DRC2 Threshold 2
0x40	0x21	Offset 1	4 / 9.23	0x00000000	DRC2 Offset 1
0x44	0x21	Offset 2	4 / 9.23	0x00000000	DRC2 Offset 2

Table 231. Memory Map — Book 0x8C (140)(1) (continued)

SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES / FORMAT	DEFAULT VALUE	DESCRIPTION
FINE VOLUME OUTPUT					
0x48	0x21	Fine volume left	4 / 2.30	0x3FFFFFFF	Left Channel Fine Volume Gain
0x4C	0x21	Fine volume right	4 / 2.30	0x3FFFFFFF	Right Channel Fine Volume Gain
INPUT MIXER					
0x50	0x21	Left in to left out	4 / 9.23	0x00800000	Left Channel Mixer Left Input Gain
0x54	0x21	Right in to left out	4 / 9.23	0x00000000	Left Channel Mixer Right Input Gain
0x58	0x21	Left in to right out	4 / 9.23	0x00000000	Right Channel Mixer Left Input Gain
0x5C	0x21	Right in to right out	4 / 9.23	0x00800000	Right Channel Mixer Right Input Gain
DPEQ GAIN SCALE					
0x60	0x21	DPEQ sense scale	4 / 6.26	0x40000000	DPEQ Sense Input Gain Scale
BYPASS EQ MUX					
0x64	0x21		4 / 32.0	0x00000000	
GANG LEFT / RIGHT EQ					
0x68	0x21		4 / 32.0	0x00000000	
BYPASS WORKLOAD TO SDOUT					
0x6C	0x21		4 /32.0	0x00000000	
BYPASS TO LEVEL METER BIT					
0x70	0x21		4 / 32.0	0x00000000	
THD BOOST					
0x74	0x21		4 / 9.23	0x00400000	
AGL					
0x78	0x21	Attack Threshold	4 / 5.27	0x40000000	Threshold linear
0x7C	0x21	Softening Filter Alpha	4 / 1.31	0x06153BD1	AGL Alpha Time constant
0x08	0x22	Attack Rate	4 / 1.31	0x0001B4E8	AGL Attack Time constant
0x0C	0x22	AGL Enable	4 / 1.31	0x40000000	AGL Enable Mux
0x10	0x22	Chomp	4 / 1.31	0x0020C49C	
0x14	0x22	Softening Filter Omega	4 / 1.31	0x79EAC42F	AGL Omega Time constant
0x18	0x22	Release Rate	4 / 1.31	0x00002BB1	AGL Release Time constant
0x1C	0x22	Volume	4 / 1.31	0x7FFFFFFF	AGL Volume

14 器件和文档支持

14.1 器件支持

14.1.1 器件命名规则

*Glossary*部分列出的术语是根据多项德州仪器 (TI) 计划定义的通用术语（包括常用的缩写和单词），符合 JEDEC、IPC、IEEE 等行业标准。本部分提供的术语定义了特定于本产品和文档、附属产品、或本产品使用的支持工具和软件的单词、短语和缩写。如对定义和术语有其他疑问，请访问e2e 音频放大器论坛。

桥接负载 (BTL) 是一种输出配置，其中扬声器的两端分别连接一个半桥。

DUT 是指*被测器件*，用于区分其他器件。

闭环架构是一种拓扑结构，其中放大器监视输出引脚、对比输出信号与输入信号，并尝试修正输出信号的非线性。

动态控件是指系统或最终用户在正常使用时可更改的控件。

GPIO 是通用输入/输出引脚。该引脚是一个高度可配置的双向数字引脚，可执行系统所需的多种功能。

主机处理器（也称系统处理器、标量、主机或系统控制器）是指用作中央系统控制器的器件，可为其连接的器件提供控制信息，从其上游器件采集音频源数据后分配给其他器件。该器件通常配置音频路径中音频处理器件（如 TAS5780M）的控件，从而根据频率响应、时间校准、目标声压级、系统安全工作区域和用户偏好优化扬声器的音频输出。

HybridFlow 通过搭配使用 RAM 内置的元件和 ROM 内置的元件构成一款可配置器件，与完全可编程器件相比更加易于使用，而且还能保持足够的灵活性以适应多种 应用

最大持续输出功率是指放大器在 25°C 工作环境温度下可持续（不关断）提供的最大输出功率。测试该参数时，当放大器温度达到热平衡点并且不再升高时停止测试

并行桥接负载 (PBTL) 是一种输出配置，其中扬声器的两端分别连接一对并行放置的半桥。

$r_{DS(on)}$ 是指放大器输出级中所用 MOSFET 的导通电阻。

静态控制/静态配置是指系统正常使用时不发生变化的控件。

过孔是指 PCB 中的镀铜通孔。

14.1.2 开发支持

有关 RDGUI 软件，请咨询当地的现场支持工程师。

14.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

14.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.4 商标

Burr-Brown, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

14.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5780MDCA	ACTIVE	HTSSOP	DCA	48	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	BURR-BROWN TAS5780M	Samples
TAS5780MDCAR	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	BURR-BROWN TAS5780M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

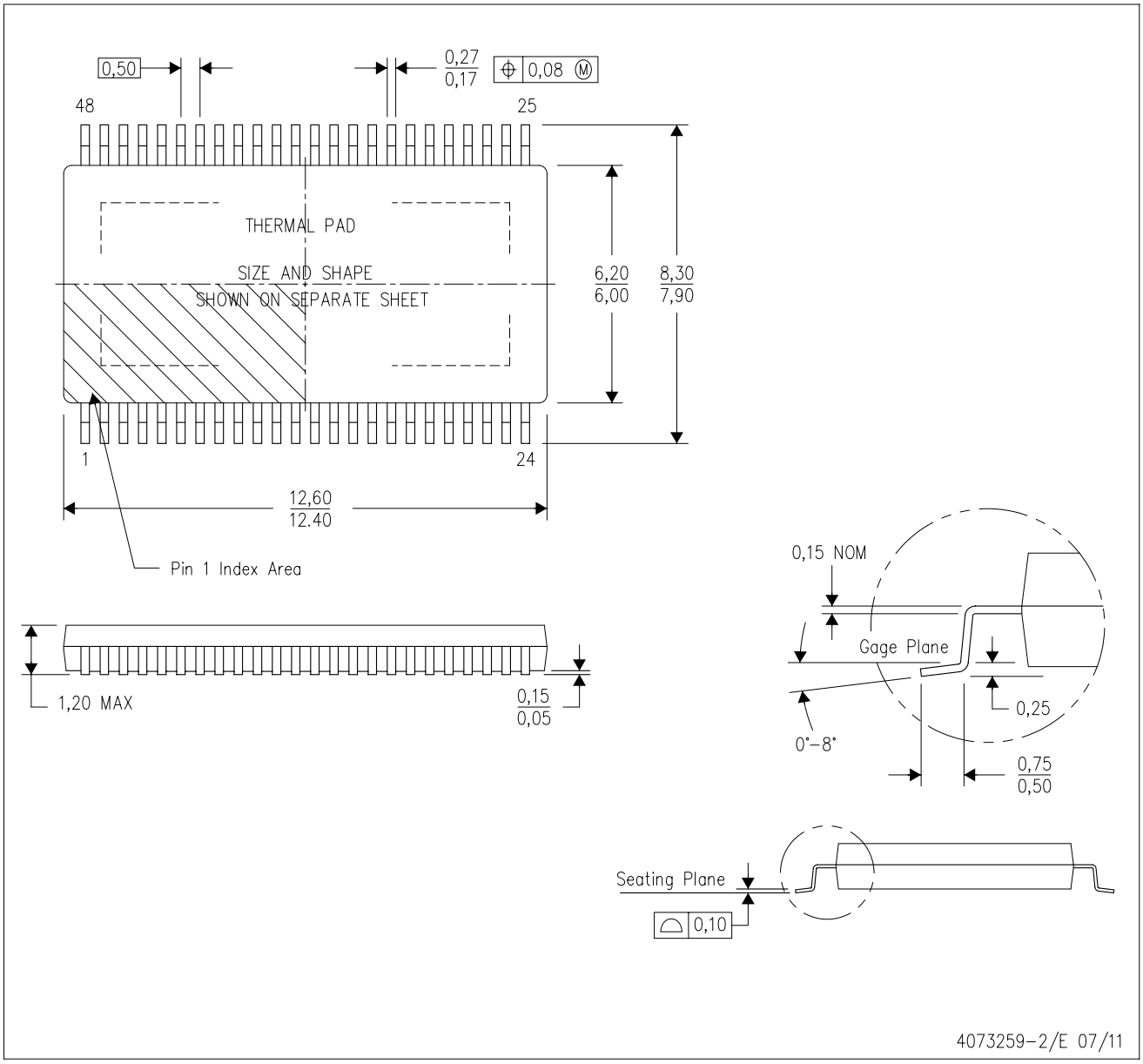
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

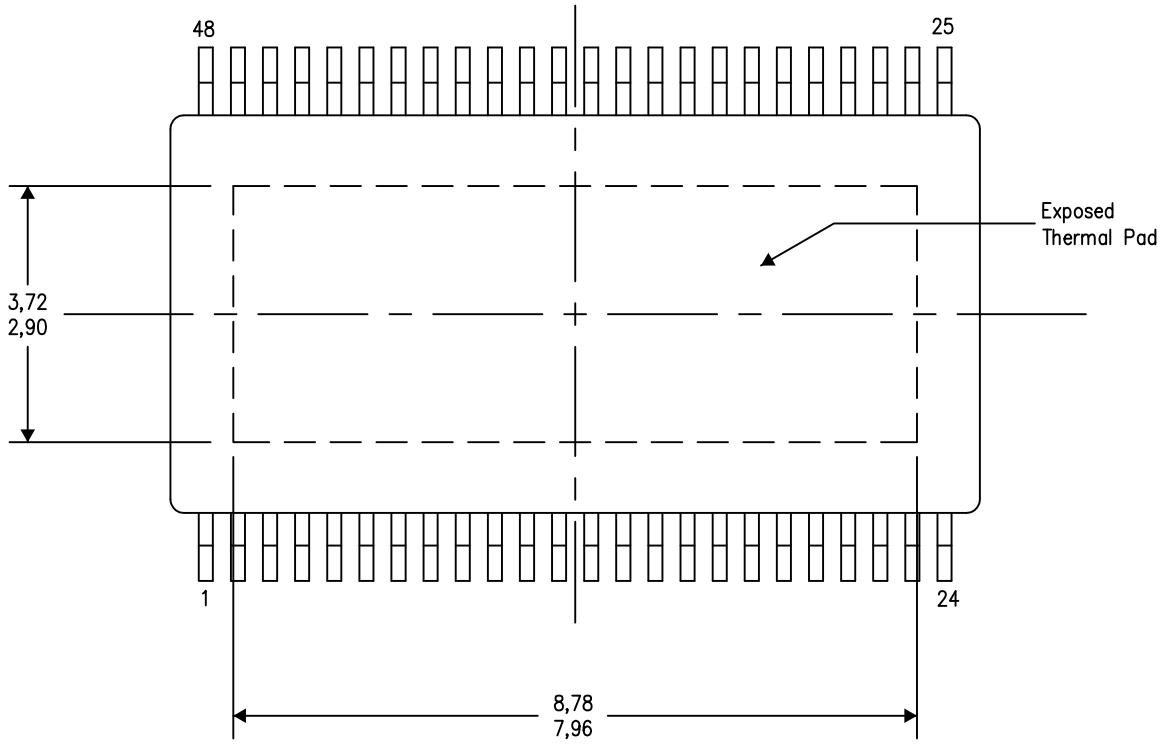
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206320–7/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

重要声明和免责声明

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