

具有可调节增益的 DRV632 DirectPath™ 2VRMS 音频线路驱动器

1 特性

- 立体声 DirectPath™ 音频线路驱动器
 - 在由 3.3V 电源供电时, 2Vrms 进入 10kΩ 负载
- 在 2Vrms 进入 10kΩ 负载时, 低总谐波失真 (THD)+N < 0.01%
- 高信噪比 (SNR), > 90dB
- 可支持 600Ω 输出负载
- 差分输入和单端输出
- 由外部增益设定电阻器实现的可调增益
- 低直流偏移, < 1mV
- 接地基准输出免除了对于隔直流电容器的需要
 - 减小电路板面积
 - 降低组件成本
 - 改善 THD+N 性能
 - 未出现因输出电容器所导致的低频响应性能下降
- 短路保护功能
- 瞬时杂音(喀哒声和噼啪声)抑制电路
- 外部欠压静音
- 用于实现无杂音音频打开/关闭控制的有源静音控制功能
- 节省空间的薄型小外形尺寸 (TSSOP) 封装

2 应用

- 机顶盒
- Blu-ray Disc™, DVD 播放器
- 液晶 (LCD) 和等离子 (PDP) 电视
- 迷你型/微型组合音响系统
- 声卡
- 笔记本电脑

3 说明

DRV632 是一款 2V_{RMS} 无杂音立体声线路驱动器, 此驱动器设计用于去除输出隔直流电容器, 以减少组件数目及成本。对于那些将尺寸和成本作为关键设计参数的单电源电子产品, 该器件是理想的选择。

DRV632 的设计运用了 TI 的 DirectPath™ 专利技术, 能够在 3.3V 电源电压供电时驱动 2V_{RMS} 进入一个 10kΩ 负载。此器件具有差分输入, 并采用外部增益设置电阻器以支持 ±1V/V 至 ±10V/V 的增益范围, 而且可为每个通道单独配置增益。线路输出具有 ±8kV IEC 静电放电 (ESD) 保护, 因而只需要使用一个简单的电阻器-电容器 ESD 保护电路即可。DRV632 具有针对无杂音音频打开/关闭控制的内置有源静音控制功能。DRV632 具有一个外部欠压检测器, 该欠压检测器在电源被移除时将输出静音, 从而确保了无杂音的关断操作。

与产生 2V_{RMS} 输出的传统方法相比, 在音频产品中使用 DRV632 能够大幅度地减少组件数量。DRV632 既不需要采用一个高于 3.3V 的电源来产生其 5.6V_{pp} 输出, 也不需要一个分离轨电源。DRV632 内部集成了电荷泵以产生一个负电源轨, 此负电源轨可提供一个良好的无杂音接地偏置 2V_{RMS} 输出。

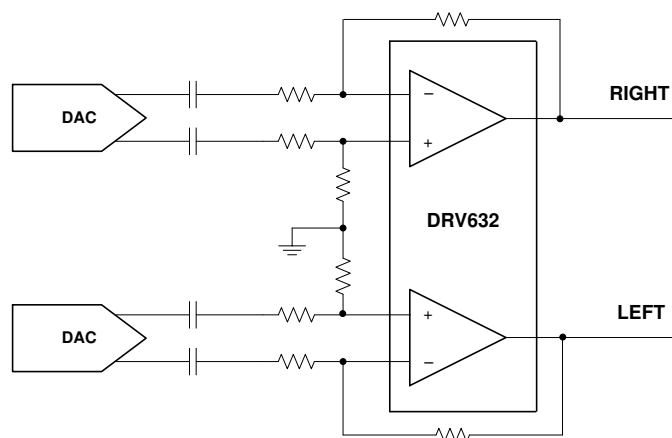
DRV632 采用 14 引脚 TSSOP 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
DRV632	TSSOP (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

简化图表



目录

1	特性	1	9.2	Functional Block Diagram	8
2	应用	1	9.3	Feature Description	9
3	说明	1	9.4	Device Functional Modes	11
4	修订历史记录	2	10	Application and Implementation	12
5	Device Comparison Table	3	10.1	Application Information	12
6	Pin Configuration and Functions	4	10.2	Typical Application	12
7	Specifications	4	11	Power Supply Recommendations	14
7.1	Absolute Maximum Ratings	4	12	Layout	15
7.2	ESD Ratings	5	12.1	Layout Guidelines	15
7.3	Recommended Operating Conditions	5	12.2	Layout Example	15
7.4	Thermal Information	5	13	器件和文档支持	16
7.5	Electrical Characteristics	5	13.1	器件支持	16
7.6	Operating Characteristics	6	13.2	社区资源	16
7.7	Typical Characteristics	7	13.3	商标	16
8	Parameter Measurement Information	7	13.4	静电放电警告	16
9	Detailed Description	8	13.5	Glossary	16
9.1	Overview	8	14	机械、封装和可订购信息	16

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (August 2015) to Revision C Page

- Added link to DRV632EVM User's Guide..... 15

Changes from Revision A (June 2013) to Revision B Page

- 已添加 添加了引脚配置和功能 部分、ESD 额定值 表、特性 说明 部分、器件功能模式、应用和实施 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 1
- Added Device Comparison table. 3

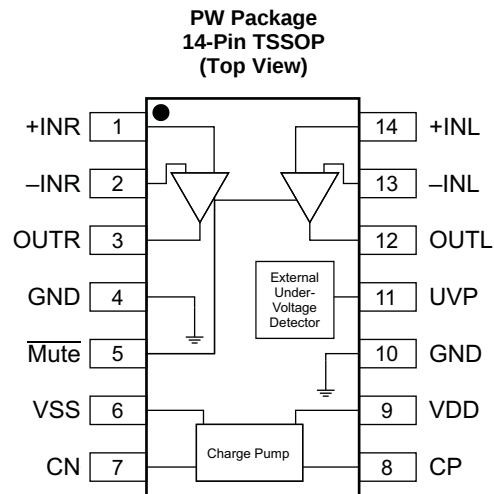
Changes from Original (January 2011) to Revision A Page

- Changed description of UVP in PIN FUNCTIONS table 4
- Deleted min value for SNR and DNR in OPERATING CHARACTERISTICS table 6

5 Device Comparison Table

DEVICE	INPUT OFFSET ($\pm\mu\text{V}$)	OUTPUT VOLTAGE (TYP) (VRMS)	MINIMUM LOAD IMPEDANCE (Ω)
DRV632	1000	2.4	600
DRV612	1000	2.2	600
DRV604	500	2.1	1000 (line output) / 8 (headphone output)
DRV603	1000	2.05 (VSS = 3.3 V) / 3.01 (VDD = 5 V)	600
DRV602	5000	2.05 (VSS = 3.3 V) / 3.01 (VDD = 5 V)	600
DRV601	8000	2.1 (VSS = 3.3 V) / 2.7 (VDD = 4.5 V)	100
DRV600	8000	2.1 (VSS = 3.3 V) / 2.7 (VDD = 4.5 V)	100

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
CN	7	I/O	Charge-pump flying capacitor negative connection
CP	8	I/O	Charge-pump flying capacitor positive connection
GND	4, 10	P	Ground
-INL	13	I	Left-channel OPAMP negative input
+INL	14	I	Left-channel OPAMP positive input
-INR	2	I	Right-channel OPAMP negative input
+INR	1	I	Right-channel OPAMP positive input
Mute	5	I	Mute, active-low
OUTL	12	O	Left-channel OPAMP output
OUTR	3	O	Right-channel OPAMP output
UVP	11	I	Undervoltage protection, internal pullup; unconnected if UVP function is unused.
VDD	9	P	Positive supply
VSS	6	P	Supply voltage

(1) I = input, O = output, P = power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range ⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, VDD to GND	-0.3	4	V
V _I Input voltage	V _{SS} - 0.3	VDD + 0.3	V
R _L Minimum load impedance – line outputs – OUTL, OTR		600	Ω
Mute to GND, UVP to GND	-0.3	VDD + 0.3	V
T _J Maximum operating junction temperature	-40	150	°C
T _{stg} Storage temperature	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±4000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD Supply voltage	DC supply voltage	3	3.3	3.6	V
R _L Load impedance		0.6	10		kΩ
V _{IL} Low-level input voltage	Mute		40		% of VDD
V _{IH} High-level input voltage	Mute		60		% of VDD
T _A Operating free-air temperature		–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV632	UNIT
		PW (TSSOP)	
		14 PINS	
R _{θJA} Junction-to-ambient thermal resistance		130	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance		49	°C/W
R _{θJB} Junction-to-board thermal resistance		63	°C/W
ψ _{JT} Junction-to-top characterization parameter		3.6	°C/W
ψ _{JB} Junction-to-board characterization parameter		62	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS} Output offset voltage	VDD = 3.3 V		0.5	1	mV
PSRR Power-supply rejection ratio			80		dB
V _{OH} High-level output voltage	VDD = 3.3 V	3.1			V
V _{OL} Low-level output voltage	VDD = 3.3 V			–3.0 5	V
V _{UVP_EX} External UVP detect voltage			1.25		V
V _{UVP_EX_HYSTERESIS} External UVP detect hysteresis current			5		μA
f _{CP} Charge pump switching frequency		200	300	400	kHz
I _{IH} High-level input current, Mute	VDD = 3.3 V, V _{IH} = VDD			1	μA
I _{IL} Low-level input current, Mute	VDD = 3.3 V, V _{IL} = 0 V			1	μA
I _{DD} Supply current	VDD = 3.3 V, no load, Mute = VDD	5	14	25	mA
	VDD = 3.3 V, no load, Mute = GND, disabled		14		

7.6 Operating Characteristics

VDD = 3.3 V, R_{DL} = 10 kΩ, R_{FB} = 30 kΩ, R_{IN} = 15 kΩ, T_A = 25°C, Charge pump: C_P = 1 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _O	Output voltage, outputs in phase	THD+N = 1%, VDD = 3.3 V, f = 1 kHz, R _L = 10 kΩ	2	2.4		V _{rms}
THD+N	Total harmonic distortion plus noise	V _O = 2 V _{RMS} , f = 1 kHz		0.002%		
SNR	Signal-to-noise ratio ⁽¹⁾	A-weighted		105		dB
DNR	Dynamic range	A-weighted		105		dB
V _N	Noise voltage	A-weighted		11		μV
Z _O	Output Impedance when muted	Mute = GND		110		mΩ
	Input-to-output attenuation when muted	Mute = GND		80		dB
	Crosstalk—L to R, R to L	V _O = 1 V _{rms}		–110		dB
I _{LIMIT}	Current limit			25		mA

(1) SNR is calculated relative to 2-V_{rms} output.

7.7 Typical Characteristics

$V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $C_{(PUMP)} = C_{(VSS)} = 1\text{ }\mu\text{F}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $R_{IN} = 15\text{ k}\Omega$, $R_{fb} = 30\text{ k}\Omega$, $R_{OUT} = 32\text{ }\Omega$, $C_{OUT} = 1\text{ nF}$ (unless otherwise noted)

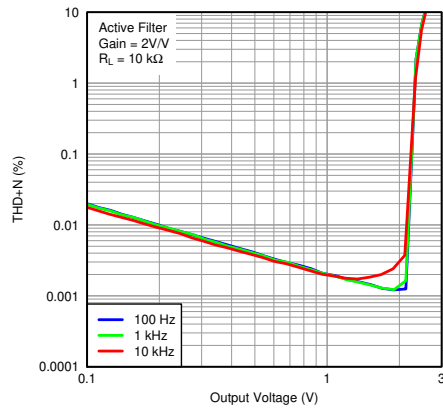


Figure 1. Total Harmonic Distortion and Noise vs Output Voltage

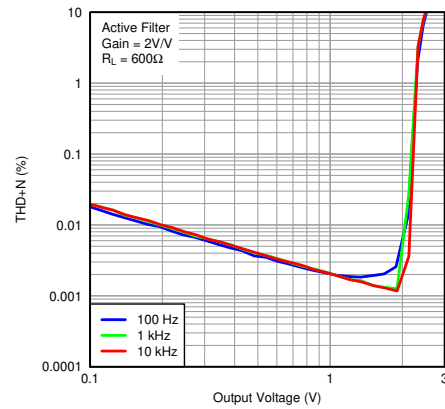


Figure 2. Total Harmonic Distortion and Noise vs Output Voltage

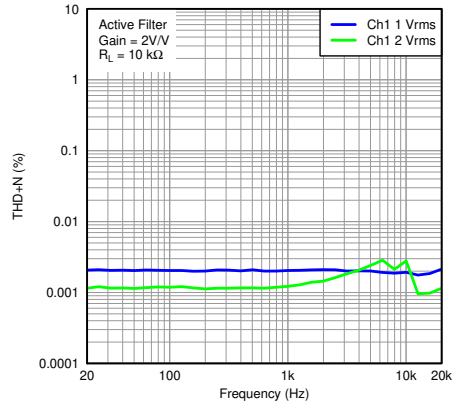


Figure 3. Total Harmonic Distortion and Noise vs Frequency

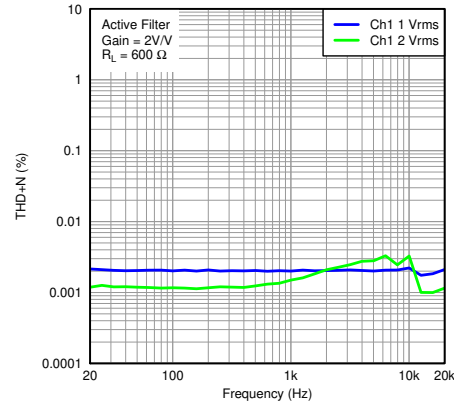


Figure 4. Total Harmonic Distortion and Noise vs Frequency

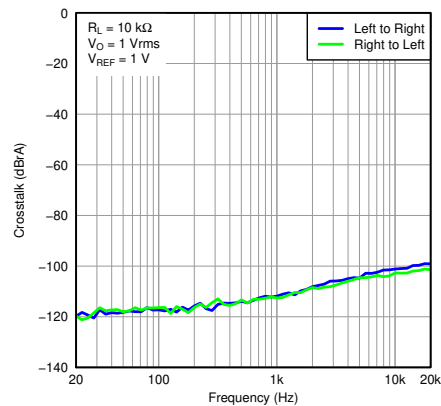


Figure 5. Crosstalk vs Frequency

8 Parameter Measurement Information

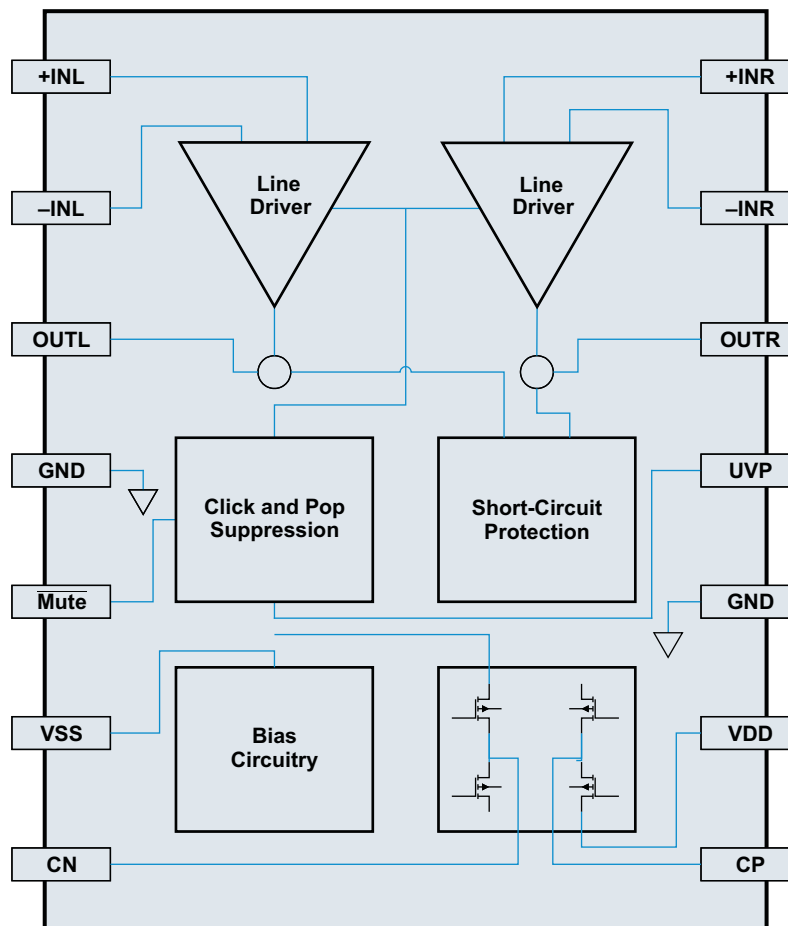
All parameters are measured according to the conditions described in [Specifications](#).

9 Detailed Description

9.1 Overview

Combining the TI's patented DirectPath technology with the built-in click and pop reduction circuit, the DRV632 is a 2-VRMS pop-free stereo line driver designed to avoid the use of the output DC-blocking capacitors, resulting in reduced component count and cost. The DRV632 is capable of driving 2-VRMS into a line load of 600 Ω to 10 k Ω with a 3.3-V supply voltage. The use of charge-pump flying, PVSS, and decoupling capacitors ensure the performance of the amplifier. The device has two channels with differential inputs that require DC input-blocking capacitors to block the DC portion of the audio source. These allow the DRV632 inputs to be properly biased to provide maximum performance. The DRV632 allows external gain-setting resistors to support a gain range of ± 1 V/V to ± 10 V/V. The gain can be configured individually for each channel. Additionally, both channels can be used as a second-order filter when the removal of out-of-band noise is required. The DRV632 has a built-in active-mute control for pop-free audio on/off, and avoids the click and pop generation by using external undervoltage detection. The device does not generate a pop or click when the power supply is removed or placed.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Line Driver Amplifiers

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 6 illustrates the conventional line-driver amplifier connection to the load and output signal. DC blocking capacitors are often large in value. The line load (typical resistive values of 600 Ω to 10 k Ω) combines with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance (R_L), the capacitor (C_O), and the cutoff frequency (f_c).

$$f_c = \frac{1}{2\pi R_L C_O} \quad (1)$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \quad (2)$$

If f_c is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

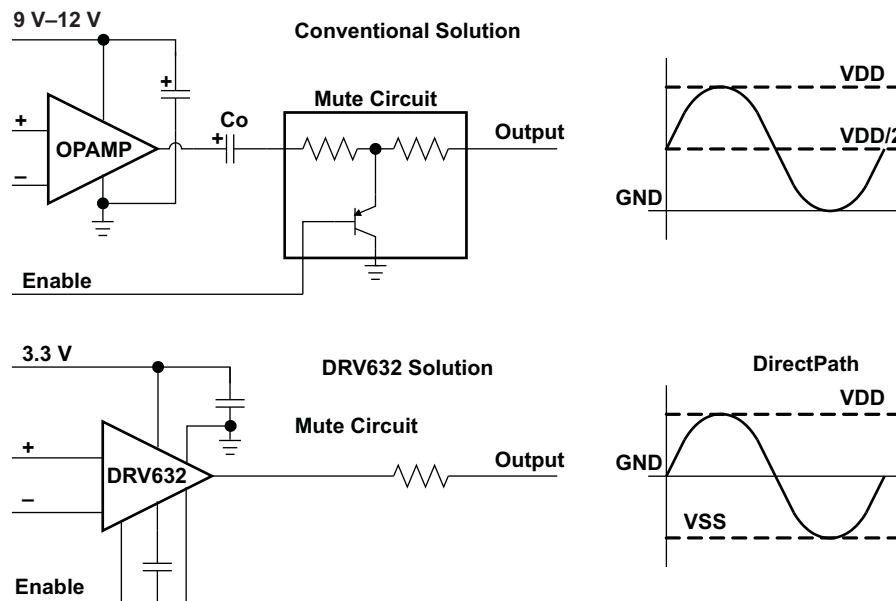


Figure 6. Conventional and DirectPath Line Drivers

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split-supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click and pop reduction circuit, the DirectPath amplifier requires no output dc blocking capacitors. The bottom block diagram and waveform of Figure 6 illustrate the ground-referenced line-driver architecture. This is the architecture of the DRV632.

9.3.2 Charge-Pump Flying Capacitor and PVSS Capacitor

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge-pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 μ F is typical. Capacitor values that are smaller than 1 μ F can be used, but the maximum output voltage may be reduced and the device may not operate to specifications. If the DRV632 is used in highly noise-sensitive circuits, TI recommends adding a small LC filter on the VDD connection.

Feature Description (continued)

9.3.3 Decoupling Capacitors

The DRV632 is a DirectPath line-driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good, low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μ F, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DRV632 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10- μ F or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

9.3.4 Gain-Setting Resistor Ranges

The gain-setting resistors, R_{IN} and R_{fb} , must be chosen so that noise, stability, and input capacitor size of the DRV632 are kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{IN} .

Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN} . Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different inverting-input gain settings.

Table 1. Recommended Resistor Values

GAIN	INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{fb}
–1 V/V	10 k Ω	10 k Ω
–1.5 V/V	8.2 k Ω	12 k Ω
–2 V/V	15 k Ω	30 k Ω
–10 V/V	4.7 k Ω	47 k Ω

9.3.5 Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV632. These capacitors block the dc portion of the audio source and allow the DRV632 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN} . The cutoff frequency is calculated using Equation 3. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

It is recommended to use electrolytic capacitors or high-voltage-rated capacitors as input blocking capacitors to ensure minimal variation in capacitance with input voltages. Such variation in capacitance with input voltages is commonly seen in ceramic capacitors and can increase low-frequency audio distortion.

$$f_{cIN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi f_{cIN} R_{IN}} \quad (3)$$

9.3.6 DRV632 UVP Operation

The shutdown threshold at the UVP pin is 1.25 V. The customer must use a resistor divider to obtain the shutdown threshold and hysteresis desired for a particular application. The customer-selected thresholds can be determined as follows:

9.3.7 External Undervoltage Detection

External undervoltage detection can be used to mute/shut down the DRV632 before an input device can generate a pop.

The shutdown threshold at the UVP pin is 1.25 V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as follows:

$$V_{UVP} = (1.25 - 6 \mu A \times R3) \times (R1 + R2) / R2$$

$$\text{Hysteresis} = 5 \mu A \times R3 \times (R1 + R2) / R2$$

For example, to obtain $V_{UVP} = 3.8$ V and 1-V hysteresis, use $R1 = 3$ k Ω , $R2 = 1$ k Ω , and $R3 = 50$ k Ω .

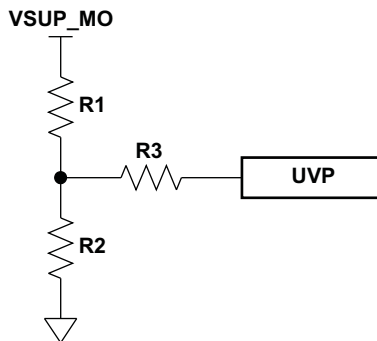


Figure 7. UVP Resistor Divider

9.4 Device Functional Modes

9.4.1 Using the DRV632 as a Second-Order Filter

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the DRV632, as it can be used like a standard operational amplifier. Several filter topologies can be implemented, both single-ended and differential. In Figure 8, multi-feedback (MFB) with differential input and single-ended input are shown.

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc gain to 1, helping to reduce the output dc offset to a minimum.

To calculate the component values, use the TI WEBENCH® Filter Designer (www.ti.com/filterdesigner).

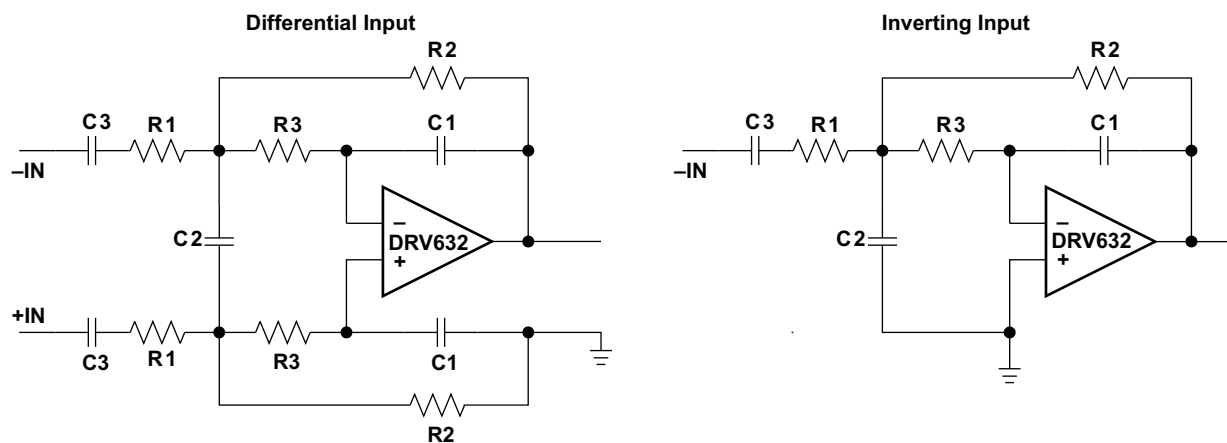


Figure 8. Second-Order Active Low-Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small-size ac-coupling capacitor. With the proposed values of $R1 = 15\text{ k}\Omega$, $R2 = 30\text{ k}\Omega$, and $R3 = 43\text{ k}\Omega$, a dynamic range (DYR) of 106 dB can be achieved with a 1- μF input ac-coupling capacitor.

9.4.2 Mute Mode

The DRV632 can be muted using the low-active Mute pin (pin 5). The click-and-pop suppression capacity ensures that when the mute mode is used, it does not generate an additional click or pop.

10 Application and Implementation

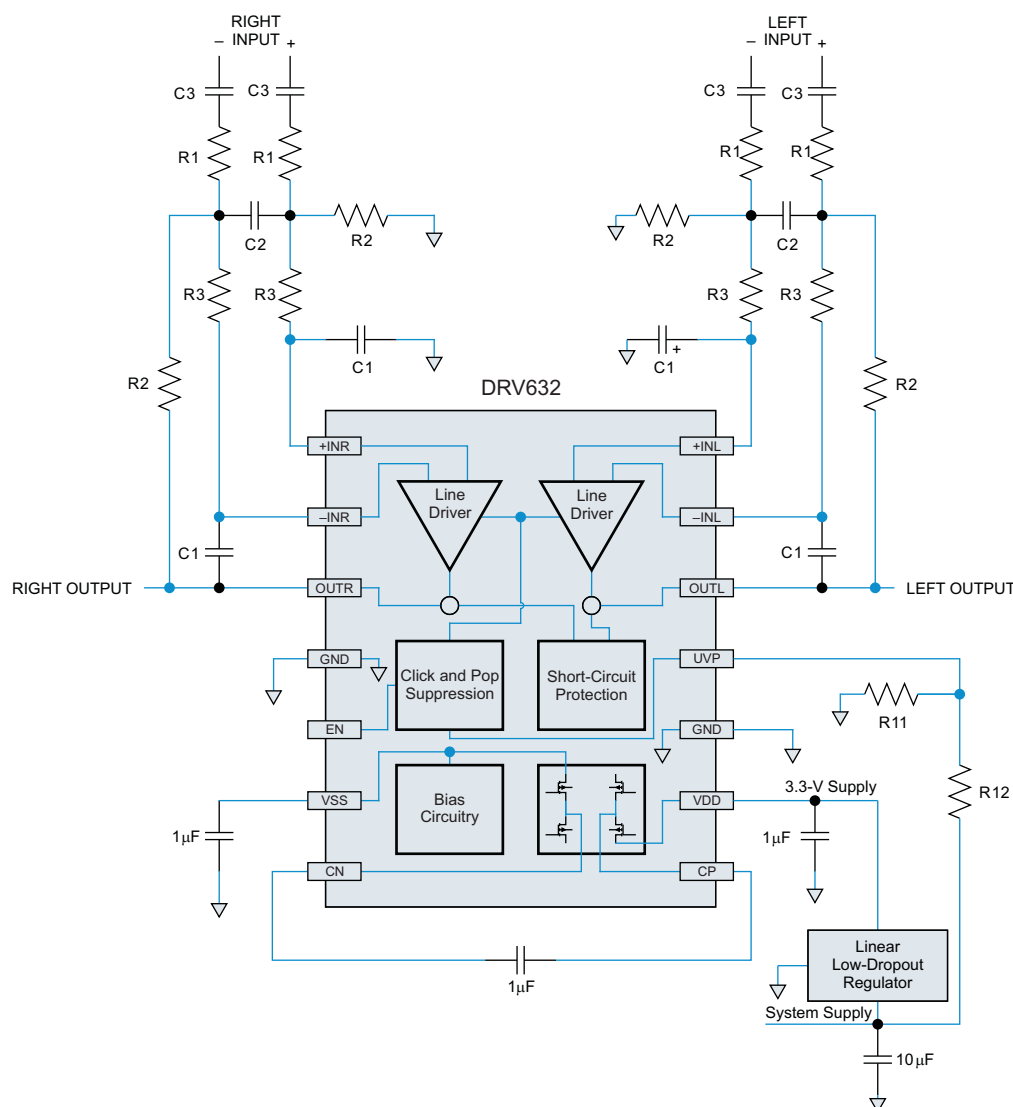
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This typical connection diagram highlights the required external components and system-level connections for proper operation of the device. This configuration can be realized using the Evaluation Module (EVM) of the device. This flexible module allows full evaluation of the device in all available modes of operation. Also see the DRV632 product page for information on ordering the EVM.

10.2 Typical Application



R1 = 15 k Ω , R2 = 30 k Ω , R3 = 43 k Ω , C1 = 47 pF, C2 = 180 pF
Differential-input, single-ended output, second-order filter

Figure 9. Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

In this design example, use the parameters listed in [Table 2](#).

Table 2. Design Parameters

KEY PARAMETERS	VALUE
Supply Voltage	3.3 V
Supply Current	0.10 A
Load Impedance	600 Ω (minimum)

10.2.2 Detailed Design Procedure

10.2.2.1 Charge-Pump Flying, PVSS and Decoupling Capacitors

To transfer charge during the generation of the negative supply voltage, an 1- μ F low equivalent-series-resistance (ESR) charge-pump flying capacitor is used for this design. Similar 1- μ F capacitors are placed in VSS, and as close as possible to VDD. See [Charge-Pump Flying Capacitor and PVSS Capacitor](#) and [Decoupling Capacitors](#) for details.

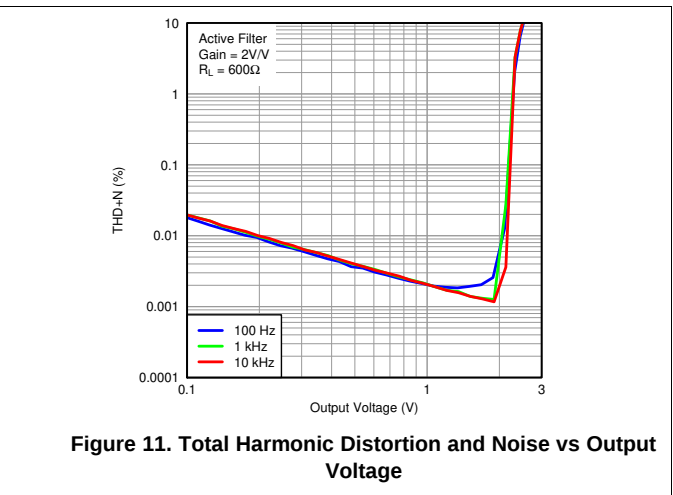
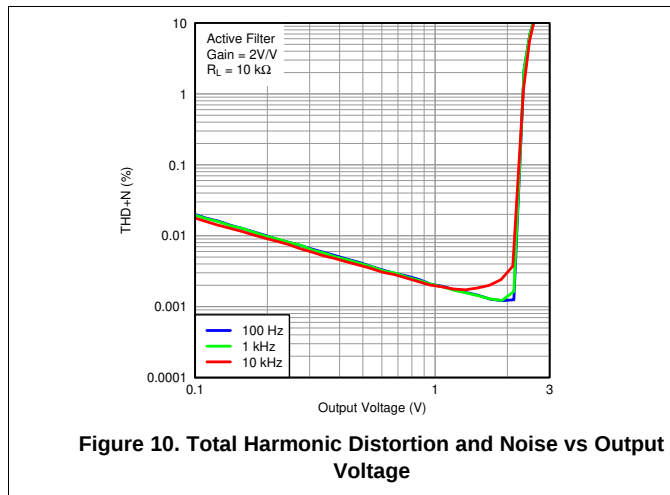
10.2.2.2 Second-Order Active Low-Pass Filters

With the help of the TI WEBENCH Filter Designer (www.ti.com/filterdesigner), the values of R1 = 15 k Ω , R2 = 30 k Ω , R3 = 43 k Ω , C1 = 47 pF, and C2 = 180 pF are proposed to design a second-order low-pass filter with a differential-input and a single-ended output. See [Using the DRV632 as a Second-Order Filter](#) for details.

10.2.2.3 UVP Resistor Divider

R11 and R12 are placed to design a resistor divider. The shutdown threshold at the UVP pin is 1.25 V. See [External Undervoltage Detection](#) for details.

10.2.3 Application Curves



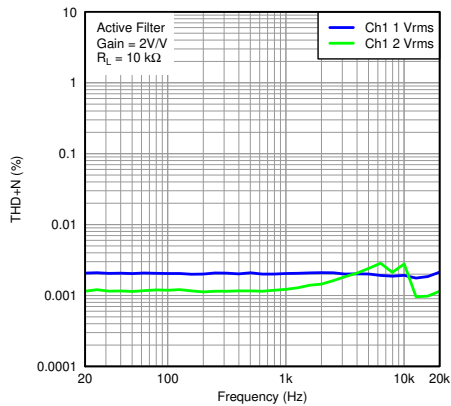


Figure 12. Total Harmonic Distortion and Noise vs Frequency

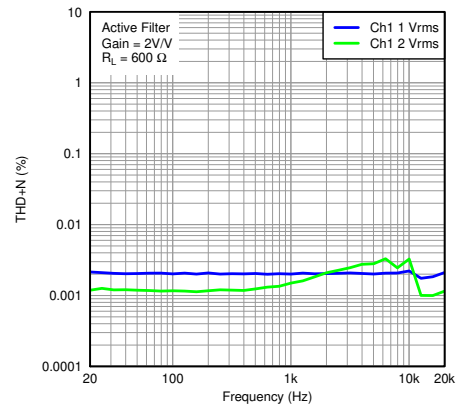


Figure 13. Total Harmonic Distortion and Noise vs Frequency

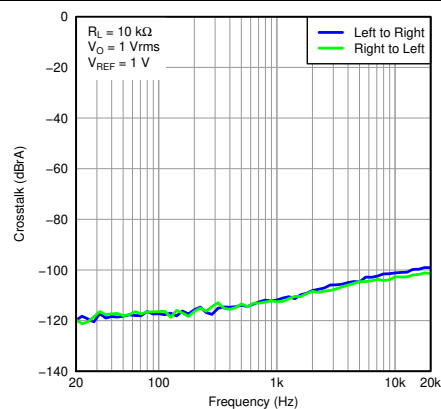


Figure 14. Crosstalk vs Frequency

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3 V and 3.6 V. This input supply must be well-regulated. If the input supply is located more than a few inches from the DRV632 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 μ F is a typical choice.

Placing a decoupling capacitor close to the DRV632 improves the performance of the line-driver amplifier. A low equivalent-series-resistance (ESR) ceramic capacitor with a value of 1 μ F is a typical choice.

If the DRV632 is used in highly noise-sensitive circuits, TI recommends adding a small LC filter on the VDD connection.

12 Layout

12.1 Layout Guidelines

12.1.1 Gain-Setting Resistors

The gain-setting resistors, R_{IN} and R_{fb} , must be placed close to pins 13 and 17, respectively, to minimize capacitive loading on these input pins and to ensure maximum stability of the DRV632. For the recommended PCB layout, see the [DRV632EVM User's Guide](#).

12.2 Layout Example

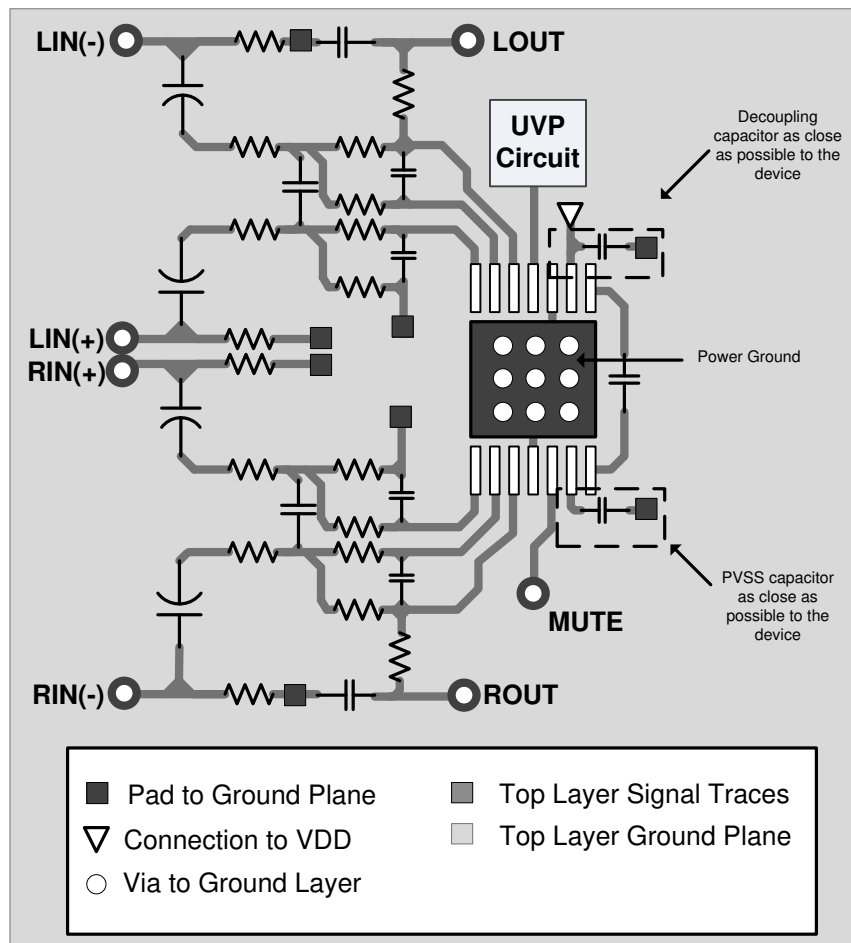


Figure 15. DRV632 Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 开发支持

如需 DRV632EVM 和 Gerber 文件, 请转到 www.ti.com.cn/tool/cn/DRV632EVM。

13.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 商标

DirectPath, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

13.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更, 恕不另行通知, 且不会对此文档进行修订。如需获取此数据表的浏览器版本, 请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV632PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV632	Samples
DRV632PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV632	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV632PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

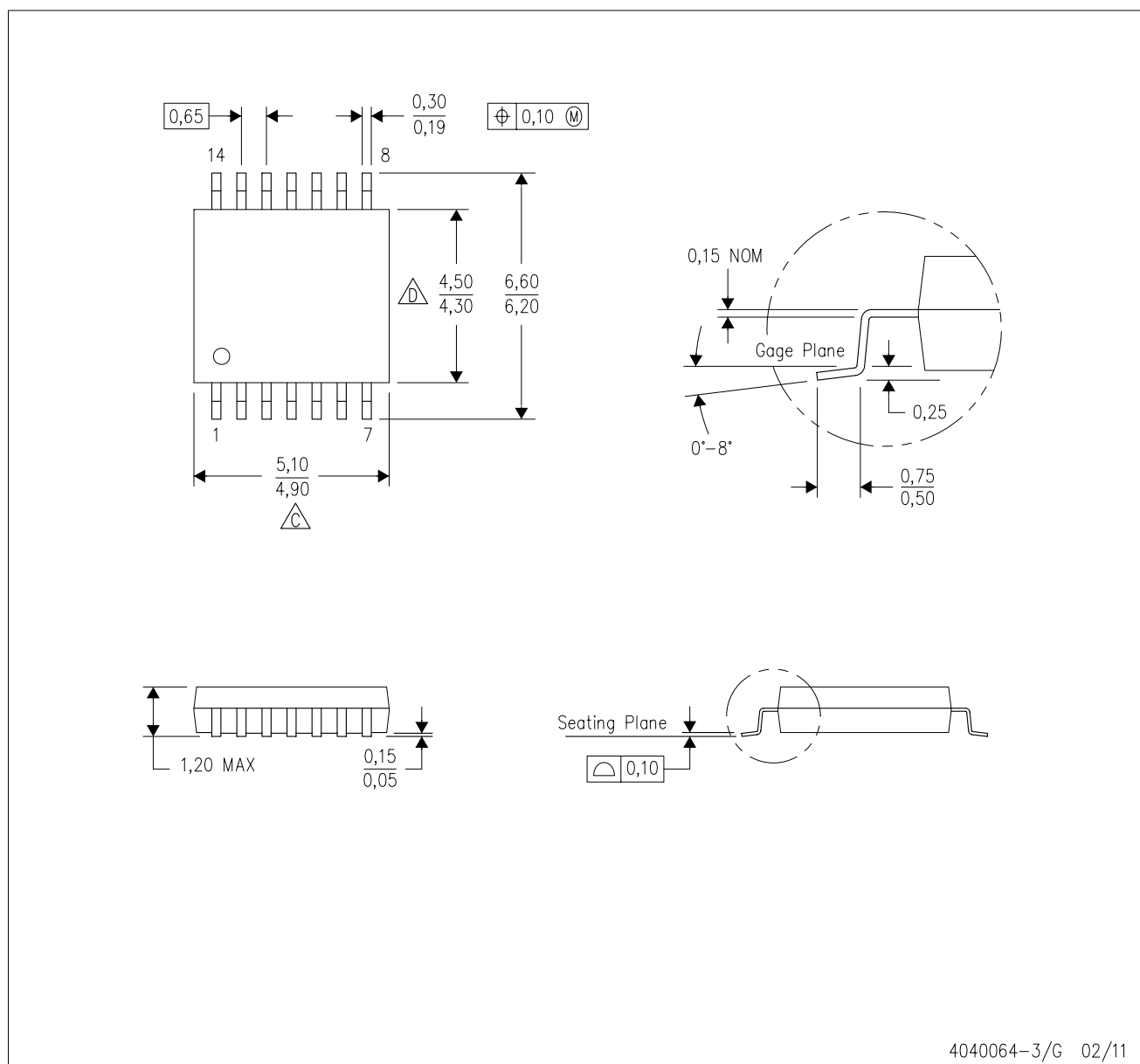


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV632PWR	TSSOP	PW	14	2000	350.0	350.0	43.0

PW (R-PDSO-G14)

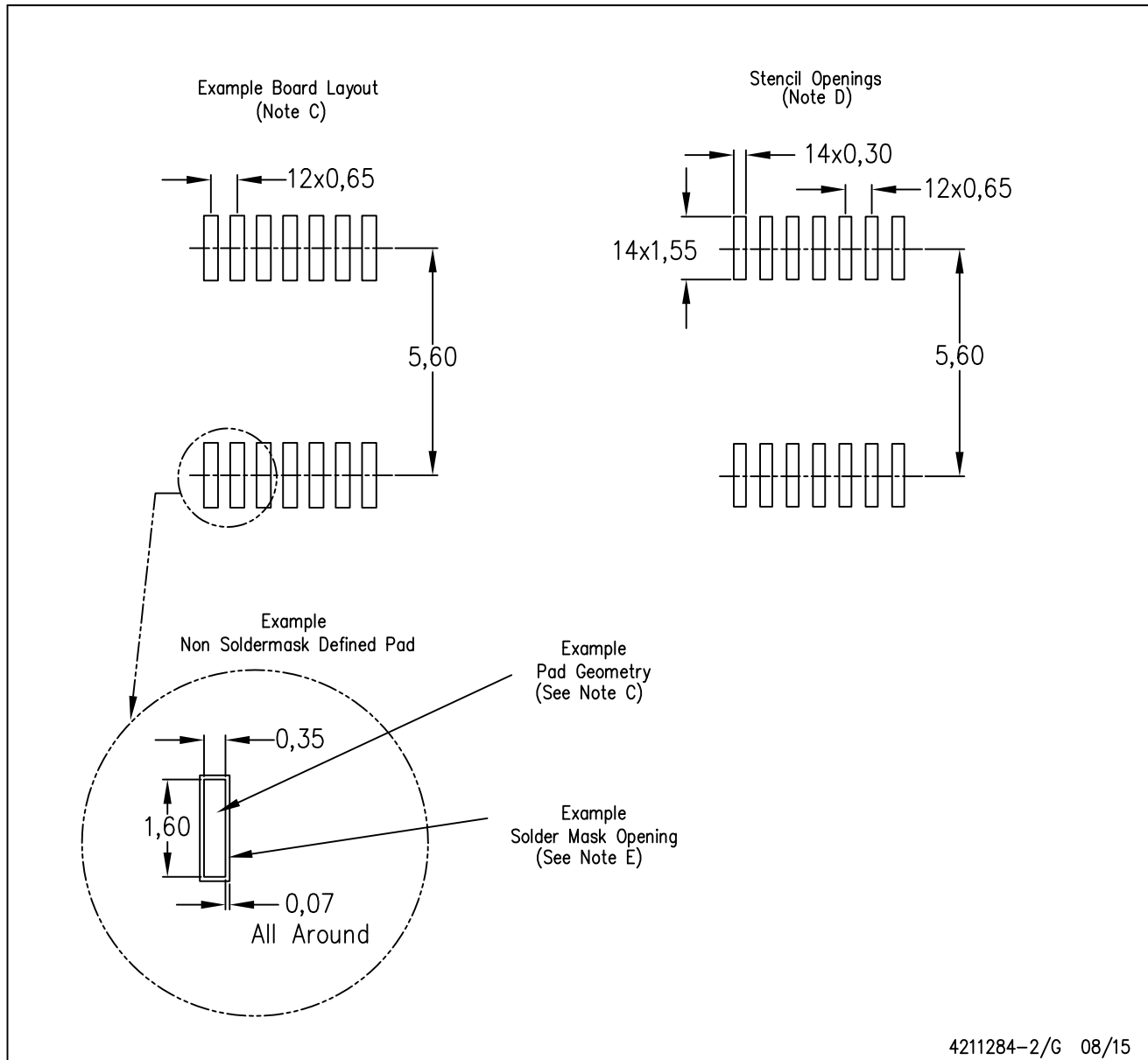
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司