

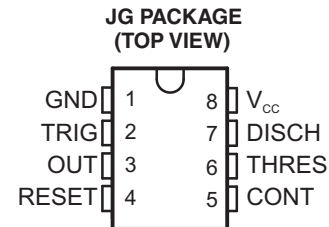
## QML CLASS V PRECISION TIMER

Check for Samples: [SE555-SP](#)

### FEATURES

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source up to 100 mA
- QML-V Qualified, SMD 5962-98555
- Military Temperature Range (-55°C to 125°C)
- Rad-Tolerant: 25 kRad (Si) TID <sup>(1)</sup>

(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.



### DESCRIPTION/ORDERING INFORMATION

The SE555 is a precision timing circuit capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V<sub>CC</sub>. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 100 mA. Operation is specified for supplies of 4.5 V to 16.5 V. With a 5-V supply, output levels are compatible with TTL inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION<sup>(1)</sup>**

<b>T<sub>A</sub></b>	<b>PACKAGE<sup>(2)</sup></b>		<b>ORDERABLE PART NUMBER</b>	<b>TOP-SIDE MARKING</b>
–55°C to 125°C	CDIP - JG	Tube of 50	5962-9855501VPA	5962-9855501VPA

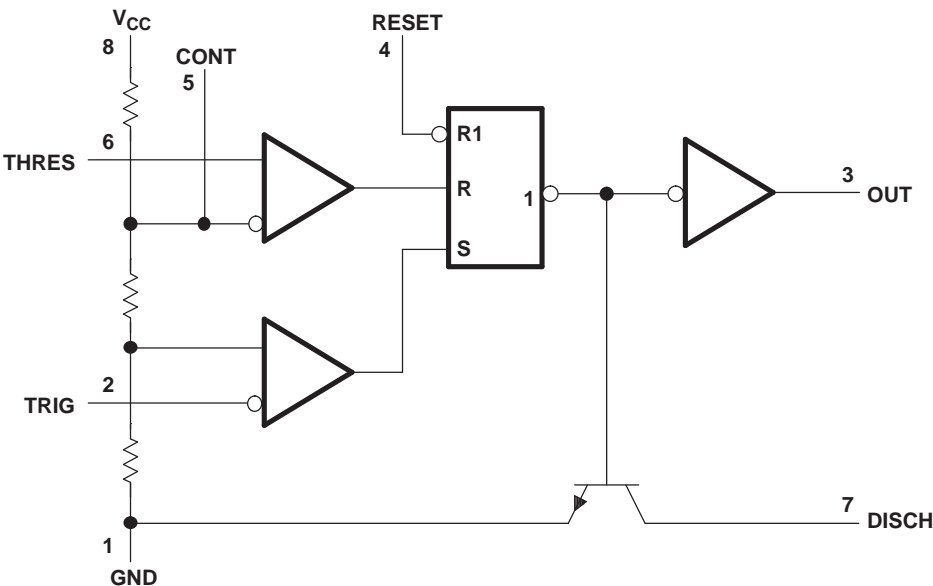
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).  
(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**Table 1. FUNCTION TABLE**

<b>RESET</b>	<b>TRIGGER VOLTAGE<sup>(1)</sup></b>	<b>THRESHOLD VOLTAGE<sup>(1)</sup></b>	<b>OUTPUT</b>	<b>DISCHARGE SWITCH</b>
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V <sub>CC</sub>	Irrelevant	High	Off
High	>1/3 V <sub>CC</sub>	>2/3 V <sub>CC</sub>	Low	On
High	>1/3 V <sub>CC</sub>	<2/3 V <sub>CC</sub>	As previously established	

(1) Voltage levels shown are nominal.

**FUNCTIONAL BLOCK DIAGRAM**



A. RESET can override TRIG, which can override THRES.

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		18	V
V <sub>I</sub>	Input voltage	CONT, RESET, THRES, TRIG	V <sub>CC</sub>	V
I <sub>O</sub>	Output current		±200	mA
θ <sub>JC</sub>	Package thermal impedance <sup>(3)</sup> (4)		45	°C/W
T <sub>J</sub>	Operating virtual junction temperature		150	°C
	Lead temperature 1, 6 mm (1/16 in) from case for 60 s		300	°C
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Maximum power dissipation is a function of T<sub>J</sub>(max), θ<sub>JC</sub>, and T<sub>C</sub>. The maximum allowable power dissipation at any allowable case temperature is P<sub>D</sub> = (T<sub>J</sub>(max) – T<sub>C</sub>)/θ<sub>JC</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with MIL-STD-883.

## Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	16.5	V
V <sub>I</sub>	Input voltage	CONT, RESET, THRES, and TRIG	V <sub>CC</sub>	V
I <sub>O</sub>	Output current		±100	mA
T <sub>A</sub>	Operating free-air temperature	–55	125	°C

## ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 4.5 V to 16.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>CC</sub>	Power supply current	V <sub>CC</sub> = 4.5 V, R <sub>L</sub> = ∞	T <sub>A</sub> = 25°C, 125°C, –55°C	5	mA
		V <sub>CC</sub> = 16.5 V, R <sub>L</sub> = ∞	T <sub>A</sub> = 25°C, 125°C, –55°C	20	
V <sub>TR</sub>	Trigger voltage	V <sub>CC</sub> = 4.5 V	T <sub>A</sub> = 25°C	1.30	V
			T <sub>A</sub> = 125°C	1.30	
			T <sub>A</sub> = –55°C	1.15	
	V <sub>CC</sub> = 16.5 V		T <sub>A</sub> = 25°C	5.20	
			T <sub>A</sub> = 125°C	5.20	
			T <sub>A</sub> = –55°C	5	
I <sub>TR</sub>	Trigger current	V <sub>CC</sub> = 16.5 V for V <sub>TR</sub> = 5 V	T <sub>A</sub> = 25°C, 125°C, –55°C	–5	μA
V <sub>TH</sub>	Threshold voltage	V <sub>CC</sub> = 4.5 V	T <sub>A</sub> = 25°C	2.70	V
			T <sub>A</sub> = 125°C, –55°C	2.60	
		V <sub>CC</sub> = 16.5 V	T <sub>A</sub> = 25°C	10.70	
			T <sub>A</sub> = 125°C, –55°C	10.60	
I <sub>TH</sub>	Threshold current	V <sub>CC</sub> = 16.5 V	T <sub>A</sub> = 25°C, 125°C	250	nA
			T <sub>A</sub> = –55°C	2.5	μA

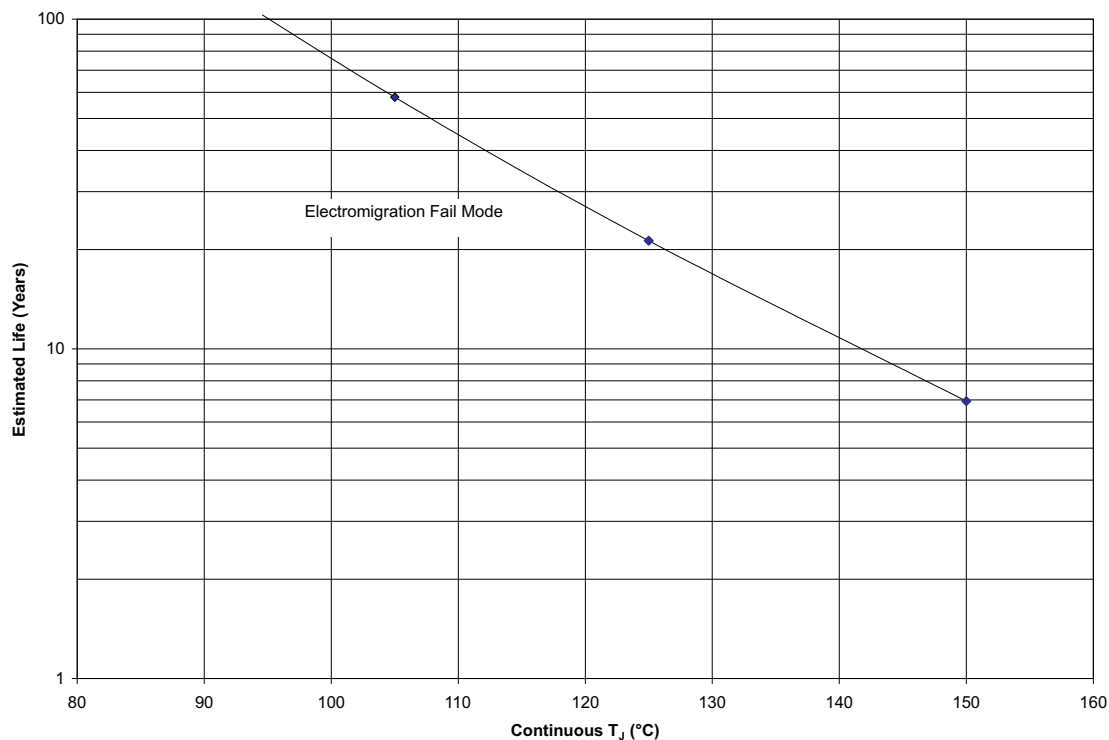
**ELECTRICAL CHARACTERISTICS (continued)**V<sub>CC</sub> = 4.5 V to 16.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>OL</sub>	Low level output voltage	V <sub>CC</sub> = 4.5 V, I <sub>SINK</sub> = 5 mA	T <sub>A</sub> = 25°C			0.25	V
			T <sub>A</sub> = 125°C, –55°C			0.35	
		V <sub>CC</sub> = 4.5 V, I <sub>SINK</sub> = 50 mA	T <sub>A</sub> = 25°C, 125°C			2.20	
			T <sub>A</sub> = –55°C			2.60	
		V <sub>CC</sub> = 16.5 V, I <sub>SINK</sub> = 10 mA	T <sub>A</sub> = 25°C, –55°C			0.15	
			T <sub>A</sub> = 125°C			0.25	
		V <sub>CC</sub> = 16.5 V, I <sub>SINK</sub> = 50 mA	T <sub>A</sub> = 25°C, –55°C			0.50	
			T <sub>A</sub> = 125°C			0.70	
V <sub>OH</sub>	High level output voltage	V <sub>CC</sub> = 4.5 V, I <sub>SOURCE</sub> = –100 mA	T <sub>A</sub> = 25°C, 125°C	2.60			V
			T <sub>A</sub> = –55°C	2.20			
		V <sub>CC</sub> = 16.5 V, I <sub>SOURCE</sub> = –100 mA	T <sub>A</sub> = 25°C, 125°C	14.60			
			T <sub>A</sub> = –55°C	14			
I <sub>CEX</sub>	Discharge transistor leakage current	V <sub>CC</sub> = 16.5 V	T <sub>A</sub> = 25°C, –55°C			100	nA
			T <sub>A</sub> = 125°C			3	μA
V <sub>SAT</sub>	Discharge transistor saturation voltage	V <sub>CC</sub> = 16.5 V, I <sub>D</sub> = 50 mA	T <sub>A</sub> = 25°C, –55°C			0.80	V
			T <sub>A</sub> = 125°C			1	
V <sub>R</sub>	Reset voltage	V <sub>CC</sub> = 16.5 V	T <sub>A</sub> = 25°C, 125°C, –55°C	0.10		1.30	V
I <sub>R</sub>	Reset current	V <sub>CC</sub> = 16.5 V, V <sub>R</sub> = 0 V	T <sub>A</sub> = 25°C, 125°C, –55°C	–1.60		0	mA
t <sub>PLH</sub>	Propagation delay time, low to high level output (monostable)	4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>T</sub> = 1 kΩ, C <sub>T</sub> = 0.1 μF	T <sub>A</sub> = 25°C, –55°C			800	ns
			T <sub>A</sub> = 125°C			900	
t <sub>TLH</sub>	Transition time, low to high level output (monostable)	4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>T</sub> = 1 kΩ, C <sub>T</sub> = 0.1 μF	T <sub>A</sub> = 25°C, 125°C, –55°C			300	ns
t <sub>THL</sub>	Transition time, high to low level output (monostable)	4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>T</sub> = 1 kΩ, C <sub>T</sub> = 0.1 μF	T <sub>A</sub> = 25°C, 125°C, –55°C			300	ns
t <sub>D(OH)</sub>	Time delay, output high (monostable)	4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>T</sub> = 1 kΩ, C <sub>T</sub> = 0.1 μF	T <sub>A</sub> = 25°C, 125°C, –55°C	106.70		113.30	μs
		4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>T</sub> = 100 kΩ, C <sub>T</sub> = 0.1 μF		10.67		11.33	ms
Δt <sub>D(OH)</sub> / ΔV <sub>CC</sub>	Drift in time delay versus change in supply voltage (monostable)	ΔV <sub>CC</sub> = 12 V, R <sub>T</sub> = 1 kΩ, C <sub>T</sub> = 0.1 μF	T <sub>A</sub> = 25°C	–220		220	ns/V
t <sub>PHL</sub>	Propagation delay time, threshold to output	4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>T</sub> = 1 kΩ	T <sub>A</sub> = 25°C, 125°C, –55°C			12	μs
Δt <sub>D(OH)</sub> / ΔT	Temperature coefficient of time delay (monostable)	V <sub>CC</sub> = 16.5 V, R <sub>T</sub> = 1 kΩ, C <sub>T</sub> = 0.1 μF	T <sub>A</sub> = 125°C, –55°C	–11		11	ns/°C
t <sub>ch</sub>	Capacitor charge time (astable)	4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>TA</sub> = R <sub>TB</sub> = 1 kΩ, C <sub>T</sub> = 0.1 μF	T <sub>A</sub> = 25°C, 125°C, –55°C	120		156	μs
		4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>TA</sub> = R <sub>TB</sub> = 100 kΩ, C <sub>T</sub> = 0.1 μF		11.30		15	ms
t <sub>dis</sub>	Capacitor discharge time (astable)	4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>TA</sub> = R <sub>TB</sub> = 1 kΩ, C <sub>T</sub> = 0.1 μF	T <sub>A</sub> = 25°C, 125°C, –55°C	57.50		80	μs
		4.5 V ≤ V <sub>CC</sub> ≤ 16.5 V, R <sub>TA</sub> = R <sub>TB</sub> = 100 kΩ, C <sub>T</sub> = 0.1 μF		5.40		7.70	ms

## ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = 4.5\text{ V}$  to  $16.5\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta t_{ch} / \Delta V_{CC}$	Drift in capacitor charge time versus change in supply voltage (astable)	$\Delta V_{CC} = 12\text{ V}$ , $R_{TA} = R_{TB} = 1\text{ k}\Omega$ , $C_T = 0.1\text{ }\mu\text{F}$	$T_A = 25^\circ\text{C}$			
			–820		820	ns/V
$\Delta t_{ch} / \Delta T$	Temperature coefficient of capacitor charge time (astable)	$\Delta V_{CC} = 16.5\text{ V}$ , $R_{TA} = R_{TB} = 1\text{ k}\Omega$ , $C_T = 0.1\text{ }\mu\text{F}$	$T_A = 125^\circ\text{C}, -55^\circ\text{C}$			
			–68		68	ns/°C
$t_{res}$	Reset time	$V_{CC} = 16.5\text{ V}$	$T_A = 25^\circ\text{C}, -55^\circ\text{C}$		1.50	$\mu\text{s}$
			$T_A = 125^\circ\text{C}$		2	



- See datasheet for absolute maximum and minimum recommended operating conditions.
- Silicon operating life design goal is 10 years at  $105^\circ\text{C}$  junction temperature (does not include package interconnect life).

**Figure 1. SE555 8/JG Package Operating Life Derating Chart**

## TYPICAL CHARACTERISTICS

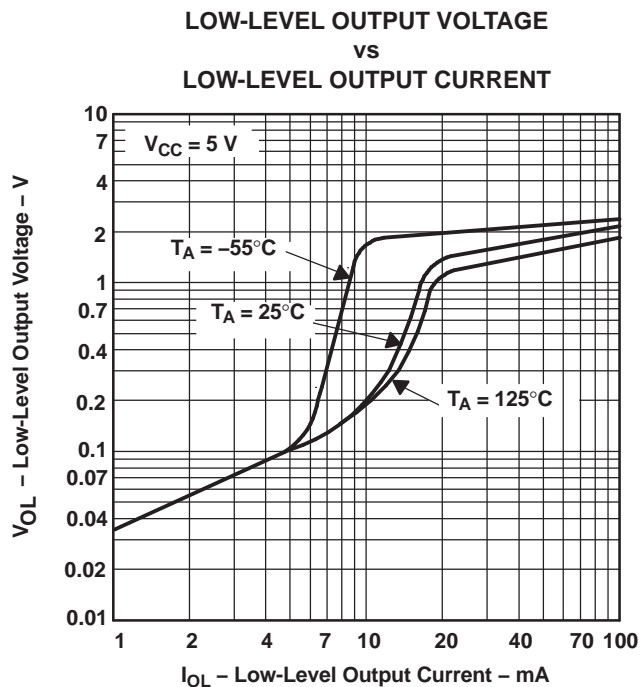


Figure 2.

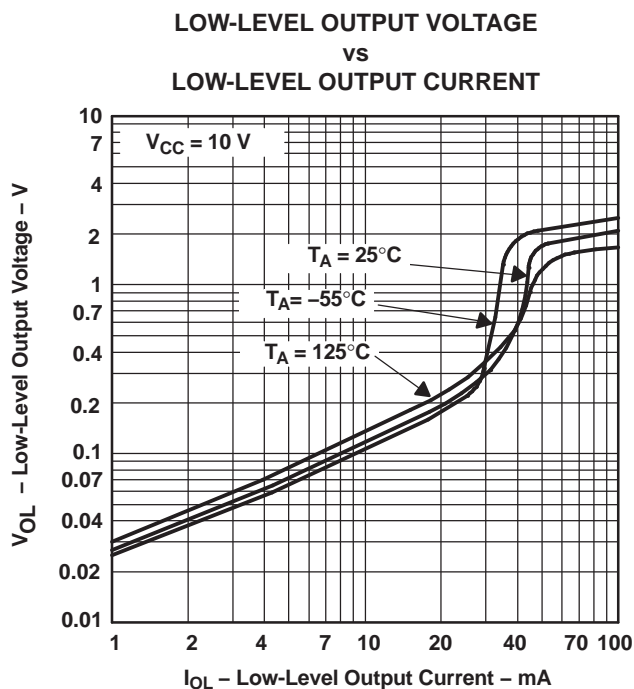


Figure 3.

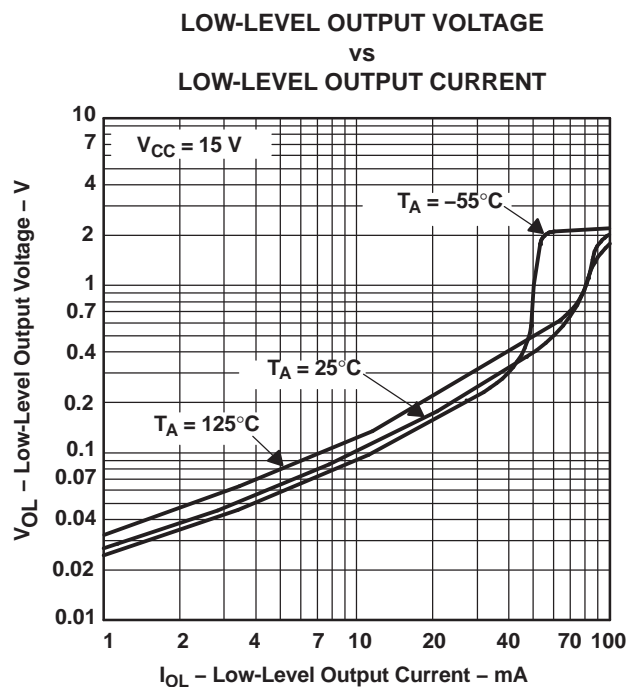


Figure 4.

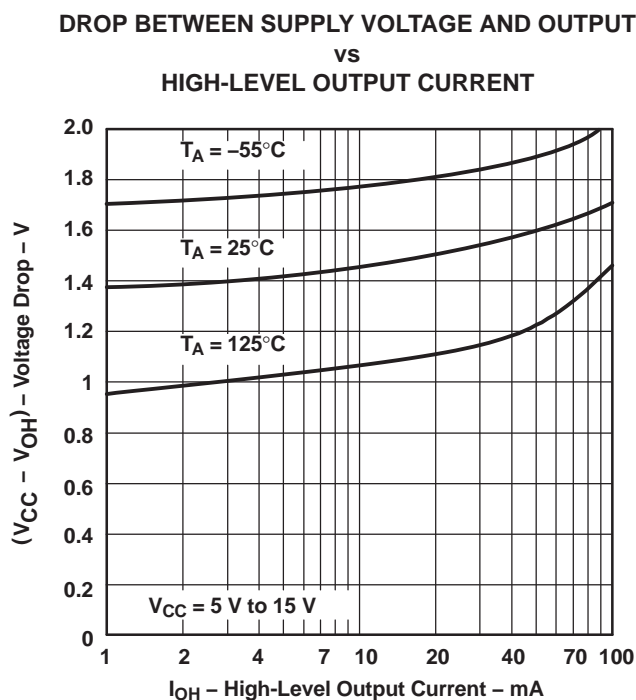


Figure 5.

# TYPICAL CHARACTERISTICS (continued)

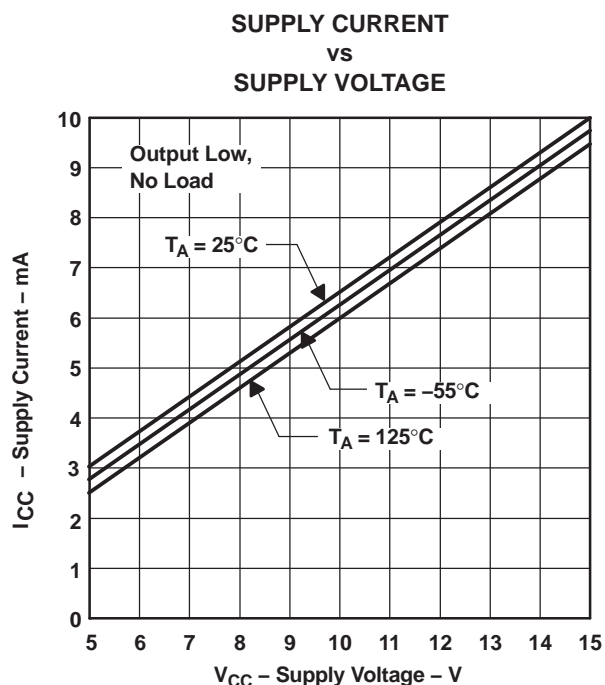


Figure 6.

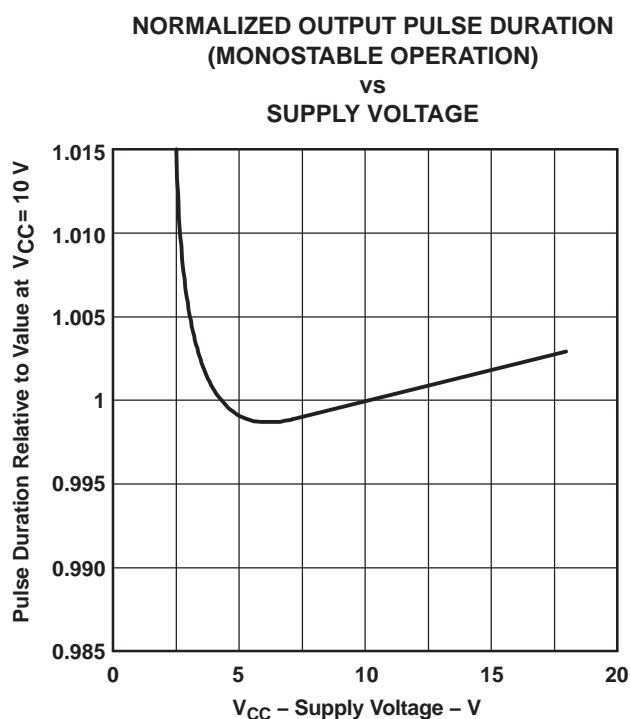


Figure 7.

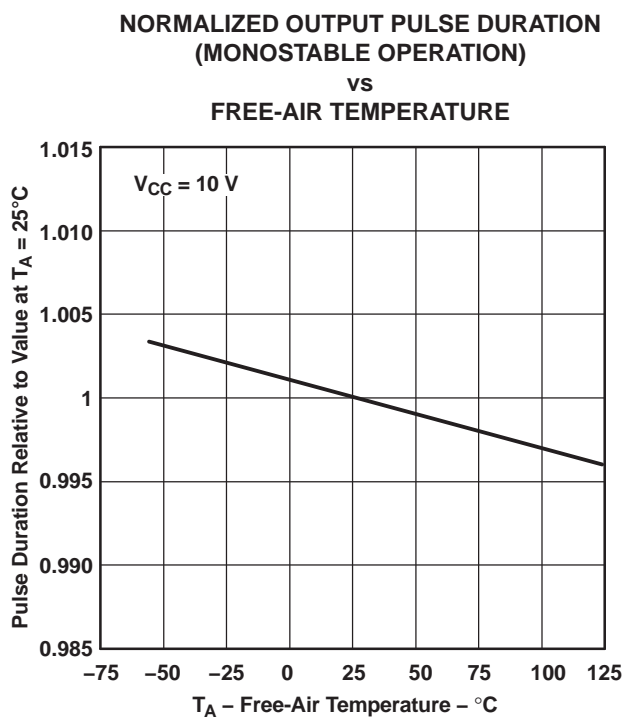


Figure 8.

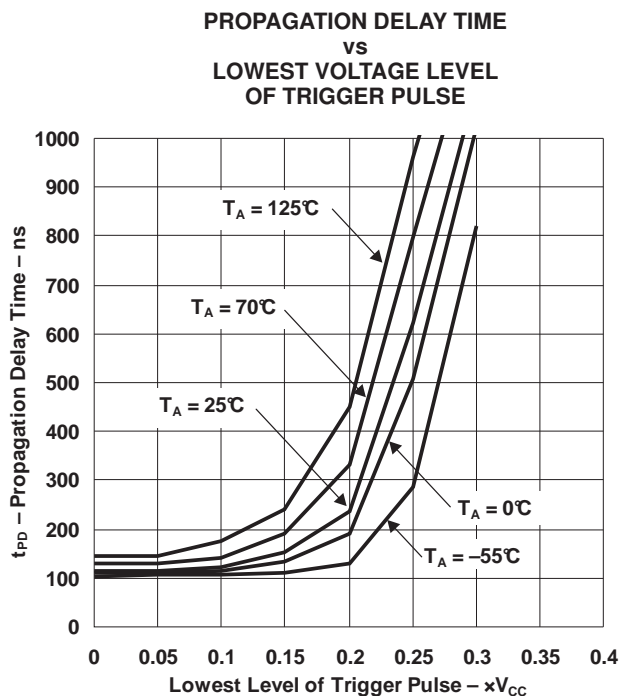
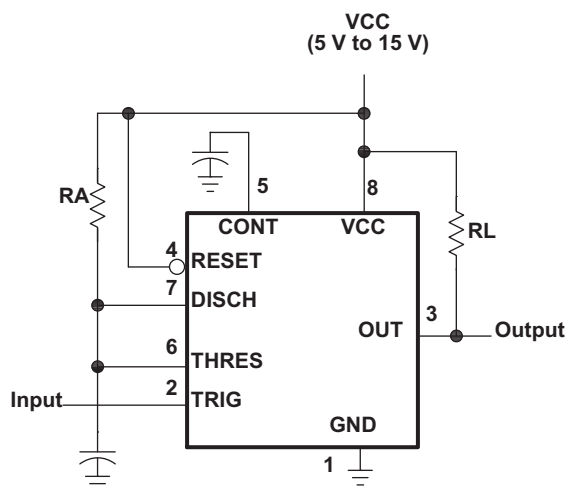


Figure 9.

## APPLICATION INFORMATION

### Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 10. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ( $\overline{Q}$  goes low), drives the output high, and turns off Q1. Capacitor C then is charged through  $R_A$  until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ( $\overline{Q}$  goes high), drives the output low, and discharges C through Q1.



**Figure 10. Circuit for Monostable Operation**

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately  $t_w = 1.1R_A C$ . Figure 12 is a plot of the time constant for various values of  $R_A$  and C. The threshold levels and charge rates both are directly proportional to the supply voltage,  $V_{CC}$ . The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to  $V_{CC}$ .



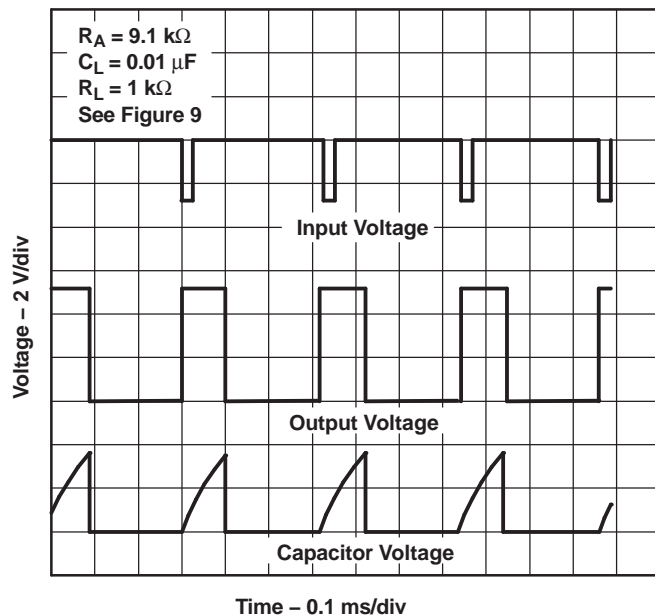


Figure 11. Typical Monostable Waveforms

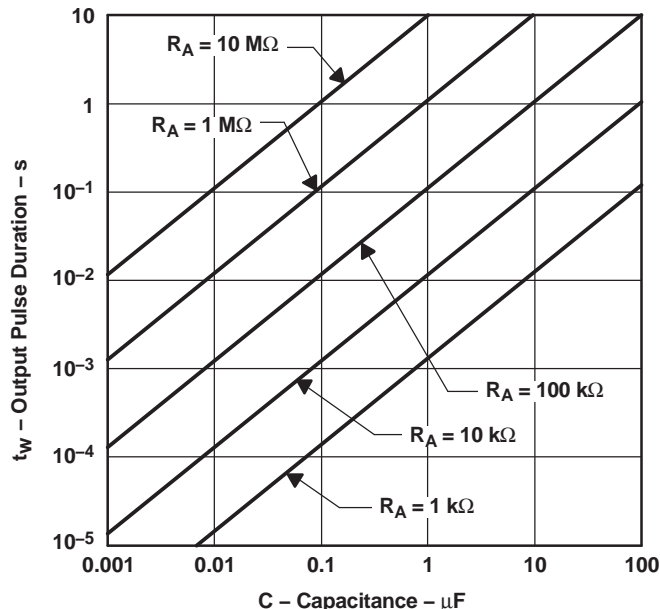
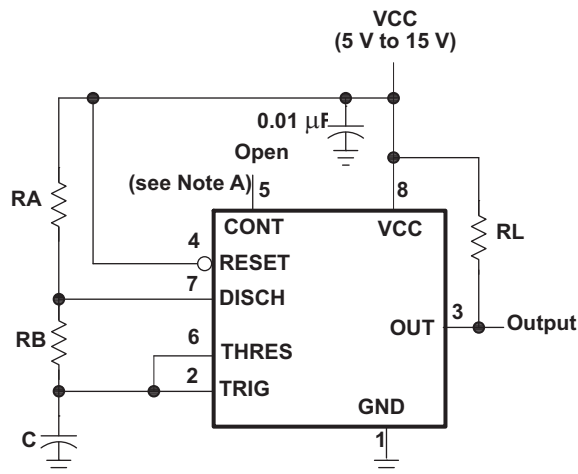


Figure 12. Output Pulse Duration vs Capacitance

## Astable Operation

As shown in Figure 13, adding a second resistor,  $R_B$ , to the circuit of Figure 10 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor  $C$  charges through  $R_A$  and  $R_B$  and then discharges through  $R_B$  only. Therefore, the duty cycle is controlled by the values of  $R_A$  and  $R_B$ .

This astable connection results in capacitor  $C$  charging and discharging between the threshold-voltage level ( $0.67 \times V_{CC}$ ) and the trigger-voltage level ( $0.33 \times V_{CC}$ ). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 13. Circuit for Astable Operation

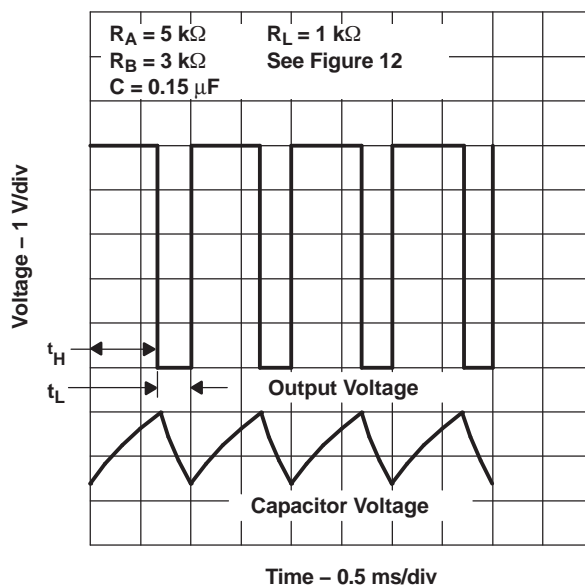


Figure 14. Typical Astable Waveforms

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration  $t_H$  and low-level duration  $t_L$  can be calculated as follows:

$$t_H = 0.693 (R_A + R_B) C \quad (1)$$

$$t_L = 0.693 (R_B) C \quad (2)$$

Other useful relationships are shown in the following equations.

$$\text{period} = t_H + t_L = 0.693 (R_A + 2R_B) C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B) C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

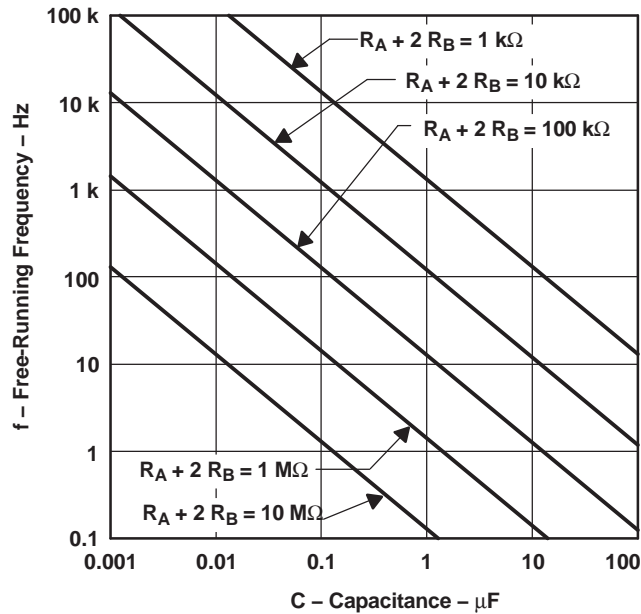
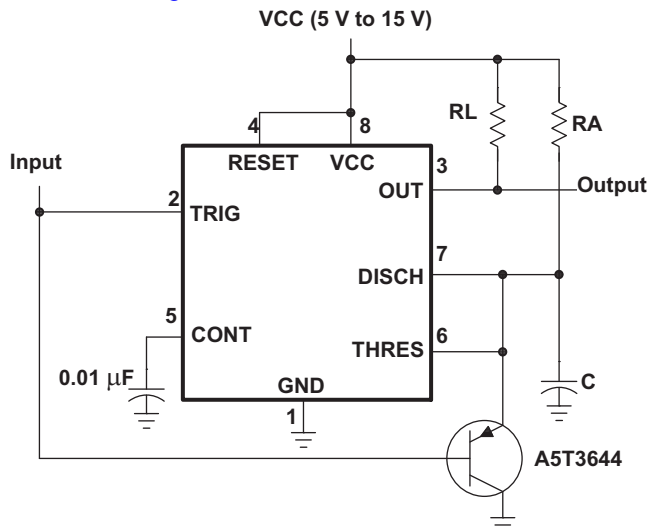


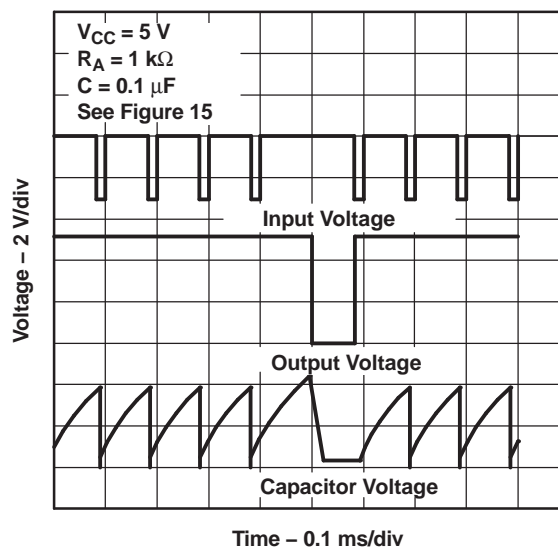
Figure 15. Free-Running Frequency

## Missing-Pulse Detector

The circuit shown in Figure 16 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 17.



**Figure 16. Circuit for Missing-Pulse Detector**



**Figure 17. Completed Timing Waveforms for Missing-Pulse Detector**

## Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of [Figure 10](#) can be made to operate as a frequency divider. [Figure 18](#) shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

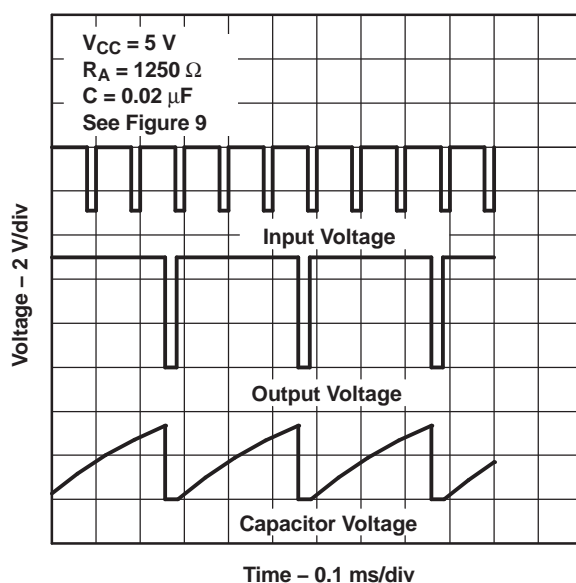
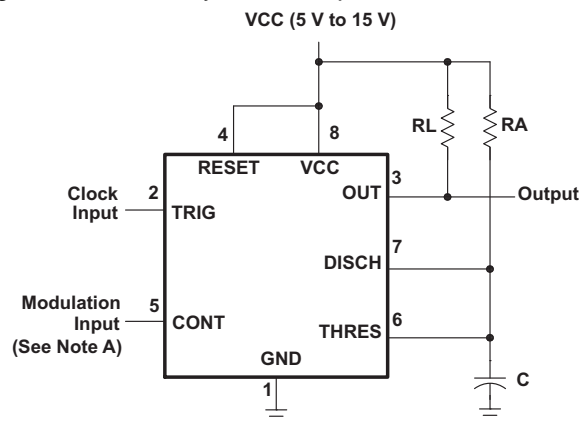


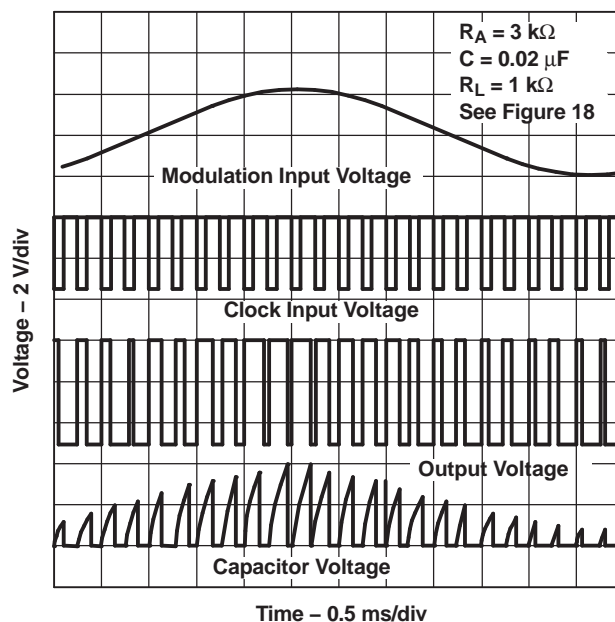
Figure 18. Divide-by-Three Circuit Waveforms

## Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 19 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 20 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

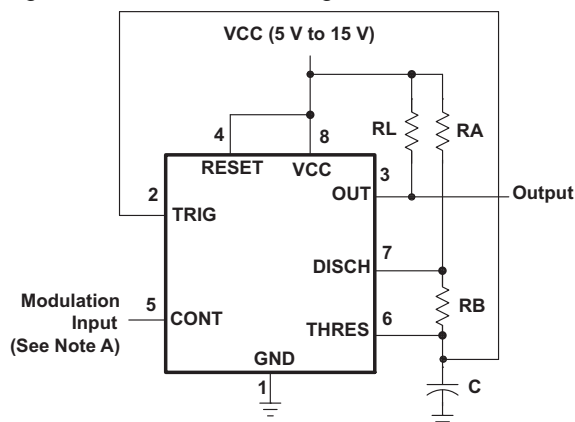


**Figure 19. Circuit for Pulse-Width Modulation**

**Figure 20. Pulse-Width-Modulation Waveforms**

## Pulse-Position Modulation

As shown in Figure 21, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 22 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

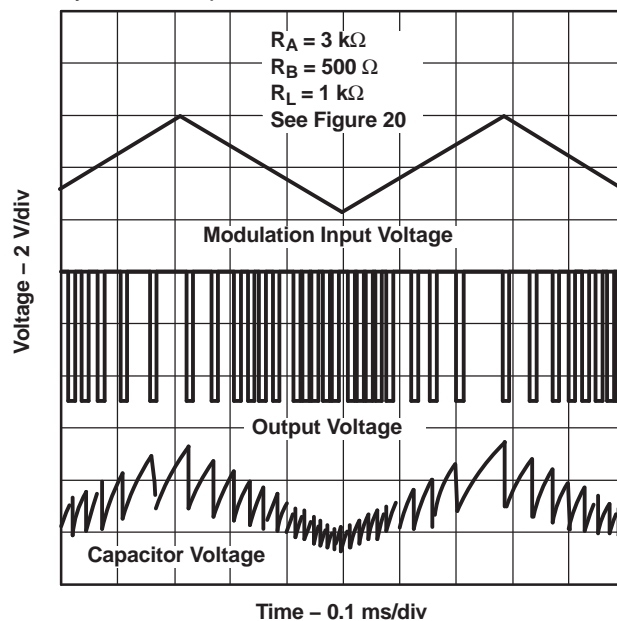
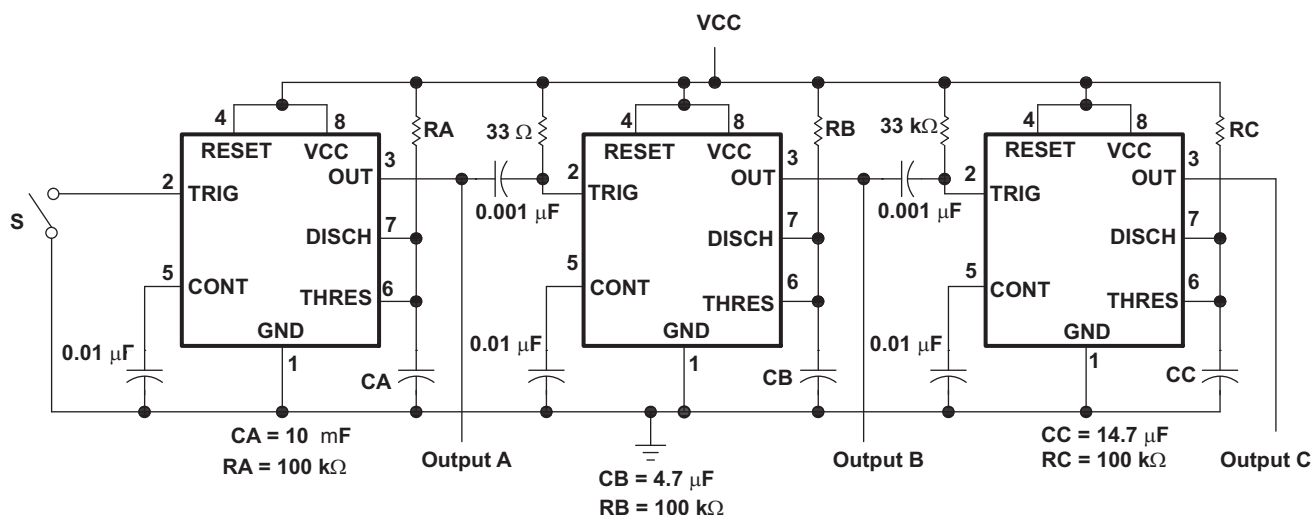


Figure 21. Circuit for Pulse-Position Modulation

Figure 22. Pulse-Position-Modulation Waveforms

## Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 23 shows a sequencer circuit with possible applications in many systems, and Figure 24 shows the output waveforms.



NOTE A: S closes momentarily at  $t = 0$ .

Figure 23. Sequential Timer Circuit

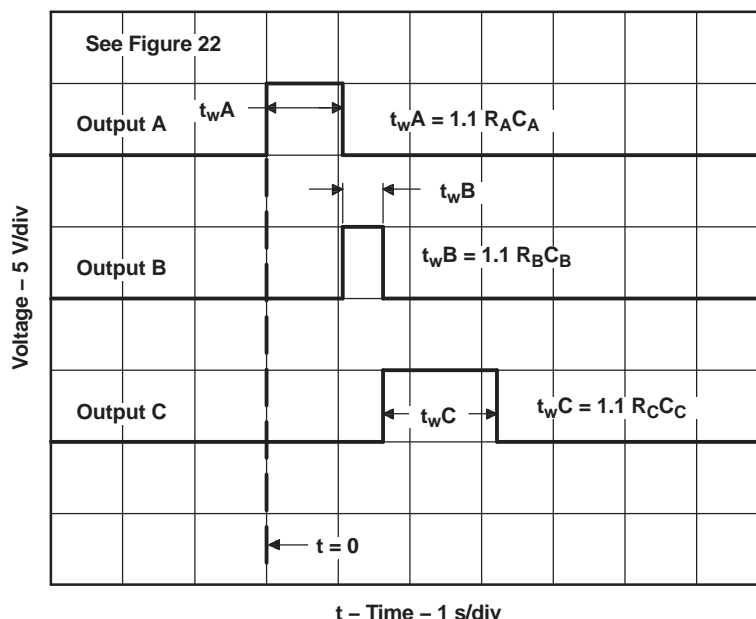


Figure 24. Sequential Timer Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9855501VPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9855501VPA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SE555-SP :**

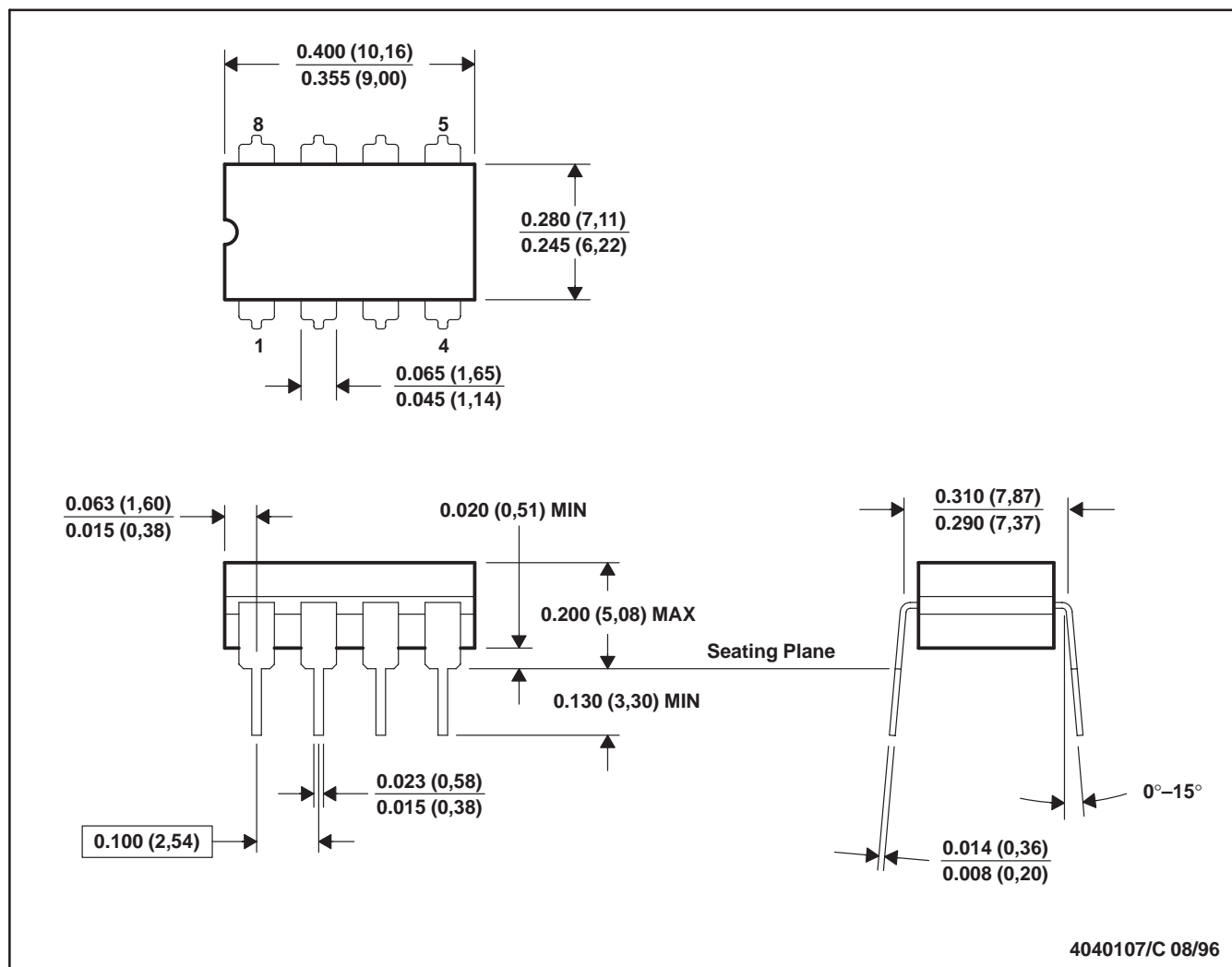
- Catalog: [SE555](#)
- Military: [SE555M](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## JG (R-GDIP-T8)

## CERAMIC DUAL-IN-LINE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification.
  - Falls within MIL STD 1835 GDIP1-T8

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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