TPL5000 具有看门狗功能的毫微功耗可编程定时器

1 特性

- 电源电压范围为 1.8V 至 5.0V
- 流耗 30nA（2.5V 时的典型值）
- 看门狗功能性
- 复位功能性
- 可选定时器间隔 1s 至 64s

2 应用

- 电池供电系统
- 能量采集系统
- 远程数据记录器
- 传感器节点
- 楼宇自动化
- 消费类电子产品
- 低功耗无线系统
- 安全平台

3 说明

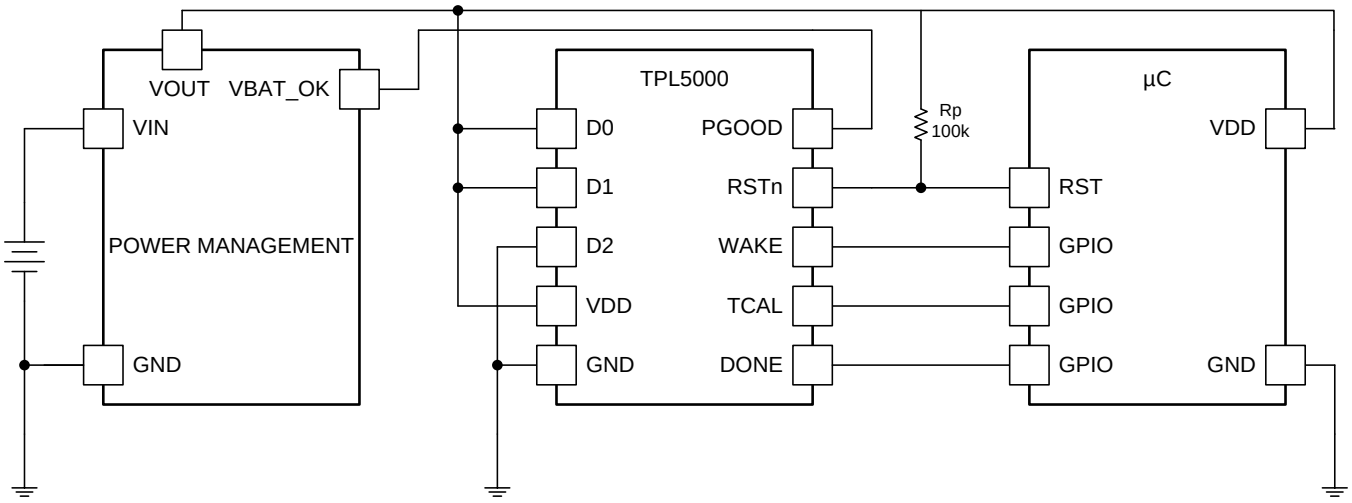
TPL5000 是一个长期定时器集成电路 (IC)，针对低功耗应用进行了优化。 TPL5000 能够替代一个微控制器 (µC) 的内部定时器，使 µC 能够保持在低功耗睡眠模式，而不用运行一个定时器，从而减少 60% 至 80% 的总功耗。 TPL5000 适用于中断驱动型应用，并且提供 1 秒至 64 秒的可选定时间隔。 出于安全考虑，某些标准（如 EN50271）要求配备看门狗功能。 TPL5000 无需增加功耗即可实现看门狗功能。 TPL5000 还可通过一个电源正常数字输入监视电池管理 IC，并根据需要复位微控制器。 此器件采用 10 引脚超薄小外形尺寸 (VSSOP) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPL5000	VSSOP (10)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化应用电路原理图



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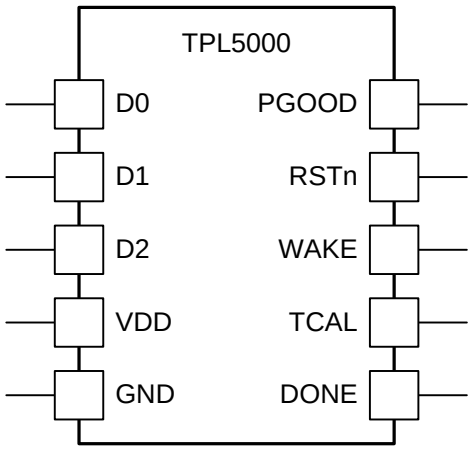
5 修订历史记录

Changes from Revision A (July 2013) to Revision B **Page**

- Added *ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section,* and *Mechanical, Packaging,* and *Orderable Information section* ... 3

6 Pin Configuration and Functions

10-Lead
VSSOP
Top View



Pin Functions

PIN		DESCRIPTION	APPLICATION INFORMATION
NAME	NO.		
D0	1	Logic Input to set period delay (t_{DP})	Connect to either GND (low logic value) or VDD (high logic value)
D1	2	Logic Input to set period delay (t_{DP})	Connect to either GND (low logic value) or VDD (high logic value)
D2	3	Logic Input to set period delay (t_{DP})	Connect to either GND (low logic value) or VDD (high logic value)
VDD	4	Supply voltage	
GND	5	Ground	
DONE	6	Logic Input for watchdog functionality	
TCAL	7	Short duration pulse output for estimation of TPL5000 timer delay.	
WAKE	8	Timer output signal generated every t_{DP} period.	
RSTn	9	Reset Output (open drain output)	
PGOOD	10	Digital power good input	

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply Voltage	–0.3	6.0	V
Input Voltage(2)	–0.3	VDD + 0.3	V
Voltage between any two pins		VDD + 0.3	V
Input Current on any pin	–5	5	mA
Operating Temperature, T_A	–40	105	
Junction Temperature, T_J(3)		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When the input voltage (V_{IN}) at any pin exceeds the power supply (V_{DD}), the current on that pin must not exceed 5 mA and must not exceed 6.0 V.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is PDMAX = ($T_{J(MAX)}$ - T_A)/ θJA. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.0	V
Temperature Range	-40	105	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPL5000 VSSOP 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	196.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics(1)

Specifications are for $T_A = T_J$ = 25°C, VDD-GND=2.5 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY						
IVDD	Supply current(4)	PGOOD = VDD		30	50	nA
		PGOOD = GND		12		nA
TIMER						
t_{DP}	Timer Delay Period			1, 2, 4, 8, 10, 16, 32, 64		s
	Timer Delay drift over life time(5)			0.06%		
	Timer Delay drift over temperature			400		ppm/°C
t_{CAL}	Calibration pulse width		14.063	15.625	17.188	ms
	t_{DP} to t_{CAL} matching error(6)	VDD ≤ 3.0 V			0.1	
t_{DONE}	DONE Pulse width (6)		100			ns
t_{RSTn}	RSTn Pulse width			15.625		ms
t_{WAKE}	WAKE Pulse width			31.25		ms
DIGITAL LOGIC LEVELS						
VIH	Logic High Threshold	PGOOD, DONE	0.7xVDD			V
VIL	Logic Low Threshold	PGOOD, DONE			0.3xVDD	V
VOH	Logic output High Level	WAKE, TCAL Iout = 100 uA	VDD-0.3			V
		WAKE, TCAL Iout = 1 mA	VDD-0.7			V
VOL	Logic output Low Level	WAKE, TCAL Iout = -100 uA			0.3	V
		WAKE, TCAL Iout = -1 mA			0.7	V
VOL_{RSTn}	RSTn Logic output Low Level	IOL= -1 mA			0.3	V
IOH_{RSTn}	RSTn High Level output current	VOH_{RSTn}=VDD		1		nA

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The supply current does not take in account load and pull-up resistor current. Input pins are at GND or VDD.
(5) Operational life time test procedure equivalent to10 years.
(6) Ensured by design.

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
tr_{TCAL}	Rise Time TCAL	Capacitive load 15 pF		50		ns
$tf_{TCAL,}$	Fall Time TCAL	Capacitive load 15 pF		50		ns
$tr_{RSTn,}$	Rise Time RSTn	Capacitive load 15 pF, Rpull-up 100Kohm		4		ns
$tf_{RSTn,}$	Fall Time RSTn	Capacitive load 15 pF, Rpull-up 100Kohm		50		ns
tr_{WAKE}	Rise Time WAKE	Capacitive load 15 pF		50		ns
tf_{WAKE}	Fall Time WAKE	Capacitive load 15 pF		50		ns
tD_{DONE}	DONE to RSTn or WAKE delay	Min delay		100		ns
		Max delay		t_{DP}-5*t_{CAL}		ms
tD_{TCAL}	TCAL to RSTn or WAKE delay			t_{CAL}/2		ms

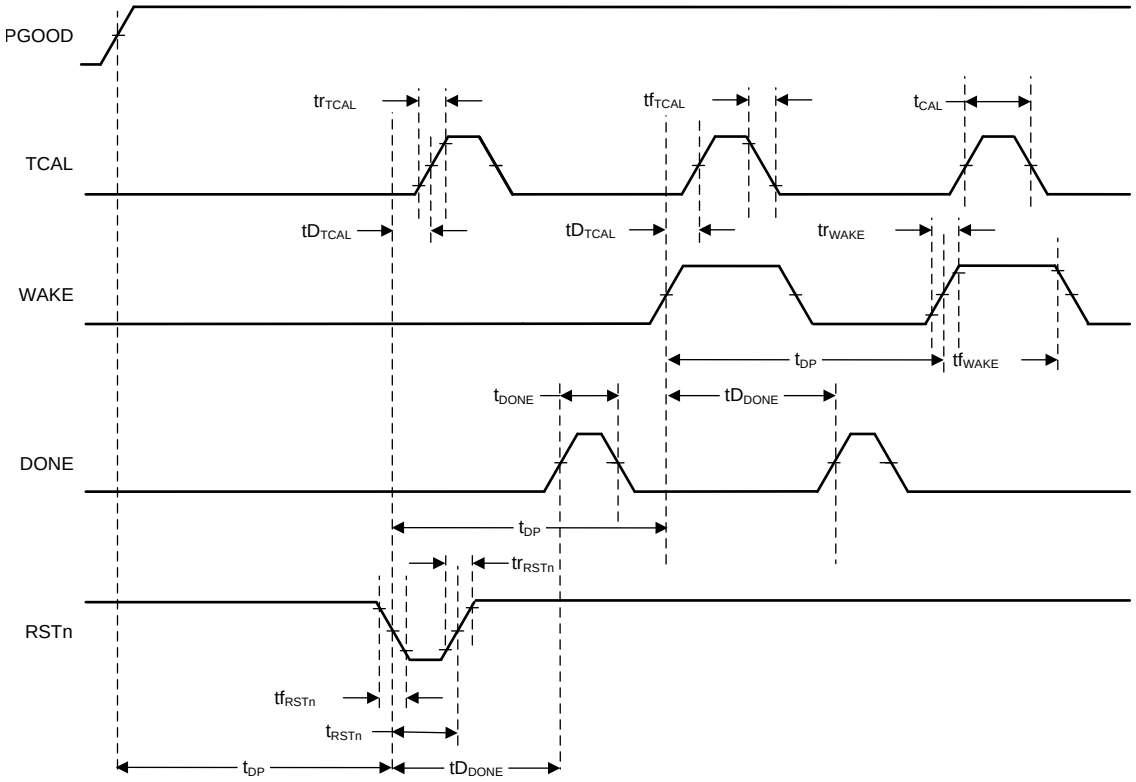


Figure 1. Timing Diagram

7.7 Typical Characteristics

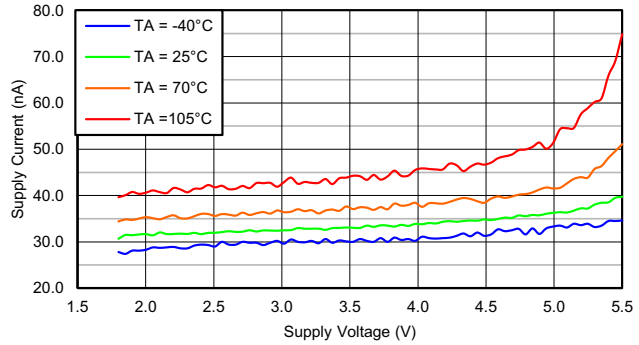


Figure 2. I_{DD} vs V_{DD}

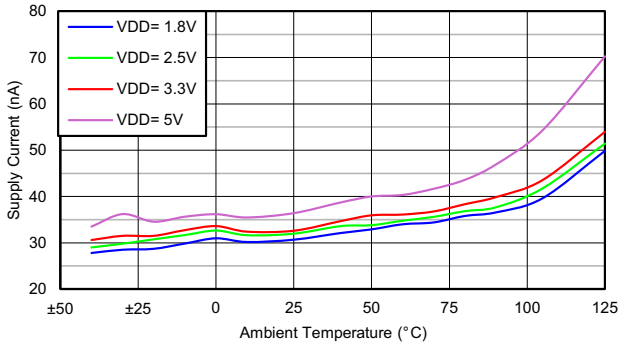


Figure 3. I_{DD} vs Temperature

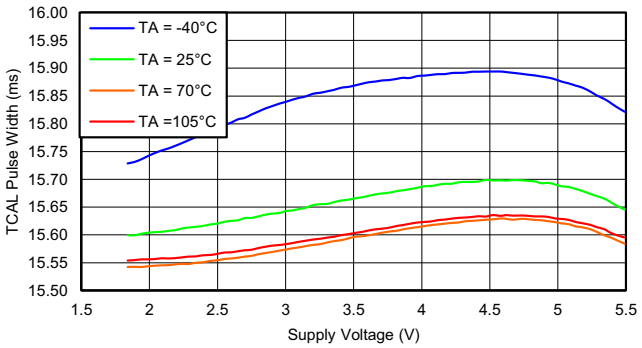


Figure 4. TCAL Pulse Width vs V_{DD}

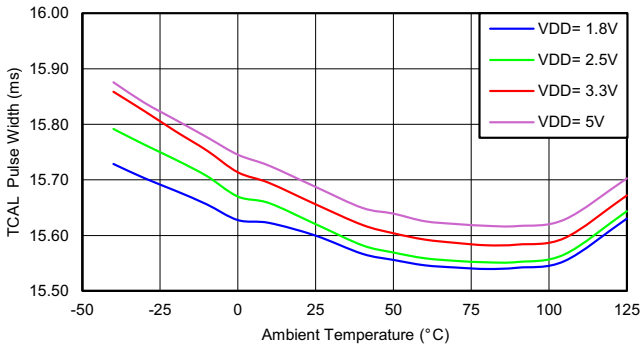


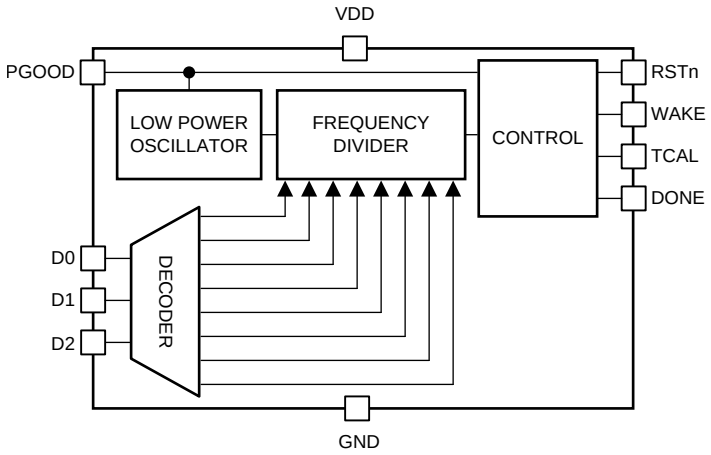
Figure 5. TCAL Pulse Width vs Temperature

8 Detailed Description

8.1 Overview

The TPL5000 is a long-term timer with a watchdog feature for low-power applications. The TPL5000 is designed for use in interrupt-driven applications and provides selectable timing from 1 s to 64 s. An additional supervisor feature is achieved through interfacing the TPL5000 to a power-management IC.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Supervisor Feature

A critical event that can corrupt the memory of a microcontroller is a voltage supply drop (supply lower than minimum operating range), and a reset of the microcontroller is mandatory if this occurs. Since the TPL5000 is the right choice in systems which stay most of the time in deep sleep, due to its ultra-low power consumption, it is fundamental that it takes into account the voltage drop events.

The TPL5000 implements a supervisory functionality when working with some power-management ICs which indicate the status of the supply voltage with a power-good or battery-good output. The supervisory functionality is enabled by simply connecting the Battery management power-good output to the TPL5000 PGOOD pin. If this feature is not used connect the PGOOD pin to VDD.

In case the power management IC detects a voltage drop, lowering the PGOOD line, while the microcontroller is in deep sleep mode (in which internal supervisors are usually off), the TPL5000 internally latches that event, and when the PGOOD returns to high, it sends out a RESET signal to the microcontroller at the end of the elapsed delay period.

Figure 6 shows the supervisor feature of the TPL5000. The sequence F, G is a standard sequence where the microcontroller is in deep sleep and a voltage supply drop occurs (which is highlighted by the PGOOD high to low transition). When PGOOD is high again, a reset pulse at the end of the delay period is sent to the microcontroller (arrow F), then the microcontroller executes its routine (memory has been reloaded upon reset) and sends the "DONE" signal.

Feature Description (continued)

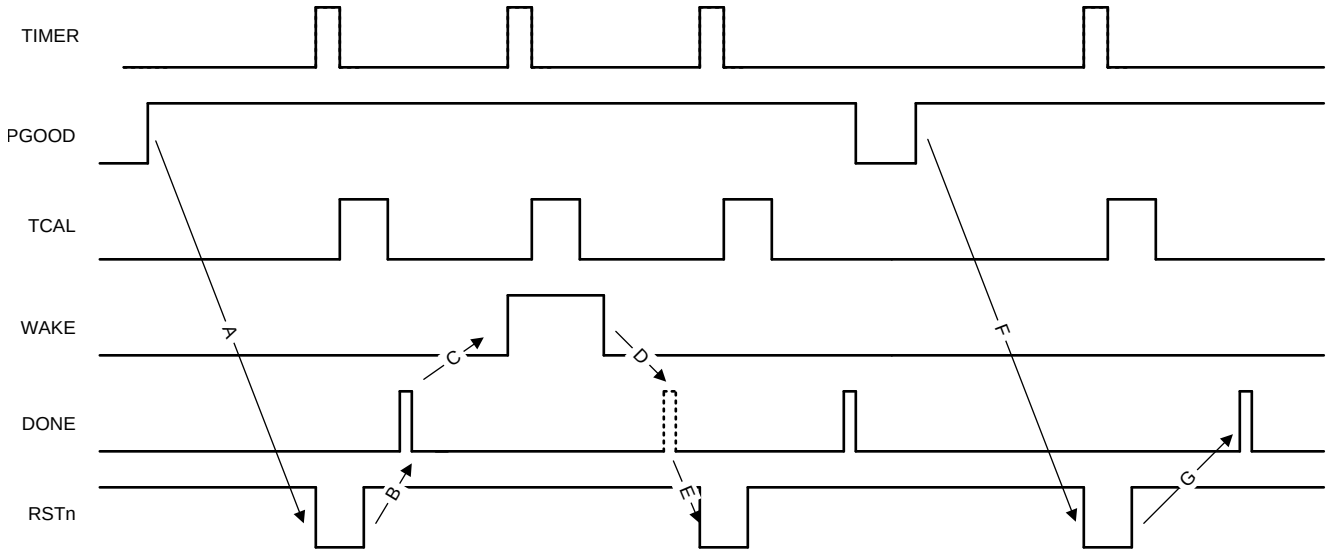


Figure 6. Watchdog and Supervisor Feature

8.3.1.1 Calibration Pulse

The TPL5000 is based on a ultra-low power oscillator which has a relatively low frequency and low accuracy; however, it shows very good cycle-to-cycle repeatability and very low temperature drift. In most of the applications, the accuracy of the oscillator is enough, but if a more accurate measure of the delay period is required, it is possible to measure the base period of the internal oscillator. A single pulse, which has the same duration as the base period of the internal oscillator, is present at the TCAL pin of the TPL5000. This pulse starts after a half period of the internal oscillator from either the falling edge of the RESET pulse, or the rising edge of the WAKE pulse.

A microcontroller connected to the TPL5000 can routinely measure the width of the TCAL pulse using a counter and an external crystal. Once the base period of the TPL5000 is measured, the actual time delay is calculated by multiplying the measured period by a factor, N (see Table 1), dependent on the nominal selected time delay.

The resolution and the accuracy of the measurement depend on the external crystal. Since the frequency of the internal oscillator of the TPL5000 is very stable, the measurement of the calibration pulse is suggested only when a high gradient of ambient temperature is observed. The measurement of the TCAL pulse is useful in battery-powered applications that implement a precise battery life counter in the microcontroller.

8.3.1.2 Overview of the Timing Signals: WAKE, RSTN, TCAL and DONE

Figure 7 shows the timing of WAKE, RSTn, and TCAL with respect to DONE. The frame, A, shows a typical sequence after the PGOOD, low to high, transition. As soon as PGOOD is high, the internal oscillator is powered ON. At the end of the delay period (t_{DP}), a reset signal (RSTn), followed by a calibration pulse, TCAL, is sent out. The calibration pulse starts after a half period of the internal oscillator from the falling edge of the reset, and lasts one internal oscillator period.

The frame, B, shows a standard sequence. A "DONE" signal has been received in the previous delay period, so at the end of the next delay period, a "WAKE", followed by a calibration pulse, is sent out. The WAKE signal stays high for 2 internal oscillator periods. The calibration pulse starts after a half period of the internal oscillator from the rising edge of the WAKE signal, and lasts one internal oscillator period. In this frame, the TPL5000 receives a "DONE" signal before the end of the delay period.

The frame, C, still shows a standard sequence, but in this case, the TPL5000 receives the DONE signal when both WAKE and TCAL pulses are still high. As soon as the TPL5000 recognizes the DONE resets the counter and puts WAKE and TCAL in the default condition (both signal low).

Feature Description (continued)

The frame, D, shows a typical PGOOD, high to low transition. As soon as PGOOD is low, the internal oscillator is powered OFF and the digital output pins, TCAL, RSTn, and WAKE, are asynchronously reset by the falling edge of the PGOOD signal, such that TCAL and WAKE reset at low logical values, while RSTn resets at a high logical value.

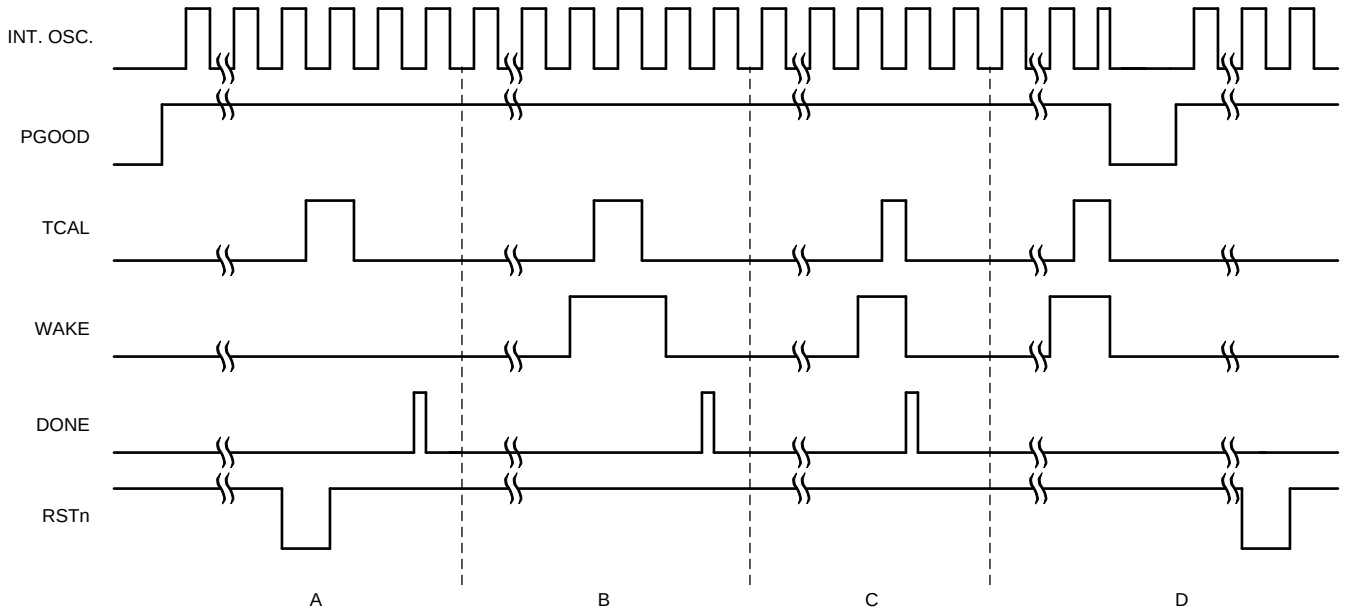


Figure 7. Timing PGOOD, WAKE, RSTN, TCAL

8.3.1.3 Watchdog Feature

Most of the microcontroller-based systems need to be self-reliant; if the software hangs for any reason, the microcontroller must be reset. The TPL5000 can provide this functionality by connecting a microcontroller programmable output pin to the DONE input pin. If the DONE line does not toggle within the selected delay period, then the microcontroller is not operating properly and must be reset.

The TPL5000 recognizes a valid DONE signal as a low to high transition; if two DONE signals are received within the delay period the second signal is ignored.

In the TPL5000, the watchdog window and the delay period are equivalent. A valid "DONE" signal resets the watchdog counter only, and not the delay time counter. A PGOOD low to high transition clears both the watchdog and delay time counters.

Figure 6 shows the watchdog feature of the TPL5000. The sequence A, B, C is a standard sequence with the microcontroller working properly. In this normal sequence, the microcontroller sends a valid "DONE" (arrow B) before the end of the delay period. The sequence C, D ,E is an anomalous sequence in which the microcontroller is not in a valid state, and it does not send the DONE signal (dashed pulse) before the end of the delay period. The TPL5000 determines the microcontroller is hung and sends a RESET signal (arrow E) when the period delay has elapsed.

8.3.1.4 Different Utilizations of the TPL5000

When either the watchdog or the supervisor feature of the TPL5000 are not required, it is possible to disable them reducing the interconnections between the TPL5000 and the microcontroller.

Connecting the DONE pin either to GND or to TCAL pin disables the watchdog feature. If connected to GND, the TPL5000 only sends a reset pulse when the time delay elapses. If DONE is connected to TCAL, the TPL5000 sends out just one RESET pulse after a PGOOD low to high transition, when the time delay elapses and then WAKE pulses when the successive time delay elapses.

Connecting the PGOOD pin to the supply pin of the TPL5000 disables the supervisor feature.

Feature Description (continued)

8.3.2 Configuration and Interface

The time interval between 2 adjacent WAKE pulses (or 2 adjacent RSTn pulses or RSTn and WAKE pulses) is selectable through 3 digital input pins (D0, D1, D2). These pins can be strapped to either VDD (1) or GND (0). Eight possible time delays can be selected, as shown in Table 1.

Table 1. Timer Delay Period

D2	D1	D0	Time (s)	Factor N
0	0	0	1	2^6
0	0	1	2	2^7
0	1	0	4	2^8
0	1	1	8	2^9
1	0	0	10	$10*2^6$
1	0	1	16	2^{10}
1	1	0	32	2^{11}
1	1	1	64	2^{12}

8.4 Device Functional Modes

The TPL5000 mode of operations are selected through the PGOOD pin. There are two factors to consider when the PGOOD pin is at a high-logic level or low-logic level. When the PGOOD pin is at a high-logic level, the TPL5000 works as a timer and conversely at a low-logic level the TLP5000 does not work as a timer. For best use of TPL5000 waiting for high-logic is necessary.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In battery powered applications the design of the system is driven by low current consumption. The TPL5000 is suitable in the applications where there is the needs to monitor environment conditions at fixed timer interval. Often in these applications the micro is kept on to enable the watchdog and to count the elapsed time. Some time due to the high frequency clock of the micro controllers special structure needs to be configured to count for long time (several seconds). The TPL5000 can do the same job burning only tens of nA.

9.2 Typical Application

The TPL5000 can be used in conjunction with environment sensors to build a low-power environment data-logger, such as an air quality data-logger. In this application due to the monitored phenomena the micro-controller and the front end of the sensor spend most of the time in idle state, waiting for the next working interval, usually few hundred of ms. The application is based on a micro-controller which represents the core of the data-logger, a front end for gas sensor, such as the LMP91000.

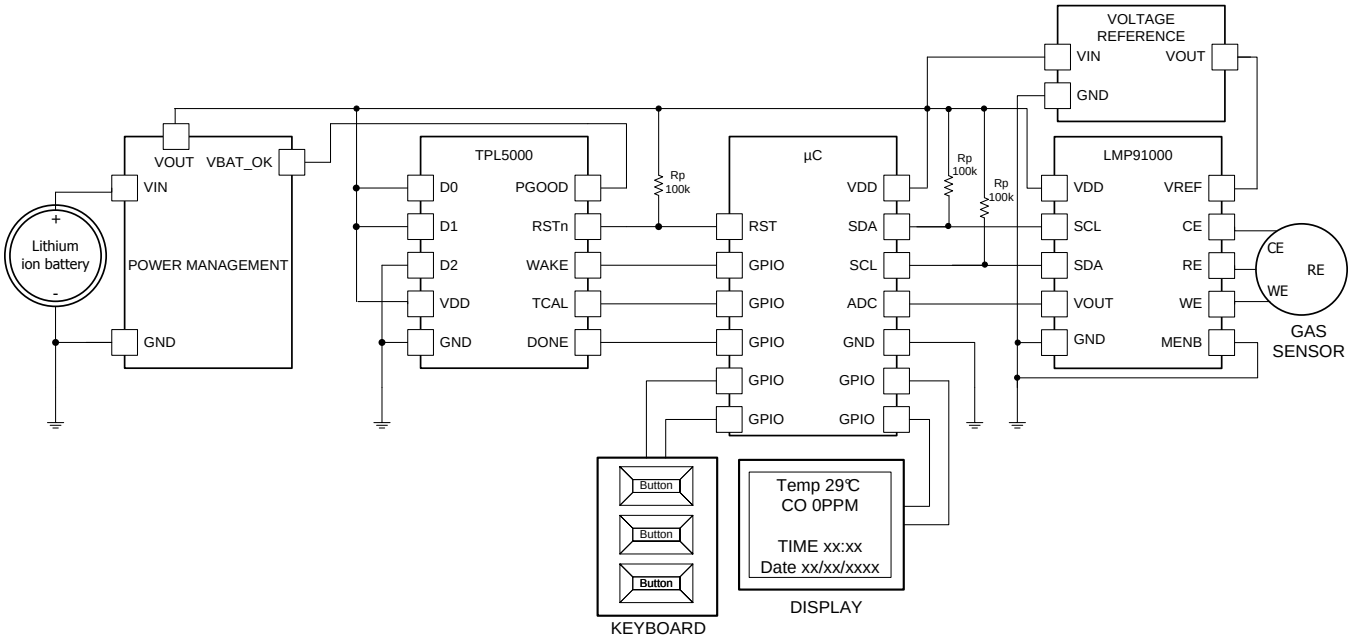


Figure 8. Data-logger

9.2.1 Design Requirements

The design is driven by the low current consumption constraint. The data are usually acquired on a rate that ranges between 1 s to 10 s. The highest necessity it the maximization of the battery life. The TPL5000 helps achieve that goal because it allows putting the micro-controller in its lowest power mode.

Typical Application (continued)

9.2.2 Detailed Design Procedure

When the focal constraint is the battery, the selection of a low power voltage reference, a micro-controller and display is mandatory. The first step in the design is the calculation of the power consumption of each device in the different mode of operations. An example is the LMP91000; the device has gas measurement mode, sleep mode and micro-controller in low-power mode which is normal operation. The different modes offer the possibility to select the appropriate timer interval which respect the application constraint and maximize the life of the battery.

9.2.3 Application Curve

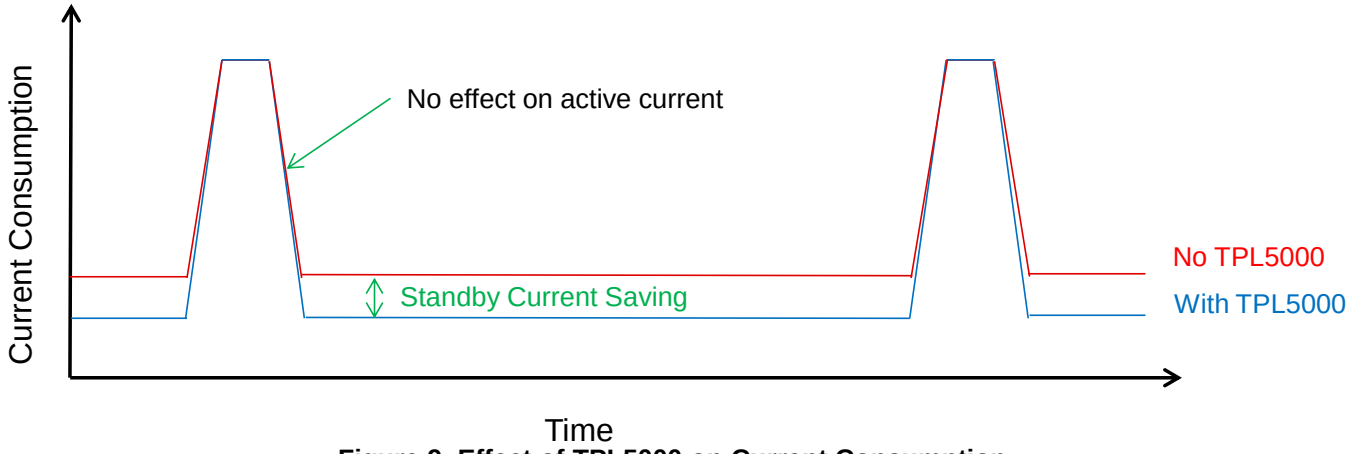


Figure 9. Effect of TPL5000 on Current Consumption

10 Power Supply Recommendations

The TPL5000 requires a voltage supply within 2.7 V and 5.5 V. A multilayer, ceramic-bypass X7R capacitor of 0.1µF between VDD and GND pin is recommended.

11 Layout

11.1 Layout Guidelines

The more sensitive pins of the TPL5000 are the digital input pins D0, D1, D2 to select the timer interval. It is mandatory to connect them to VDD or GND through short traces avoiding series resistance. It is mandatory to keep these pins far from traces of high frequency signals, such as clock or communication bus. Signal integrity of WAKE, RSTn and TCAL signal is achieved reducing parasitic capacitance on the traces between the TPL5000 and the micro-controller. In the application where the watchdog feature is not used, the DONE pin is required to be tied to TCAL pin.

11.2 Layout Example

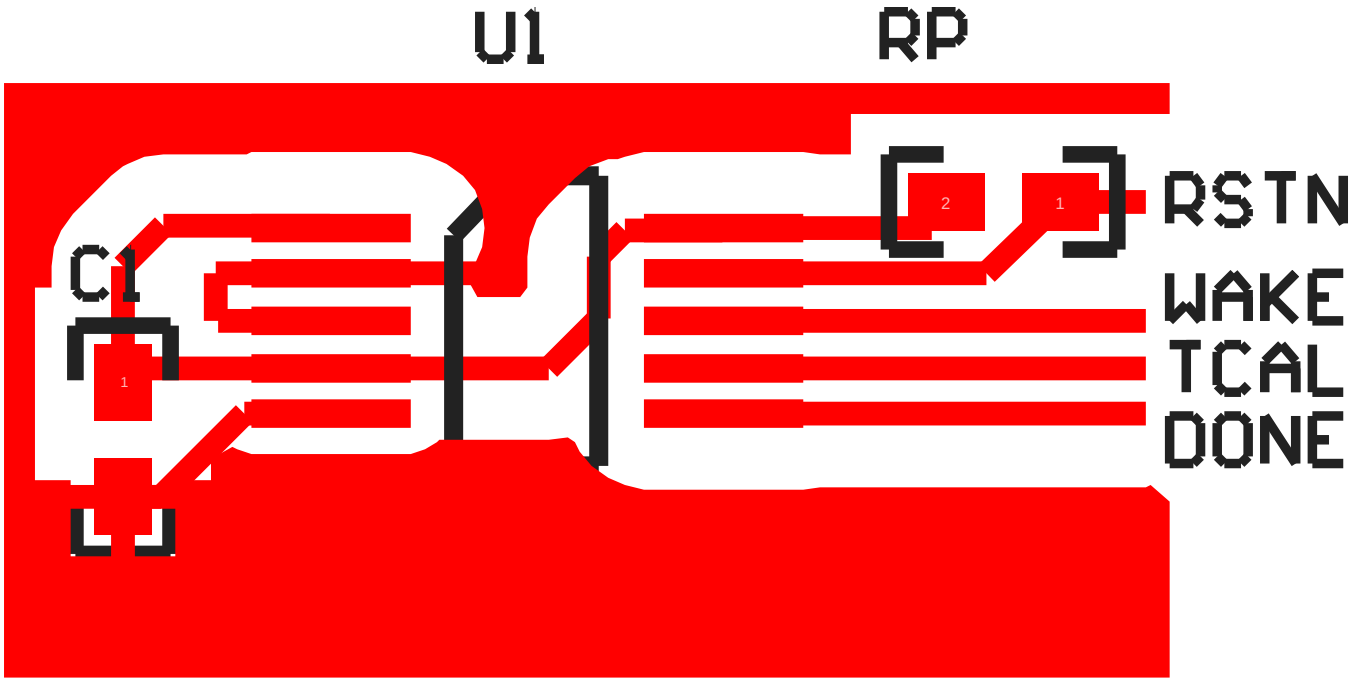


Figure 10. PCB Layout

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL5000DGSR	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	ARAA	Samples
TPL5000DGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	ARAA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

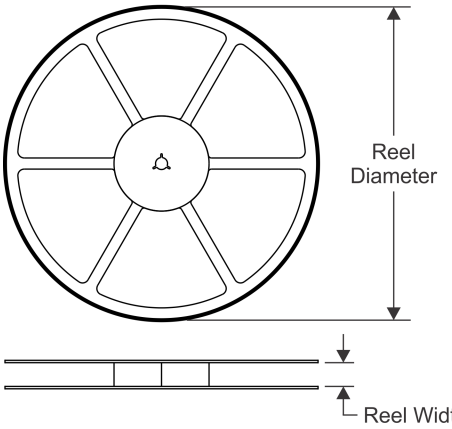
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

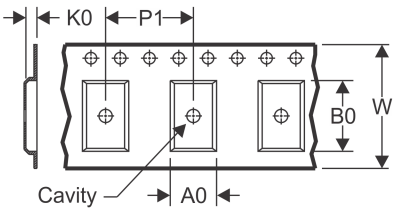
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

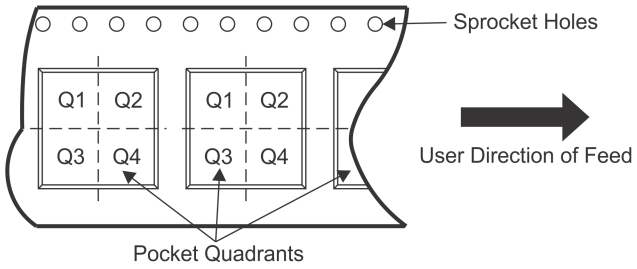


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

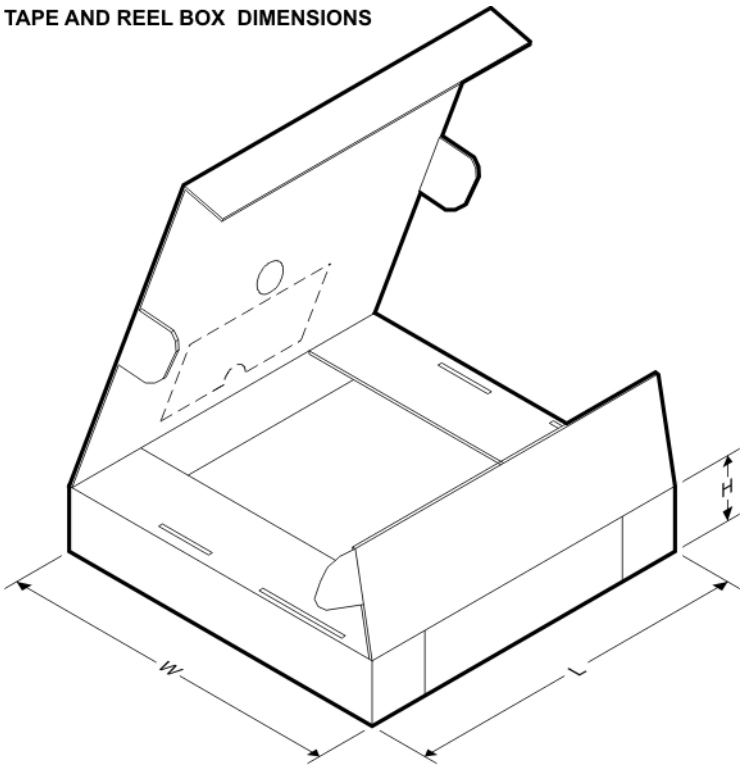
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5000DGSR	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPL5000DGST	VSSOP	DGS	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

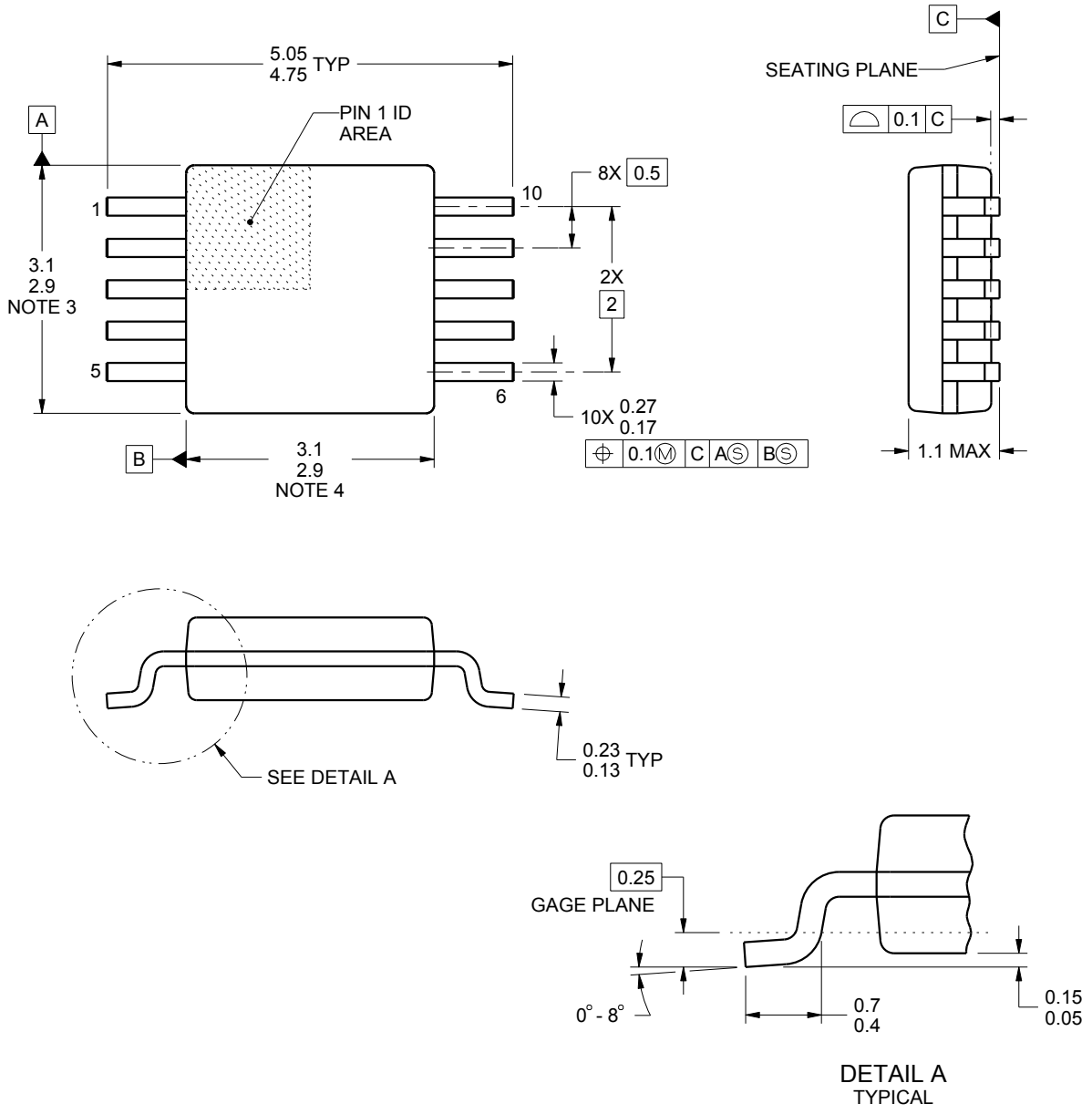
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5000DGSR	VSSOP	DGS	10	3500	367.0	367.0	35.0
TPL5000DGST	VSSOP	DGS	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

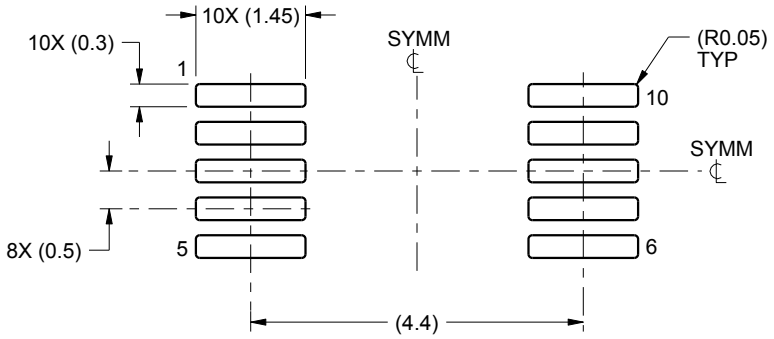
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

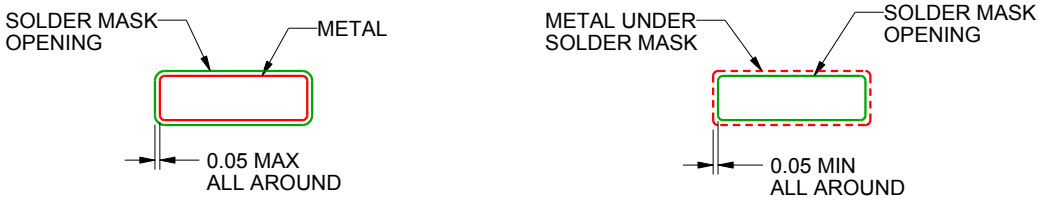


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

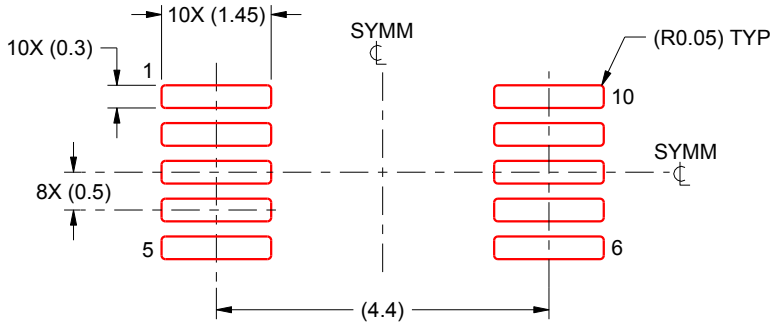


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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