CSD25484F4 –20V P 通道 FemtoFET™MOSFET

1 特性

- 低导通电阻
- 超低 Q_g 和 Q_{gd}
- 低阈值电压
- 超小型封装尺寸（0402 外壳尺寸）
  - 1.0mm × 0.6mm
- 超薄
  - 高度为 0.2mm
- 集成静电放电 (ESD) 保护二极管
  - 额定值 > 4kV 人体模型 (HBM)
  - 额定值 > 2kV 组件充电模式 (CDM)
- 无铅且无卤素
- 符合 RoHS 环保标准

2 应用范围

- 针对负载开关应用进行了 优化
- 针对通用开关应用进行了 优化
- 电池 应用
- 手持式和移动类 应用

3 说明

这款 80mΩ、–20V P 通道 FemtoFET™MOSFET 经过了设计和优化，能够最大限度减小许多手持式和移动类应用的 尺寸。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小 60% 以上。

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	1090		pC
Q_{gd}	栅极电荷（栅极到漏极）	150		pC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = –1.8V	405	mΩ
		V_{GS} = -2.5V	150	
		V_{GS} = –4.5V	93	
		V_{GS} = -8.0V	80	
$V_{GS(th)}$	阈值电压	-0.95		V

器件信息(1)

器件	数量	包装介质	封装	运输
CSD25484F4	3000	7 英寸卷带	Femto (0402) 1.00mm × 0.60mm 接合栅格阵列 (LGA)	卷带封装
CSD25484F4T	250			

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

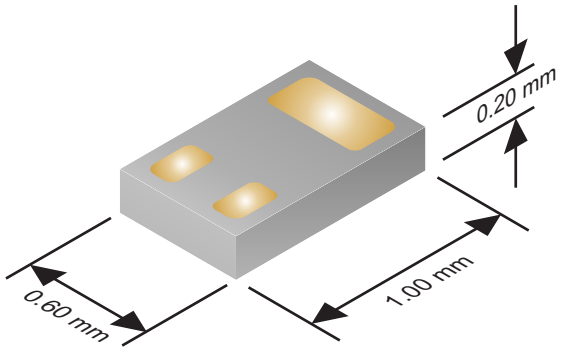
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-12	V
I_D	持续漏极电流(1)	-2.5	A
I_{DM}	脉冲漏极电流(1)(2)	–22	A
I_G	持续栅极钳位电流	-35	mA
	脉冲栅极钳位电流(2)	-350	
P_D	功率耗散(1)	500	mW
$V_{(ESD)}$	人体模型 (HBM)	4	kV
	带电器件模型 (CDM)	2	
T_J, T_{stg}	工作结温，储存温度	-55 至 150	°C

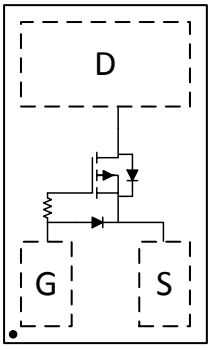
(1) 典型 $R_{\theta JA}$ = 85°C/W（当在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上将其安装在 1 平方英寸 (6.45cm^2)、2oz (0.071mm) 厚的铜焊盘上时）。

(2) 脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。

典型部件尺寸



顶视图



目录

1 特性 1
2 应用范围 1
3 说明 1
4 修订历史记录 2
5 **Specifications** 3
5.1 Electrical Characteristics 3
5.2 Thermal Information 3
5.3 Typical MOSFET Characteristics 4
6 器件和文档支持 7
6.1 接收文档更新通知 7
6.2 社区资源 7
6.3 商标 7
6.4 静电放电警告 7
6.5 Glossary 7
7 机械、封装和可订购信息 8
7.1 机械尺寸 8
7.2 推荐的最小 PCB 布局 9
7.3 推荐的模板布局 9

4 修订历史记录

Changes from Original (May 2015) to Revision A **Page**

- 已添加 将 *接收文档更新通知* 和 *社区资源* 部分添加到 *器件和文档支持* 7
- 更新了 *推荐的最小 PCB 布局* 和 *推荐的模板布局* 部分 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V			–50	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.7	–0.95	–1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		405	825	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.5 A		150	180	
		V_{GS} = –4.5 V, I_{DS} = –0.5 A		93	109	
		V_{GS} = –8 V, I_{DS} = –0.5 A		80	94	
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.5 A		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		175	230	pF
C_{oss}	Output capacitance			78	102	pF
C_{rss}	Reverse transfer capacitance			5.5	7.2	pF
R_G	Series gate resistance			20		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.5 A		1090	1415	pC
Q_{gd}	Gate charge gate-to-drain			150		pC
Q_{gs}	Gate charge gate-to-source			350		pC
$Q_{g(th)}$	Gate charge at V_{th}			210		pC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		1290		pC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.5 A, R_G = 10 Ω		9.5		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turnoff delay time			18		ns
t_f	Fall Time			8.5		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.5 A, V_{GS} = 0 V		–0.75		V
Q_{rr}	Reverse recovery charge	V_{DS}= –10 V, I_F = –0.5 A, di/dt = 100 A/μs		970		pC
t_{rr}	Reverse recovery time			7.5		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	85	°C/W
	Junction-to-ambient thermal resistance(2)	245	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

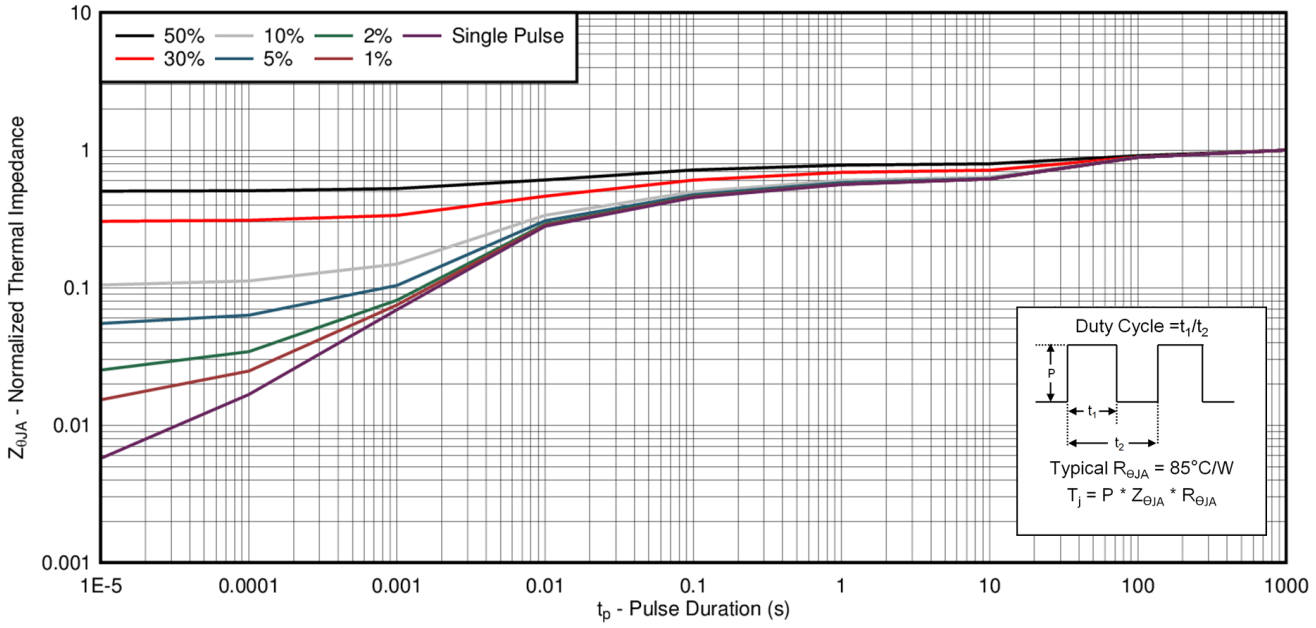


Figure 1. Transient Thermal Impedance

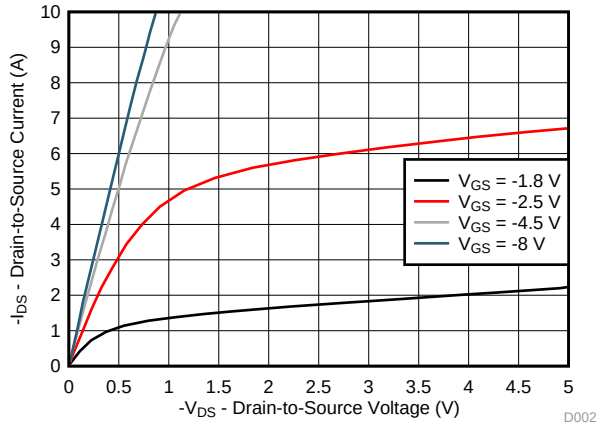


Figure 2. Saturation Characteristics

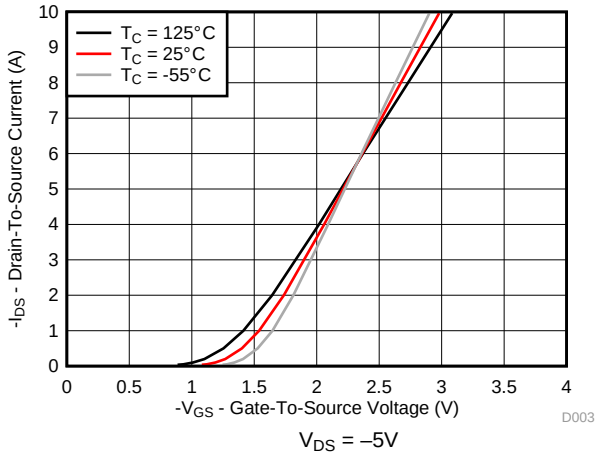


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

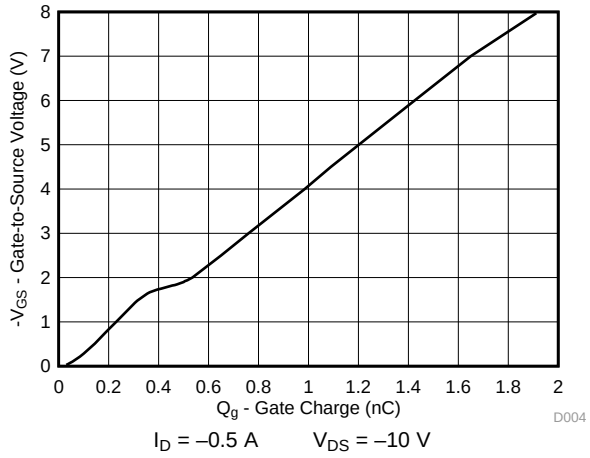


Figure 4. Gate Charge

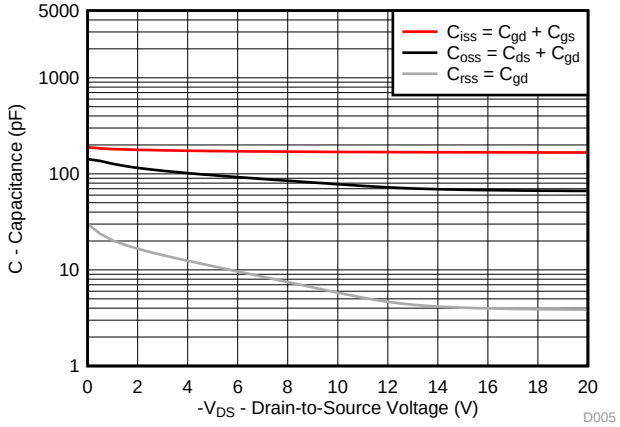


Figure 5. Capacitance

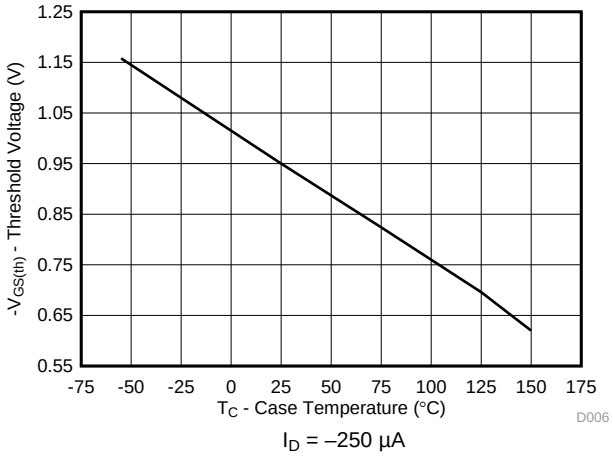


Figure 6. Threshold Voltage vs Temperature

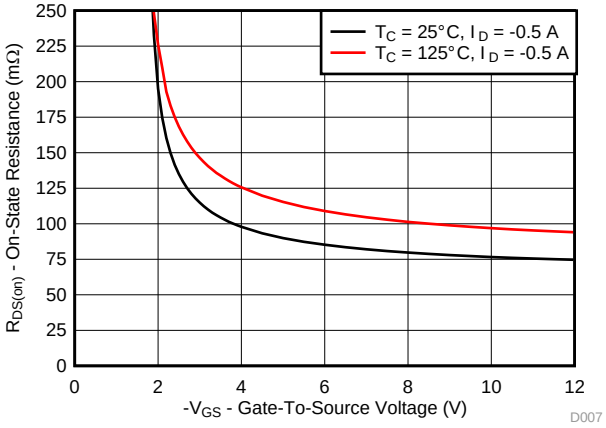


Figure 7. On-State Resistance vs Gate-to-Source Voltage

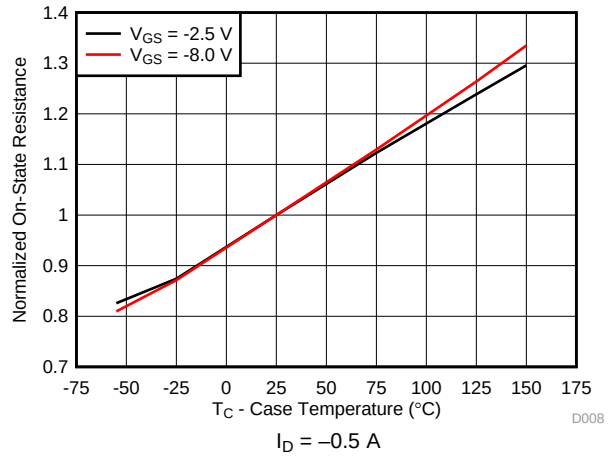


Figure 8. Normalized On-State Resistance vs Temperature

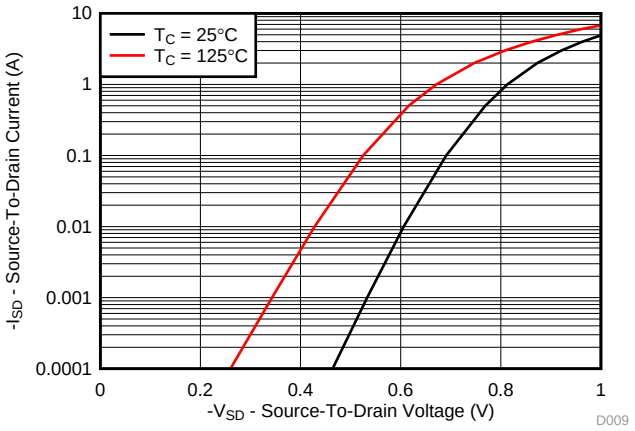


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

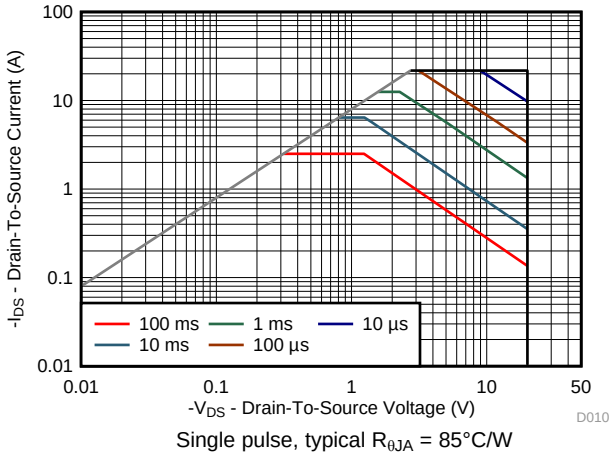


Figure 10. Maximum Safe Operating Area

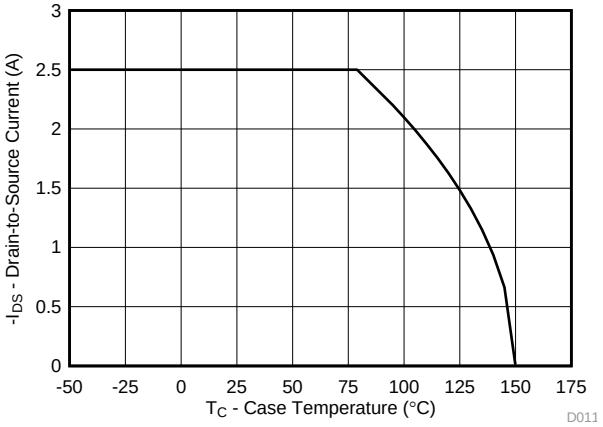


Figure 11. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

6.3 商标

FemtoFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

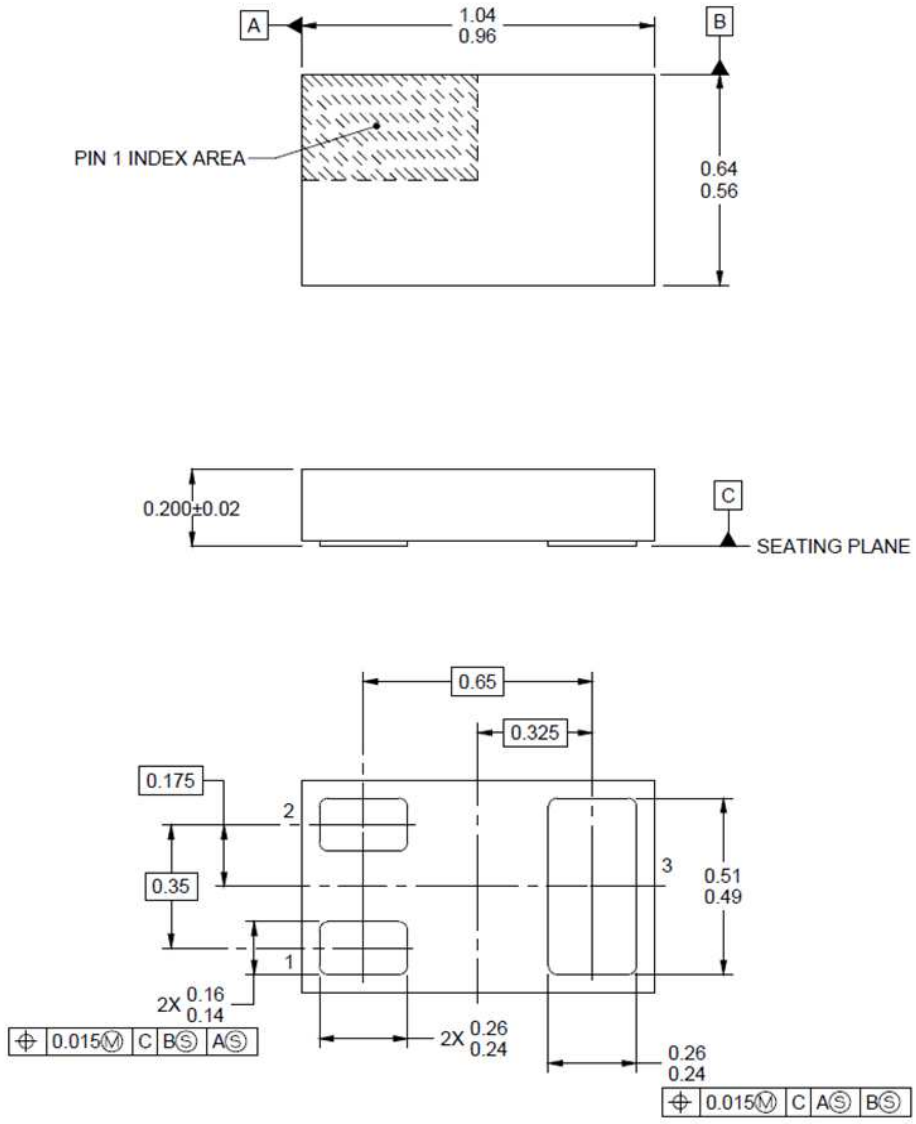
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

7.1 机械尺寸



(1) 所有线性尺寸的单位都是毫米（尺寸和容限值遵循 AME T14.5M-1994）。

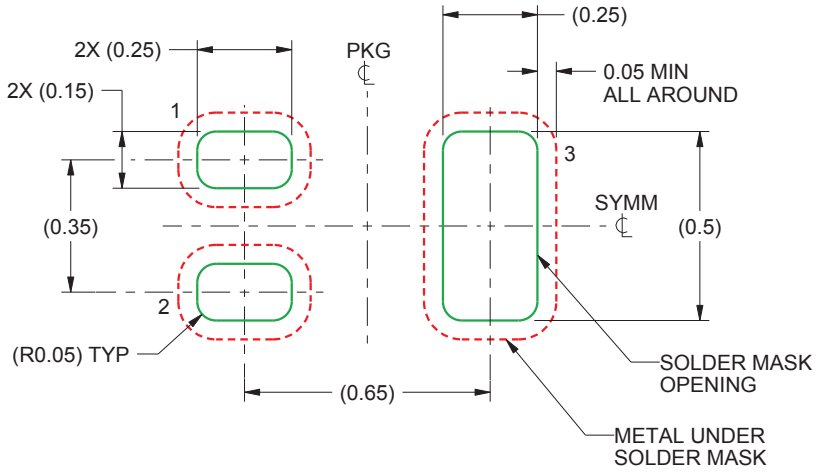
(2) 本图纸如有变更，恕不通知。

(3) 此封装采用无铅焊盘设计。

表 **1.** 引脚配置

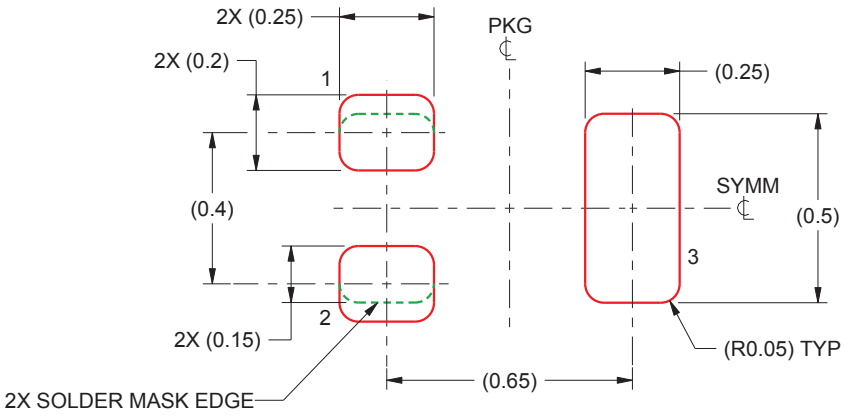
位置	名称
引脚 1	栅极
引脚 2	源极
引脚 3	漏极

7.2 推荐的最小 PCB 布局



(1) 所有尺寸的单位都是毫米。

7.3 推荐的模板布局



(1) 所有尺寸的单位都是毫米。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25484F4	ACTIVE	PICOSTAR	YJJ	3	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	G3	Samples
CSD25484F4T	ACTIVE	PICOSTAR	YJJ	3	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	G3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

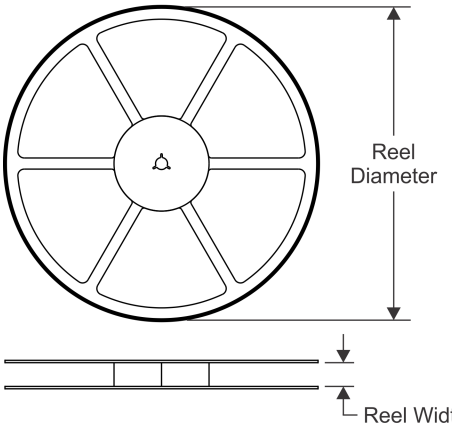
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

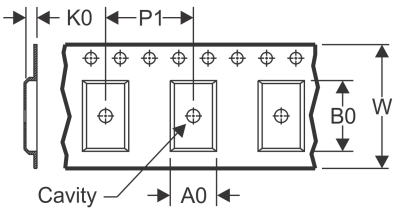
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

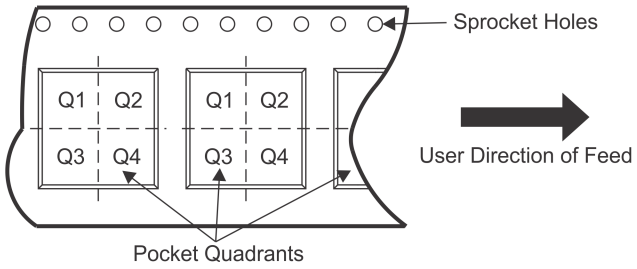


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

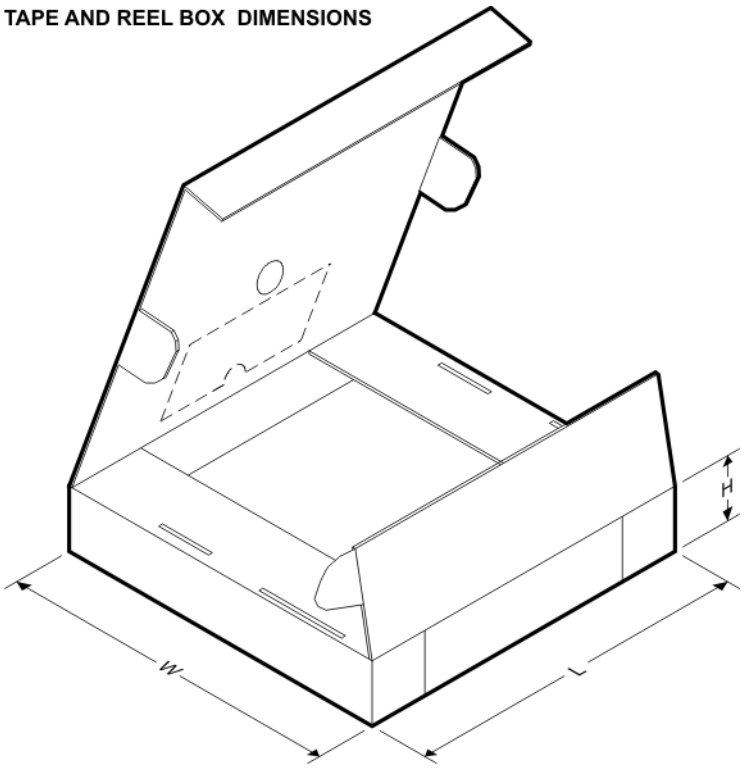
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25484F4	PICOSTAR	YJJ	3	3000	178.0	9.2	0.7	1.1	0.28	4.0	8.0	Q2
CSD25484F4T	PICOSTAR	YJJ	3	250	178.0	9.2	0.7	1.1	0.28	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25484F4	PICOSTAR	YJJ	3	3000	220.0	220.0	35.0
CSD25484F4T	PICOSTAR	YJJ	3	250	220.0	220.0	35.0

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122