

# SN54BCT25244, SN74BCT25244 25-Ω OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS064A – JUNE 1990 – REVISED NOVEMBER 1993

- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater
- Distributed  $V_{CC}$  and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacs (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

## description

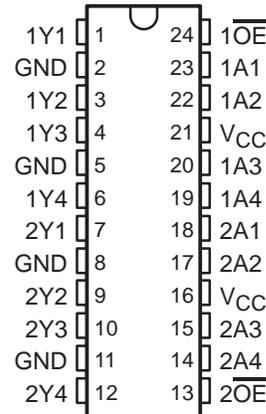
These 25-Ω octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These buffers are capable of sinking 188-mA  $I_{OL}$ , which facilitates switching 25-Ω transmission lines on the incident wave. The distributed  $V_{CC}$  and GND pins minimize switching noise for more reliable system operation.

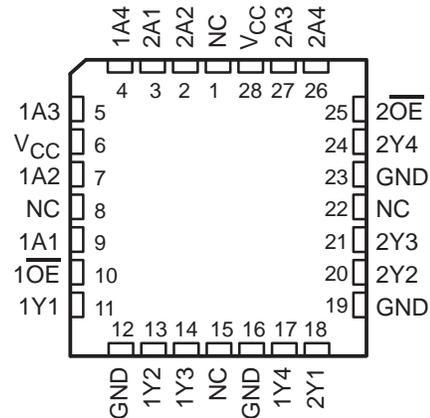
When the output-enable ( $1\overline{OE}$  and  $2\overline{OE}$ ) inputs are low, the device transmits data from the A inputs to the Y outputs. When  $1\overline{OE}$  and  $2\overline{OE}$  are high, the outputs are in the high-impedance state.

The SN54BCT25244 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74BCT25244 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54BCT25244 . . . JT OR W PACKAGE  
SN74BCT25244 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54BCT25244 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

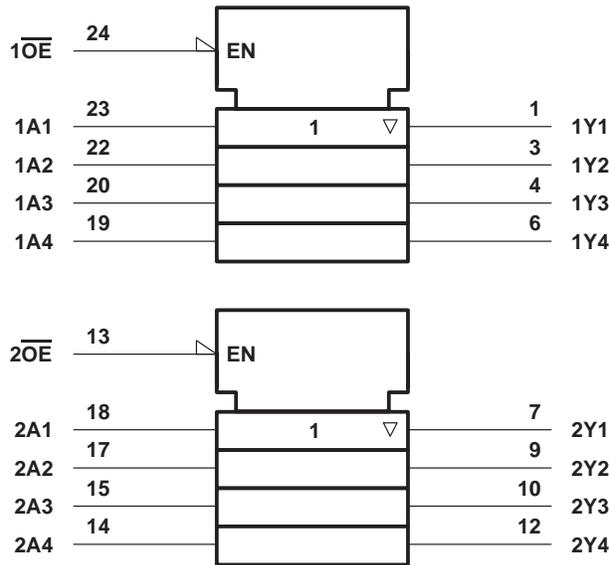
FUNCTION TABLE  
(each buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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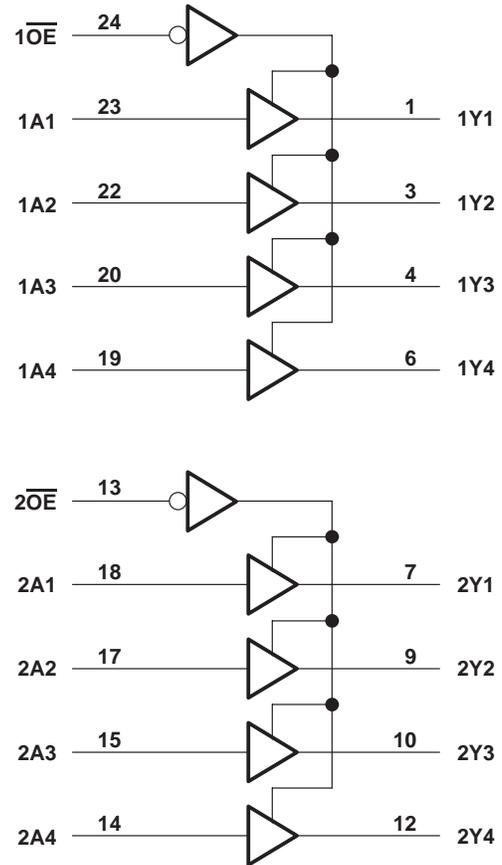
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ .....	-0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-30 mA
Current into any output in the low state, $I_O$ : SN54BCT25244 .....	250 mA
SN74BCT25244 .....	376 mA
Operating free-air temperature range: SN54BCT25244 .....	-55°C to 125°C
SN74BCT25244 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# SN54BCT25244, SN74BCT25244 25-Ω OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 2)

		SN54BCT25244			SN74BCT25244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			-18			-18	mA
$I_{OH}$	High-level output current			-53			-80	mA
$I_{OL}$	Low-level output current			125			188	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: Unused or floating inputs must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT25244			SN74BCT25244			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2			-1.2	V	
$V_{OH}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3\text{ mA}$				2.7			V	
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -53\text{ mA}$	2							
		$I_{OH} = -80\text{ mA}$				2				
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 94\text{ mA}$	0.38	0.55		0.42	0.55		V	
		$I_{OL} = 125\text{ mA}$			0.8					
		$I_{OL} = 188\text{ mA}$						0.7		
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 5.5\text{ V}$			0.1			0.1	mA	
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20			20	μA	
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			-0.6			-0.6	mA	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			50			50	μA	
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$			-50			-50	μA	
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open			90	119		90	119	mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open			59	78		59	78	mA
$I_{CCZ}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open			7	11		7	11	mA
$C_i$	$V_{CC} = 5\text{ V}$ ,	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$			5.5			5.5		pF
$C_o$	$V_{CC} = 5\text{ V}$ ,	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$			17			17		pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			SN54BCT25244		SN74BCT25244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1	3.2	4.9	1	5.6	1	5.5	ns
$t_{PHL}$			2	4	5.6	2	6.3	2	6	
$t_{PZH}$	OE	Y	3.2	5.6	8.5	3.2	9.7	3.2	9.3	ns
$t_{PZL}$			3.7	6.3	9.2	3.7	10.4	3.7	10.2	
$t_{PHZ}$	$\overline{OE}$	Y	1.6	3.6	5.5	1.6	6.5	1.6	6.3	ns
$t_{PLZ}$			3.1	5.3	7.8	3.1	9.5	3.1	8.4	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74BCT25244DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT25244	<a href="#">Samples</a>
SN74BCT25244DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT25244	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

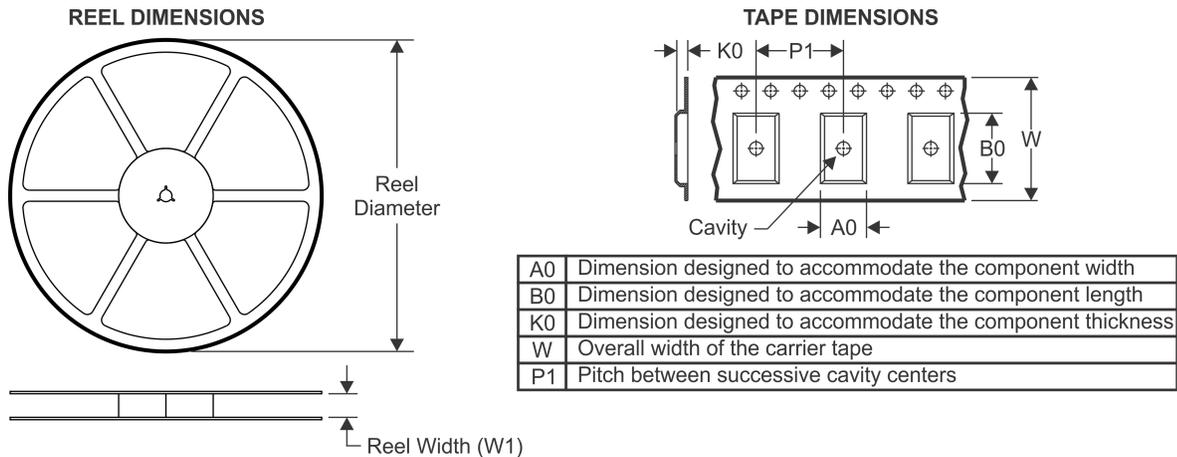
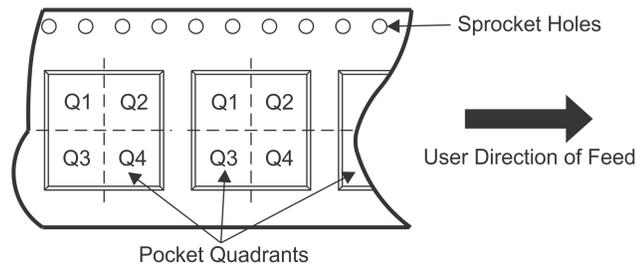
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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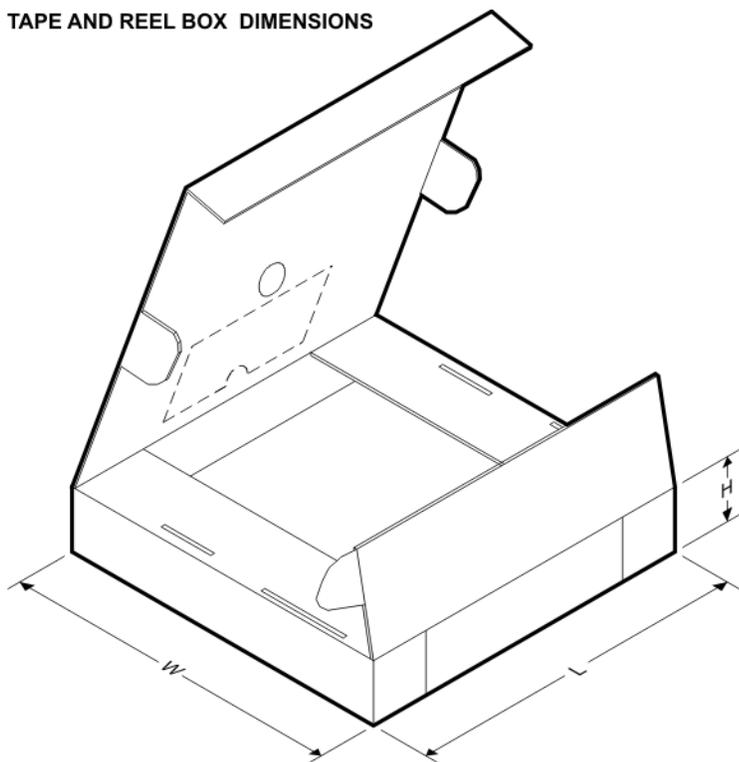


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT25244DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

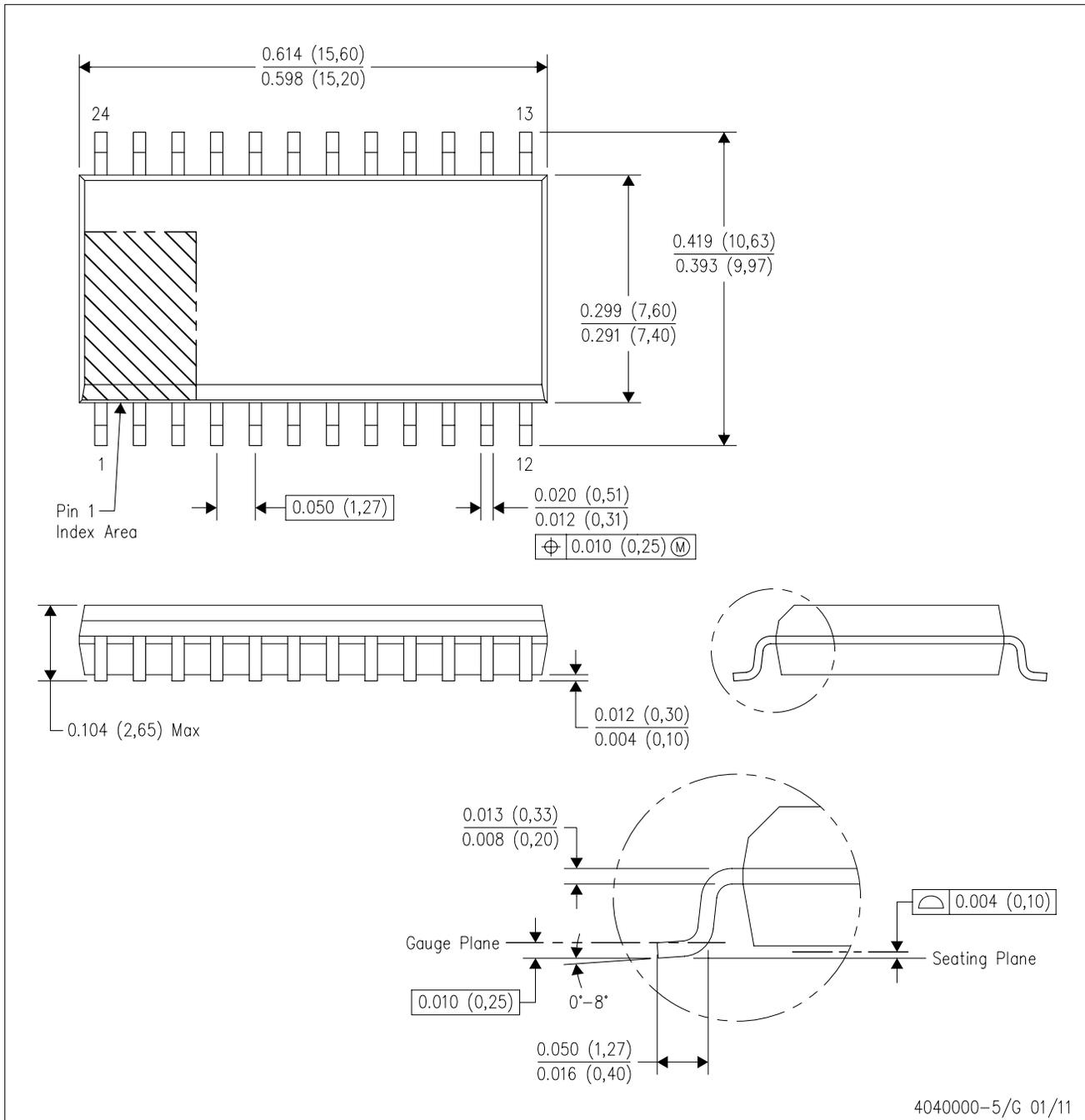


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT25244DWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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