

用于气流和水流计量应用的 MSP430FR604x、MSP430FR504x 超声波 传感 MSP430™ 微 控制器

1 器件概述

1.1 特性

- 功耗超低的一流超声波水流和气流测量
 - 水
 - 在低流速到高流速的情况下以及工作温度范围内的差分飞行时间 (dToF) 精度为 $\pm 12.5\text{ps}$
 - 可在 500:1 的宽动态范围内实现 $\pm 1\%$ 精度
 - 在直径为 25mm 的管道上，能够测量的最大流速为 8800 升/小时 (40 加仑/分钟)
 - 能够检测的最小流速小于 1 升/小时 (0.005 加仑/分钟)
 - 高精度时间测量分辨率小于 5ps
 - 在每秒获取一组结果的条件下总体电流消耗大约为 3 μA
 - 能够支持直径为 15mm 至 1000mm 的宽管道尺寸
 - 气体
 - 在低流速到高流速的情况下以及工作温度范围内的差分飞行时间 (dToF) 精度为 $\pm 250\text{ps}$
 - 可在流速高达 12000 升/小时的条件下实现 $\pm 1\%$ 的精度，具有 200:1 的宽动态范围
 - 能够测量的流速大于 25000 升/小时
 - 能够检测的最小流速小于 3 升/小时
 - 高精度时间测量分辨率小于 100ps
 - 在每秒获取一组结果的条件下总体电流消耗大约为 20 μA
- 符合并超出 ISO4064、OIML R49、EN 14236 和 EN 1434 精度标准
- 能够直接与标准超声波传感器 (高达 2.5MHz) 连接
- 集成模拟前端 – 超声波传感解决方案 (USS_A)，包括
 - 用于在各种频率下生成多音调脉冲的可编程脉冲发生器 (PPG)
 - 用于控制输入和输出通道且具有低阻抗输出驱动器 (4 Ω) 的集成 PHY
- 具有高达 8MSPS 输出数据速率的高性能高速 12 位模数转换器 (SDHS)
- 具有 -6.5dB 至 30.8dB 增益的可编程增益放大器 (PGA)
- 输出范围为 68MHz 至 80MHz 的高性能 PLL
- 计量测试接口 (MTIF)
 - 脉冲发生器和脉冲计数器
 - 脉冲率高达 1024 次脉冲/秒 (p/s)
 - 计数容量高达 65535 (16 位)
 - 在 LPM3.5 下以 200nA (典型值) 运行
- 低功耗加速器 (LEA)
 - 独立于 CPU 运行
 - 与 CPU 共享 8KB RAM
 - 256 点高效复变 FFT：比 Arm® Cortex®-M0+ 内核快 40 倍
- 嵌入式微控制器
 - 时钟频率高达 16MHz 的 16 位精简指令集计算机 (RISC) 架构
 - 宽电源电压范围：1.8V 至 3.6V ⁽¹⁾
- 优化的超低功耗模式
 - 激活模式：大约 120 $\mu\text{A}/\text{MHz}$
 - 具有实时时钟 (RTC) 的待机模式 (LPM3.5)：450nA ⁽²⁾
 - 关断电流 (LPM4.5)：30nA
- 铁电随机存取存储器 (FRAM)
 - 容量高达 64KB 的非易失性存储器
 - 超低功耗写入
 - 以 125ns/字 (4ms 内写入 64KB) 的速度快速写入
 - 统一的存储器 = 程序 + 数据 + 存储都处于同一存储空间
 - 耐写次数达 10^{15} 次
 - 抗辐射和非磁性
- 智能数字外设
 - 32 位硬件乘法器 (MPY)
 - 6 通道内部 DMA
 - 带有日历和报警功能的 RTC
 - 6 个 16 位计时器，每个计时器具有多达 7 个捕捉/比较寄存器
 - 32 位和 16 位循环冗余校验 (CRC)
- 高性能模拟
 - 12 通道模拟比较器
 - 12 位 ADC，具有窗口比较器、内部基准和采样

(1) 最低电源电压受限于 SVS 电平，请参阅 [SVS 规格](#)

(2) RTC 由 3.7pF 晶振生成。



- 保持功能以及多达 8 条外部输入通道
- 具有高达 248 段对比度控制的集成 LCD 驱动器
- 多功能输入/输出端口
 - 所有引脚均支持电容式触控功能，无需外部组件
 - 可按位、字节和字进行访问（成对访问）
 - 所有端口均可从 LPM 进行边沿可选唤醒
 - 所有端口均具有可设定的上拉电阻或下拉电阻
- 代码安全性和加密
 - 128 位或 256 位 AES 安全加密和解密协处理器
 - 用于随机数生成算法的随机数种子
 - IP 封装可保护存储器免遭外部访问
 - FRAM 可提供固有安全性优势
- 增强型串行通信
 - 多达 4 个 eUSCI_A 串行通信端口
 - 支持自动波特率检测的 UART
 - IrDA 编码和解码
 - 多达 2 个 eUSCI_B 串行通信端口
 - 支持多从器件寻址的 I²C
 - 硬件 UART 或 I²C 引导加载程序 (BSL)
- 灵活的时钟系统
 - 具有 10 个可选厂家调整频率的固定频率数控振荡器 (DCO)
 - 低功耗低频内部时钟源 (VLO)
 - 32kHz 晶振 (LFXT)
 - 高频晶振 (HFXT)
- 开发工具和软件
 - 超声波传感设计中心图形用户界面
 - 超声波传感软件库
 - EVM430-FR6043 燃气表评估模块板
 - 用于 80 引脚封装的 MSP-TS430PN80C 目标插座板
 - 采用 EnergyTrace++ 技术的免费专业开发环境
 - 用于 MSP 微控制器的 MSP430Ware
- 器件比较 汇总了可用的器件型号和封装选项
- 有关完整的模块说明，请参阅《MSP430FR58xx、MSP430FR59xx 和 MSP430FR6xx 系列用户指南》

1.2 应用

- 超声波智能水表
- 超声波智能燃气表
- 超声波智能热量计
- 流量发送器

1.3 说明

德州仪器 (TI) MSP430FR6043 SoC 隶属 [MSP430 超声波传感微控制器 \(MCU\)](#) 系列产品，该器件功能强大、集成度高，专为超声波水表、热量计和燃气表而设计。这些 MCU 提供集成的超声波传感解决方案 (USS_A) 模块，该模块可针对多种流速提供高精度测量。USS_A 高度集成，需要的外部组件极少，因而有助于实现超低功耗计量并降低系统成本。

MSP430FR6043 器件采用低功耗加速器 (LEA)，可实现基于高速 ADC 的信号采集以及后续优化数字信号处理，为电池供电型计量提供了一款超低功耗、高精度的计量解决方案 应用。

USS_A 模块包括可编程脉冲发生器 (PPG) 和具有低阻抗输出驱动器的物理接口 (PHY)，以实现最佳传感器激励和准确的阻抗匹配，从而在零流量漂移 (ZFD) 方面达到最佳效果。USS_A 模块还包含可编程增益放大器 (PGA) 和高速 12 位 8Msps Σ - Δ ADC (SDHS)，便于通过行业标准超声波传感器实现精确的信号采集。

MSP430FR6043 MCU 还集成了其他外设，以针对计量提高系统集成度。它具有计量测试接口 (MTIF) 模块，能够通过脉冲生成来指示仪表测量的流量。它还具有片上 8 通道多路复用器 LCD 驱动器、实时时钟 (RTC)、12 位 SAR ADC、模拟比较器、高级加密 (AES256) 和循环冗余校验 (CRC) 模块。

MSP430FR604x 和 MSP430FR504x MCU 由广泛的硬件和软件生态系统提供支持，随附参考设计和代码示例，便于您快速开始设计。开发套件包括 [MSP-TS430PN80C 80 引脚目标开发板](#) 和 [EVM430-FR6043 超声波气流计 EVM](#)。TI 还提供免费软件，包括[超声波传感设计中心](#)、超声波传感软件库和 [MSP430Ware™ 软件](#)。

MSP430FR604x MCU 系列集成了 TI 的 FRAM（铁电 RAM）和功耗整体超低 MSP 系统架构，从而使系统设计人员能够在降低能耗的同时提升性能。FRAM 技术兼有 RAM 的低功耗快速写入、灵活性、耐用性和闪存非易失性等特性。

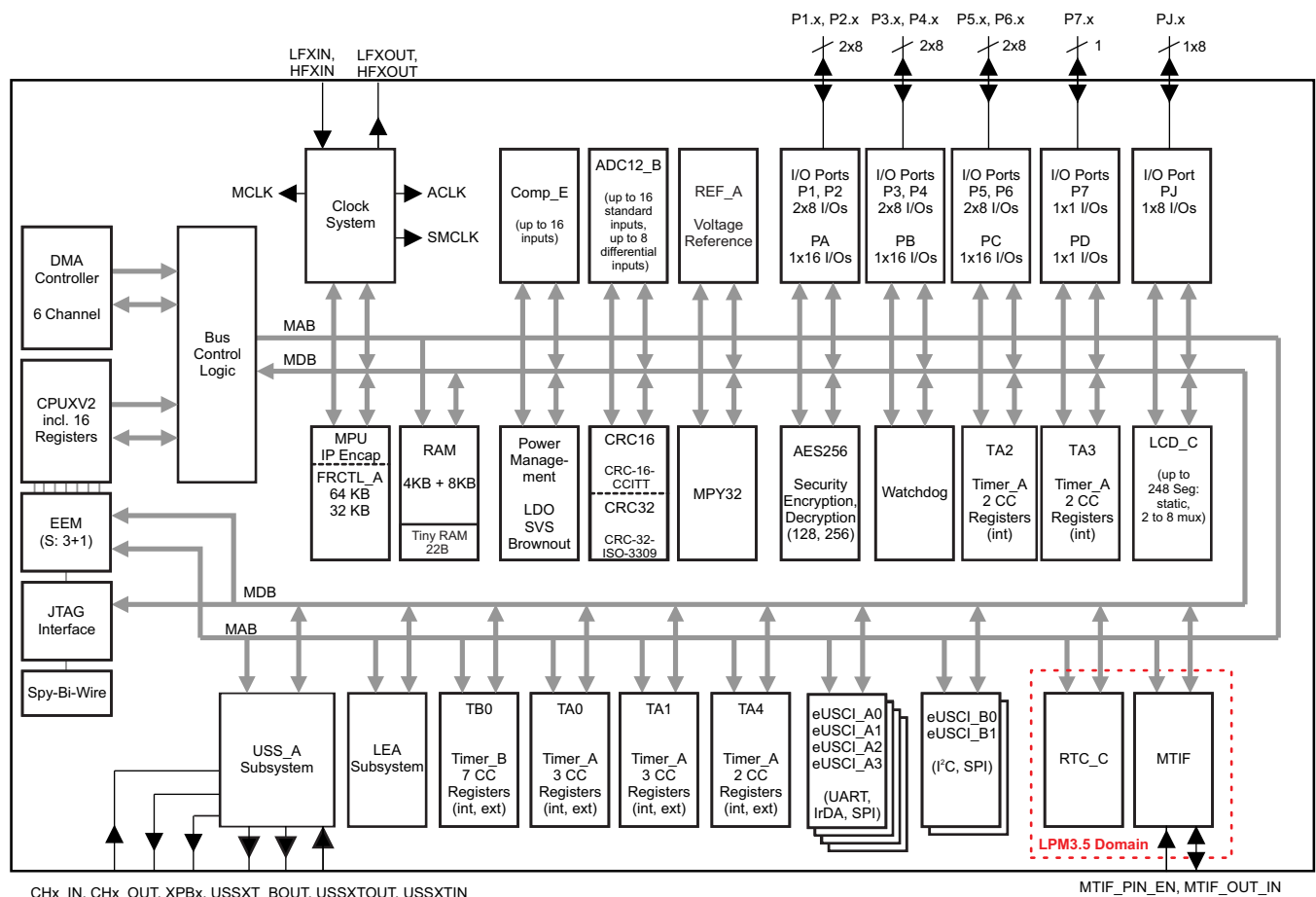
器件信息 (1)(2)

器件型号	封装	封装尺寸(3)
MSP430FR6043IPN	LQFP (80)	12mm x 12mm
MSP430FR60431IPN	LQFP (80)	12mm x 12mm
MSP430FR6041IPN	LQFP (80)	12mm x 12mm
MSP430FR5043IPM	LQFP (64)	10mm x 10mm
MSP430FR50431IPM	LQFP (64)	10mm x 10mm
MSP430FR5041IPM	LQFP (64)	10mm x 10mm
MSP430FR5043IRGC	VQFN (64)	9mm x 9mm
MSP430FR50431IRGC	VQFN (64)	9mm x 9mm
MSP430FR5041IRGC	VQFN (64)	9mm x 9mm

- (1) 要获得所有可用器件的最新部件、封装和订购信息，请参见封装选项附录（节 9）或浏览 TI 网站 www.ti.com.cn。
- (2) 有关提供的所有器件变型的对比，请参见节 3。
- (3) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见机械数据（节 9）。

1.4 功能方框图

图 1-1 显示了器件的功能方框图。



A. 该器件具备 12KB RAM，其中 8KB RAM 与 LEA 子系统共享。

图 1-1. 功能方框图

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2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	备注
2019 年 1 月	*	初始发行版

3 Device Comparison

表 3-1 summarizes the available family members.

表 3-1. Device Comparison⁽¹⁾⁽²⁾

DEVICE	FRAM (KB)	SRAM (KB)	CLOCK SYSTEM	LEA	LCD	MTIF	ADC12_B	Comp_E	Timer_A ⁽³⁾	Timer_B ⁽⁴⁾	eUSCI		AES	BSL	I/O	PACKAGE
											A ⁽⁵⁾	B ⁽⁶⁾				
MSP430FR6043	64	12	DCO HFXT LFXT	Yes	Yes	Yes	8 ext, 2 int ch.	12 ch.	3, 3 ⁽⁷⁾ 2, 2, 2 ⁽⁸⁾	7	4	2	Yes	UART	57	80 PN (LQFP)
MSP430FR60431	64	12	DCO HFXT LFXT	Yes	Yes	Yes	8 ext, 2 int ch.	12 ch.	3, 3 ⁽⁷⁾ 2, 2, 2 ⁽⁸⁾	7	4	2	Yes	I2C	57	80 PN (LQFP)
MSP430FR6041	32	12	DCO HFXT LFXT	Yes	Yes	Yes	8 ext, 2 int ch.	12 ch.	3, 3 ⁽⁷⁾ 2, 2, 2 ⁽⁸⁾	7	4	2	Yes	UART	57	80 PN (LQFP)
MSP430FR5043	64	12	DCO HFXT LFXT	Yes	No	Yes	7 ext, 2 int ch.	11 ch.	3, 3 ⁽⁷⁾ 2, 2, 2 ⁽⁸⁾	7	4	2	Yes	UART	44	64 PM (LQFP) 64 RGC (VQFN)
MSP430FR50431	64	12	DCO HFXT LFXT	Yes	No	Yes	7 ext, 2 int ch.	11 ch.	3, 3 ⁽⁷⁾ 2, 2, 2 ⁽⁸⁾	7	4	2	Yes	I2C	44	64 PM (LQFP) 64 RGC (VQFN)
MSP430FR5041	32	12	DCO HFXT LFXT	Yes	No	Yes	7 ext, 2 int ch.	11 ch.	3, 3 ⁽⁷⁾ 2, 2, 2 ⁽⁸⁾	7	4	2	Yes	UART	44	64 PM (LQFP) 64 RGC (VQFN)

- (1) For the most current package and ordering information, see the *Package Option Addendum* in 节 9, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
- (3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
- (4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
- (5) eUSCI_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
- (6) eUSCI_B supports I²C with multiple slave addresses and SPI.
- (7) Timers TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
- (8) Timers TA2 and TA3 provide only internal capture/compare inputs and only internal PWM outputs (if any) whereas Timer TA4 provides internal, external capture/compare inputs and internal, external PWM outputs (Note: TA4 in the RGZ package provide only internal capture/compare inputs and only internal PWM outputs.).

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing and measurement microcontrollers One platform. One ecosystem. Endless possibilities.

Products for MSP430 ultrasonic and performance sensing microcontrollers Ultra-low-power single-chip MCUs with integrated sensing peripherals

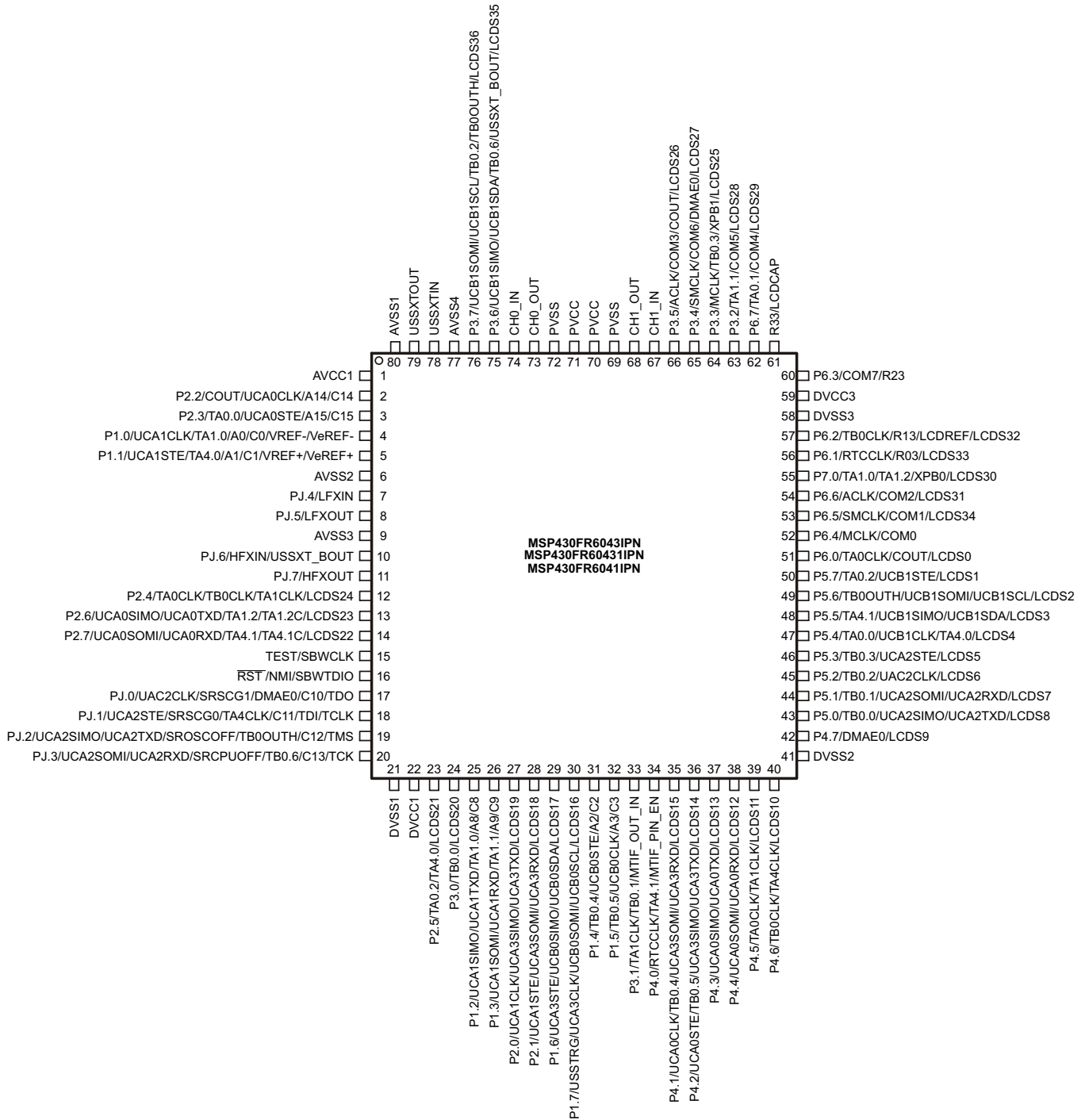
Companion products for MSP430FR6043 Review products that are frequently purchased or used with this product.

Reference designs The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

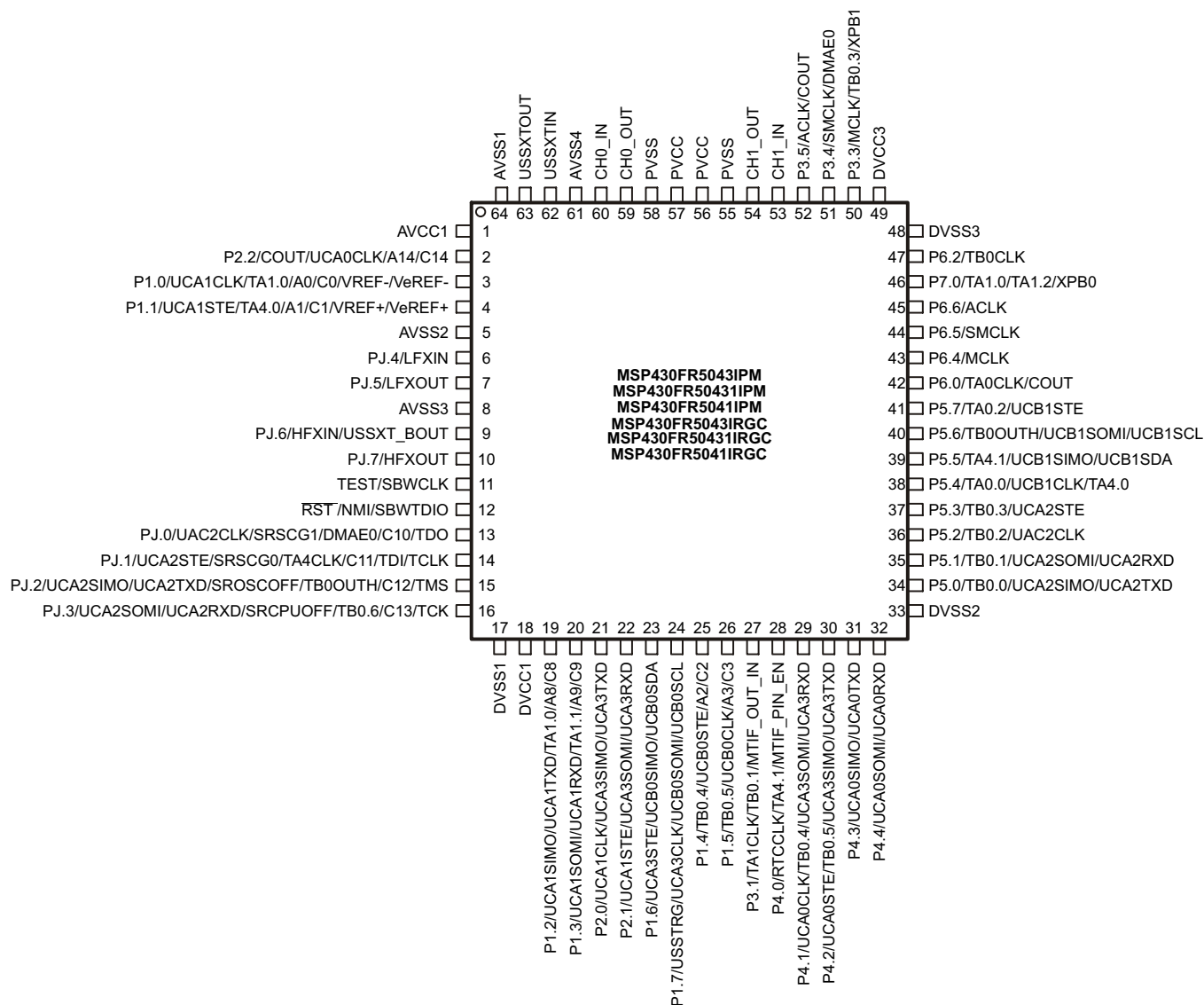
图 4-1 shows the pinout of the 80-pin PM package.



- A. On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX
- B. On devices with I²C BSL: P1.6 is BSLSDA, P1.7 is BSLSLC

图 4-1. 80-Pin PN Package (Top View)

图 4-2 shows the pinout of the 64-pin PM and 64-pin RGC package.



- A. On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX
- B. On devices with I²C BSL: P1.6 is BSLSDA, P1.7 is BSLSCL

图 4-2. 64-Pin PM or RGC Package (Top View)

4.2 Pin Attributes

表 4-1. Pin Attributes

PIN NUMBER ⁽¹⁾		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
FR6043, FR6041	FR5043, FR5041					
1	1	AVCC1	P	Power	–	N/A
2	2	P2.2	I/O	LVC MOS	DVCC	OFF
		COUT	O	LVC MOS	DVCC	–
		UCA0CLK	I/O	LVC MOS	DVCC	–
		A14	I	Analog	DVCC	–
		C14	I	Analog	DVCC	–
3	–	P2.3	I/O	LVC MOS	DVCC	OFF
		TA0.0	I/O	LVC MOS	DVCC	–
		UCA0STE	I/O	LVC MOS	DVCC	–
		A15	I	Analog	DVCC	–
		C15	I	Analog	DVCC	–
4	3	P1.0	I/O	LVC MOS	DVCC	OFF
		UCA1CLK	I/O	LVC MOS	DVCC	–
		TA1.0	I/O	LVC MOS	DVCC	–
		A0	I	Analog	DVCC	–
		C0	I	Analog	DVCC	–
		VREF-	O	Analog	DVCC	–
		VeREF-	I	Analog	DVCC	–
5	4	P1.1	I/O	LVC MOS	DVCC	OFF
		UCA1STE	I/O	LVC MOS	DVCC	–
		TA4.0	I/O	LVC MOS	DVCC	–
		A1	I	Analog	DVCC	–
		C1	I	Analog	DVCC	–
		VREF+	O	Analog	DVCC	–
		VeREF+	I	Analog	DVCC	–
6	5	AVSS2	P	Power	–	N/A
7	6	PJ.4	I/O	LVC MOS	DVCC	OFF
		LFXIN	I	Analog	DVCC	–
8	7	PJ.5	I/O	LVC MOS	DVCC	OFF
		LFXOUT	O	Analog	DVCC	–
9	8	AVSS3	P	Power	–	N/A
10	9	PJ.6	I/O	LVC MOS	DVCC	–
		HFXIN	I	Analog	DVCC	–
		USSXT_BOUT	O	Analog	DVCC	–
11	10	PJ.7	I/O	LVC MOS	DVCC	OFF
		HFXOUT	O	Analog	DVCC	–

(1) The signal that is listed first for each pin is the reset default pin name.

(2) To determine the pin mux encodings for each pin, see .

(3) Signal Types: I = Input, O = Output, I/O = Input or Output.

(4) Buffer Types: LVC MOS, Analog, or Power (see 表 4-3 for details)

(5) The power source shown in this table is the I/O power source, which may differ from the module power source.

(6) Reset States:

OFF = High impedance with Schmitt-trigger input and pullup or pulldown (if available) disabled

PU = Pullup is enabled

PD = Pulldown is enabled

N/A = Not applicable

表 4-1. Pin Attributes (continued)

PIN NUMBER ⁽¹⁾		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
FR6043, FR6041	FR5043, FR5041					
12	–	P2.4	I/O	LVC MOS	DVCC	OFF
		TA0CLK	I	LVC MOS	DVCC	–
		TB0CLK	I	LVC MOS	DVCC	–
		TA1CLK	I	LVC MOS	DVCC	–
		S24	O	Analog	DVCC	–
13	–	P2.6	I/O	LVC MOS	DVCC	OFF
		UCA0TXD	O	LVC MOS	DVCC	–
		UCA0SIMO	I/O	LVC MOS	DVCC	–
		TA1.2	I/O	LVC MOS	DVCC	–
		TA1.2C	I/O	LVC MOS	DVCC	–
		S23	O	Analog	DVCC	–
14	–	P2.7	I/O	LVC MOS	DVCC	OFF
		UCA0RXD	I	LVC MOS	DVCC	–
		UCA0SOMI	I/O	LVC MOS	DVCC	–
		TA4.1	I/O	LVC MOS	DVCC	–
		TA4.1C	I/O	LVC MOS	DVCC	–
		S22	O	Analog	DVCC	–
15	11	TEST	I	LVC MOS	DVCC	PD
		SBWTCK	I	LVC MOS	DVCC	–
16	12	$\overline{\text{RST}}$	I/O	LVC MOS	DVCC	PU
		NMI	I	LVC MOS	DVCC	–
		SBWTDIO	I/O	LVC MOS	DVCC	–
17	13	PJ.0	I/O	LVC MOS	DVCC	OFF
		TDO	O	LVC MOS	DVCC	–
		UCA2CLK	I/O	LVC MOS	DVCC	–
		SRSCG1	O	LVC MOS	DVCC	–
		DMAE0	I	LVC MOS	DVCC	–
		C10	I	Analog	DVCC	–
18	14	PJ.1	I/O	LVC MOS	DVCC	OFF
		TDI	I	LVC MOS	DVCC	–
		TCLK	I	LVC MOS	DVCC	–
		UCA2STE	I/O	LVC MOS	DVCC	–
		SRSCG0	O	LVC MOS	DVCC	–
		TA4CLK	I	LVC MOS	DVCC	–
		C11	I	Analog	DVCC	–
19	15	PJ.2	I/O	LVC MOS	DVCC	OFF
		TMS	I	LVC MOS	DVCC	–
		UCA2TXD	O	LVC MOS	DVCC	–
		UCA2SIMO	I/O	LVC MOS	DVCC	–
		SROSCOFF	O	LVC MOS	DVCC	–
		TB0OUTH	I	LVC MOS	DVCC	–
		C12	I	Analog	DVCC	–

表 4-1. Pin Attributes (continued)

PIN NUMBER ⁽¹⁾		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
FR6043, FR6041	FR5043, FR5041					
20	16	PJ.3	I/O	LVC MOS	DVCC	OFF
		TCK	I	LVC MOS	DVCC	–
		UCA2RXD	I	LVC MOS	DVCC	–
		UCA2SOMI	I/O	LVC MOS	DVCC	–
		SRCPUOFF	O	LVC MOS	DVCC	–
		TB0.6	I/O	LVC MOS	DVCC	–
		C13	I	Analog	DVCC	–
21	17	DVSS1	P	Power	–	N/A
22	18	DVCC1	P	Power	–	N/A
23	–	P2.5	I/O	LVC MOS	DVCC	OFF
		TA0.2	I/O	LVC MOS	DVCC	–
		TA4.0	I/O	LVC MOS	DVCC	–
		S21	O	Analog	DVCC	–
24	–	P3.0	I/O	LVC MOS	DVCC	OFF
		TB0.0	I/O	LVC MOS	DVCC	–
		S20	O	Analog	DVCC	–
25	19	P1.2	I/O	LVC MOS	DVCC	OFF
		UCA1TXD	O	LVC MOS	DVCC	–
		UCA1SIMO	I/O	LVC MOS	DVCC	–
		TA1.0	I/O	LVC MOS	DVCC	–
		A8	I	Analog	DVCC	–
		C8	I	Analog	DVCC	–
26	20	P1.3	I/O	LVC MOS	DVCC	OFF
		UCA1RXD	I	LVC MOS	DVCC	–
		UCA1SOMI	I/O	LVC MOS	DVCC	–
		TA1.1	I/O	LVC MOS	DVCC	–
		A9	I	Analog	DVCC	–
		C9	I	Analog	DVCC	–
27	21	P2.0	I/O	LVC MOS	DVCC	OFF
		UCA1CLK	I/O	LVC MOS	DVCC	–
		UCA3TXD	O	LVC MOS	DVCC	–
		UCA3SIMO	I/O	LVC MOS	DVCC	–
		S19	O	Analog	DVCC	–
28	22	P2.1	I/O	LVC MOS	DVCC	OFF
		UCA1STE	I/O	LVC MOS	DVCC	–
		UCA3RXD	I	LVC MOS	DVCC	–
		UCA3SOMI	I/O	LVC MOS	DVCC	–
		S18	O	Analog	DVCC	–
29	23	P1.6	I/O	LVC MOS	DVCC	OFF
		UCA3STE	I/O	LVC MOS	DVCC	–
		UCB0SIMO	I/O	LVC MOS	DVCC	–
		UCB0SDA	I/O	LVC MOS	DVCC	–
		S17	O	Analog	DVCC	–

表 4-1. Pin Attributes (continued)

PIN NUMBER ⁽¹⁾		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
FR6043, FR6041	FR5043, FR5041					
30	24	P1.7	I/O	LVC MOS	DVCC	OFF
		USSTRG	I	LVC MOS	DVCC	–
		UCA3CLK	I/O	LVC MOS	DVCC	–
		UCB0SOMI	I/O	LVC MOS	DVCC	–
		UCB0SCL	I/O	LVC MOS	DVCC	–
		S16	O	Analog	DVCC	–
31	25	P1.4	I/O	LVC MOS	DVCC	OFF
		TB0.4	I/O	LVC MOS	DVCC	–
		UCA0STE	I/O	LVC MOS	DVCC	–
		A2	I	Analog	DVCC	–
		C2	I	Analog	DVCC	–
32	26	P1.5	I/O	LVC MOS	DVCC	OFF
		TB0.5	I/O	LVC MOS	DVCC	–
		UCB0CLK	I/O	LVC MOS	DVCC	–
		A3	I	Analog	DVCC	–
		C3	I	Analog	DVCC	–
33	27	P3.1	I/O	LVC MOS	DVCC	OFF
		TA1CLK	I	LVC MOS	DVCC	–
		TB0.1	I/O	LVC MOS	DVCC	–
		MTIF_OUT_IN	I/O	LVC MOS	DVCC	–
34	28	P4.0	I/O	LVC MOS	DVCC	OFF
		RTCCLK	O	LVC MOS	DVCC	–
		TA4.1	O	LVC MOS	DVCC	–
		MTIF_PIN_EN	I	LVC MOS	DVCC	–
35	29	P4.1	I/O	LVC MOS	DVCC	OFF
		UCA0CLK	I/O	LVC MOS	DVCC	–
		TB0.4	I/O	LVC MOS	DVCC	–
		UCA3RXD	I	LVC MOS	DVCC	–
		UCA3SOMI	I/O	LVC MOS	DVCC	–
		S15	O	Analog	DVCC	–
36	30	P4.2	I/O	LVC MOS	DVCC	OFF
		UCA0STE	I/O	LVC MOS	DVCC	–
		TB0.5	I/O	LVC MOS	DVCC	–
		UCA3SIMO	I/O	LVC MOS	DVCC	–
		UCA3TXD	O	LVC MOS	DVCC	–
		S14	O	Analog	DVCC	–
37	31	P4.3	I/O	LVC MOS	DVCC	OFF
		UCA0TXD	O	LVC MOS	DVCC	–
		UCA0SIMO	I/O	LVC MOS	DVCC	–
		S13	O	Analog	DVCC	–
38	32	P4.4	I/O	LVC MOS	DVCC	OFF
		UCA0RXD	I	LVC MOS	DVCC	–
		UCA0SOMI	I/O	LVC MOS	DVCC	–
		S12	O	Analog	DVCC	–

表 4-1. Pin Attributes (continued)

PIN NUMBER ⁽¹⁾		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
FR6043, FR6041	FR5043, FR5041					
39	–	P4.5	I/O	LVC MOS	DVCC	OFF
		TA0CLK	I	LVC MOS	DVCC	–
		TA1CLK	I	LVC MOS	DVCC	–
		S11	O	Analog	DVCC	–
40	–	P4.6	I/O	LVC MOS	DVCC	OFF
		TB0CLK	I	LVC MOS	DVCC	–
		TA4CLK	I	LVC MOS	DVCC	–
		S10	O	Analog	DVCC	–
41	33	DVSS2	P	Power	–	N/A
42	–	P4.7	I/O	LVC MOS	DVCC	OFF
		DMAE0	I	LVC MOS	DVCC	–
		S9	O	Analog	DVCC	–
43	34	P5.0	I/O	LVC MOS	DVCC	OFF
		TB0.0	I/O	LVC MOS	DVCC	–
		UCA2TXD	O	LVC MOS	DVCC	–
		UCA2SIMO	I/O	LVC MOS	DVCC	–
		S8	O	Analog	DVCC	–
44	35	P5.1	I/O	LVC MOS	DVCC	OFF
		TB0.1	O	LVC MOS	DVCC	–
		UCA2RXD	I	LVC MOS	DVCC	–
		UCA2SOMI	I/O	LVC MOS	DVCC	–
		S7	O	Analog	DVCC	–
45	36	P5.2	I/O	LVC MOS	DVCC	OFF
		TB0.2	O	LVC MOS	DVCC	–
		UCA2CLK	I/O	LVC MOS	DVCC	–
		S6	O	Analog	DVCC	–
46	37	P5.3	I/O	LVC MOS	DVCC	OFF
		TB0.3	O	LVC MOS	DVCC	–
		UCA2STE	I/O	LVC MOS	DVCC	–
		S5	O	Analog	DVCC	–
47	38	P5.4	I/O	LVC MOS	DVCC	OFF
		TA0.0	I/O	LVC MOS	DVCC	–
		UCB1CLK	I/O	LVC MOS	DVCC	–
		TA4.0	O	LVC MOS	DVCC	–
		S4	O	Analog	DVCC	–
48	39	P5.5	I/O	LVC MOS	DVCC	OFF
		TA4.1	I/O	LVC MOS	DVCC	–
		UCB1SIMO	I/O	LVC MOS	DVCC	–
		UCB1SDA	I/O	LVC MOS	DVCC	–
		S3	O	Analog	DVCC	–
49	40	P5.6	I/O	LVC MOS	DVCC	OFF
		TB0OUTH	I	LVC MOS	DVCC	–
		UCB1SOMI	I/O	LVC MOS	DVCC	–
		UCB1SCL	I/O	LVC MOS	DVCC	–
		S2	O	Analog	DVCC	–

表 4-1. Pin Attributes (continued)

PIN NUMBER ⁽¹⁾		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
FR6043, FR6041	FR5043, FR5041					
50	41	P5.7	I/O	LVC MOS	DVCC	OFF
		TA0.2	I/O	LVC MOS	DVCC	–
		UCB1STE	I/O	LVC MOS	DVCC	–
		S1	O	Analog	DVCC	–
51	42	P6.0	I/O	LVC MOS	DVCC	OFF
		TA0CLK	I	LVC MOS	DVCC	–
		COU T	I	LVC MOS	DVCC	–
		S0	O	Analog	DVCC	–
52	43	P6.4	I/O	LVC MOS	DVCC	OFF
		MCLK	O	LVC MOS	DVCC	–
		COM0	O	Analog	DVCC	–
53	44	P6.5	I/O	LVC MOS	DVCC	OFF
		SMCLK	O	LVC MOS	DVCC	–
		COM1	O	Analog	DVCC	–
		S34	O	Analog	DVCC	–
54	45	P6.6	I/O	LVC MOS	DVCC	OFF
		ACLK	O	LVC MOS	DVCC	–
		COM2	O	Analog	DVCC	–
		S31	O	Analog	DVCC	–
55	46	P7.0	I/O	LVC MOS	DVCC	OFF
		TA1.0	I/O	LVC MOS	DVCC	–
		TA1.2	I/O	LVC MOS	DVCC	–
		XPB0	O	Analog	1.5 V	–
		S30	O	Analog	DVCC	–
56	–	P6.1	I/O	LVC MOS	DVCC	OFF
		RTCCLK	O	LVC MOS	DVCC	–
		R03	I/O	Analog	DVCC	–
		S33	O	Analog	DVCC	–
57	47	P6.2	I/O	LVC MOS	DVCC	OFF
		TB0CLK	I	LVC MOS	DVCC	–
		R13	I/O	Analog	DVCC	–
		LCDREF	I	Analog	–	–
		S32	O	Analog	DVCC	–
58	48	DVSS3	P	Power	–	N/A
59	49	DVCC3	P	Power	–	N/A
60	–	P6.3	I/O	LVC MOS	DVCC	OFF
		COM7	O	Analog	DVCC	–
		R23	I/O	Analog	DVCC	–
61	–	R33	I/O	Analog	DVCC	–
		LDCAP	I/O	Analog	DVCC	–
62	–	P6.7	I/O	LVC MOS	DVCC	OFF
		TA0.1	I/O	LVC MOS	DVCC	–
		COM4	O	Analog	DVCC	–
		S29	O	Analog	DVCC	–

表 4-1. Pin Attributes (continued)

PIN NUMBER ⁽¹⁾		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
FR6043, FR6041	FR5043, FR5041					
63	–	P3.2	I/O	LVC MOS	DVCC	OFF
		TA1.1	I/O	LVC MOS	DVCC	–
		COM5	O	Analog	DVCC	–
		S28	O	Analog	DVCC	–
64	50	P3.3	I/O	LVC MOS	DVCC	OFF
		MCLK	O	LVC MOS	DVCC	–
		TB0.3	I/O	LVC MOS	DVCC	–
		XPB1	O	Analog	1.5 V	–
		S25	O	Analog	DVCC	–
65	51	P3.4	I/O	LVC MOS	DVCC	OFF
		SMCLK	O	LVC MOS	DVCC	–
		COM6	O	Analog	DVCC	–
		DMAE0	I	LVC MOS	DVCC	–
		S27	O	Analog	DVCC	–
66	52	P3.5	I/O	LVC MOS	DVCC	OFF
		ACLK	O	LVC MOS	DVCC	–
		COM3	O	Analog	DVCC	–
		COUT	O	LVC MOS	DVCC	–
		S26	O	Analog	DVCC	–
67	53	CH1_IN	I	Analog	PVCC	–
68	54	CH1_OUT	O	Analog	PVCC	–
69	55	PVSS	P	Power	–	N/A
70	56	PVCC	P	Power	–	N/A
71	57	PVCC	P	Power	–	N/A
72	58	PVSS	P	Power	–	N/A
73	59	CH0_OUT	O	Analog	PVCC	–
74	60	CH0_IN	I	Analog	PVCC	–
75	–	P3.6	I/O	LVC MOS	DVCC	OFF
		UCB1SIMO	I/O	LVC MOS	DVCC	–
		UCB1SDA	I/O	LVC MOS	DVCC	–
		TB0.6	I/O	LVC MOS	DVCC	–
		USSXT_BOUT	I/O	LVC MOS	DVCC	–
		S35	O	Analog	DVCC	–
76	–	P3.7	I/O	LVC MOS	DVCC	OFF
		UCB1SOMI	I/O	LVC MOS	DVCC	–
		UCB1SCL	I/O	LVC MOS	DVCC	–
		TB0.2	I/O	LVC MOS	DVCC	–
		TB0OUTH	I	LVC MOS	DVCC	–
		S36	O	Analog	DVCC	–
77	61	AVSS4	P	Power	–	N/A
78	62	USSXTIN ⁽⁷⁾	I	Analog	1.5 V	–
79	63	USSXTOUT ⁽⁷⁾	O	Analog	1.5 V	–
80	64	AVSS1	P	Power	–	N/A

(7) Do not connect the USSXTIN and USSXTOUT pins to AVCC or DVCC. USSXTIN does not support bypass mode, so do not drive an external clock to USSXTIN pin.

4.3 Signal Descriptions

表 4-2 describes the signals for all device variants and package options.

表 4-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
ADC	A0	4	3	I	ADC analog input A0
	A1	5	4	I	ADC analog input A1
	A2	31	25	I	ADC analog input A2
	A3	32	26	I	ADC analog input A3
	–	AVSS	AVSS	I	ADC analog input A4
	–	AVSS	AVSS	I	ADC analog input A5
	–	AVSS	AVSS	I	ADC analog input A6
	–	AVSS	AVSS	I	ADC analog input A7
	A8	25	19	I	ADC analog input A8
	A9	26	20	I	ADC analog input A9
	–	AVSS	AVSS	I	ADC analog input A10
	–	AVSS	AVSS	I	ADC analog input A11
	–	AVSS	AVSS	I	ADC analog input A12
	–	AVSS	AVSS	I	ADC analog input A13
	A14	2	2	I	ADC analog input A14
	A15	3	–	I	ADC analog input A15
	VREF+	5	4	O	Output of positive reference voltage
	VREF-	4	3	O	Output of negative reference voltage
	VeREF+	5	4	I	Input for an external positive reference voltage to the ADC
	VeREF-	4	3	I	Input for an external negative reference voltage to the ADC
Clock	ACLK	54, 66	45, 52	O	ACLK output
	HFXIN	10	9	I	Input for high-frequency crystal oscillator HFXT
	HFXOUT	11	10	O	Output for high-frequency crystal oscillator HFXT
	LFXIN	7	6	I	Input for low-frequency crystal oscillator LFXT
	LFXOUT	8	7	O	Output of low-frequency crystal oscillator LFXT
	MCLK	52, 64	43, 50	O	MCLK output
	SMCLK	53, 65	44, 51	O	SMCLK output

(1) N/A = not available

(2) I = input, O = output, P = power

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
Comparator	C0	4	3	I	Comparator input C0
	C1	5	4	I	Comparator input C1
	C2	31	25	I	Comparator input C2
	C3	32	26	I	Comparator input C3
	Not connected	4	3	I	Comparator input C4
	Not connected	4	3	I	Comparator input C5
	Not connected	4	3	I	Comparator input C6
	Not connected	4	3	I	Comparator input C7
	C8	25	19	I	Comparator input C8
	C9	26	20	I	Comparator input C9
	C10	17	13	I	Comparator input C10
	C11	18	14	I	Comparator input C11
	C12	19	15	I	Comparator input C12
	C13	20	16	I	Comparator input C13
	C14	2	2	I	Comparator input C14
	C15	3	–	I	Comparator input C15
	COUT	2, 51, 66	2, 42, 52	O	Comparator output
DMA	DMAE0	17, 42, 65	13, 51	I	External DMA trigger
Debug	SBWTCK	15	11	I	Spy-Bi-Wire input clock
	SBWTDIO	16	12	I/O	Spy-Bi-Wire data input/output
	SRCPUOFF	20	16	O	Low-power debug: CPU Status register bit CPUOFF
	SROSCOFF	19	15	O	Low-power debug: CPU Status register bit OSCOFF
	SRSCG0	18	14	O	Low-power debug: CPU Status register bit SCG0
	SRSCG1	17	13	O	Low-power debug: CPU Status register bit SCG1
	TCK	20	16	I	Test clock
	TCLK	18	14	I	Test clock input
	TDI	18	14	I	Test data input
	TDO	17	13	O	Test data output port
	TEST	15	11	I	Test mode pin – select digital I/O on JTAG pins
	TMS	19	15	I	Test mode select
GPIO, P1	P1.0	4	3	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.1	5	4	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.2	25	19	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.3	26	20	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.4	31	25	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.5	32	26	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.6	29	23	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.7	30	24	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
GPIO, P2	P2.0	27	21	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.1	28	22	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.2	2	2	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.3	3	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.4	12	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.5	23	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.6	13	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.7	14	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO, P3	P3.0	24	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.1	33	27	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.2	63	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.3	64	50	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.4	65	51	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.5	66	52	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.6	75	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.7	76	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO, P4	P4.0	34	28	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.1	35	29	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.2	36	30	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.3	37	31	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.4	38	32	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.5	39	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.6	40	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.7	42	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
GPIO, P5	P5.0	43	34	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.1	44	35	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.2	45	36	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.3	46	37	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.4	47	38	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.5	48	39	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.6	49	40	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.7	50	41	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO, P6	P6.0	51	42	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.1	56	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.2	57	47	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.3	60	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.4	52	43	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.5	53	44	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.6	54	45	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.7	62	–	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO, P7	P7.0	55	46	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO, PJ	PJ.0	17	13	I/O	General-purpose digital I/O
	PJ.1	18	14	I/O	General-purpose digital I/O
	PJ.2	19	15	I/O	General-purpose digital I/O
	PJ.3	20	16	I/O	General-purpose digital I/O
	PJ.4	7	6	I/O	General-purpose digital I/O
	PJ.5	8	7	I/O	General-purpose digital I/O
	PJ.6	10	9	I/O	General-purpose digital I/O
	PJ.7	11	10	I/O	General-purpose digital I/O
I ² C	UCB0SCL	30	24	I/O	I ² C clock – eUSCI_B0 I ² C mode
	UCB0SDA	29	23	I/O	I ² C data – eUSCI_B0 I ² C mode
	UCB1SCL	49, 76	40	I/O	I ² C clock – eUSCI_B1 I ² C mode
	UCB1SDA	48, 75	39	I/O	I ² C data – eUSCI_B1 I ² C mode

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
LCD	COM0	52	–	O	LCD common output COM0 for LCD backplane
	COM1	53	–	O	LCD common output COM1 for LCD backplane
	COM2	54	–	O	LCD common output COM2 for LCD backplane
	COM3	66	–	O	LCD common output COM3 for LCD backplane
	COM4	62	–	O	LCD common output COM4 for LCD backplane
	COM5	63	–	O	LCD common output COM5 for LCD backplane
	COM6	65	–	O	LCD common output COM6 for LCD backplane
	COM7	60	–	O	LCD common output COM7 for LCD backplane
	LDCAP	61	–	I/O	LCD capacitor connection CAUTION: LDCAP/R33 must be connected to DVSS if not used.
	LCDREF	57	–	I	External reference voltage input for regulated LCD voltage
	R03	56	–	I/O	Input/output port of lowest analog LCD voltage (V5)
	R13	57	–	I/O	Input/output port of third most positive analog LCD voltage (V3 or V4)
	R23	60	–	I/O	Input/output port of second most positive analog LCD voltage (V2)
	R33	61	–	I/O	Input/output port of most positive analog LCD voltage (V1) CAUTION: LDCAP/R33 must be connected to DVSS if not used.

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
LCD	S0	51	–	O	LCD segment output 0
	S1	50	–	O	LCD segment output 1
	S2	49	–	O	LCD segment output 2
	S3	48	–	O	LCD segment output 3
	S4	47	–	O	LCD segment output 4
	S5	46	–	O	LCD segment output 5
	S6	45	–	O	LCD segment output 6
	S7	44	–	O	LCD segment output 7
	S8	43	–	O	LCD segment output 8
	S9	42	–	O	LCD segment output 9
	S10	40	–	O	LCD segment output 10
	S11	39	–	O	LCD segment output 11
	S12	38	–	O	LCD segment output 12
	S13	37	–	O	LCD segment output 13
	S14	36	–	O	LCD segment output 14
	S15	35	–	O	LCD segment output 15
	S16	30	–	O	LCD segment output 16
	S17	29	–	O	LCD segment output 17
	S18	28	–	O	LCD segment output 18
	S19	27	–	O	LCD segment output 19
	S20	24	–	O	LCD segment output 20
	S21	23	–	O	LCD segment output 21
	S22	14	–	O	LCD segment output 22
	S23	13	–	O	LCD segment output 23
	S24	12	–	O	LCD segment output 24
	S25	64	–	O	LCD segment output 25
	S26	66	–	O	LCD segment output 26
	S27	65	–	O	LCD segment output 27
	S28	63	–	O	LCD segment output 28
	S29	62	–	O	LCD segment output 29
	S30	55	–	O	LCD segment output 30
	S31	54	–	O	LCD segment output 31
	S32	57	–	O	LCD segment output 32
	S33	56	–	O	LCD segment output 33
	S34	53	–	O	LCD segment output 34
	S35	75	–	O	LCD segment output 35
	S36	76	–	O	LCD segment output 36
MTIF	MTIF_PIN_EN	34	28	I	Meter test Interface pin enable
	MTIF_OUT_IN	33	27	I/O	Meter test Interface In/Out

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
Power	AVCC1	1	1	P	Analog power supply
	AVSS1	80	64	P	Analog ground supply
	AVSS2	6	5	P	Analog ground supply
	AVSS3	9	8	P	Analog ground supply
	AVSS4	77	61	P	Analog ground supply
	DVCC1	22	18	P	Digital power supply
	DVCC3	59	49	P	Digital power supply
	DVSS1	21	17	P	Digital ground supply
	DVSS2	41	33	P	Digital ground supply
	DVSS3	58	48	P	Digital ground supply
	PVCC	70, 71	56, 57	P	USS power supply
	PVSS	69, 72	55, 58	P	USS ground supply
RTC	RTCCLK	34, 56	28	O	RTC clock calibration output
SPI	UCA0CLK	2, 35	2, 29	I/O	Clock signal input – eUSCI_A0 SPI slave mode Clock signal output – eUSCI_A0 SPI master mode
	UCA0SIMO	13, 37	31	I/O	Slave in/master out – eUSCI_A0 SPI mode
	UCA0SOMI	14, 38	32	I/O	Slave out/master in – eUSCI_A0 SPI mode
	UCA0STE	3, 36	30	I/O	Slave transmit enable – eUSCI_A0 SPI mode
	UCA1CLK	4, 27	3, 21	I/O	Clock signal input – eUSCI_A1 SPI slave mode Clock signal output – eUSCI_A1 SPI master mode
	UCA1SIMO	25	19	I/O	Slave in/master out – eUSCI_A1 SPI mode
	UCA1SOMI	26	20	I/O	Slave out/master in – eUSCI_A1 SPI mode
	UCA1STE	5, 28	4, 22	I/O	Slave transmit enable – eUSCI_A1 SPI mode
	UCA2CLK	45	36	I/O	Clock signal input – eUSCI_A2 SPI slave mode Clock signal output – eUSCI_A2 SPI master mode
	UCA2SIMO	19, 43	34	I/O	Slave in/master out – eUSCI_A2 SPI mode
	UCA2SOMI	20, 44	35	I/O	Slave out/master in – eUSCI_A2 SPI mode
	UCA2STE	46	37	I/O	Slave transmit enable – eUSCI_A2 SPI mode
	UCA3CLK	30	24	I/O	Clock signal input – eUSCI_A3 SPI slave mode Clock signal output – eUSCI_A3 SPI master mode
	UCA3SIMO	27, 36	21, 30	I/O	Slave in/master out – eUSCI_A3 SPI mode
	UCA3SOMI	28, 35	22, 29	I/O	Slave out/master in – eUSCI_A3 SPI mode
	UCA3STE	29	23	I/O	Slave transmit enable – eUSCI_A3 SPI mode
	UCB0CLK	32	26	I/O	Clock signal input – eUSCI_B0 SPI slave mode Clock signal output – eUSCI_B0 SPI master mode
	UCB0SIMO	29	23	I/O	Slave in/master out – eUSCI_B0 SPI mode
	UCB0SOMI	30	24	I/O	Slave out/master in – eUSCI_B0 SPI mode
	UCB0STE	31	25	I/O	Slave transmit enable – eUSCI_B0 SPI mode
	UCB1CLK	47	38	I/O	Clock signal input – eUSCI_B1 SPI slave mode Clock signal output – eUSCI_B1 SPI master mode
	UCB1SIMO	48, 75	39	I/O	Slave in/master out – eUSCI_B1 SPI mode
	UCB1SOMI	49, 76	40	I/O	Slave out/master in – eUSCI_B1 SPI mode
	UCB1STE	50	41	I/O	Slave transmit enable – eUSCI_B1 SPI mode
System	NMI	16	12	I	Nonmaskable interrupt input
	RST	16	12	I/O	Reset input active low

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
Timer	TA0.0	3	–	I/O	TA0 CCR0 capture: CCI0A input, compare: Out0
	TA0.0	47	38	I/O	TA0 CCR0 capture: CCI0B input, compare: Out0
	TA0.1	62	–	I/O	TA0 CCR1 capture: CCI1A input, compare: Out1
	TA0.2	50	41	I/O	TA0 CCR2 capture: CCI2A input, compare: Out2
	TA0.2	23	–	O	TA0 compare: Out2 enabled by COUT
	TA0CLK	12, 39, 51	42	I	TA0 input clock
	TA1.0	4	3	I/O	TA1 CCR0 capture: CCI0A input, compare: Out0
	TA1.0	55	46	I/O	TA1 CCR0 capture: CCI0B input, compare: Out0
	TA1.0	25	19	O	TA1 CCR0 compare: Out0
	TA1.1	63	–	I/O	TA1 CCR1 capture: CCI1A input, compare: Out1
	TA1.1	26	20	O	TA1 CCR1 compare: Out1
	TA1.2	13	–	I/O	TA1 CCR2 capture: CCI2A input, compare: Out2
	TA1.2	55	46	O	TA1 CCR2 compare: Out2
	TA1.2C	13	–	O	TA1 CCR2 compare: Out2 enabled by COUT
	TA1CLK	12, 33, 39	27	I	TA1 input clock
	TA4.0	5	4	I/O	TA4 CCR0 capture: CCI0A input, compare: Out0
	TA4.0	23	–	I/O	TA4 CCR0 capture: CCI0B input, compare: Out0
	TA4.0	47	38	O	TA4 CCR0 compare: Out0
	TA4.1	14	–	I/O	TA4CCR1 capture: CCI1B input, compare: Out1
	TA4.1	48	39	I/O	TA4 CCR1 capture: CCI1A input, compare: Out1
	TA4.1	34	28	O	TA4 CCR1 compare: Out1
	TA4.1C	14	–	O	TA4 CCR1 compare: Out1 enabled by COUT
	TA4CLK	18, 40	14	I	TA4 input clock
	TB0.0	43	34	I/O	TB0 CCR0 capture: CCI0B input, compare: Out0
	TB0.0	24	–	I/O	TB0 CCR0 capture: CCI0A input, compare: Out0
	TB0.1	33	27	I/O	TB0 CCR1 capture: CCI1A input, compare: Out1
	TB0.1	44	35	O	TB0 CCR1 compare: Out1
	TB0.2	76	–	I/O	TB0 CCR2 capture: CCI2A input, compare: Out2
	TB0.2	45	36	O	TB0 CCR2 compare: Out2
	TB0.3	46	37	I/O	TB0 CCR3 capture: CCI3A input, compare: Out3
	TB0.3	64	50	I/O	TB0 CCR3 capture: CCI3B input, compare: Out3
	TB0.4	31	25	I/O	TB0 CCR4 capture: CCI4A input, compare: Out4
	TB0.4	35	29	I/O	TB0 CCR4 capture: CCI4B input, compare: Out4
	TB0.5	32	26	I/O	TB0 CCR5 capture: CCI5A input, compare: Out5
	TB0.5	36	30	I/O	TB0CCR5 capture: CCI5B input, compare: Out5
	TB0.6	75	–	I/O	TB0 CCR6 capture: CCI6B input, compare: Out6
	TB0.6	20	16	I/O	TB0 CCR6 capture: CCI6A input, compare: Out6
	TB0CLK	12, 40, 57	47	I	TB0 clock input
	TB0OUTH	19, 49, 76	15	I	Switch all PWM outputs high impedance input – TB0

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. ⁽¹⁾		PIN TYPE ⁽²⁾	DESCRIPTION
		80-PIN PN	64-PIN PM OR RGC		
UART	UCA0RXD	14, 38	32	I	Receive data – eUSCI_A0 UART mode
	UCA0TXD	13, 37	31	O	Transmit data – eUSCI_A0 UART mode
	UCA1RXD	26	20	I	Receive data – eUSCI_A1 UART mode
	UCA1TXD	25	19	O	Transmit data – eUSCI_A1 UART mode
	UCA2RXD	20, 44	16, 35	I	Receive data – eUSCI_A2 UART mode
	UCA2TXD	19, 43	15, 34	O	Transmit data – eUSCI_A2 UART mode
	UCA3RXD	28, 35	22, 29	I	Receive data – eUSCI_A3 UART mode
	UCA3TXD	27, 36	21, 30	O	Transmit data – eUSCI_A3 UART mode
USS_A	USSTRG	30	24	I	USS UUPS trigger
	USSXTIN	78	62	I	Input for an oscillator USSXT
	USSXTOUT	79	63	O	Output for an oscillator USSXT
	USSXT_BOUT	75, 10	9	O	Buffered output clock of USSXT
	CH0_IN	74	60	I	USS Channel 0 RX
	CH0_OUT	73	59	I/O	USS Channel 0 TX
	CH1_IN	67	53	I	USS Channel 1 RX
	CH1_OUT	68	54	I/O	USS Channel 1 TX
	XPB0	55	46	O	External bias output
	XPB1	64	50	O	External bias output

4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see 节 6.14.

4.5 Buffer Type

表 4-3 describes the buffer types that are referenced in 表 4-1.

表 4-3. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PULLUP (PU) OR PULLDOWN (PD)	NOMINAL PU OR PD STRENGTH (μ A)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
Analog ⁽¹⁾	3.0 V	N	N/A	N/A	N/A	See analog modules in <i>Specifications</i> for details
LVC MOS	3.0 V	Y ⁽²⁾	Programmable	See <i>General-Purpose I/Os</i>	See <i>Typical Characteristics – Outputs</i>	
Power (DVCC) ⁽³⁾	3.0 V	N	N/A	N/A	N/A	SVS enables hysteresis on DVCC
Power (AVCC) ⁽³⁾	3.0 V	N	N/A	N/A	N/A	
Power (PVCC) ⁽³⁾	3.0 V	N	N/A	N/A	N/A	
Power (DVSS and AVSS) ⁽³⁾	0 V	N	N/A	N/A	N/A	

(1) This is a switch, not a buffer.

(2) Only for input pins

(3) This is supply input, not a buffer.

4.6 Connection of Unused Pins

表 4-4 lists the correct termination of all unused pins.

表 4-4. Connection of Unused Pins⁽¹⁾

PIN	POTENTIAL	COMMENT
AVCC	DV _{CC}	
PVCC	DV _{CC}	
AVSS	DV _{SS}	
PVSS	DV _{SS}	
USS_CHx_IN, USS_CHx_OUT	DV _{SS}	
USSXTIN	DV _{SS}	
USSXTOUT	DV _{SS}	
Px.0 to Px.7	Open	Switched to port function, output direction (PxDIR.n = 1)
RST/NMI	DV _{CC} or V _{CC}	47-k Ω pullup or internal pullup selected with 10-nF (2.2 nF ⁽²⁾) pulldown
PJ.0/TDO PJ.1/TDI PJ.2/TMS PJ.3/TCK	Open	The JTAG pins are shared with general-purpose I/O function (PJ.x). If not being used, these should be switched to port function, output direction. When used as JTAG pins, these pins should remain open.
TEST	Open	This pin always has an internal pulldown enabled.

(1) For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px.0 to Px.7 pins.

(2) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	Min	Max	Unit
Voltage applied at DVCC and AVCC pins to V _{SS}	−0.3	4.1	V
Voltage applied at DVCC, AVCC, and PVCC pins to V _{SS}	−0.3	4.1	V
Voltage difference between DVCC and AVCC pins ⁽²⁾		±0.3	V
Voltage difference between DVCC, AVCC, and PVCC pins ⁽²⁾		±0.3	V
Voltage applied to CHx_IN	−0.3	1.65	V
Voltage applied to CHx_IN (duty cycle of 10% over 1ms)	−0.3	1.8	V
Voltage applied to USSXTIN (USSXTOUT)	−0.3	1.5	V
Voltage applied to any other pin ⁽³⁾	−0.3	V _{CC} + 0.3 V (4.1 V Max)	V
Diode current at any device pin		±2	mA
Storage temperature, T _{stg} ⁽⁴⁾	−40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
- (3) All voltages referenced to V_{SS}.
- (4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge (all except CHx_OUT terminals)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	
V _(ESD)	Electrostatic discharge (on CHx_OUT terminals)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

TYP data are based on $V_{CC} = 3.0\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins ^{(1) (2) (3) (4)}	1.8 ⁽⁵⁾		3.6	V
V_{CC}	Supply voltage range applied at PVCC pin ⁽¹⁾	2.2		3.6	V
V_{SS}	Supply voltage applied at all DVSS, AVSS, and PVSS pins.		0		V
T_A	Operating free-air temperature	-40		85	°C
C_{DVCC}	Capacitor value at DVCC ⁽⁶⁾	1 – 20%			μF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency) ⁽⁷⁾	No FRAM wait states (NWAITSx = 0)		0	8 ⁽⁸⁾
		With FRAM wait states (NWAITSx = 1) ⁽⁹⁾		0	16 ⁽¹⁰⁾
f_{LEA}	LEA processor frequency		0	16 ⁽¹⁰⁾	MHz
f_{ACLK}	Maximum ACLK frequency			50	kHz
f_{SMCLK}	Maximum SMCLK frequency			16 ⁽¹⁰⁾	MHz

- (1) TI recommends powering AVCC, DVCC, PVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference among AVCC, DVCC, PVCC must not exceed the limits specified under *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
- (2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond ($\pm 0.05\text{ V}/\mu\text{s}$). Following the data sheet recommendation for capacitor C_{DVCC} should limit the slopes accordingly.
- (3) Modules may have a different supply voltage range specification. Refer to the specification of the respective module in this data sheet.
- (4) USS module must be disabled if AVCC and DVCC are lower than 2.2V.
- (5) The minimum supply voltage is defined by the supervisor SVS levels. See the PMM SVS threshold parameters for the exact values.
- (6) As decoupling capacitor for each supply pin pair of DVCC/ DVSS and AVCC/AVSS, place a low-ESR ceramic capacitor of 100 nF (minimum) as close as possible (few millimeters) to the respective pin pairs, for PVCC/PVSS pair, place a low-ESR ceramic capacitor of 22 μF (minimum) as close as possible (few millimeters) to the respective pin pairs.
- (7) Modules may have a different maximum input clock specification. See the specification of each module in this data sheet.
- (8) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted.
- (9) Wait states only occur on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always executed without wait states.
- (10) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted. If a clock source with a higher typical value is used, the clock must be divided in the clock system.

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)^{(1) (2)}

PARAMETER	EXECUTION MEMORY	V _{CC}	FREQUENCY (f _{MCLK} = f _{SMCLK})										UNIT
			1 MHz 0 WAIT STATES (NWAITS _x = 0)		4 MHz 0 WAIT STATES (NWAITS _x = 0)		8 MHz 0 WAIT STATES (NWAITS _x = 0)		12 MHz 1 WAIT STATE (NWAITS _x = 1)		16 MHz 1 WAIT STATE (NWAITS _x = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{AM, FRAM_UNI} (Unified memory) ⁽³⁾	FRAM	3.0 V	225		665		1275		1550		1970		μA
I _{AM, FRAM} (0%) ^{(4) (5)}	FRAM 0% cache hit ratio	3.0 V	420		1455		2850		2330		3000		μA
I _{AM, FRAM} (50%) ^{(4) (5)}	FRAM 50% cache hit ratio	3.0 V	275		855	1022	1650	1888	1770	2041	2265	2606	μA
I _{AM, FRAM} (66%) ^{(4) (5)}	FRAM 66% cache hit ratio	3.0 V	220		650		1240	1443	1490	1735	1880	2197	μA
I _{AM, FRAM} (75%) ^{(4) (5)}	FRAM 75% cache hit ratio	3.0 V	192	261	535		1015	1170	1290	1490	1620	1870	μA
I _{AM, FRAM} (100%) ^{(4) (5)}	FRAM 100% cache hit ratio	3.0 V	125		237		450		670		790		μA
I _{AM, RAM} ^{(6) (5)}	RAM	3.0 V	140		323		590		880		1070		μA
I _{AM, RAM only} ^{(7) (5)}	RAM	3.0 V	90	182	292		540		830		1020	1313	μA

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Characterized with program executing typical data processing.

$f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency, except for 12 MHz. For 12 MHz, $f_{DCO} = 24$ MHz and $f_{MCLK} = f_{SMCLK} = f_{DCO}/2$.

At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ($f_{MCLK,eff}$) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.

The following equation can be used to compute $f_{MCLK,eff}$:

$$f_{MCLK,eff} = f_{MCLK} / [\text{wait states} \times (1 - \text{cache hit ratio}) + 1]$$

For example, with 1 wait state and 75% cache hit ratio, $f_{MCLK,eff} = f_{MCLK} / [1 \times (1 - 0.75) + 1] = f_{MCLK} / 1.25$.

(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.

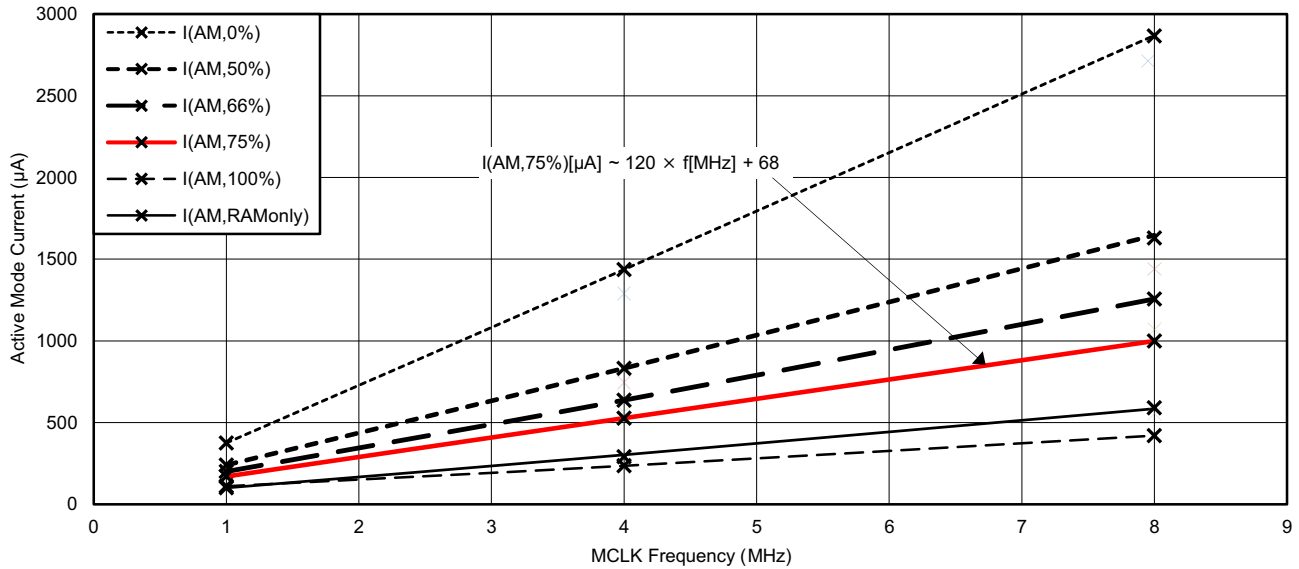
(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

(5) See for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in [Section 5.4](#).

(6) Program and data reside entirely in RAM. All execution is from RAM.

(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

5.5 Typical Characteristics, Active Mode Supply Currents



- A. I_{AM} , cache hit ratio): Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.
- B. I_{AM} , RAM only): Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

图 5-1. Typical Active Mode Supply Currents, No Wait States

5.6 Low-Power Mode (LPM0, LPM1) Supply Currents Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾

PARAMETER	V _{CC}	FREQUENCY (f _{SMCLK})										UNIT
		1 MHz		4 MHz		8 MHz		12 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{LPM0}	2.2 V	80		115		180		276		250		μA
	3.0 V	95	148	125	178	190	245	286	340	265	316	
I _{LPM1}	2.2 V	40		70		136		230		205		μA
	3.0 V	40	70	70		136		235		210	250	

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

$f_{ACLK} = 32768$ Hz, $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO}$ at specified frequency, except for 12 MHz. For 12 MHz, $f_{DCO} = 24$ MHz and $f_{MCLK} = f_{SMCLK} = f_{DCO} / 2$.

5.7 Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	TEMPERATURE								UNIT
			−40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{LPM2,XT12}	Low-power mode 2, 12-pF crystal ^{(1) (2) (3)}	2.2 V	0.8		1.3		4.1		10.8		μA
		3 V	0.8		1.3		4.1		10.8		
I _{LPM2,XT3.7}	Low-power mode 2, 3.7-pF crystal ^{(1) (4) (3)}	2.2 V	0.6		1.2		4.0		10.7		μA
		3 V	0.6		1.2		4.0		10.7		
I _{LPM2,VLO}	Low-power mode 2, VLO, includes SVS ⁽⁵⁾	2.2 V	0.5		1.0		3.8		10.5		μA
		3 V	0.5		1.0		3.8		10.5		
I _{LPM3,XT12}	Low-power mode 3, 12-pF crystal, includes SVS ^{(1) (2) (6)}	2.2 V	0.8	1.1	1.0		2.2		4.5	10.1	μA
		3 V	0.8		1.0		2.2		4.5		
I _{LPM3,XT3.7}	Low-power mode 3, 3.7-pF crystal, excludes SVS ^{(1) (4) (7)}	2.2 V	0.5		0.7		2.1		4.4	9.8	μA
		3 V	0.5		0.7		2.1		4.4	9.8	
I _{LPM3,VLO}	Low-power mode 3, VLO, excludes SVS ⁽⁸⁾	2.2 V	0.4		0.5	1.2	1.9		4.2	9.6	μA
		3 V	0.4		0.5		1.9		4.2		
I _{LPM3,VLO, RAMoff}	Low-power mode 3, VLO, excludes SVS, RAM powered-down completely ⁽⁸⁾	2.2 V	0.36		0.47	1.1	1.4	2.9	2.6	8.2	μA
		3 V	0.36		0.47		1.4		2.6		
I _{LPM4,SVS}	Low-power mode 4, includes SVS ⁽⁹⁾	2.2 V	0.5		0.6	1.2	1.9		4.3	9.7	μA
		3 V	0.5	0.8	0.6		1.9		4.3		

- (1) Not applicable for devices with HF crystal oscillator only.
- (2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
- (3) Low-power mode 2, crystal oscillator test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2), f_{XT1} = 32768 Hz, f_{ACLK} = f_{XT1} , f_{MCLK} = f_{SMCLK} = 0 MHz
- (4) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
- (5) Low-power mode 2, VLO test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2), f_{XT1} = 0 Hz, f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = 0 MHz
- (6) Low-power mode 3, 12-pF crystal including SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3), f_{XT1} = 32768 Hz, f_{ACLK} = f_{XT1} , f_{MCLK} = f_{SMCLK} = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
- (7) Low-power mode 3, 3.7-pF crystal excluding SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3), f_{XT1} = 32768 Hz, f_{ACLK} = f_{XT1} , f_{MCLK} = f_{SMCLK} = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
- (8) Low-power mode 3, VLO excluding SVS test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). RAM disabled (RCCTL0 = 5A55h). Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3), f_{XT1} = 0 Hz, f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
- (9) Low-power mode 4 including SVS test conditions:
Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4), f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, f_{MCLK} = f_{SMCLK} = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.

Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	TEMPERATURE								UNIT
			-40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{LPM4}	Low-power mode 4, excludes SVS ⁽¹⁰⁾	2.2 V	0.3		0.4	1.1	1.7		4.0	9.4	μA
		3 V	0.3		0.4		1.7		4.0		
I _{LPM4,RAMoff}	Low-power mode 4, excludes SVS, RAM powered-down completely ⁽¹⁰⁾	2.2 V	0.3		0.37	1.0	1.2	2.8	2.5	8	μA
		3 V	0.3		0.37		1.2		2.5		
I _{IDLE,GroupA}	Additional idle current if one or more modules from Group A (see 表 6-3) are activated in LPM3 or LPM4	3 V			0.02				0.3		μA
I _{IDLE,GroupB}	Additional idle current if one or more modules from Group B (see 表 6-3) are activated in LPM3 or LPM4	3 V			0.02				0.35		μA
I _{IDLE,GroupC}	Additional idle current if one or more modules from Group C (see 表 6-3) are activated in LPM3 or LPM4	3 V			0.02				0.38		μA

(10) Low-power mode 4 excluding SVS test conditions:

Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4), f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, f_{MCLK} = f_{SMCLK} = 0 MHz

Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.

5.8 Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	TEMPERATURE (T _A)								UNIT
			-40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{LPM3,XT12} LCD, ext. bias	Low-power mode 3 (LPM3) current,12 pF crystal, LCD 4-mux mode, external biasing, excludes SVS ^{(1) (2)}	3.0 V	0.9		1.1		2.5		5.1		μA
I _{LPM3,XT12} LCD, int. bias	Low-power mode 3 (LPM3) current,12 pF crystal, LCD 4-mux mode, internal biasing, charge pump disabled, excludes SVS ^{(1) (3)}	3.0 V	1.3		1.4	2.0	2.2	4.5	4.9	12.5	μA

(1) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),

f_{XT1} = 32768 Hz, f_{ACLK} = f_{XT1} , f_{MCLK} = f_{SMCLK} = 0 MHz

Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current - idle current of Group containing LCD module already included. Refer to the idle currents specified for the respective peripheral groups.

(2) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)

Current through external resistors not included (voltage levels are supplied by test equipment).

Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(3) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)

Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current (*continued*)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	TEMPERATURE (T _A)								UNIT
			-40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{LPM3,XT12} LCD,CP	Low-power mode 3 (LPM3) current,12 pF crystal, LCD 4-mux mode, internal biasing, charge pump enabled, 1/3 bias, excludes SVS ⁽¹⁾ (4)	2.2 V	3.6		4		5.1		8.1		μA
		3.0 V	3.4		3.7		4.9		8.1		μA

(4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDPEN = 1 (charge pump enabled), VLCDx = 1000 ($V_{LCD} = 3$ V typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD} = 32768$ Hz / 32 / 4 = 256 Hz) Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

5.9 Low-Power Mode (LPMx.5) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	TEMPERATURE (T _A)								UNIT
			−40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{LPM3.5,XT12}	Low-power mode 3.5, 12-pF crystal including SVS ⁽¹⁾ (2) (3)	2.2 V	0.45		0.5		0.55		0.75		μA
		3.0 V	0.45		0.5		0.55		0.75		
I _{LPM3.5,XT3.7}	Low-power mode 3.5, 3.7-pF crystal excluding SVS ⁽¹⁾ (4) (5)	2.2 V	0.3		0.35		0.4		0.65		μA
		3.0 V	0.3		0.35		0.4		0.65		
I _{LPM4.5,SVS}	Low-power mode 4.5, including SVS ⁽⁶⁾	2.2 V	0.23		0.2		0.28		0.4		μA
		3.0 V	0.23		0.2		0.28		0.4		
I _{LPM4.5}	Low-power mode 4.5, excluding SVS ⁽⁷⁾	2.2 V	0.035		0.045		0.075		0.15		μA
		3.0 V	0.035		0.045		0.075		0.15		

(1) Not applicable for devices with HF crystal oscillator only.

(2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.

(3) Low-power mode 3.5, 1-pF crystal including SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz

(4) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.

(5) Low-power mode 3.5, 3.7-pF crystal excluding SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz

(6) Low-power mode 4.5 including SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz

(7) Low-power mode 4.5 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz

5.10 Typical Characteristics, Low-Power Mode Supply Currents

图 5-2, 图 5-3, 图 5-4, 和 图 5-5 show the supply current vs temperature typical characteristics for selected low-power modes.

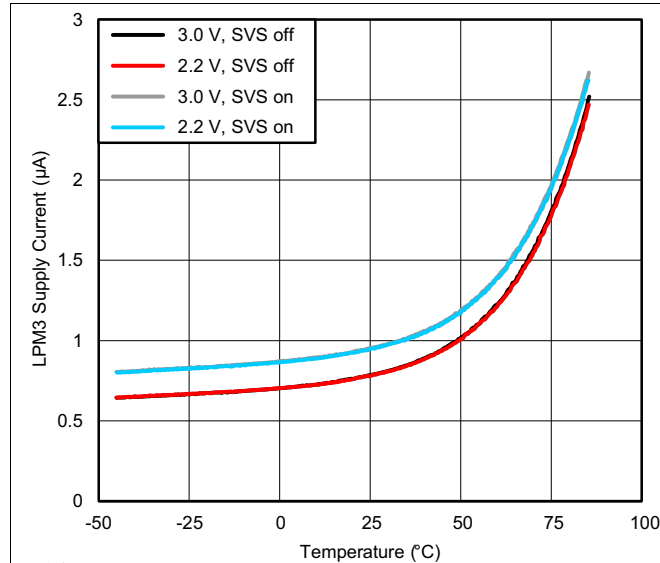


图 5-2. LPM3 Supply Current vs Temperature (LPM3,XT3.7)

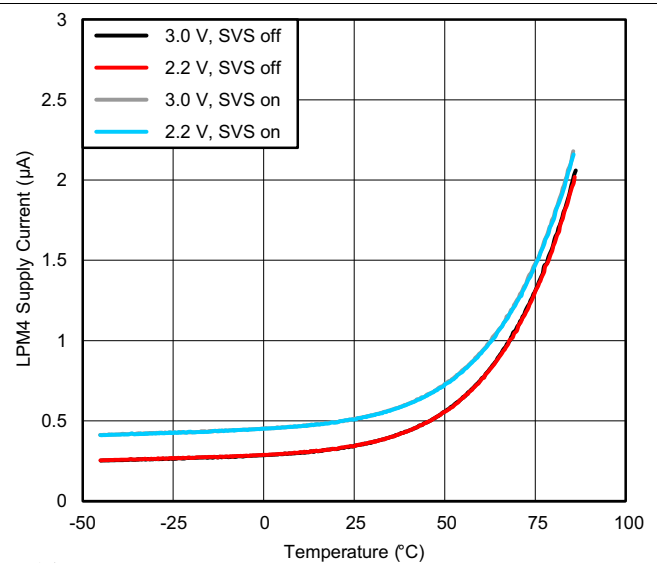


图 5-3. LPM4 Supply Current vs Temperature (LPM4,SVS)

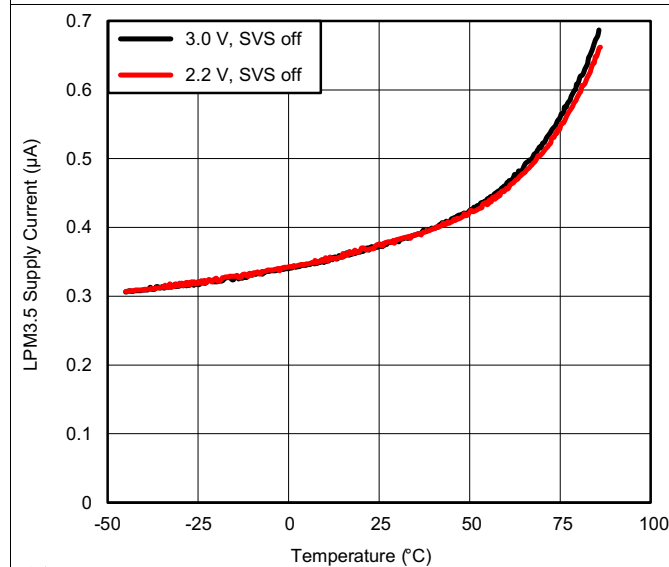


图 5-4. LPM3.5 Supply Current vs Temperature (LPM3.5,XT3.7)

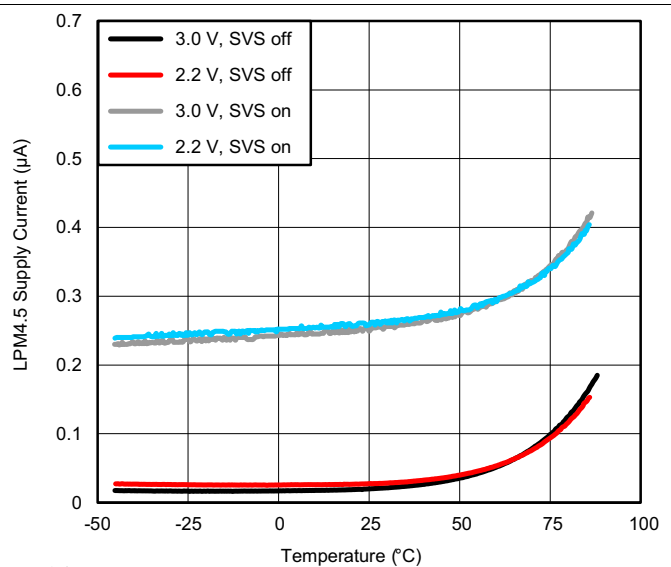


图 5-5. LPM4.5 Supply Current vs Temperature (LPM4.5)

5.11 Typical Characteristics, Current Consumption per Module⁽¹⁾

MODULE	TEST CONDITIONS	REFERENCE CLOCK	MIN	TYP	MAX	UNIT
Timer_A		Module input clock		2.5		μA/MHz
Timer_B		Module input clock		3.7		μA/MHz
eUSCI_A	UART mode	Module input clock		6.3	7.0	μA/MHz
eUSCI_A	SPI mode	Module input clock		4.4	4.8	μA/MHz
eUSCI_B	SPI mode	Module input clock		4.4		μA/MHz
eUSCI_B	I ² C mode, 100 kbaud	Module input clock		4.4		μA/MHz
RTC_C		32 kHz		100		nA
MPY	Only from start to end of operation	MCLK		28		μA/MHz
CRC16	Only from start to end of operation	MCLK		3.3		μA/MHz
CRC32	Only from start to end of operation	MCLK		3.3		μA/MHz
LEA	256 Point Complex FFT, Data = non zero	MCLK	70	78	85	uA/MHz
LEA	256 Point Complex FFT, Data = zero	MCLK		55	60	uA/MHz
MTIF	Generator and counter are enabled at 256 Hz, no terminal activity. Pulse rate:15 pulses	LFXT		0.20		uA

(1) For other module currents not listed here, see the module-specific parameter sections.

5.12 Thermal Resistance Characteristics

THERMAL METRIC		PACKAGE	VALUE	UNIT
R _{θJA}	Junction-to-ambient thermal resistance, still air	QFP-80 (PN)	53.3	°C/W
R _{θJC(TOP)}	Junction-to-case (top) thermal resistance		15.2	°C/W
R _{θJB}	Junction-to-board thermal resistance		28.4	°C/W
Ψ _{JB}	Junction-to-board thermal characterization parameter		28.0	°C/W
Ψ _{JT}	Junction-to-top thermal characterization parameter		0.7	°C/W
R _{θJC(BOTTOM)}	Junction-to-case (bottom) thermal resistance		n/a	°C/W
R _{θJA}	Junction-to-ambient thermal resistance, still air	QFP-64 (PM)	56.6	°C/W
R _{θJC(TOP)}	Junction-to-case (top) thermal resistance		16.4	°C/W
R _{θJB}	Junction-to-board thermal resistance		27.8	°C/W
Ψ _{JB}	Junction-to-board thermal characterization parameter		27.5	°C/W
Ψ _{JT}	Junction-to-top thermal characterization parameter		0.8	°C/W
R _{θJC(BOTTOM)}	Junction-to-case (bottom) thermal resistance		n/a	°C/W
R _{θJA}	Junction-to-ambient thermal resistance, still air	RGC-64	24.7	°C/W
R _{θJC(TOP)}	Junction-to-case (top) thermal resistance		12.3	°C/W
R _{θJB}	Junction-to-board thermal resistance		8.8	°C/W
Ψ _{JB}	Junction-to-board thermal characterization parameter		8.7	°C/W
Ψ _{JT}	Junction-to-top thermal characterization parameter		0.1	°C/W
R _{θJC(BOTTOM)}	Junction-to-case (bottom) thermal resistance		n/a	°C/W

5.13 Timing and Switching Characteristics

5.13.1 Power Supply Sequencing

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

表 5-1 lists the power ramp requirements for brownout and power up.

表 5-1. Brownout and Device Reset Power Ramp Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{VCC_BOR-} Brownout power-down level ⁽¹⁾	dV _{CC} /d _t < 3 V/s	0.7	1.66	V
V _{VCC_BOR+} Brownout power-up level ⁽¹⁾	dV _{CC} /d _t < 3 V/s ⁽²⁾	0.79	1.68	V

- (1) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (± 0.05 V/ μ s). Following the data sheet recommendation for capacitor C_{DVCC} should limit the slopes accordingly.
- (2) The brownout levels are measured with a slowly changing supply.

表 5-2 lists the characteristics of the SVS.

表 5-2. SVS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{SVSH,LPM} SVS _H current consumption, low power modes			170	300	nA
V _{SVSH-} SVS _H power-down level		1.75	1.80	1.85	V
V _{SVSH+} SVS _H power-up level		1.77	1.88	1.99	V
V _{SVSH_hys} SVS _H hysteresis		40		120	mV
t _{PD,SVSH, AM} SVS _H propagation delay, active mode	dV _{VCC} /dt = -10 mV/ μ s			10	μ s

5.13.2 Reset Timing

表 5-3 lists the requirements for the reset input.

表 5-3. Reset Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	V _{CC}	MIN	TYP	MAX	UNIT
t _(RST) External reset pulse duration on $\overline{\text{RST}}$ ⁽¹⁾	2.2 V, 3.0 V	2			μ s

- (1) Not applicable if $\overline{\text{RST}}$ /NMI pin configured as NMI.

5.13.3 Clock Specifications

Table 5-4 lists the characteristics of the low-frequency oscillator.

Table 5-4. Low-Frequency Crystal Oscillator, LFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{VCC,LFXT} Current consumption	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T _A = 25°C, C _{L,eff} = 3.7 pF, ESR ≈ 44 kΩ	3.0 V		180		nA
	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {1}, T _A = 25°C, C _{L,eff} = 6 pF, ESR ≈ 40 kΩ	3.0 V		185		nA
	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {2}, T _A = 25°C, C _{L,eff} = 9 pF, ESR ≈ 40 kΩ	3.0 V		225		nA
	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T _A = 25°C, C _{L,eff} = 12.5 pF, ESR ≈ 40 kΩ	3.0 V		330		nA
f _{LFXT} LFXT oscillator crystal frequency	LFXTBYPASS = 0			32768		Hz
DC _{LFXT} LFXT oscillator duty cycle	Measured at ACLK, f _{LFXT} = 32768 Hz		30%		70%	
f _{LFXT,SW} LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 ⁽²⁾ ⁽³⁾		10.5	32.768	50	kHz
DC _{LFXT, SW} LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		30%		70%	
OA _{LFXT} Oscillation allowance for LF crystals ⁽⁴⁾	LFXTBYPASS = 0, LFXTDRIVE = {1}, f _{LFXT} = 32768 Hz, C _{L,eff} = 6 pF			210		kΩ
	LFXTBYPASS = 0, LFXTDRIVE = {3}, f _{LFXT} = 32768 Hz, C _{L,eff} = 12.5 pF			300		
C _{LFXIN} Integrated load capacitance at LFXIN terminal ⁽⁵⁾ ⁽⁶⁾				2		pF
C _{LFXOUT} Integrated load capacitance at LFXOUT terminal ⁽⁵⁾ ⁽⁶⁾				2		pF

- (1) To improve EMI on the LFXT oscillator, observe the following guidelines:
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins LFXIN and LFXOUT.
 - Avoid running PCB traces underneath or adjacent to the LFXIN and LFXOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by DC_{LFXT, SW}.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For LFXTDRIVE = {0}, C_{L,eff} = 3.7 pF
 - For LFXTDRIVE = {1}, C_{L,eff} = 6 pF
 - For LFXTDRIVE = {2}, 6 pF ≤ C_{L,eff} ≤ 9 pF
 - For LFXTDRIVE = {3}, 9 pF ≤ C_{L,eff} ≤ 12.5 pF
- (5) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, C_{L,eff} can be computed as C_{IN} × C_{OUT} / (C_{IN} + C_{OUT}), where C_{IN} and C_{OUT} is the total capacitance at the LFXIN and LFXOUT terminals, respectively.
- (6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.

Table 5-4. Low-Frequency Crystal Oscillator, LFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{START,LFXT} Start-up time ⁽⁷⁾	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T _A = 25°C, C _{L,eff} = 3.7 pF	3.0 V		800		ms
	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T _A = 25°C, C _{L,eff} = 12.5 pF	3.0 V		1000		
f _{Fault,LFXT} Oscillator fault frequency ⁽⁸⁾ (9)			0		3500	Hz

(7) Includes start-up counter of 1024 clock cycles.

(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications may set the flag. A static condition or stuck at fault condition will set the flag.

(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the characteristics of the high-frequency oscillator.

Table 5-5. High-Frequency Crystal Oscillator, HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{DVCC,HFXT} HFXT oscillator crystal current HF mode at typical ESR	f _{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1 ⁽²⁾ , T _A = 25°C, C _{L,eff} = 18 pF, typical ESR, C _{shunt}	3.0 V		75		μA
	f _{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, T _A = 25°C, C _{L,eff} = 18 pF, typical ESR, C _{shunt}			120		
	f _{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, T _A = 25°C, C _{L,eff} = 18 pF, typical ESR, C _{shunt}			190		
	f _{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T _A = 25°C, C _{L,eff} = 18 pF, typical ESR, C _{shunt}			250		
f _{HFXT} HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 1 ^{(2) (3)}		4		8	MHz
	HFXTBYPASS = 0, HFFREQ = 2 ⁽³⁾		8.01		16	
	HFXTBYPASS = 0, HFFREQ = 3 ⁽³⁾		16.01		24	
DC _{HFXT} HFXT oscillator duty cycle	Measured at SMCLK, f _{HFXT} = 16 MHz		40%	50%	60%	
f _{HFXT,SW} HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1, HFFREQ = 0 ^{(4) (3)}		0.9		4	MHz
	HFXTBYPASS = 1, HFFREQ = 1 ^{(4) (3)}		4.01		8	
	HFXTBYPASS = 1, HFFREQ = 2 ^{(4) (3)}		8.01		16	
	HFXTBYPASS = 1, HFFREQ = 3 ^{(4) (3)}		16.01		24	

(1) To improve EMI on the HFXT oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins HFXIN and HFXOUT.
- Avoid running PCB traces underneath or adjacent to the HFXIN and HFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) HFFREQ = {0} is not supported for HFXT crystal mode of operation.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. Duty cycle requirements are defined by DC_{HFXT, SW}.

Table 5-5. High-Frequency Crystal Oscillator, HFXT (continued)over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
DC _{HFXT, SW}	HFXT oscillator logic-level square-wave input duty cycle	HFXTBYPASS = 1		40%		60%	
OA _{HFXT}	Oscillation allowance for HFXT crystals ⁽⁵⁾	HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1 ⁽²⁾ , f _{HFXT, HF} = 4 MHz, C _{L, eff} = 16 pF			450		Ω
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, f _{HFXT, HF} = 8 MHz, C _{L, eff} = 16 pF			320		
		HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, f _{HFXT, HF} = 16 MHz, C _{L, eff} = 16 pF			200		
		HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, f _{HFXT, HF} = 24 MHz, C _{L, eff} = 16 pF			200		
t _{START, HFXT}	Start-up time ⁽⁶⁾	f _{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1, T _A = 25°C, C _{L, eff} = 16 pF	3.0 V		1.6		ms
		f _{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T _A = 25°C, C _{L, eff} = 16 pF	3.0 V		0.6		
C _{HFXIN}	Integrated load capacitance at HFXIN terminal ^{(7) (8)}				2		pF
C _{HFXOUT}	Integrated load capacitance at HFXOUT terminal ^{(7) (8)}				2		pF
f _{Fault, HFXT}	Oscillator fault frequency ^{(9) (10)}			0		800	kHz

⁽⁵⁾ Oscillation allowance is based on a safety factor of 5 for recommended crystals.⁽⁶⁾ Includes start-up counter of 1024 clock cycles.⁽⁷⁾ This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, C_{L, eff} can be computed as C_{IN} × C_{OUT} / (C_{IN} + C_{OUT}), where C_{IN} and C_{OUT} is the total capacitance at the HFXIN and HFXOUT terminals, respectively.⁽⁸⁾ Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.⁽⁹⁾ Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition will set the flag.⁽¹⁰⁾ Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-6 lists the characteristics of the DCO.

Table 5-6. DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{DCO1}	DCO frequency range 1 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 0, DCORSEL = 1, DCOFSEL = 0			1	±3.5%	MHz
f _{DCO2.7}	DCO frequency range 2.7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 1			2.667	±3.5%	MHz
f _{DCO3.5}	DCO frequency range 3.5 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 2			3.5	±3.5%	MHz
f _{DCO4}	DCO frequency range 4 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 3			4	±3.5%	MHz
f _{DCO5.3}	DCO frequency range 5.3 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 4, DCORSEL = 1, DCOFSEL = 1			5.333	±3.5%	MHz

Table 5-6. DCO (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{DCO7}	DCO frequency range 7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 5, DCORSEL = 1, DCOFSEL = 2			7	±3.5%	MHz
f _{DCO8}	DCO frequency range 8 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 6, DCORSEL = 1, DCOFSEL = 3			8	±3.5%	MHz
f _{DCO16}	DCO frequency range 16 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 1, DCOFSEL = 4			16	±3.5% (1)	MHz
f _{DCO21}	DCO frequency range 21 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 5			21	±3.5% (1)	MHz
f _{DCO24}	DCO frequency range 24 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 6			24	±3.5% (1)	MHz
f _{DCO,DC}	Duty cycle	Measured at SMCLK, divide by 1, No external divide, all DCORSEL and DCOFSEL settings except DCORSEL = 1, DCOFSEL = 5 and DCORSEL = 1, DCOFSEL = 6		48	50	52	%
t _{DCO, JITTER}	DCO jitter	Based on f _{signal} = 10 kHz and DCO used for 12-bit SAR ADC sampling source. This achieves >74-dB SNR due to jitter; that is, limited by ADC performance.			2	3	ns
df _{DCO} /dT	DCO temperature drift ⁽²⁾		3.0 V		0.01		%/°C

(1) After a wakeup from LPM1, LPM2, LPM3, or LPM4, the DCO frequency f_{DCO} might exceed the specified frequency range for a few clock cycles by up to 5% before settling to the specified steady state frequency range.

(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

Table 5-7 lists the characteristics of the VLO.

Table 5-7. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{VLO}	Current consumption				100		nA
f _{VLO}	VLO frequency	Measured at ACLK		6	9.4	14	kHz
df _{VLO} /dT	VLO frequency temperature drift	Measured at ACLK ⁽¹⁾			0.2		%/°C
df _{VLO} /dV _{CC}	VLO frequency supply voltage drift	Measured at ACLK ⁽²⁾			0.7		%/V
f _{VLO,DC}	Duty cycle	Measured at ACLK		40	50	60	%

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8 lists the characteristics of the MODOSC.

Table 5-8. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption	Enabled		25		μA
f_{MODOSC}	MODOSC frequency		4.0	4.8	5.4	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift ⁽¹⁾			0.08		%/°C
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift ⁽²⁾			1.4		%/V
DC_{MODOSC}	Duty cycle (<i>excl. first clock cycle</i> ; $DC = t_{high} \times f$)	Measured at SMCLK, divide by 1	40	50	60	%

(1) Calculated using the box method: $(MAX(-40^{\circ}C \text{ to } 85^{\circ}C) - MIN(-40^{\circ}C \text{ to } 85^{\circ}C)) / MIN(-40^{\circ}C \text{ to } 85^{\circ}C) / (85^{\circ}C - (-40^{\circ}C))$

(2) Calculated using the box method: $(MAX(1.8 \text{ V to } 3.6 \text{ V}) - MIN(1.8 \text{ V to } 3.6 \text{ V})) / MIN(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$

5.13.4 Wake-up Characteristics

Table 5-9 lists the times required to wake up from LPM or reset.

Table 5-9. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP \text{ FRAM}}$	(Additional) wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from an LPM if immediate activation is selected for wake up				6	10	μs
$t_{WAKE-UP \text{ LPM0}}$	Wake-up time from LPM0 to active mode ⁽¹⁾		2.2 V, 3.0 V			$400 + 1.5 / f_{DCO}$	ns
$t_{WAKE-UP \text{ LPM1}}$	Wake-up time from LPM1 to active mode ⁽¹⁾		2.2 V, 3.0 V		6		μs
$t_{WAKE-UP \text{ LPM2}}$	Wake-up time from LPM2 to active mode ⁽¹⁾		2.2 V, 3.0 V		6		μs
$t_{WAKE-UP \text{ LPM3}}$	Wake-up time from LPM3 to active mode ⁽¹⁾		2.2 V, 3.0 V		$6.6 + 2.0 / f_{DCO}$	$9.6 + 2.5 / f_{DCO}$	μs
$t_{WAKE-UP \text{ LPM4}}$	Wake-up time from LPM4 to active mode ⁽¹⁾		2.2 V, 3.0 V		$6.6 + 2.0 / f_{DCO}$	$9.6 + 2.5 / f_{DCO}$	μs
$t_{WAKE-UP \text{ LPM3.5}}$	Wake-up time from LPM3.5 to active mode ⁽²⁾		2.2 V, 3.0 V		350	450	μs
$t_{WAKE-UP \text{ LPM4.5}}$	Wake-up time from LPM4.5 to active mode ⁽²⁾	SVSHE = 1	2.2 V, 3.0 V		350	450	μs
		SVSHE = 0	2.2 V, 3.0 V		0.4	0.8	ms
$t_{WAKE-UP \text{ RST}}$	Wake-up time from a $\overline{RST}$ pin triggered reset to active mode ⁽²⁾		2.2 V, 3.0 V		480	596	μs
$t_{WAKE-UP \text{ BOR}}$	Wake-up time from power-up to active mode ⁽²⁾		2.2 V, 3.0 V		0.5	1	ms

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge with MCLKREQEN = 1. This time includes the activation of the FRAM during wake up. With MCLKREQEN = 0, the externally observable MCLK clock is gated one additional cycle.

(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

Table 5-10 lists the typical charges used during wakeup.

Table 5-10. Typical Wake-up Charges

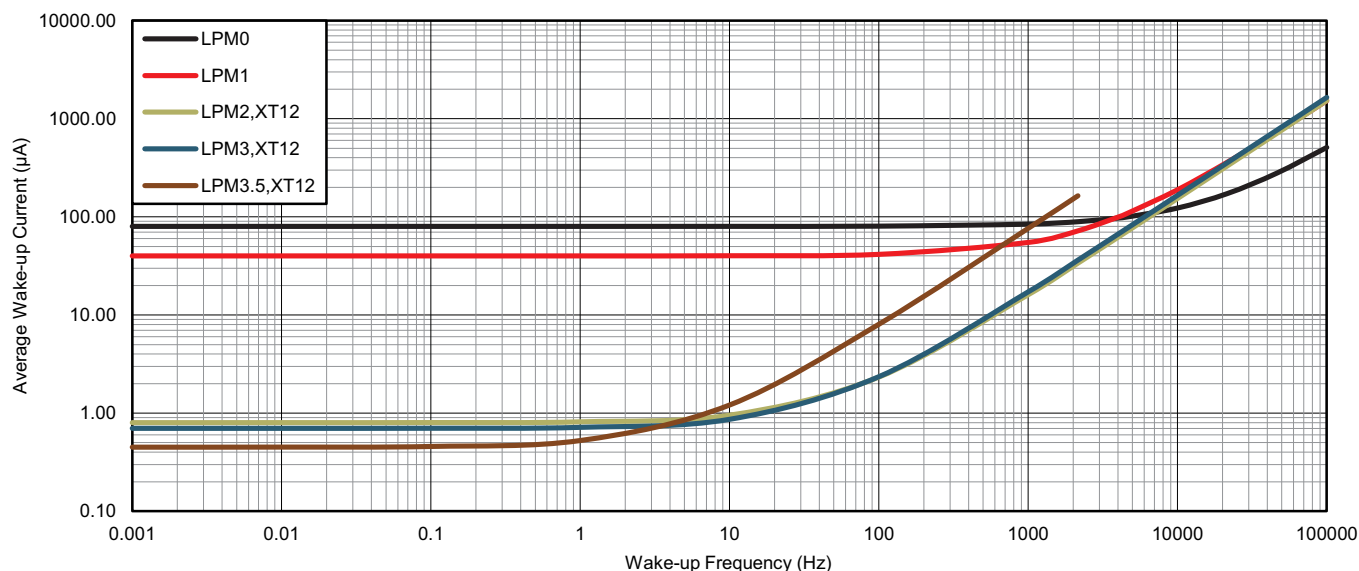
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q _{WAKE-UP FRAM}	Charge used for activating the FRAM in AM or during wakeup from LPM0 if previously disabled by the FRAM controller.			16.5		nAs
Q _{WAKE-UP LPM0}	Charge used to wake up from LPM0 to active mode (with FRAM active)			3.8		nAs
Q _{WAKE-UP LPM1}	Charge used to wake up from LPM1 to active mode (with FRAM active)			21		nAs
Q _{WAKE-UP LPM2}	Charge used to wake up from LPM2 to active mode (with FRAM active)			22		nAs
Q _{WAKE-UP LPM3}	Charge used to wake up from LPM3 to active mode (with FRAM active)			28		nAs
Q _{WAKE-UP LPM4}	Charge used to wake up from LPM4 to active mode (with FRAM active)			28		nAs
Q _{WAKE-UP LPM3.5}	Charge used to wake up from LPM3.5 to active mode ⁽²⁾			170		nAs
Q _{WAKE-UP LPM4.5}	Charge used to wake up from LPM4.5 to active mode ⁽²⁾	SVSHE = 1		173		nAs
		SVSHE = 0		171		
Q _{WAKE-UP-RESET}	Charge used for reset from $\overline{\text{RST}}$ or BOR event to active mode ⁽²⁾			148		nAs

(1) Charge used during the wake-up time from a given low-power mode to active mode. This does not include the energy required in active mode (for example, for an interrupt service routine).

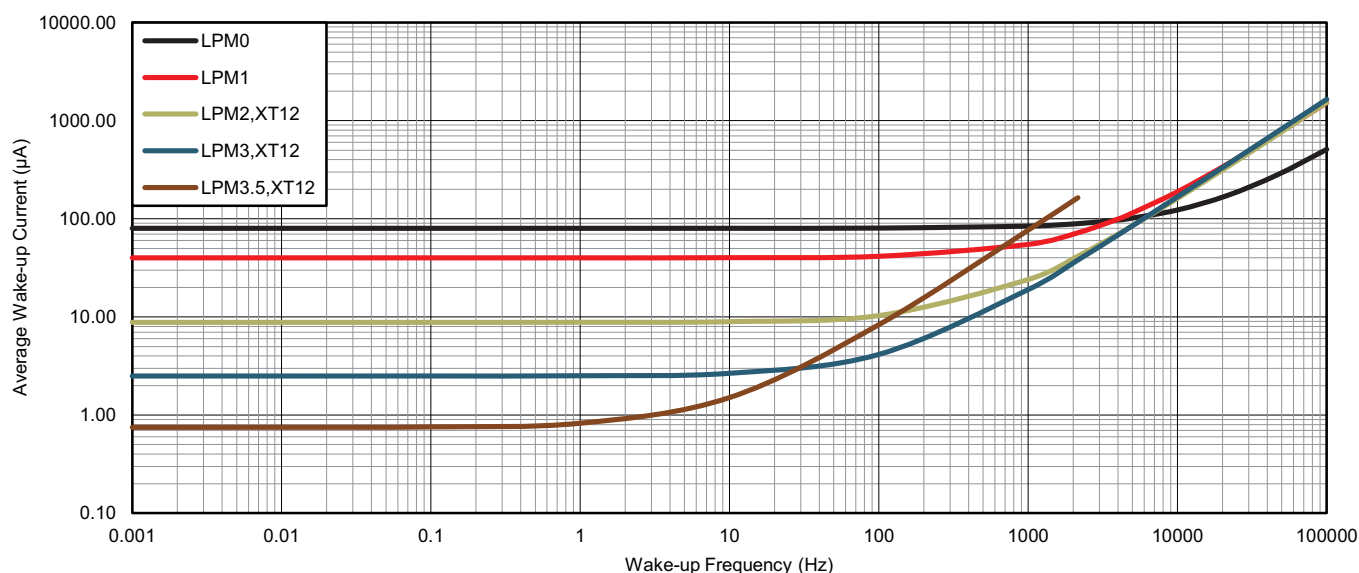
(2) Charge required until start of user code. This does not include the energy required to reconfigure the device.

5.13.4.1 Typical Characteristics, Average LPM Currents vs Wake-up Frequency



NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

图 5-6. Average LPM Currents vs Wake-up Frequency at 25°C



NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

图 5-7. Average LPM Currents vs Wake-up Frequency at 85°C

5.13.5 Digital I/Os

Table 5-11 lists the characteristics of the digital inputs.

Table 5-11. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+} Positive-going input threshold voltage		2.2 V	1.2		1.65	V
		3.0 V	1.65		2.25	
V _{IT-} Negative-going input threshold voltage		2.2 V	0.55		1.00	V
		3.0 V	0.75		1.35	
V _{hys} Input voltage hysteresis (V _{IT+} – V _{IT-})		2.2 V	0.44		0.98	V
		3.0 V	0.60		1.30	
R _{Pull} Pullup or pulldown resistor	For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC}		20	35	50	kΩ
C _{i,dig} Input capacitance, digital only port pins	V _{IN} = V _{SS} or V _{CC}			3		pF
C _{i,ana} Input capacitance, port pins with shared analog functions ⁽¹⁾	V _{IN} = V _{SS} or V _{CC}			5		pF
I _{lkg(Px.y)} High-impedance input leakage current	Refer to notes ⁽²⁾ and ⁽³⁾	2.2 V, 3.0 V	–20		+20	nA
t _(int) External interrupt timing (external trigger pulse duration to set interrupt flag) ⁽⁴⁾	Ports with interrupt capability (see block diagram and terminal function descriptions).	2.2 V, 3.0 V	20			ns
t _(RST) External reset pulse duration on $\overline{\text{RST}}$ ⁽⁵⁾		2.2 V, 3.0 V	2			μs

- (1) If the port pins PJ.4/LFXIN and PJ.5/LFXOUT are used as digital I/Os, they are connected by a 4-pF capacitor and a 35-MΩ resistor in series. At frequencies of approximately 1 kHz and lower, the 4-pF capacitor can add to the pin capacitance of PJ.4/LFXIN and/or PJ.5/LFXOUT.
- (2) The input leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
- (3) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
- (4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).
- (5) Not applicable if $\overline{\text{RST}}$ /NMI pin configured as NMI.

Table 5-12 lists the characteristics of the digital outputs.

Table 5-12. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH} High-level output voltage	I _(OHmax) = -1 mA ⁽¹⁾	2.2 V	V _{CC} - 0.25		V _{CC}	V
	I _(OHmax) = -3 mA ⁽²⁾		V _{CC} - 0.60		V _{CC}	
	I _(OHmax) = -2 mA ⁽¹⁾	3.0 V	V _{CC} - 0.25		V _{CC}	
	I _(OHmax) = -6 mA ⁽²⁾		V _{CC} - 0.60		V _{CC}	
V _{OL} Low-level output voltage	I _(OLmax) = 1 mA ⁽¹⁾	2.2 V	V _{SS}		V _{SS} + 0.25	V
	I _(OLmax) = 3 mA ⁽²⁾		V _{SS}		V _{SS} + 0.60	
	I _(OLmax) = 2 mA ⁽¹⁾	3.0 V	V _{SS}		V _{SS} + 0.25	
	I _(OLmax) = 6 mA ⁽²⁾		V _{SS}		V _{SS} + 0.60	
f _{PX,y} Port output frequency (with load) ⁽³⁾	C _L = 20 pF, R _L ^{(4) (5)}	2.2 V	16			MHz
		3.0 V	16			
f _{Port_CLK} Clock output frequency ⁽³⁾	ACLK, MCLK, or SMCLK at configured output port, C _L = 20 pF ⁽⁵⁾	2.2 V	16			MHz
		3.0 V	16			
t _{rise,dig} Port output rise time, digital only port pins	C _L = 20 pF	2.2 V		4	15	ns
		3.0 V		3	15	
t _{fall,dig} Port output fall time, digital only port pins	C _L = 20 pF	2.2 V		4	15	ns
		3.0 V		3	15	
t _{rise,ana} Port output rise time, port pins with shared analog functions	C _L = 20 pF	2.2 V		6	15	ns
		3.0 V		4	15	
t _{fall,ana} Port output fall time, port pins with shared analog functions	C _L = 20 pF	2.2 V		6	15	ns
		3.0 V		4	15	

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
- (3) The port can output frequencies at least up to the specified limit, and the port might support higher frequencies.
- (4) A resistive divider with 2 × R1 and R1 = 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.
- (5) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.13.5.1 Typical Characteristics, Digital Outputs

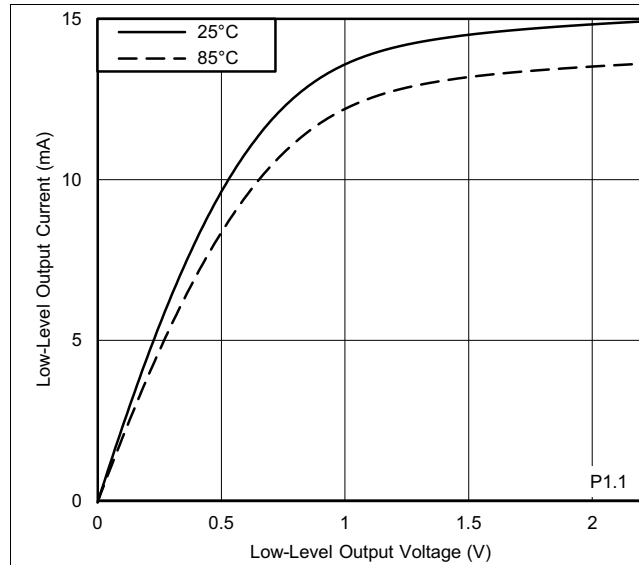


图 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage

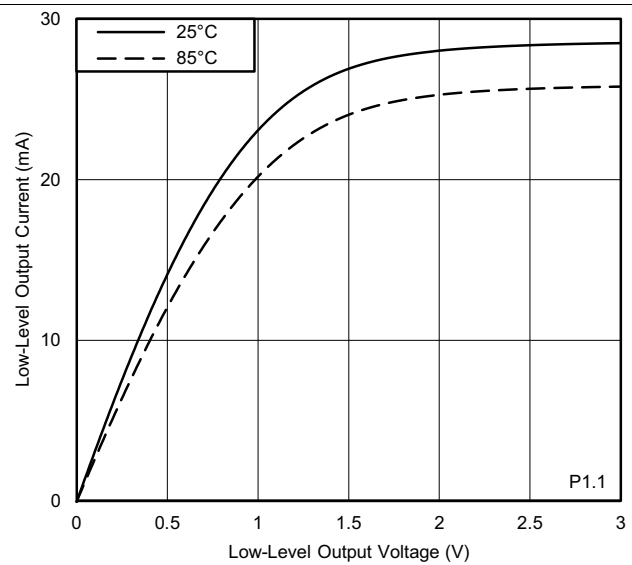


图 5-9. Typical Low-Level Output Current vs Low-Level Output Voltage

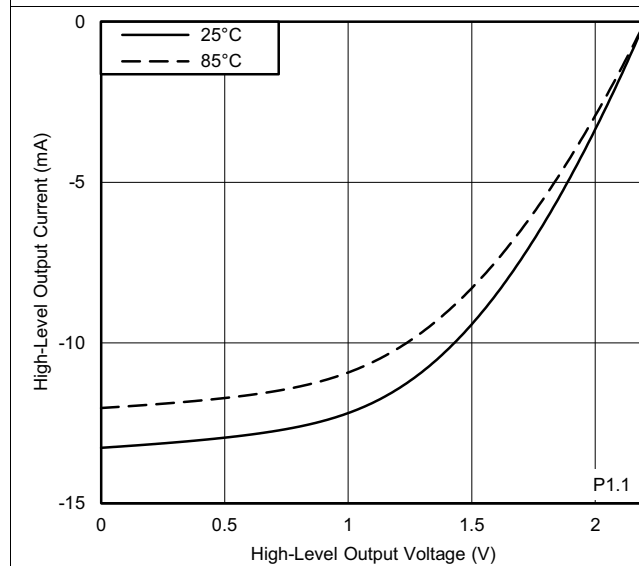


图 5-10. Typical High-Level Output Current vs High-Level Output Voltage

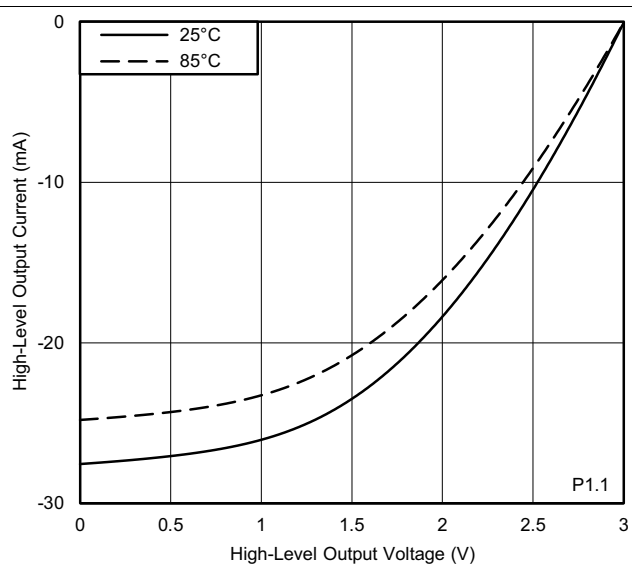


图 5-11. Typical High-Level Output Current vs High-Level Output Voltage

5.13.6 LEA

Table 5-13 lists the characteristics of the LEA.

Table 5-13. Low-Energy Accelerator (LEA) Performance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{LEA}	Frequency for specified performance	MCLK			16		MHz
W_LEA_FFT	LEA-SC subsystem energy on fast fourier transform	Complex FFT 128 pt. Q.15 with random data in LEA-RAM	$V_{CORE} = 3\text{ V}$, MCLK = 16 MHz		350		nJ
W_LEA_FIR	LEA-SC subsystem energy on finite impulse response	Real FIR on random Q.31 data with 128 taps on 24 points	$V_{CORE} = 3\text{ V}$, MCLK = 16 MHz		2.6		μJ
W_LEA_ADD	LEA-SC subsystem energy on additions	On 32 Q.31 elements with random value out of LEA-RAM with linear address increment	$V_{CORE} = 3\text{ V}$, MCLK = 16 MHz		6.6		nJ

5.13.7 Timer_A and Timer_B

Table 5-14 lists the characteristics of Timer_A.

Table 5-14. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	2.2 V, 3.0 V			16	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

Table 5-15 lists the characteristics of Timer_B.

Table 5-15. Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V, 3.0 V			16	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

5.13.8 eUSCI

Table 5-16 lists the supported clock frequencies of the eUSCI in UART mode.

Table 5-16. eUSCI (UART Mode) Clock Frequency

PARAMETER	CONDITIONS	MIN	MAX	UNIT
f_{eUSCI} eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% $\pm$ 10%		16	MHz
f_{BITCLK} BITCLK clock frequency (equals baud rate in MBaud)			4	MHz

Table 5-17 lists the switching characteristics of the eUSCI in UART mode.

Table 5-17. eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t UART receive deglitch time ⁽¹⁾	UCGLITx = 0	2.2 V, 3.0 V	5		30	ns
	UCGLITx = 1		20		90	
	UCGLITx = 2		35		160	
	UCGLITx = 3		50		220	

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-18 lists the supported clock frequency of the eUSCI in SPI master mode.

Table 5-18. eUSCI (SPI Master Mode) Clock Frequency

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI} eUSCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% $\pm$ 10%		16	MHz

Table 5-19 lists the switching characteristics of the eUSCI in SPI master mode.

Table 5-19. eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{STE,LEAD}	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10		1			UCxCLK cycles
t _{STE,LAG}	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10		1			
t _{STE,ACC}	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V			60	ns
t _{STE,DIS}	STE disable time, STE inactive to SOMI high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V			80	ns
t _{SU,MI}	SOMI input data setup time		2.2 V	40			ns
			3.0 V	40			
t _{HD,MI}	SOMI input data hold time		2.2 V	0			ns
			3.0 V	0			
t _{VALID,MO}	SIMO output data valid time ⁽²⁾	UCLK edge to SIMO valid, C _L = 20 pF	2.2 V			11	ns
			3.0 V			10	
t _{HD,MO}	SIMO output data hold time ⁽³⁾	C _L = 20 pF	2.2 V		0		ns
			3.0 V		0		

- (1) $f_{UCxCLK} = 1/2 t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO}(eUSCI) + t_{SU,SI}(Slave), t_{SU,MI}(eUSCI) + t_{VALID,SO}(Slave))$.
For the slave parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$, see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [图 5-12](#) and [图 5-13](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [图 5-12](#) and [图 5-13](#).

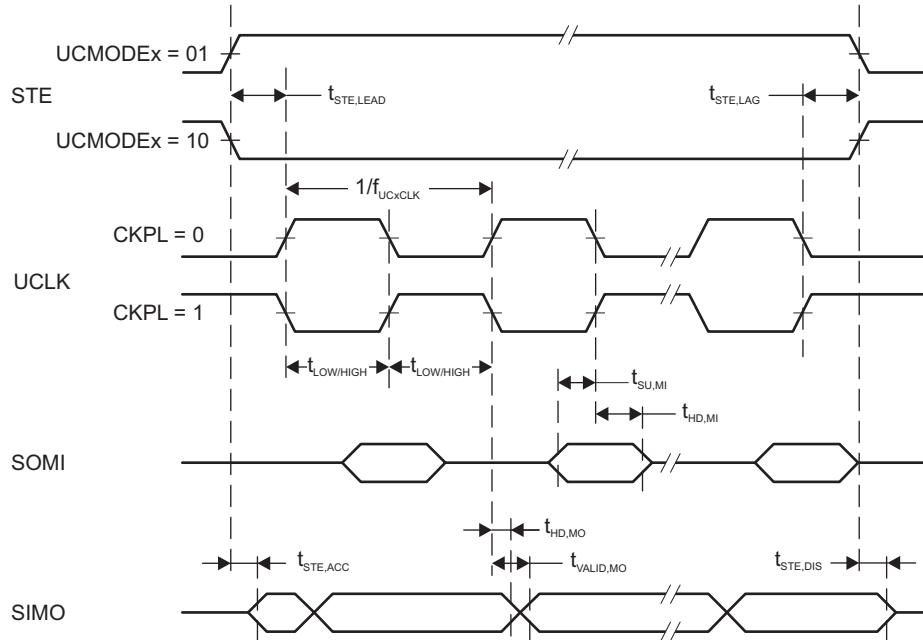


图 5-12. SPI Master Mode, CKPH = 0

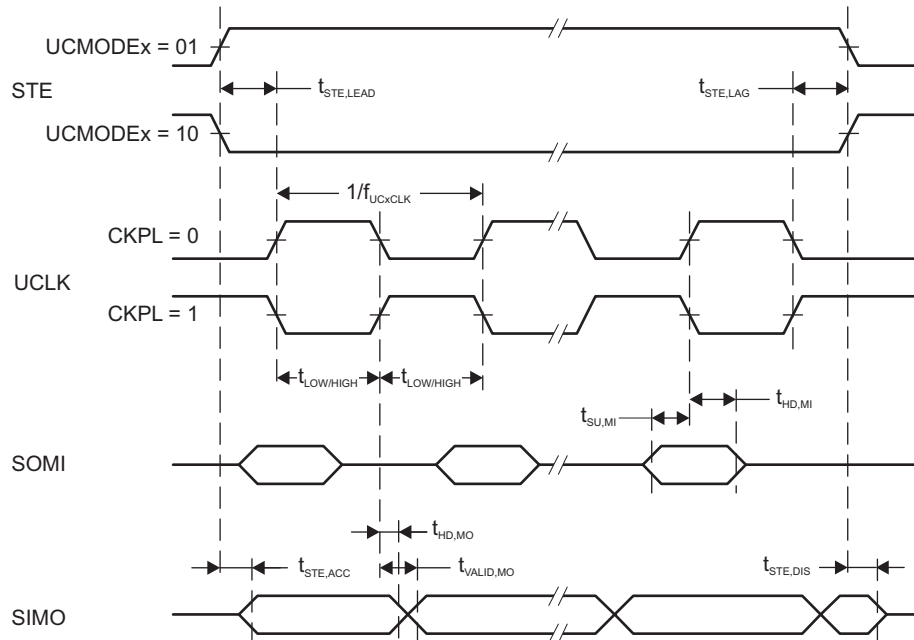


图 5-13. SPI Master Mode, CKPH = 1

Table 5-20 lists the switching characteristics of the eUSCI in SPI slave mode.

Table 5-20. eUSCI (SPI Slave Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
t _{STE,LEAD} STE lead time, STE active to clock		2.2 V	45		ns
		3.0 V	40		
t _{STE,LAG} STE lag time, Last clock to STE inactive		2.2 V	2		ns
		3.0 V	3		
t _{STE,ACC} STE access time, STE active to SOMI data out		2.2 V		45	ns
		3.0 V		40	
t _{STE,DIS} STE disable time, STE inactive to SOMI high impedance		2.2 V		50	ns
		3.0 V		45	
t _{SU,SI} SIMO input data setup time		2.2 V	4		ns
		3.0 V	4		
t _{HD,SI} SIMO input data hold time		2.2 V	7		ns
		3.0 V	7		
t _{VALID,SO} SOMI output data valid time ⁽²⁾	UCLK edge to SOMI valid, C _L = 20 pF	2.2 V		35	ns
		3.0 V		35	
t _{HD,SO} SOMI output data hold time ⁽³⁾	C _L = 20 pF	2.2 V	0		ns
		3.0 V	0		

- (1) $f_{UCXCLK} = 1/2 t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [图 5-14](#) and [图 5-15](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [图 5-14](#) and [图 5-15](#).

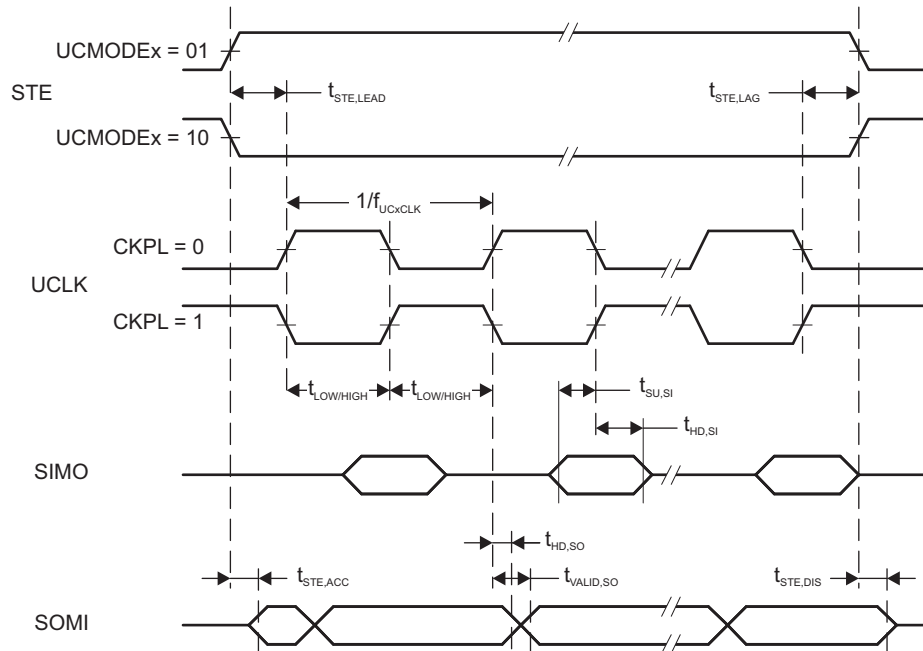


图 5-14. SPI Slave Mode, CKPH = 0

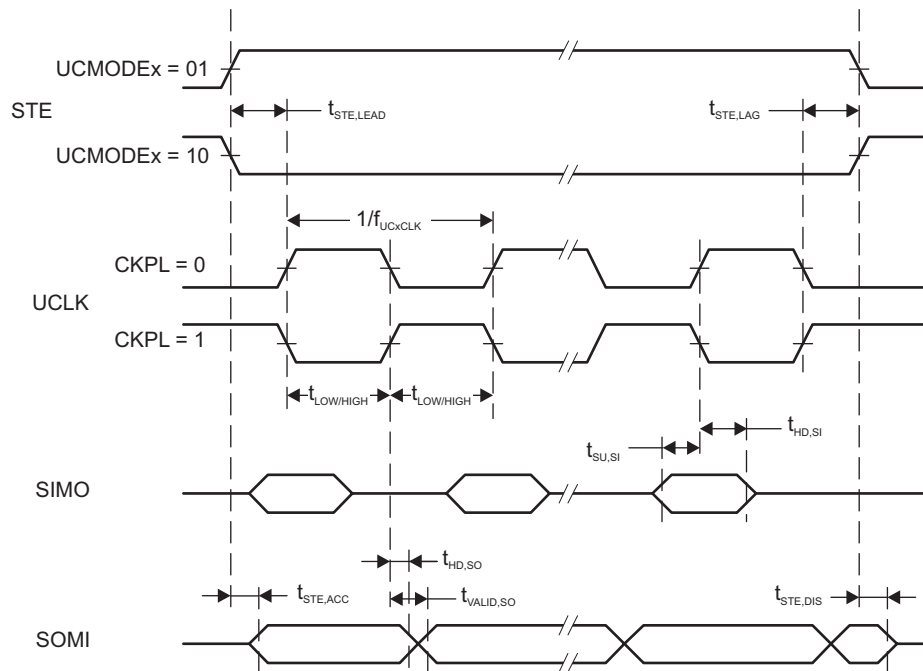


图 5-15. SPI Slave Mode, CKPH = 1

Table 5-21 lists the switching characteristics of the eUSCI in I²C mode.

Table 5-21. eUSCI (I²C Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 5-16)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{eUSCI}	eUSCI input clock frequency Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				16	MHz
f _{SCL}	SCL clock frequency	2.2 V, 3.0 V	0		400	kHz
t _{HD,STA}	Hold time (repeated) START	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	4.0 0.6			μs
t _{SU,STA}	Setup time for a repeated START	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	4.7 0.6			μs
t _{HD,DAT}	Data hold time	2.2 V, 3.0 V	0			ns
t _{SU,DAT}	Data setup time	2.2 V, 3.0 V	100			ns
t _{SU,STO}	Setup time for STOP	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	4.0 0.6			μs
t _{BUF}	Bus free time between a STOP and START condition	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	4.7 1.3			us
t _{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0 UCGLITx = 1 UCGLITx = 2 UCGLITx = 3	50 25 12.5 6.3		250 125 62.5 31.5	ns
t _{TIMEOUT}	Clock low time-out	UCCLTOx = 1 UCCLTOx = 2 UCCLTOx = 3		27 30 33		ms

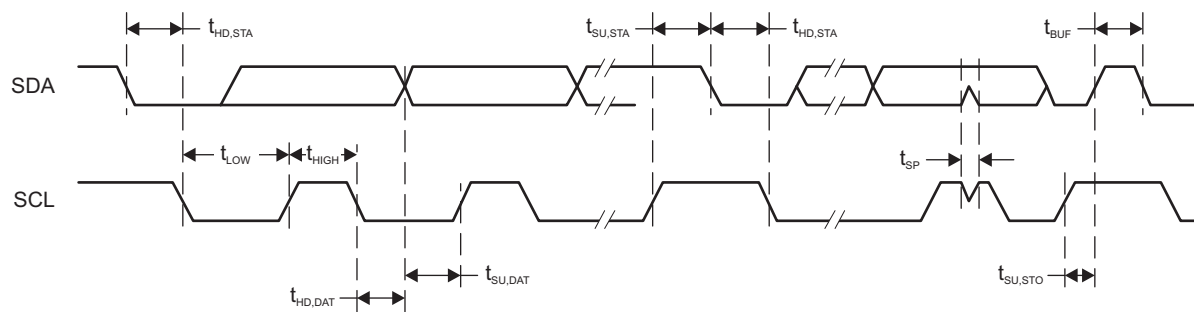


图 5-16. I²C Mode Timing

5.13.9 Segment LCD Controller

Table 5-22 lists the recommended operating conditions for the LCD controller.

Table 5-22. LCD_C Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$V_{CC,LCD_C,CP\ en,3.6}$	Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.6$ V	LCDCPEN = 1, 0000b < VLCDx ≤ 1111b (charge pump enabled, $V_{LCD} \leq 3.6$ V)			V
$V_{CC,LCD_C,CP\ en,3.3}$	Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.3$ V	LCDCPEN = 1, 0000b < VLCDx ≤ 1100b (charge pump enabled, $V_{LCD} \leq 3.3$ V)			V
$V_{CC,LCD_C,int.\ bias}$	Supply voltage range, internal biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0			V
$V_{CC,LCD_C,ext.\ bias}$	Supply voltage range, external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0			V
$V_{CC,LCD_C,VLCDEXT}$	Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1			V
V_{LCDCAP}	External LCD voltage at LCDCAP, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1			V
C_{LCDCAP}	Capacitor value on LCDCAP when charge pump enabled	LCDCPEN = 1, VLCDx > 0000b (charge pump enabled)			μF
$f_{ACLK,in}$	ACLK input frequency range	30	32.768	40	kHz
f_{LCD}	LCD frequency range	$f_{FRAME} = (1 / (2 \times mux)) \times f_{LCD}$ with mux = 1 (static) to 8			Hz
$f_{FRAME,4mux}$	LCD frame frequency range	$f_{FRAME,4mux}(MAX) = (1 / (2 \times 4)) \times f_{LCD}(MAX) = (1 / (2 \times 4)) \times 1024$ Hz			Hz
C_{Panel}	Panel capacitance	$f_{LCD} = 1024$ Hz, all common lines equally loaded			pF
V_{R33}	Analog input voltage at R33	LCDCPEN = 0, VLCDEXT = 1			V
$V_{R23,1/3bias}$	Analog input voltage at R23	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0			V
$V_{R13,1/3bias}$	Analog input voltage at R13 with 1/3 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0			V
$V_{R13,1/2bias}$	Analog input voltage at R13 with 1/2 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1			V
V_{R03}	Analog input voltage at R03	R0EXT = 1			V
$V_{LCD} - V_{R03}$	Voltage difference between V_{LCD} and R03	LCDCPEN = 0, R0EXT = 1			V
V_{LCDREF}	External LCD reference voltage applied at LCDREF	VLCDDREFx = 01			V

Table 5-23 lists the electrical characteristics the LCD controller.

Table 5-23. LCD_C Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{LCD,0}	LCD voltage	VLCDx = 0000, VLCDxEXT = 0	2.4 V to 3.6 V		V _{CC}		V
V _{LCD,1}		LCDCPEN = 1, VLCDx = 0001b	2 V to 3.6 V	2.49	2.60	2.72	
V _{LCD,2}		LCDCPEN = 1, VLCDx = 0010b	2 V to 3.6 V		2.66		
V _{LCD,3}		LCDCPEN = 1, VLCDx = 0011b	2 V to 3.6 V		2.72		
V _{LCD,4}		LCDCPEN = 1, VLCDx = 0100b	2 V to 3.6 V		2.78		
V _{LCD,5}		LCDCPEN = 1, VLCDx = 0101b	2 V to 3.6 V		2.84		
V _{LCD,6}		LCDCPEN = 1, VLCDx = 0110b	2 V to 3.6 V		2.90		
V _{LCD,7}		LCDCPEN = 1, VLCDx = 0111b	2 V to 3.6 V		2.96		
V _{LCD,8}		LCDCPEN = 1, VLCDx = 1000b	2 V to 3.6 V		3.02		
V _{LCD,9}		LCDCPEN = 1, VLCDx = 1001b	2 V to 3.6 V		3.08		
V _{LCD,10}		LCDCPEN = 1, VLCDx = 1010b	2 V to 3.6 V		3.14		
V _{LCD,11}		LCDCPEN = 1, VLCDx = 1011b	2 V to 3.6 V		3.20		
V _{LCD,12}		LCDCPEN = 1, VLCDx = 1100b	2 V to 3.6 V		3.26		
V _{LCD,13}		LCDCPEN = 1, VLCDx = 1101b	2.2 V to 3.6 V		3.32		
V _{LCD,14}		LCDCPEN = 1, VLCDx = 1110b	2.2 V to 3.6 V		3.38		
V _{LCD,15}		LCDCPEN = 1, VLCDx = 1111b	2.2 V to 3.6 V	3.32	3.44	3.6	
V _{LCD,7,0.8}	LCD voltage with external reference of 0.8 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V _{LCDREF} = 0.8 V	2 V to 3.6 V		2.96 × 0.8 V		V
V _{LCD,7,1.0}	LCD voltage with external reference of 1.0 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V _{LCDREF} = 1.0 V	2 V to 3.6 V		2.96 × 1.0 V		V
V _{LCD,7,1.2}	LCD voltage with external reference of 1.2 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V _{LCDREF} = 1.2 V	2.2 V to 3.6 V		2.96 × 1.2 V		V
ΔV _{LCD}	Voltage difference between consecutive VLCDx settings	ΔV _{LCD} = V _{LCD,x} – V _{LCD,x-1} with x = 0010b to 1111b		40	60	80	mV
I _{CC,Peak,CP}	Peak supply currents due to charge pump activities	LCDCPEN = 1, VLCDx = 1111b external, with decoupling capacitor on DVCC supply ≥ 1 μF	2.2 V		600		μA
t _{LCD,CP,on}	Time to charge C _{LCD} when discharged	C _{LCD} = 4.7 μF, LCDCPEN = 0→1, VLCDx = 1111b	2.2 V		100	500	ms
I _{CP,Load}	Maximum charge pump load current	LCDCPEN = 1, VLCDx = 1111b	2.2 V	50			μA
R _{LCD,Seg}	LCD driver output impedance, segment lines	LCDCPEN = 0, I _{LOAD} = ±10 μA	2.2 V			10	kΩ
R _{LCD,COM}	LCD driver output impedance, common lines	LCDCPEN = 0, I _{LOAD} = ±10 μA	2.2 V			10	kΩ

5.13.10 ADC12_B

Table 5-24 lists the power and input requirements of the ADC.

Table 5-24. 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	NOM	MAX	UNIT
V _(Ax) Analog input voltage range ⁽¹⁾	All ADC12 analog input pins Ax		0		AVCC	V
I _(ADC12_B) single-ended mode	f _{ADC12CLK} = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		145	199	μA
	f _{ADC12CLK} = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	2.2 V		140	190	
I _(ADC12_B) differential mode	f _{ADC12CLK} = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 1, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		175	245	μA
	f _{ADC12CLK} = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 1, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	2.2 V		170	230	
I _(ADC12_B) single-ended low-power mode	f _{ADC12CLK} = MODCLK/4, ADC12ON = 1, ADC12PWRMD = 1, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		85	125	μA
	f _{ADC12CLK} = MODCLK/4, ADC12ON = 1, ADC12PWRMD = 1, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	2.2 V		83	120	
I _(ADC12_B) differential low-power mode	f _{ADC12CLK} = MODCLK/4, ADC12ON = 1, ADC12PWRMD = 1, ADC12DIF = 1, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		110	165	μA
	f _{ADC12CLK} = MODCLK/4, ADC12ON = 1, ADC12PWRMD = 1, ADC12DIF = 1, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	2.2 V		109	160	
C _I Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		10	15	pF
R _I Input MUX ON resistance	0 V ≤ V _(Ax) ≤ AV _{CC}	>2 V		0.5	4	kΩ
		<2 V		1	10	

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.

(2) The internal reference supply current is not included in current consumption parameter I(ADC12_B).

(3) Approximately 60% (typical) of the total current into the AVCC and DVCC terminal is from AVCC.

Table 5-25 lists the timing requirements of the ADC.

Table 5-25. 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADC12CLK} Frequency for specified performance	For specified performance of ADC12 linearity parameters with ADC12PWRMD = 0, If ADC12PWRMD = 1, the maximum is 1/4 of the value shown here	0.45		5.4	MHz
f_{ADC12CLK} Frequency for reduced performance	Linearity parameters have reduced performance		32.768		kHz
f_{ADC12OSC} Internal oscillator ⁽¹⁾	ADC12DIV = 0, $f_{\text{ADC12CLK}} = f_{\text{ADC12OSC}}$ from MODCLK	4	4.8	5.4	MHz
t_{CONVERT} Conversion time	REFON = 0, Internal oscillator, $f_{\text{ADC12CLK}} = f_{\text{ADC12OSC}}$ from MODCLK, ADC12WINC = 0	2.6		3.5	μs
	External f_{ADC12CLK} from ACLK, MCLK, or SMCLK, ADC12SSEL $\neq$ 0		See ⁽²⁾		
t_{ADC12ON} Turnon settling time of the ADC	See ⁽³⁾			100	ns
t_{ADC12OFF} Time ADC must be off before can be turned on again	Note: t_{ADC12OFF} must be met to make sure that t_{ADC12ON} time holds	100			ns
t_{Sample} Sampling time	$R_S = 400\ \Omega$, $R_I = 4\ \text{k}\Omega$, $C_I = 15\ \text{pF}$, $C_{\text{pext}} = 8\ \text{pF}$ ⁽⁴⁾	All pulse sample mode (ADC12SHP = 1) and extended sample mode (ADC12SHP = 0) with buffered reference (ADC12VRSEL = 0x1, 0x3, 0x5, 0x7, 0x9, 0xB, 0xD, 0xF)		1	μs
		Extended sample mode (ADC12SHP = 0) with unbuffered reference (ADC12VRSEL = 0x0, 0x2, 0x4, 0x6, 0xC, 0xE)		See ⁽⁵⁾	μs

(1) The ADC12OSC is sourced directly from MODOSC in the UCS.

(2) $14 \times 1 / f_{\text{ADC12CLK}}$. If ADC12WINC = 1 then $15 \times 1 / f_{\text{ADC12CLK}}$.

(3) The condition is that the error in a conversion started after t_{ADC12ON} is less than ± 0.5 LSB. The reference and input signal are already settled.

(4) Approximately 10 Tau (τ) are needed to get an error of less than ± 0.5 LSB: $t_{\text{sample}} = \ln(2^{n+2}) \times (R_S + R_I) \times (C_I + C_{\text{pext}})$, where n = ADC resolution = 12, R_S = external source resistance, C_{pext} = external parasitic capacitance.

(5) $6 \times 1 / f_{\text{ADC12CLK}}$

Table 5-26 lists the linearity parameters of the ADC.

Table 5-26. 12-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E _I	Integral linearity error (INL) for differential input	With external voltage reference (ADC12VRSEL = 0x2, 0x3, 0x4, 0x14, 0x15), 1.2 V ≤ V _{R+} – V _{R-} ≤ AV _{CC}			±1.8	LSB
	Integral linearity error (INL) for single ended inputs	With external voltage reference (ADC12VRSEL = 0x2, 0x3, 0x4, 0x14, 0x15), 1.2 V ≤ V _{R+} – V _{R-} ≤ AV _{CC}			±2.2	LSB
E _D	Differential linearity error (DNL)	With external voltage reference (ADC12VRSEL = 0x2, 0x3, 0x4, 0x14, 0x15),	–0.99		+1.0	LSB
E _O	Offset error ^{(1) (2)}	ADC12VRSEL = 0x1 without TLV calibration, TLV calibration data can be used to improve the parameter ⁽³⁾		±0.5	±1.5	mV
E _G	Gain error	With internal voltage reference V _{REF} = 2.5 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)		±0.2	±1.7	%
		With internal voltage reference V _{REF} = 1.2 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)		±0.2	±2.5	
		With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, V _{R+} = 2.5 V, V _{R-} = AVSS		±1	±3	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V _{R+} = 2.5 V, V _{R-} = AVSS		±2	±27	
E _T	Total unadjusted error	With internal voltage reference V _{REF} = 2.5 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)		±0.2	±1.8	%
		With internal voltage reference V _{REF} = 1.2 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)		±0.2	±2.6	
		With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, V _{R+} = 2.5 V, V _{R-} = AVSS		±1	±5	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V _{R+} = 2.5 V, V _{R-} = AVSS		±1	±28	

(1) Offset is measured as the input voltage (at which ADC output transitions from 0 to 1) minus 0.5 LSB.

(2) Offset increases as IR drop increases when V_{R-} is AVSS.

(3) For details, see the *Device Descriptor Table* section in the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

Table 5-27 lists the dynamic performance characteristics of the ADC with an external reference.

Table 5-27. 12-Bit ADC, Dynamic Performance With External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Number of no missing code output-code bits		12			bits
SNR	Signal-to-noise with differential inputs	$V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		71		dB
	Signal-to-noise with single-ended inputs	$V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		70		
ENOB	Effective number of bits with differential inputs ⁽¹⁾	$V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		11.4		bits
	Effective number of bits with single-ended inputs ⁽¹⁾	$V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		11.1		
	Effective number of bits with 32.768-kHz clock (reduced performance) ⁽¹⁾	Reduced performance with $f_{ADC12CLK}$ from ACLK LFXT 32.768 kHz, $V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		10.9		

(1) $ENOB = (SINAD - 1.76) / 6.02$

Table 5-28 lists the dynamic performance characteristics of the ADC with an internal reference.

Table 5-28. 12-Bit ADC, Dynamic Performance With Internal Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Number of no missing code output-code bits		12			bits
SNR	Signal-to-noise with differential inputs	$V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		70		dB
	Signal-to-noise with single-ended inputs	$V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		69		
ENOB	Effective number of bits with differential inputs ⁽¹⁾	$V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		11.4		bits
	Effective number of bits with single-ended inputs ⁽¹⁾	$V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		11.0		
	Effective number of bits with 32.768-kHz clock (reduced performance) ⁽¹⁾	Reduced performance with $f_{ADC12CLK}$ from ACLK LFXT 32.768 kHz, $V_{R+} = 2.5\text{ V}$, $V_{R-} = AV_{SS}$		10.9		

(1) $ENOB = (SINAD - 1.76) / 6.02$

Table 5-29 lists the characteristics of the temperature sensor and the $V_{1/2}$.

Table 5-29. 12-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SENSOR}	Temperature sensor voltage ^{(1) (2)}	ADC12ON = 1, ADC12TCMAP = 1, $T_A = 0^\circ\text{C}$		700		mV
TC_{SENSOR}	See ⁽²⁾	ADC12ON = 1, ADC12TCMAP = 1		2.5		mV/ $^\circ\text{C}$
$t_{SENSOR(sample)}$	Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected ⁽³⁾	ADC12ON = 1, ADC12TCMAP = 1, Error of conversion result ≤ 1 LSB	30			μs
$V_{1/2}$	AVCC voltage divider for ADC12BATMAP = 1 on MAX input channel	ADC12ON = 1, ADC12BATMAP = 1	47.5	50	52.5	%
$I_{V1/2}$	Current for battery monitor during sample time	ADC12ON = 1, ADC12BATMAP = 1		38	72	μA
$t_{V1/2 (sample)}$	Sample time required if ADC12BATMAP = 1 and channel MAX is selected ⁽⁴⁾	ADC12ON = 1, ADC12BATMAP = 1	1.7			μs

- (1) The temperature sensor offset can be as much as $\pm 30^\circ\text{C}$. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for $30^\circ\text{C} \pm 3^\circ\text{C}$ and $85^\circ\text{C} \pm 3^\circ\text{C}$ for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature}, ^\circ\text{C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
- (3) The typical equivalent impedance of the sensor is 250 k Ω . The sample time required includes the sensor-on time, $t_{SENSOR(on)}$.
- (4) The on-time $t_{V1/2(on)}$ is included in the sampling time $t_{V1/2(sample)}$; no additional on time is needed.

Table 5-30 lists the characteristics of the external reference for the ADC.

Table 5-30. 12-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{R+}	Positive external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	1.2		AV_{CC}	V
V_{R-}	Negative external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	0		1.2	V
$V_{R+} - V_{R-}$	Differential external reference voltage input	$V_{R+} > V_{R-}$	1.2		AV_{CC}	V
I_{VeREF+} , I_{VeREF-}	Static input current singled-ended input mode	$1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$, $V_{eREF-} = 0\text{ V}$ $f_{ADC12CLK} = 5\text{ MHz}$, $ADC12SHTx = 1h$, $ADC12DIF = 0$, $ADC12PWRMD = 0$			± 10	μA
		$1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$, $V_{eREF-} = 0\text{ V}$ $f_{ADC12CLK} = 5\text{ MHz}$, $ADC12SHTx = 8h$, $ADC12DIF = 0$, $ADC12PWRMD = 01$			± 2.5	μA
I_{VeREF+} , I_{VeREF-}	Static input current differential input mode	$1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$, $V_{eREF-} = 0\text{ V}$ $f_{ADC12CLK} = 5\text{ MHz}$, $ADC12SHTx = 1h$, $ADC12DIF = 1$, $ADC12PWRMD = 0$			± 20	μA
		$1.2\text{ V} \leq V_{eREF+} \leq V_{AVCC}$, $V_{eREF-} = 0\text{ V}$ $f_{ADC12CLK} = 5\text{ MHz}$, $ADC12SHTx = 8h$, $ADC12DIF = 1$, $ADC12PWRMD = 1$			± 5	μA
I_{VeREF+}	Peak input current with single-ended input	$0\text{ V} \leq V_{eREF+} \leq V_{AVCC}$, $ADC12DIF = 0$			1.5	mA
I_{VeREF+}	Peak input current with differential input	$0\text{ V} \leq V_{eREF+} \leq V_{AVCC}$, $ADC12DIF = 1$			3	mA
$C_{VeREF+/-}$	Capacitance at VeREF+ or VeREF- terminal	See ⁽²⁾	10			μF

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance (C_i) is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) Connect two decoupling capacitors, 10 μF and 470 nF, to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_B. Also see the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

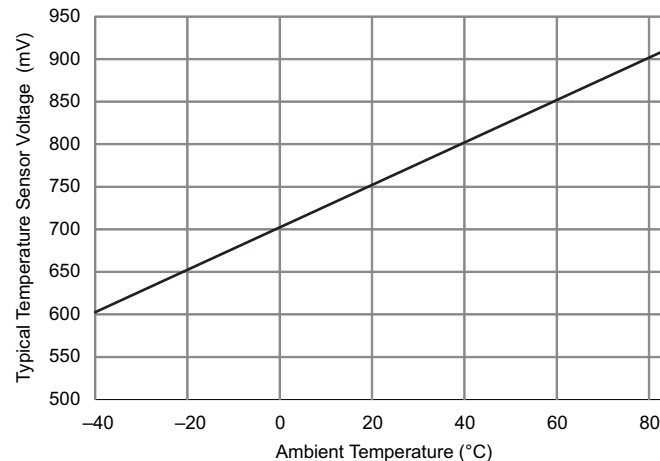


图 5-17. Typical Temperature Sensor Voltage

5.13.11 Reference

Table 5-31 lists the characteristics of the internal reference.

Table 5-31. REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = 1	2.7 V		2.5	±1.5%	V
		REFVSEL = {1} for 2.0 V, REFON = 1	2.2 V		2.0	±1.5%	
		REFVSEL = {0} for 1.2 V, REFON = 1	1.8 V		1.2	±1.8%	
Noise	RMS noise at VREF ⁽¹⁾	From 0.1 Hz to 10 Hz, REFVSEL = {0}			30	130	μV
V _{OS_BUF_INT}	VREF ADC BUF_INT buffer offset ⁽²⁾	T _A = 25°C, ADC on, REFVSEL = {0}, REFON = 1, REFOUT = 0		–16		+16	mV
V _{OS_BUF_EXT}	VREF ADC BUF_EXT buffer offset ⁽³⁾	T _A = 25°C, REFVSEL = {0}, REFOUT = 1, REFON = 1 or ADC on		–16		+16	mV
AV _{CC(min)}	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I _{REF+}	Operating supply current into AVCC terminal ⁽⁴⁾	REFON = 1	3 V		19	26	μA
I _{REF+_ADC_BUF}	Operating supply current into AVCC terminal ⁽⁴⁾	ADC ON, REFOUT = 0, REFVSEL = {0, 1, or 2}, ADC12PWRMD = 0	3 V		247	400	μA
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0	3 V		1053	1820	
		ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1	3 V		153	240	
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1	3 V		581	1030	
		ADC OFF, REFON = 1, REFOUT = 1, REFVSEL = {0, 1, 2}	3 V		1105	1890	
I _{O(VREF+)}	VREF maximum load current, VREF+ terminal	REFVSEL = {0, 1, 2}, AV _{CC} = AV _{CC(min)} for each reference level, REFON = REFOUT = 1		–1000		+10	μA
ΔV _{OUT} /ΔI _O (VREF+)	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 2}, I _{O(VREF+)} = +10 μA or –1000 μA, AV _{CC} = AV _{CC(min)} for each reference level, REFON = REFOUT = 1				1500	μV/mA
C _{VREF+/-}	Capacitance at VREF+ and VREF- terminals	REFON = REFOUT = 1		0		100	pF
TC _{REF+}	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2}, REFON = REFOUT = 1, T _A = –40°C to 85°C ⁽⁵⁾			24	50	ppm/K
PSRR _{DC}	Power supply rejection ratio (DC)	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1			100	400	μV/V
PSRR _{AC}	Power supply rejection ratio (AC)	dAV _{CC} = 0.1 V at 1 kHz			3.0		mV/V
t _{SETTLE}	Settling time of reference voltage ⁽⁶⁾	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFON = 0 → 1			40	80	μs
T _{buf_settle}	Settling time of ADC reference voltage buffer ⁽⁶⁾	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFON = 1			0.4	2	us

- (1) Internal reference noise affects ADC performance when ADC uses the internal reference. See [Designing With the MSP430FR59xx and MSP430FR58xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal or external reference.
- (2) Buffer offset affects ADC gain error and thus total unadjusted error.
- (3) Buffer offset affects ADC gain error and thus total unadjusted error.
- (4) The internal reference current is supplied through the AVCC terminal.
- (5) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
- (6) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.13.12 Comparator

Table 5-32 lists the characteristics of the comparator.

Table 5-32. Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{AVCC_COMP} Comparator operating supply current into AVCC, excludes reference resistor ladder	CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)	2.2 V, 3.0 V		12	16	μA
	CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)			10	14	
	CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T _A = 30°C			0.1	0.3	
	CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T _A = 85°C			0.3	1.3	
I _{AVCC_COMP_REF} Quiescent current of resistor ladder into AVCC, including REF module current	CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 1, CEREFAcc = 0	2.2 V, 3.0 V		31	38	μA
	CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 1, CEREFAcc = 1			16	19	
V _{REF} Reference voltage level	CERSx = 11, CEREFLx = 01, CEREFAcc = 0	1.8 V	1.152	1.2	1.248	V
	CERSx = 11, CEREFLx = 10, CEREFAcc = 0	2.2 V	1.92	2.0	2.08	
	CERSx = 11, CEREFLx = 11, CEREFAcc = 0	2.7 V	2.40	2.5	2.60	
	CERSx = 11, CEREFLx = 01, CEREFAcc = 1	1.8 V	1.10	1.2	1.245	
	CERSx = 11, CEREFLx = 10, CEREFAcc = 1	2.2 V	1.90	2.0	2.08	
	CERSx = 11, CEREFLx = 11, CEREFAcc = 1	2.7 V	2.35	2.5	2.60	
V _{IC} Common-mode input range			0	V _{CC} – 1		V
V _{OFFSET} Input offset voltage	CEPWRMD = 00		–16		16	mV
	CEPWRMD = 01		–12		12	
	CEPWRMD = 10		–37		37	
C _{IN} Input capacitance	CEPWRMD = 00 or CEPWRMD = 01			10		pF
	CEPWRMD = 10			10		
R _{SIN} Series input resistance	ON (switch closed)			1	3	kΩ
	OFF (switch open)		50			MΩ
t _{PD} Propagation delay, response time	CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV			193	330	ns
	CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV			230	400	
	CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV			5	15	μs
t _{PD,filter} Propagation delay with filter active	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLy = 00			700	1000	ns
	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLy = 01			1.0	1.9	μs
	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLy = 10			2.0	3.7	
	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLy = 11			4.0	7.7	

Table 5-32. Comparator_E (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{EN_CMP}	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 00			0.9	1.5	μs
	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 01			0.9	1.5	
	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 10			15	65	
t _{EN_CMP_VREF}	Comparator and reference ladder and reference voltage enable time	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 10 or 11, CEREF ₀ = CEREF ₁ = 0x0F, REFON = 0		120	220	μs
t _{EN_CMP_RL}	Comparator and reference ladder enable time	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 10, REFON = 1, CEREF ₀ = CEREF ₁ = 0x0F		10	30	
V _{CE_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		$VIN \times (n + 0.5) / 32$	$VIN \times (n + 1) / 32$	V

5.13.13 FRAM

Table 5-33 lists the characteristics of the FRAM.

Table 5-33. FRAM Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	T _J	MIN	TYP	MAX	UNIT
Read and write endurance		10 ¹⁵			cycles
t _{Retention}	25°C	100			years
	70°C	40			
	85°C	10			
I _{WRITE}	Current to write into FRAM ⁽¹⁾		I _{READ}		nA
I _{ERASE}	Erase current ⁽²⁾		N/A ⁽³⁾		nA
t _{WRITE}	Write time ⁽⁴⁾		t _{READ}		ns
t _{READ}	Read time ⁽⁵⁾	NWAITS _x = 0	1 / f _{SYSTEM}		ns
		NWAITS _x = 1	2 / f _{SYSTEM}		ns

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption, I_{AM,FRAM}.

(2) FRAM does not require a special erase sequence.

(3) N/A = Not applicable

(4) Writing into FRAM is as fast as reading.

(5) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITS_x).

5.13.14 USS

Table 5-34 lists the USS recommended operating conditions.

Table 5-34. USS Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PV _{CC}	Analog supply voltage at PVCC pins for LDO operation	2.2		3.6	V
PV _{CC}	Analog supply voltage at PVCC pins for USS operation	2.2		3.6	V

Table 5-35 lists the characteristics of the USS LDO.

Table 5-35. USS LDO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{CC_} I _{do}	Analog supply voltage at PVCC pins		2.2		3.6	V
V _{USS}	USS voltage	0 ≤ I _{LOAD} ≤ I _{LOAD,MAX}	1.52	1.6	1.65	V
T _{holdoff}	Hold off delay on power up	LBHDEL = 0	0		μs	
		LBHDEL = 1	100			
		LBHDEL = 2	200			
		LBHDEL = 3	300			
T _{timeout}	Timeout on transition OFF to READY		160+T _h oldoff			μs

Table 5-36 lists the characteristics of the USS crystal.

Table 5-36. USSXTAL

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
N _{phase_osc}	Integrated phase noise	f _{osc} = 4 MHz or 8 MHz, range = 10 kHz to 4 MHz	–74		dBc
FRQ _{XTAL}	Resonator frequency		4	8	MHz
DC _{osc}	Duty cycle		35	65	%
I _{osc}	OSC supply current	f _{osc} = 4 MHz or 8 MHz, C _L = 18 pF, C _S = 4 pF, fully settled, ceramic resonator	180		μA
		f _{osc} = 4 MHz or 8 MHz, C _L = 12 pF (4MHz), 16pF(8MHz), C _S = 7 pF, fully settled, crystal resonator	240		
A _{osc}	Oscillation allowance	f _{osc} = 4 MHz, C _L = 18 pF, C _S = 4 pF, ceramic resonator	1500		Ω
		f _{osc} = 4 MHz, C _L = 12 pF, C _S = 7 pF, crystal resonator	1000		
		f _{osc} = 8 MHz, C _L = 18 pF, C _S = 4 pF, ceramic resonator	500		
		f _{osc} = 8 MHz, C _L = 16 pF, C _S = 7 pF, crystal resonator	350		
T _{start_osc}	Startup time (gate)	f _{osc} = 4 MHz, crystal resonator	2.8	4.6	ms
		f _{osc} = 8 MHz, crystal resonator	1	1.9	
		f _{osc} = 4 MHz, ceramic resonator	0.14	0.17	
		f _{osc} = 8 MHz, ceramic resonator	0.08	0.12	

Table 5-37 lists the characteristics of the USS HSPLL.

Table 5-37. USS HSPLL

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PLL_CLK _{in}	Input clock to HSPLL	4		8	MHz
PLL_CLK _{out}	Output clock from HSPLL	68		80	MHz
LOCK _{pwr}	Lock time from PLL power up	Reference clock = PLL_CLK _{in} , Sequence: Set USS.CTL.USSPWRUP bit = 1, then measure the time between PSQ_PLLUP (internal control signal) is set to 1 and HSPLL.CTL.PLL_LOCK is set to 1			64 cycles

Table 5-38 lists the characteristics of the USS SDHS.

Table 5-38. USS SDHS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{sdhs}	SDHS power domain supply voltage	$V_{sdhs} = V_{uss}$		1.52	1.6	1.65	V
$I_{sdhs_product}$	Operating supply current into AVCC and DVCC	Includes PLL, PGA, SDHS, and DTC, Modulator clock = 80MHz, Output Data Rate = 8MSPS			5.2		mA
F_m	Modulator clock ⁽¹⁾			68		80	MHz
BW_{mod}	Frequency @ -3dB SNR	Modulator clock = 80MHz. Modulator only (no filter is enabled)			1.5		MHz
SNR	Signal-to-noise ratio ⁽²⁾	Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 1000 mVpp, PVCC = 3.0 V, Fmod = 80MHz, OSR = 20	58.5	62.5		dB
		Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 760 mVpp, PVCC = 2.5 V, Fmod = 80MHz, OSR = 20	57.5	62		
		Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 200 mVpp, PVCC = 2.5 V, Fmod = 80MHz, OSR = 20	54.5	57		
		Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 100 mVpp, PVCC = 2.5 V, Fmod = 80MHz, OSR = 20	49	53		
		Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 30 mVpp, PVCC = 2.5 V, Fmod = 80MHz, OSR = 20	38.5	43		
T_{MOD_Settle}	SDHS settling time (PGA + Modulator)	TM2 - TM1, AUTOSSDIS = 0, 1% of settled DC level				40	μ s
		TM2 - TM1, AUTOSSDIS = 1, 1% of settled DC level				40	
$DROUT_{sdhs}$	Output data rate					8	MSPS

(1) Informative parameter, not characterized

(2) SNR as specified, SINAD and THD not specified over complete signal chain

Table 5-39 lists the characteristics of the USS PHY outputs.

Table 5-39. USS PHY Output Stage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PVCC	PHY supply voltage	PVCC = V _{CC} , PVSS = V _{SS}	2.2		3.6	V
R _{DSonT}	Output impedance of CH0OUT and CH1OUT for high and low side (trimmed at 3-V PV _{DD})	PVCC ≥ 2.5 V		3		Ω
R _{Term}	Termination impedance of CH0OUT and CH1OUT towards PVSS (trimmed)	PVCC ≥ 2.5 V		3		Ω
DrvM	High side to low side drive mismatch (trimmed)	PVCC ≥ 2.5 V		5	12.5	%
TermM	Termination to drive mismatch (trimmed)	PVCC ≥ 2.5 V		5	12.5	%
f _{MAX}	Maximum output frequency	PVCC = V _{CC} (2.5 V to 3.6 V)	4.5			MHz
C _{SUPP}	Supply buffering capacitance (low ESR type)	PVCC = V _{CC}	22	100		uF
R _{SUPP}	Series resistance to C _{SUPP}	PVCC = V _{CC}		22		Ω

Table 5-40 lists the characteristics of the USS PHY inputs.

Table 5-40. USS PHY Input Stage, Multiplexer

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage on CH0IN or CH1IN	PVCC = V _{CC} , PVSS = V _{SS}	PVSS – 0.3		1.8	V

Table 5-41 lists the characteristics of the USS PGA.

Table 5-41. USS PGA

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PV _{CC}	Supply voltage		2.2		3.6	V
G _N	Gain ⁽¹⁾		–6.5		30.8	dB
V _{inr1}	Input range	2.2 V ≤ PVCC	30		800	mVpp
V _{inr2}	Input range	2.5 V ≤ PVCC	30		1000	mVpp
G _{tol}	Gain tolerance	Full PGA gain range, V _{OUT} = 600 mV	–1.5		1.5	dB
GTdrift	Gain drift over temperature	Full PGA gain range, V _{OUT} = 600 mV		0.0019		dB/°C
GVdrift	Gain drift over voltage	Full PGA gain range, V _{OUT} = 600 mV		0.15		dB/V
T _{SET}	Gain settling time	Gain setting: from 0 dB to 6 dB, to ±5%		0.65	1.4	μs
DC _{offset}	DC offset (PGA and SDHS)	Full PGA gain range, measured at SDHS output		5.5		mV
DC _{drift}	DC offset drift (PGA and SDHS)	Full PGA gain range, measured at SDHS output		4.7		μV/°C
PSRR _{AC}	AC power supply rejection ratio	V _{CC} = 3 V + 50 mVpp × sin(2π × f _C) where f _C = 1 MHz, V _{IN} = ground, PSRR _{AC} = 20log(V _{OUT} / 50 mV)	PGA gain = 0 dB		–41	dB
			PGA gain = 10 dB		–37	
			PGA gain = 30 dB		–19	

(1) See PGA Gain Table in the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

Table 5-42 lists the characteristics of the USS bias voltage generator.

Table 5-42. USS Bias Voltage Generator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{exc_bias}}$ Excitation bias voltage (coupling capacitors)	PVCC = V_{CC} (2.2 V to 3.6 V), EXCBias = 0		200		mV
	PVCC = V_{CC} (2.2 V to 3.6 V), EXCBias = 1		300		
	PVCC = V_{CC} (2.2 V to 3.6 V), EXCBias = 2		400		
	PVCC = V_{CC} (2.2 V to 3.6 V), EXCBias = 3		600		
R_{VBE} Impedance of excitation bias generator	PVCC = V_{CC} (2.2 V to 3.6 V), BIMP = 0		450		Ω
	PVCC = V_{CC} (2.2 V to 3.6 V), BIMP = 1		850		
	PVCC = V_{CC} (2.2 V to 3.6 V), BIMP = 2		1450		
	PVCC = V_{CC} (2.2 V to 3.6 V), BIMP = 3		2900		
T_{SBE} Excitation bias settling time	PVCC = V_{CC} (2.2 V to 3.6 V) to 0.1% end value $R_{\text{ET}} = 200 \Omega$, $C_K + C_{\text{OP}} = 1 \text{ nF}$, BIMP = 2		20		μs
$V_{\text{pga_bias}}$ PGA bias voltage (coupling caps)	PVCC = V_{CC} (2.2 V to 3.6 V), PGABias = 0		750		mV
	PVCC = V_{CC} (2.2 V to 3.6 V), PGABias = 1		800		
	PVCC = V_{CC} (2.2 V to 3.6 V), PGABias = 2		900		
	PVCC = V_{CC} (2.2 V to 3.6 V), PGABias = 3		950		
R_{VBA} Impedance of acquisition bias generator	PVCC = V_{CC} (2.2 V to 3.6 V), BIMP = 0		500		Ω
	PVCC = V_{CC} (2.2 V to 3.6 V), BIMP = 1		900		
	PVCC = V_{CC} (2.2 V to 3.6 V), BIMP = 2		1500		
	PVCC = V_{CC} (2.2 V to 3.6 V), BIMP = 3		2950		
T_{SBA} Acquisition bias settling time	PVCC = V_{CC} (2.2 V to 3.6 V) to 0.1% end value $R_{\text{ET}} = 200 \Omega$, $C_K + C_{\text{OP}} = 1 \text{ nF}$, BIMP = 2		22		μs
R_{VBX} Impedance of bias switches on XPB0/1 terminals on top of R_{VBA}	PVCC = V_{CC} (2.2 V to 3.6 V), PGABias = 0;1;2;3 , BIMP = 0;1;2;3		1000		Ω

5.13.15 Emulation and Debug

Table 5-43 lists the characteristics of the JTAG and SBW interface.

Table 5-43. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	MIN	TYP	MAX	UNIT
I _{JTAG}	Supply current adder when JTAG active (but not clocked)	2.2 V, 3.0 V		40	100	μA
f _{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3.0 V	0		10	MHz
t _{SBW,Low}	Spy-Bi-Wire low clock pulse duration	2.2 V, 3.0 V	0.04		15	μs
t _{SBW, En}	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾	2.2 V, 3.0 V			110	μs
t _{SBW,Rst}	Spy-Bi-Wire return to normal operation time		15		100	μs
f _{TCK}	TCK input frequency, 4-wire JTAG ⁽²⁾	2.2 V	0		16	MHz
		3.0 V	0		16	
R _{internal}	Internal pulldown resistance on TEST	2.2 V, 3.0 V	20	35	50	kΩ
f _{TCLK}	TCLK/MCLK frequency during JTAG access, no FRAM access (limited by f _{SYSTEM})				16	MHz
t _{TCLK,Low/High}	TCLK low or high clock pulse duration, no FRAM access				25	ns
f _{TCLK,FRAM}	TCLK/MCLK frequency during JTAG access, including FRAM access (limited by f _{SYSTEM} with no FRAM wait states)				4	MHz
t _{TCLK,FRAM,Low/High}	TCLK low or high clock pulse duration, including FRAM accesses				100	ns

(1) Tools that access the Spy-Bi-Wire and the BSL interfaces must wait for the t_{SBW,En} time after the first transition of the TEST/SBW_{TCK} pin (low to high), before the second transition of the pin (high to low) during the entry sequence.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 Overview

The TI MSP430FR50xx/MSP430FR60xx(1) family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with seven low-power modes, is optimized to achieve extended battery life for example in portable measurement applications. The devices features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The device is an MSP430FR50xx/MSP430FR60xx family device with Ultrasonic-Sensing-Solution (USS), Low-Energy Accelerator (LEA), up to six 16-bit timers, up to six eUSCIs that support UART, SPI, and I²C, a comparator, a hardware multiplier, an AES accelerator, a 6-channel DMA, an RTC module with alarm capabilities, up to 57 I/O pins, and a high-performance 12-bit ADC. The MSP430FR60xx(1) devices also include an LCD module with contrast control for displays with up to 248 segments.

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

6.3 Ultrasonic-Sensing Solution (USS_A)

The USS_A module provides a high-precision ultrasonic-sensing solution. The USS_A module is a sophisticated system that consists of six submodules:

- UUPS (universal USS power supply)
- HSPLL (high-speed PLL) with oscillator
- ASQ (acquisition sequencer)
- PHY (physical interface)
- PPG_A (programmable pulse generator "A") with low output impedance driver
- PGA (programmable gain amplifier)
- SDHS (sigma-delta high-speed ADC) with DTC (data transfer controller)

The submodules have different roles, and together they enable high-precision data acquisition in ultrasonic applications. See the dedicated chapter for each submodule in the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

The USS module performs complete measurement sequence without CPU involvement to achieve ultra-low power consumption for ultrasonic metrology. 节 4.1 shows the USS subsystem block diagram. The USS module has dedicated I/O pins without secondary functions. See the *Ultrasonic Sensing Solution (USS)* chapter in the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#) for details.

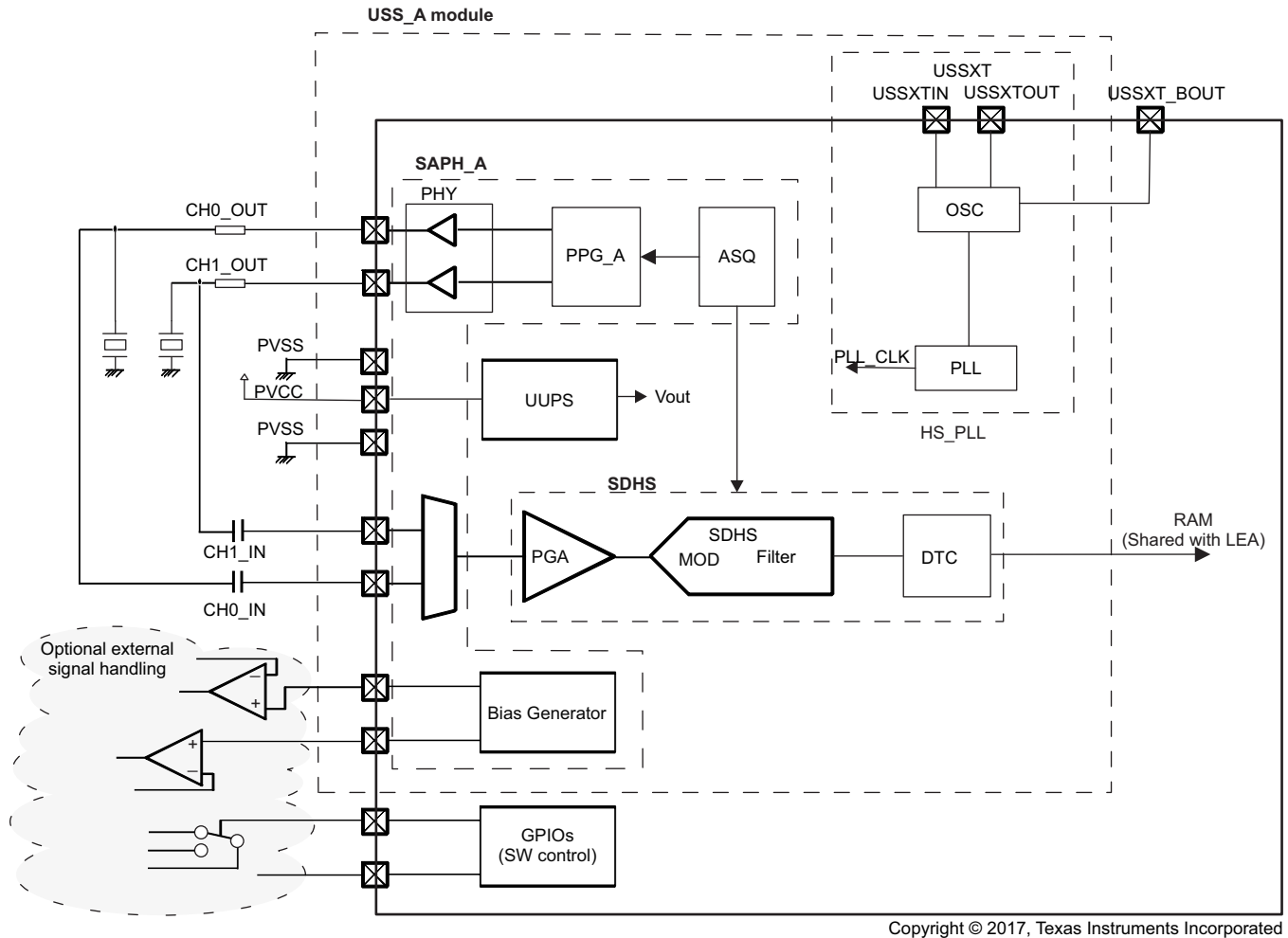


图 6-1. USS_A Subsystem Block Diagram

6.4 Low-Energy Accelerator (LEA) for Signal Processing

The LEA is a hardware engine designed for operations that involve vector-based signal processing, such as FIR, IIR, and FFT. The LEA offers fast performance and low energy consumption when performing vector-based digital signal processing computations. For performance benchmarks comparing LEA to using the CPU or other processors, see [Benchmarking the Signal Processing Capabilities of the Low-Energy Accelerator](#).

The LEA requires MCLK to be operational; therefore, LEA runs only in active mode or LPM0. While the LEA is running, the LEA data operations are performed on a shared 8KB of RAM out of the 12KB of total RAM (see 表 6-52). This shared RAM can also be used by the regular application. The MSP CPU and the LEA can run simultaneously and independently unless they access the same system RAM.

Direct access to LEA registers is not supported, and TI recommends using the optimized [Digital Signal Processing \(DSP\) Library for MSP Microcontrollers](#) for the operations that the LEA module supports.

6.5 Operating Modes

The MCU has one active mode and seven software selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 through LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

表 6-1. Operating Modes

MODE	AM		LPM0	LPM1	LPM2	LPM3	LPM4	LPM3.5	LPM4.5	
	ACTIVE	ACTIVE, FRAM OFF ⁽¹⁾	CPU OFF ⁽²⁾	CPU OFF	STANDBY	STANDBY	OFF	RTC ONLY	SHUTDOWN WITH SVS	SHUTDOWN WITHOUT SVS
Maximum system clock	16 MHz		16 MHz	16 MHz	50 kHz	50 kHz	0 ⁽³⁾	50 kHz	0 ⁽³⁾	
Typical current consumption, T _A = 25°C	103 µA/MHz	65 µA/MHz	70 µA at 1 MHz	35 µA at 1 MHz	0.7 µA	0.4 µA	0.3 µA	0.25 µA	0.2 µA	0.02 µA
Typical wake-up time	N/A		instant	6 µs	6 µs	7 µs	7 µs	250 µs	250 µs	1000 µs
Wake-up events	N/A		all	all	LF, RTC, I/O, Comp	LF, RTC, I/O, Comp	I/O, Comp	RTC, I/O	I/O	
CPU	on		off	off	off	off	off	reset	reset	
USS_A	on		on	off	off	off	off	reset	reset	
LEA	on		on ⁽⁴⁾ off	off	off	off	off	reset	reset	
FRAM	on	off ⁽¹⁾	standby (or off ⁽¹⁾)	off	off	off	off	off	off	
High-frequency peripherals	available		available	available	off	off	off	reset	reset	
Low-frequency peripherals	available		available	available	available	available ⁽⁵⁾	off	RTC MTIF	reset	
Unclocked peripherals ⁽⁶⁾	available		available	available	available	available ⁽⁵⁾	available ⁽⁵⁾	reset	reset	
MCLK	on		on ⁽⁴⁾ off	off	off	off	off	off	off	
SMCLK	optional ⁽⁷⁾		optional ⁽⁷⁾	optional ⁽⁷⁾	off	off	off	off	off	
ACLK	on		on	on	on	on	off	off	off	
Full retention	yes		yes	yes	yes	yes	yes	no	no	
SVS	always		always	always	optional ⁽⁸⁾	optional ⁽⁸⁾	optional ⁽⁸⁾	optional ⁽⁸⁾	on ⁽⁹⁾	off ⁽¹⁰⁾
Brownout	always		always	always	always	always	always	always	always	

(1) FRAM is disabled in the FRAM controller A (FRCTL_A).

(2) Disabling the FRAM through the FRAM controller A (FRCTL_A) allows the application to lower the LPM current consumption but the wake-up time increases as soon as FRAM is accessed (for example, to fetch an interrupt vector). For a non-FRAM wake-up (for example, DMA transfer to RAM) the wake-up is not delayed.

(3) All clocks are disabled.

(4) Only while LEA is performing the task enabled by CPU during AM. LEA cannot be enabled in LPM0.

(5) See 节 6.5.2, which describes the use of peripherals in LPM3 and LPM4.

(6) "Unclocked peripherals" are peripherals that do not require a clock source to operate; for example, the comparator and REF, or the eUSCI when operated as an SPI slave.

(7) Controlled by SMCLKOFF.

(8) Activated SVS (SVSHE = 1) results in higher current consumption. SVS is not included in typical current consumption.

(9) SVSHE = 1

(10) SVSHE = 0

6.5.1 Peripherals in Low-Power Modes

Peripherals can be in different states that impact the achievable power modes of the device. The states depend on the operational modes of the peripherals (see 表 6-2). The states are:

- A peripheral is in a "high-frequency state" if it requires or uses a clock with a "high" frequency of more than 50 kHz.
- A peripheral is in a "low-frequency state" if it requires or uses a clock with a "low" frequency of 50 kHz or less.
- A peripheral is in an "unlocked state" if it does not require or use an internal clock.

If the CPU requests a power mode that does not support the current state of all active peripherals, the device does not enter the requested power mode, but it does enter a power mode that still supports the current state of the peripherals, except if an external clock is used. If an external clock is used, the application must use the correct frequency range for the requested power mode.

表 6-2. Peripheral States

PERIPHERAL	IN HIGH-FREQUENCY STATE ⁽¹⁾	IN LOW-FREQUENCY STATE ⁽²⁾	IN UNLOCKED STATE ⁽³⁾
WDT	Clocked by SMCLK	Clocked by ACLK	Not applicable
DMA ⁽⁴⁾	Not applicable	Not applicable	Waiting for a trigger.
RTC_C	Not applicable	Clocked by LFXT.	Not applicable
LCD_C	Not applicable	Clocked by ACLK or VLOCLK.	Not applicable
Timer_A TAx	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
Timer_B TBx	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
eUSCI_Ax in UART mode	Clocked by SMCLK	Clocked by ACLK	Waiting for first edge of START bit.
eUSCI_Ax in SPI master mode	Clocked by SMCLK	Clocked by ACLK	Not applicable
eUSCI_Ax in SPI slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
eUSCI_Bx in I ² C master mode	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Not applicable
eUSCI_Bx in I ² C slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Waiting for START condition or clocked by external clock ≤50 kHz
eUSCI_Bx in SPI master mode	Clocked by SMCLK	Clocked by ACLK	Not applicable
eUSCI_Bx in SPI slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
ADC12_B	Clocked by SMCLK or by MODOSC	Clocked by ACLK	Waiting for a trigger
REF_A	Not applicable	Not applicable	Always
COMP_E	Not applicable	Not applicable	Always
CRC ⁽⁵⁾	Not applicable	Not applicable	Not applicable
MPY ⁽⁵⁾	Not applicable	Not applicable	Not applicable
AES ⁽⁵⁾	Not applicable	Not applicable	Not applicable

(1) Peripherals are in a state that requires or uses a clock with a "high" frequency of more than 50 kHz.

(2) Peripherals are in a state that requires or uses a clock with a "low" frequency of 50 kHz or less.

(3) Peripherals are in a state that does not require or does not use an internal clock.

(4) The DMA always transfers data in active mode but can wait for a trigger in any low-power mode. A DMA trigger during a low-power mode causes a temporary transition into active mode for the time of the transfer.

(5) This peripheral operates during active mode only and will delay the transition into a low-power mode until its operation is completed.

6.5.2 Idle Currents of Peripherals in LPM3 and LPM4

Most peripherals can be operational in LPM3 if clocked by ACLK. Some modules are operational in LPM4, because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To reduce the idle current adder, certain peripherals are grouped together. To achieve optimal current consumption, use modules within one group and limit the number of groups with active modules. 表 6-3 lists the groups. Modules not listed in this table are either already included in the standard LPM3 current consumption or cannot be used in LPM3 or LPM4.

The idle current adder is very small at room temperature (25°C) but increases at high temperatures (85°C). See the I_{IDLE} current parameters in 节 5 for details.

表 6-3. Peripheral Groups

GROUP A	GROUP B	GROUP C
Timer TA1	Timer TA0	Timer TA4
Timer TA2	Timer TA3	eUSCI_A2
Timer TB0	Comparator	eUSCI_A3
eUSCI_A0	ADC12_B	eUSCI_B1
eUSCI_A1	REF_A	LCD_C
eUSCI_B0		

6.6 Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address and signatures are in the address range 0FFFFh to 0FF80h. 图 6-2 summarizes the content of this address range.

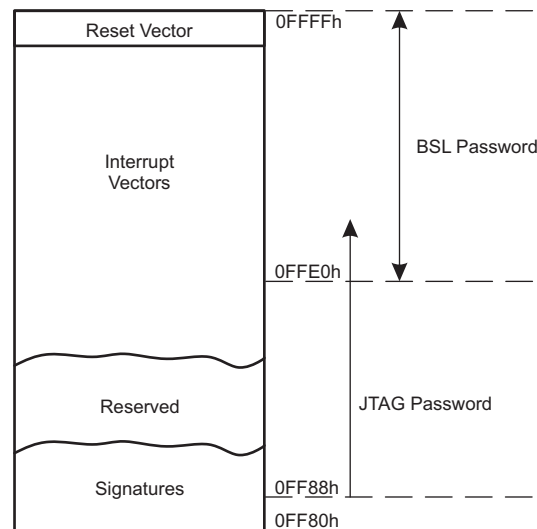


图 6-2. Interrupt Vectors, Signatures and Passwords

The power-up start address or reset vector is at 0FFFFh to 0FFFEh. It contains the 16-bit address pointing to the start address of the application program.

The interrupt vectors start at 0FFFDh and extend to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. 表 6-4 shows the device specific interrupt vector locations.

The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as BSL password (if enabled by the corresponding signature).

The signatures are located at 0FF80h and extend to higher addresses. Signatures are evaluated during device start-up. 表 6-5 shows the device specific signature locations.

A JTAG password can be programmed starting from address 0FF88h and extending to higher addresses. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password. The length of the JTAG password depends on the JTAG signature.

Refer to the chapter "System Resets, Interrupts, and Operating Modes, System Control Module (SYS)" in the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#) for details.

表 6-4. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up, brownout, supply supervisor External reset $\overline{\text{RST}}$ Watchdog time-out (watchdog mode) WDT, FRCTL MPU, CS, PMM password violation FRAM uncorrectable bit error detection MPU segment violation Software POR, BOR	SVSHIFG PMMRSTIFG WDTIFG WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW UBDIFG MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG PMMPORIFG, PMMBORIFG (SYSRSTIV) ^{(1) (2)}	Reset	0FFFEh	Highest
System NMI Vacant memory access JTAG mailbox FRAM access time error FRAM write protection error FRAM bit error detection MPU segment violation	VMAIFG JMBINIFG, JMBOUTIFG ACCTEIFG, WPIFG CBDIFG, UBDIFG MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG (SYSSNIV) ^{(1) (3)}	(Non)maskable	0FFFCh	
User NMI External NMI Oscillator fault LEA RAM access conflict	NMIIIFG, OFIFG DACCESSIFG (SYSUNIV) ^{(1) (3)}	(Non)maskable	0FFFAh	
Comparator_E	CEIFG, CEIIFG (CEIV) ⁽¹⁾	Maskable	0FFF8h	
TB0	TB0CCR0.CCIFG	Maskable	0FFF6h	
TB0	TB0CCR1.CCIFG ... TB0CCR6.CCIFG, TB0CTL.TBIFG (TB0IV) ⁽¹⁾	Maskable	0FFF4h	
Watchdog timer (interval timer mode)	WDTIFG	Maskable	0FFF2h	
eUSCI_A0 receive or transmit	UCA0IFG: UCRXIFG, UCTXIFG (SPI mode) UCA0IFG: UCSTTIFG, UCTXCPITIFG, UCRXIFG, UCTXIFG (UART mode) (UCA0IV) ⁽¹⁾	Maskable	0FFF0h	
eUSCI_B0 receive or transmit	UCB0IFG: UCRXIFG, UCTXIFG (SPI mode) UCB0IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I ² C mode) (UCB0IV) ⁽¹⁾	Maskable	0FFEEh	
ADC12_B	ADC12IFG0 to ADC12IFG31 ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC12OVIFG, ADC12TOVIFG (ADC12IV) ^{(1) (4)}	Maskable	0FFECCh	
TA0	TA0CCR0.CCIFG	Maskable	0FFEAh	

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space.

(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.

(4) Only on devices with ADC, otherwise reserved.

表 6-4. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
TA0	TA0CCR1.CCIFG, TA0CCR2.CCIFG, TA0CTL.TAIFG (TA0IV) ⁽¹⁾	Maskable	0FFE8h	
eUSCI_A1 receive or transmit	UCA1IFG: UCRXIFG, UCTXIFG (SPI mode) UCA1IFG: UCSTTIFG, UCTXCPITIFG, UCRXIFG, UCTXIFG (UART mode) (UCA1IV) ⁽¹⁾	Maskable	0FFE6h	
DMA	DMA0CTL.DMAIFG, DMA1CTL.DMAIFG, DMA2CTL.DMAIFG (DMAIV) ⁽¹⁾	Maskable	0FFE4h	
TA1	TA1CCR0.CCIFG	Maskable	0FFE2h	
TA1	TA1CCR1.CCIFG, TA1CCR2.CCIFG, TA1CTL.TAIFG (TA1IV) ⁽¹⁾	Maskable	0FFE0h	
I/O port P1	P1IFG.0 to P1IFG.7 (P1IV) ⁽¹⁾	Maskable	0FFDEh	
TA2	TA2CCR0.CCIFG	Maskable	0FFDCh	
TA2	TA2CCR1.CCIFG TA2CTL.TAIFG (TA2IV) ⁽¹⁾	Maskable	0FFDAh	
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV) ⁽¹⁾	Maskable	0FFD8h	
TA3	TA3CCR0.CCIFG	Maskable	0FFD6h	
TA3	TA3CCR1.CCIFG TA3CTL.TAIFG (TA3IV) ⁽¹⁾	Maskable	0FFD4h	
I/O port P3	P3IFG.0 to P3IFG.7 (P3IV) ⁽¹⁾	Maskable	0FFD2h	
I/O port P4	P4IFG.0 to P4IFG.2 (P4IV) ⁽¹⁾	Maskable	0FFD0h	
LCD_C	LCD_C Interrupt Flags (LDCIV) ⁽¹⁾	Maskable	0FFCEh	
RTC_C	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) ⁽¹⁾	Maskable	0FFCCh	
AES	AESRDYIFG	Maskable	0FFCAh	
TA4	TA4CCR0.CCIFG	Maskable	0FFC8h	
TA4	TA4CCR1.CCIFG TA4CTL.TAIFG (TA4IV) ⁽¹⁾	Maskable	0FFC6h	
I/O port P5	P5IFG.0 to P5IFG.2 (P5IV) ⁽¹⁾	Maskable	0FFC4h	
I/O port P6	P6IFG.0 to P6IFG.2 (P6IV) ⁽¹⁾	Maskable	0FFC2h	
eUSCI_A2 receive or transmit	UCA2IFG: UCRXIFG, UCTXIFG (SPI mode) UCA2IFG: UCSTTIFG, UCTXCPITIFG, UCRXIFG, UCTXIFG (UART mode) (UCA2IV) ⁽¹⁾	Maskable	0FFC0h	
eUSCI_A3 receive or transmit	UCA3IFG: UCRXIFG, UCTXIFG (SPI mode) UCA3IFG: UCSTTIFG, UCTXCPITIFG, UCRXIFG, UCTXIFG (UART mode) (UCA3IV) ⁽¹⁾	Maskable	0FFBEh	
eUSCI_B1 receive or transmit	UCB1IFG: UCRXIFG, UCTXIFG (SPI mode) UCB1IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I ² C mode) (UCB1IV) ⁽¹⁾	Maskable	0FFBCh	

表 6-4. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
I/O port P7	P7IFG.0 (P7IV) ⁽¹⁾	Maskable	0FFBAh	
LEA	CMDIFG, SDIIFG, OORIFG, TIFG, COVLIFG (LEAIV) ⁽¹⁾	Maskable	0FFB8h	
UUPS	PTMOUT, PREQIG (IIDX) ⁽¹⁾	Maskable	0FFB6h	
HSPLL	PLLUNLOCK (IIDX) ⁽¹⁾	Maskable	0FFB4h	
SAPH_A	DATAERR, TAMTO, SEQDN, PNGDN (IIDX) ⁽¹⁾	Maskable	0FFB2h	
SDHS	OVF, ACQDONE, SSTRG, DTRDY, WINHI, WINLO (IIDX) ⁽¹⁾	Maskable	0FFB0h	Lowest

表 6-5. Signatures

SIGNATURE	WORD ADDRESS
IP Encapsulation Signature2	0FF8Ah
IP Encapsulation Signature1 ⁽¹⁾	0FF88h
BSL Signature2	0FF86h
BSL Signature1	0FF84h
JTAG Signature2	0FF82h
JTAG Signature1	0FF80h

(1) Must not contain 0AAAAh if used as the JTAG password.

6.7 Bootloader (BSL)

The BSL can program the FRAM or RAM using a UART serial interface (FRxxxx devices) or an I²C interface (FRxxxx1 devices). Access to the device memory through the BSL is protected by an user-defined password. 表 6-6 lists the pins that are required for use of the BSL. BSL entry requires a specific entry sequence on the RST/NMI/SBWDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the [MSP430™ FRAM Devices Bootloader \(BSL\) User's Guide](#). More information on the BSL can be found at www.ti.com/tool/mspbsl.

表 6-6. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
RST/NMI/SBWDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P2.0	Devices with UART BSL (FRxxxx): Data transmit
P2.1	Devices with UART BSL (FRxxxx): Data receive
P1.6	Devices with I ² C BSL (FRxxxx1): Data
P1.7	Devices with I ² C BSL (FRxxxx1): Clock
DVCC, AVCC	Power supply
DVSS, AVSS	Ground supply

6.8 JTAG Operation

6.8.1 JTAG Standard Interface

The MSP family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$ /NMI/SBWDIO is required to interface with MSP development tools and device programmers. 表 6-7 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

表 6-7. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$ /NMI/SBWDIO	IN	External reset
DVCC, AVCC	na	Power supply
DVSS, AVSS	na	Ground supply

6.8.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in 表 6-8. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

表 6-8. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$ /NMI/SBWDIO	IN, OUT	Spy-Bi-Wire data input and output
DVCC, AVCC	na	Power supply
DVSS, AVSS	na	Ground supply

6.9 FRAM Controller A (FRCTL_A)

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Ultra-low-power ultra-fast-write nonvolatile memory
- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

注

Wait States

For MCLK frequencies >8 MHz, wait states must be configured as described in the *Wait State Control* section of the *FRAM Controller A (FRCTL_A)* chapter in the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#).

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see [MSP430™ FRAM Technology – How To and Best Practices](#).

6.10 RAM

The RAM is made up of three sectors. Sector 0 = 2KB, Sector 1 = 2KB, Sector 2 = 8KB (shared with LEA). Each sector can be individually powered down in LPM3 and LPM4 to save leakage. Data is lost when sectors are powered down in LPM3 and LPM4.

6.11 Tiny RAM

22 bytes of Tiny RAM are provided in addition to the complete RAM (see [表 6-52](#)). This memory is always available, even in LPM3 and LPM4, while the complete RAM can be powered down in LPM3 and LPM4. Tiny RAM can be used to hold data or a very small stack when the complete RAM is powered down in LPM3 and LPM4. No memory is available in LPMx.5.

6.12 Memory Protection Unit (MPU) Including IP Encapsulation

The FRAM can be protected by the MPU from inadvertent CPU execution, read access, or write access. Features of the MPU include:

- IP encapsulation with programmable boundaries in steps of 1KB (prevents reads from "outside"; for example, through JTAG or by non-IP software).
- Main memory partitioning is programmable up to three segments in steps of 1KB.
- Access rights of each segment can be individually selected (main and information memory).
- Access violation flags with interrupt capability for easy servicing of access violations.

6.13 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be controlled using all instructions. For complete module descriptions, see the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

6.13.1 Digital I/O

Up to eight 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wakeup input capability is available for all pins of ports P1, P2, P3, P4, P5, P6, and P7.
- Read and write access to port control registers is supported by all instructions.
- Ports P1/P2, P3/P4, P5/P6, P7/(P8) can be accessed byte-wise or word-wise in pairs.
- No cross-currents during start-up.

注

Configuration of Digital I/Os After BOR Reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and their module functions disabled. To enable the I/O functionality after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, refer to the "Configuration After Reset" section of the *Digital I/O* chapter in the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

6.13.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch-crystal oscillator XT1 (LF), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2 (HF). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK). ACLK can be sourced from a 32-kHz watch crystal (LFXT1), the internal VLO, or a digital external low-frequency (<50 kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal DCO, a 32-kHz watch crystal (LFXT1), the internal VLO, or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.
- The high frequency oscillator XT2 (HF) can be sourced from the oscillator of the ultrasonic subsystem USSXT through an internal connection.

6.13.3 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a safe level and below a user-selectable level. SVS circuitry is available on the primary and core supplies.

6.13.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations.

6.13.5 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock (RTC) with the following features:

- Calendar mode with leap year correction
- General-purpose counter mode

The internal calendar compensates for months with fewer than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption.

6.13.6 Measurement Test Interface (MTIF)

The MTIF module provides a simple pulse-based test interface that is used to implement consumption monitoring of "legal relevant data" with high integrity. MTIF consists of the a pulse generator, a pulse counter, and a pulse interface. MTIF has following features:

- Independent passwords for generator counter and pulse interface
- Pulse rates up to 1016 pulses/second
- Pulse frame duration from 1/16 s to 16 s
- Count capacity up to 65535 (16 bit)
- Operating in LPM3.5 with 200 nA
- 2-pin interface with MTIF_OUT_IN and MTIF_PIN_EN

6.13.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart if a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. 表 6-9 lists the clocks that can be selected by the WDT.

表 6-9. WDT_A Clocks

WDTSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	LFMODCLK

6.13.8 System Module (SYS)

The SYS module manages many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader (BSL) entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. 表 6-10 lists the SYS module interrupt vector registers.

表 6-10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$ /NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog timeout (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		MPUPW MPU password violation (PUC)	22h	
		CSPW CS password violation (PUC)	24h	
		MPUSEGPIFG encapsulated IP memory segment violation (PUC)	26h	
		Reserved	28h	
		MPUSEG1IFG segment 1 memory violation (PUC)	2Ah	
		MPUSEG2IFG segment 2 memory violation (PUC)	2Ch	
		MPUSEG3IFG segment 3 memory violation (PUC)	2Eh	
SYSSNIV, System NMI	019Ch	Reserved	30h to 3Eh	Lowest
		No interrupt pending	00h	
		Reserved	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		FRAM Access Time Error	06h	
		MPUSEGPIFG encapsulated IP memory segment violation	08h	
		Reserved	0Ah	
		MPUSEG1IFG segment 1 memory violation	0Ch	
		MPUSEG2IFG segment 2 memory violation	0Eh	
		MPUSEG3IFG segment 3 memory violation	10h	
		VMAIFG Vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		FRAM Write Protection Detection	1Ah	
		LEA Time-out Fault	1Ch	
		LEA Command Fault	1Eh	Lowest

表 6-10. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG NMI pin	02h	Highest
		OFIFG oscillator fault	04h	
		DACCESSIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

6.13.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. 表 6-11 lists the available DMA trigger assignments.

表 6-11. DMA Trigger Assignments⁽¹⁾

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4	CHANNEL 5
0	DMAREQ	DMAREQ	DMAREQ	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	TA4CCR0 CCIFG	TA4CCR0 CCIFG	TA4CCR0 CCIFG	TA4CCR0 CCIFG	TA4CCR0 CCIFG	TA4CCR0 CCIFG
10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11	AES Trigger 0	AES Trigger 0	AES Trigger 0	AES Trigger 0	AES Trigger 0	AES Trigger 0
12	AES Trigger 1	AES Trigger 1	AES Trigger 1	AES Trigger 1	AES Trigger 1	AES Trigger 1
13	AES Trigger 2	AES Trigger 2	AES Trigger 2	AES Trigger 2	AES Trigger 2	AES Trigger 2
14	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG	UCA2RXIFG	UCA2RXIFG	UCA2RXIFG
15	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG	UCA2TXIFG	UCA2TXIFG	UCA2TXIFG
16	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG	UCA3RXIFG	UCA3RXIFG	UCA3RXIFG
17	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG	UCA3TXIFG	UCA3TXIFG	UCA3TXIFG
18	UCB0RXIFG (SPI) UCB0RXIFG0 (I ² C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I ² C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I ² C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I ² C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I ² C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I ² C)
19	UCB0TXIFG (SPI) UCB0TXIFG0 (I ² C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I ² C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I ² C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I ² C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I ² C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I ² C)
20	UCB0RXIFG1 (I ² C)	UCB0RXIFG1 (I ² C)	UCB0RXIFG1 (I ² C)	UCB1RXIFG1 (I ² C)	UCB1RXIFG1 (I ² C)	UCB1RXIFG1 (I ² C)
21	UCB0TXIFG1 (I ² C)	UCB0TXIFG1 (I ² C)	UCB0TXIFG1 (I ² C)	UCB1TXIFG1 (I ² C)	UCB1TXIFG1 (I ² C)	UCB1TXIFG1 (I ² C)
22	UCB0RXIFG2 (I ² C)	UCB0RXIFG2 (I ² C)	UCB0RXIFG2 (I ² C)	UCB1RXIFG2 (I ² C)	UCB1RXIFG2 (I ² C)	UCB1RXIFG2 (I ² C)
23	UCB0TXIFG2 (I ² C)	UCB0TXIFG2 (I ² C)	UCB0TXIFG2 (I ² C)	UCB1TXIFG2 (I ² C)	UCB1TXIFG2 (I ² C)	UCB1TXIFG2 (I ² C)
24	UCB0RXIFG3 (I ² C)	UCB0RXIFG3 (I ² C)	UCB0RXIFG3 (I ² C)	UCB1RXIFG3 (I ² C)	UCB1RXIFG3 (I ² C)	UCB1RXIFG3 (I ² C)
25	UCB0TXIFG3 (I ² C)	UCB0TXIFG3 (I ² C)	UCB0TXIFG3 (I ² C)	UCB1TXIFG3 (I ² C)	UCB1TXIFG3 (I ² C)	UCB1TXIFG3 (I ² C)
26	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion
27	LEA Ready	LEA Ready	USS_A PPGTRIG	USS_A PPGTRIG	LEA Ready	LEA Ready
28	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

(1) If a reserved trigger source is selected, no trigger is generated.

表 6-11. DMA Trigger Assignments⁽¹⁾ (continued)

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4	CHANNEL 5
29	MPY ready	MPY ready	MPY ready	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG	DMA5IFG	DMA3IFG	DMA4IFG
31	DMAE0	DMAE0	DMAE0	DMAE0	DMAE0	DMAE0

6.13.10 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_A0, eUSCI_A1, eUSCI_A2, and eUSCI_A3 module provides support for SPI (3- or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_B0 and eUSCI_B1 module provides support for SPI (3- or 4-pin) and I²C.

Up to four eUSCI_A modules and up to two eUSCI_B modules are implemented.

6.13.11 TA0, TA1, and TA4

TA0, TA1, and TA4 are 16-bit timers and counters (Timer_A type) with three (TA0 and TA1) or two (TA4) capture/compare registers each. Each timer can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-12, 表 6-13, and 表 6-14). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-12. TA0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.4, P4.5, P6.0	TA0CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.4, P4.5, P6.0	TA0CLK	INCLK	CCR0	TA0	TA0.0	
P2.3	TA0.0	CCI0A				P2.3
P5.4	TA0.0	CCI0B				P5.4
	DVSS	GND				
	DVCC	V _{CC}	CCR1	TA1	TA0.1	
P6.7	TA0.1	CCI1A				P6.7
	COUT (internal)	CCI1B				ADC12(internal) ⁽¹⁾ ADC12SHSx = {1}
	DVSS	GND				
	DVCC	V _{CC}	CCR2	TA2	TA0.2	
P5.7	TA0.2	CCI2A				P5.7
	ACLK (internal)	CCI2B				P2.5
	DVSS	GND				UUPS Trigger (USSPWRUP) UUPS.CTL.USSPWR UPSEL = {2}
	DVCC	V _{CC}				

(1) Only on devices with ADC.

表 6-13. TA1 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.4, P4.5, P3.1	TA1CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.4, P4.5, P3.1	$\overline{\text{TA1CLK}}$	INCLK				
P1.0	TA1.0	CCI0A	CCR0	TA0	TA1.0	P1.0
P7.0	TA1.0	CCI0B				P1.2
	DVSS	GND				P7.0
	DVCC	V _{CC}				
P3.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	P1.3
	COU _T (internal)	CCI1B				P3.2
	DVSS	GND				ADC12(internal) ⁽¹⁾ ADC12SHSx = {4}
	DVCC	V _{CC}				
P2.6	TA1.2	CCI2A	CCR2	TA2	TA1.2	P2.6
	ACLK (internal)	CCI2B				P7.0
	DVSS	GND				ASQ Trigger (ASQTRIG) SAPH.ASCTL0.TRIG SEL={2}
	DVCC	V _{CC}				

(1) Only on devices with ADC.

表 6-14. TA4 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
PJ.1, P4.6, PPGTick	TA4CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
PJ.1, P4.6, PPGTick	$\overline{\text{TA4CLK}}$	INCLK				
P1.1	TA4.0	CCI0A	CCR0	TA0	TA4.0	P1.1
P2.5	TA4.0	CCI0B				P2.5
	DVSS	GND				
	DVCC	V _{CC}				
P5.5	TA4.1	CCI1A	CCR1	TA1	TA4.1	P5.5
P2.7	TA4.1	CCI1B				P2.7
	DVSS	GND				ADC12(internal) ⁽¹⁾ ADC12SHSx = {7}
	DVCC	V _{CC}				

(1) Only on devices with ADC.

6.13.12 TA2 and TA3

TA2 and TA3 are 16-bit timers and counters (Timer_A type) with two capture/compare registers each and with internal connections only. Each timer can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-15 and 表 6-16). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-15. TA2 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
Reserved	INCLK			
TA3 CCR0 output (internal)	CCI0A	CCR0	TA0	TA3 CCI0A input
ACLK (internal)	CCI0B			
DVSS	GND			
DVCC	V _{CC}			
Reserved	CCI1A	CCR1	TA1	ADC12(internal) ⁽¹⁾ ADC12SHSx = {5}
COUT (internal)	CCI1B			PPG Trigger (PPGTRIG) SAPH.PGCTL.TRSEL={2}
DVSS	GND			
DVCC	V _{CC}			

(1) Only on devices with ADC

表 6-16. TA3 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
Reserved	INCLK			
TA2 CCR0 output (internal)	CCI0A	CCR0	TA0	TA2 CCI0A input
ACLK (internal)	CCI0B			
DVSS	GND			
DVCC	V _{CC}			
Reserved	CCI1A	CCR1	TA1	ADC12(internal) ⁽¹⁾ ADC12SHSx = {6}
COUT (internal)	CCI1B			
DVSS	GND			
DVCC	V _{CC}			

(1) Only on devices with ADC

6.13.13 TB0

TB0 is a 16-bit timer and counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-17). TB0 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-17. TB0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.4, P4.6, P6.2	TB0CLK	TBCLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.4, P4.6, P6.2	TB0CLK	INCLK	CCR0	TB0	TB0.0	
P3.0	TB0.0	CCI0A				P3.0
P5.0	TB0.0	CCI0B				P5.0
	DVSS	GND				ADC12 (internal) ⁽¹⁾ ADC12SHSx = {2}
	DVCC	V _{CC}	CCR1	TB1	TB0.1	
P3.1	TB0.1	CCI1A				P3.1
	COU (internal)	CCI1B				P5.1
	DVSS	GND				ADC12 (internal) ⁽¹⁾ ADC12SHSx = {3}
	DVCC	V _{CC}	CCR2	TB2	TB0.2	
P3.7	TB0.2	CCI2A				P3.7
	ACLK (internal)	CCI2B				P5.2
	DVSS	GND				
	DVCC	V _{CC}	CCR3	TB3	TB0.3	
P5.3	TB0.3	CCI3A				P5.3
P3.3	TB0.3	CCI3B				P3.3
	DVSS	GND				
	DVCC	V _{CC}	CCR4	TB4	TB0.4	
P1.4	TB0.4	CCI4A				P1.4
P4.1	TB0.4	CCI4B				P4.1
	DVSS	GND				
	DVCC	V _{CC}	CCR5	TB5	TB0.5	
P1.5	TB0.5	CCI5A				P1.5
P4.2	TB0.5	CCI5B				P4.2
	DVSS	GND				
	DVCC	V _{CC}	CCR6	TB6	TB0.6	
PJ.3	TB0.6	CCI6A				PJ.3
P3.6	TB0.6	CCI6B				P3.6
	DVSS	GND				
	DVCC	V _{CC}				

(1) Only on devices with ADC.

6.13.14 ADC12_B

The ADC12_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, a reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

表 6-18 lists the available external trigger sources. 表 6-19 lists the available multiplexing between internal and external analog inputs.

表 6-18. ADC12_B Trigger Signal Connections

ADC12SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC12SC)
001	1	TA0 CCR1 output
010	2	TB0 CCR0 output
011	3	TB0 CCR1 output
100	4	TA1 CCR1 output
101	5	TA2 CCR1 output
110	6	TA3 CCR1 output
111	7	TA4 CCR1 output

表 6-19. ADC12_B External and Internal Signal Mapping

CONTROL BIT IN ADC12CTL3 REGISTER	EXTERNAL ADC INPUT (CONTROL BIT = 0)	INTERNAL ADC INPUT (CONTROL BIT = 1)
ADC12BATMAP	A31	Battery monitor
ADC12TCMAP	A30	Temperature sensor
ADC12CH0MAP	A29	N/A ⁽¹⁾
ADC12CH1MAP	A28	N/A ⁽¹⁾
ADC12CH2MAP	A27	N/A ⁽¹⁾
ADC12CH3MAP	A26	N/A ⁽¹⁾

(1) N/A = No internal signal is available on this device.

6.13.15 USS_A

表 6-20 lists the available connections for the UUPS trigger signal.

表 6-20. UUPS Trigger Signal Connections

UUPS.CTL.USSPWR UPSEL	CONNECTED TRIGGER SOURCE
BINARY	
00	Software (UUPS.CTL.USSPWRUP)
01	RTC(any enabled interrupt events)
10	TA0 CCR2 output
11	P1.7

表 6-21 lists the available connections for the PPG trigger signal.

表 6-21. PPG Trigger Signal Connections

SAPH.PGCTL.TRSEL	CONNECTED TRIGGER SOURCE
BINARY	
00	Software (SAPH.PPGTRIG.PPGTRIG)
01	ASQ (acquisition sequencer)
10	TA2 CCR1 output
11	Reserved

表 6-22 lists the available connections for the ASQ trigger signal.

表 6-22. ASQ Trigger Signal Connections

SAPH.ASCTL0.TRIG SEL	CONNECTED TRIGGER SOURCE
BINARY	
00	Software (SAPH.ASQTRIG.ASQTRIG)
01	PSQ (power sequencer)
10	TA1 CCR2 output
11	Reserved

6.13.16 Comparator_E

The primary function of the Comparator_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.13.17 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.13.18 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC32 signature is based on the ISO 3309 standard.

6.13.19 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-, 192-, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

6.13.20 True Random Seed

The Device Descriptor Information (TLV) section contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

6.13.21 Shared Reference (REF)

The REF module is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

6.13.22 LCD_C

The LCD_C driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, and 2-mux up to 8-mux LCDs are supported. The module can provide an LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments in static, 2-mux, 3-mux, and 4-mux modes.

To reduce system noise the charge pump can be temporarily disabled. lists the available automatic charge pump disable options.

表 6-23. LCD Automatic Charge Pump Disable Bits (LCDCPDISx)

CONTROL BIT	DESCRIPTION
LDCPDIS0	LCD charge pump disable during ADC12 conversion 0b = LCD charge pump not automatically disabled during conversion. 1b = LCD charge pump automatically disabled during conversion.
LDCPDIS1 to LDCPDIS7	No functionality

6.13.23 Embedded Emulation

6.13.23.1 Embedded Emulation Module (EEM) (S Version)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.13.23.2 EnergyTrace++ Technology

The devices implement circuitry to support EnergyTrace++ technology. The EnergyTrace++ technology allows you to observe information about the internal states of the microcontroller. These states include the CPU Program Counter (PC), the ON or OFF status of the peripherals and the system clocks (regardless of the clock source), and the low-power mode currently in use. These states can always be read by a debug tool, even when the microcontroller sleeps in LPMx.5 modes.

The activity of the following modules can be observed:

- LEA is running.
- MPY is calculating.
- WDT is counting.
- RTC is counting.
- ADC: a sequence, sample, or conversion is active.
- REF: REFBG or REFGEN active and BG in static mode.
- COMP is on.
- AES is encrypting or decrypting.
- eUSCI_A0 is transferring (receiving or transmitting) data.
- eUSCI_A1 is transferring (receiving or transmitting) data.
- eUSCI_A2 is transferring (receiving or transmitting) data.
- eUSCI_A3 is transferring (receiving or transmitting) data.
- eUSCI_B0 is transferring (receiving or transmitting) data.
- eUSCI_B1 is transferring (receiving or transmitting) data.
- TB0 is counting.
- TA0 is counting.
- TA1 is counting.
- TA2 is counting.
- TA3 is counting.
- TA4 is counting.
- LCD_C is running.
- USS status

6.14 Input/Output (in Migration) Diagrams

6.14.1 Port Function Select Registers (PySEL1 , PySEL0)

Port pins are multiplexed with peripheral module functions as described in the [MSP430FR58xx](#), [MSP430FR59xx](#), [MSP430FR68xx](#), [MSP430FR69xx Family User's Guide](#). The functions of each port pin are controlled by its port function select registers, PySEL1 and PySEL0, where y = port number. The bits in the registers are mapped to the pins in the port. The primary module function, secondary module function, and tertiary module function of the pins are determined by the configuration of the PySEL1.x bit and the PySEL0.x bit as shown in . For example, P1SEL1.0 and P1SEL0.0 determine the primary module function, secondary module function, and tertiary module function of the P1.0 pin, which is in port 1. The module functions may also require the PxDIR bits to be configured according to the direction needed for the module function.

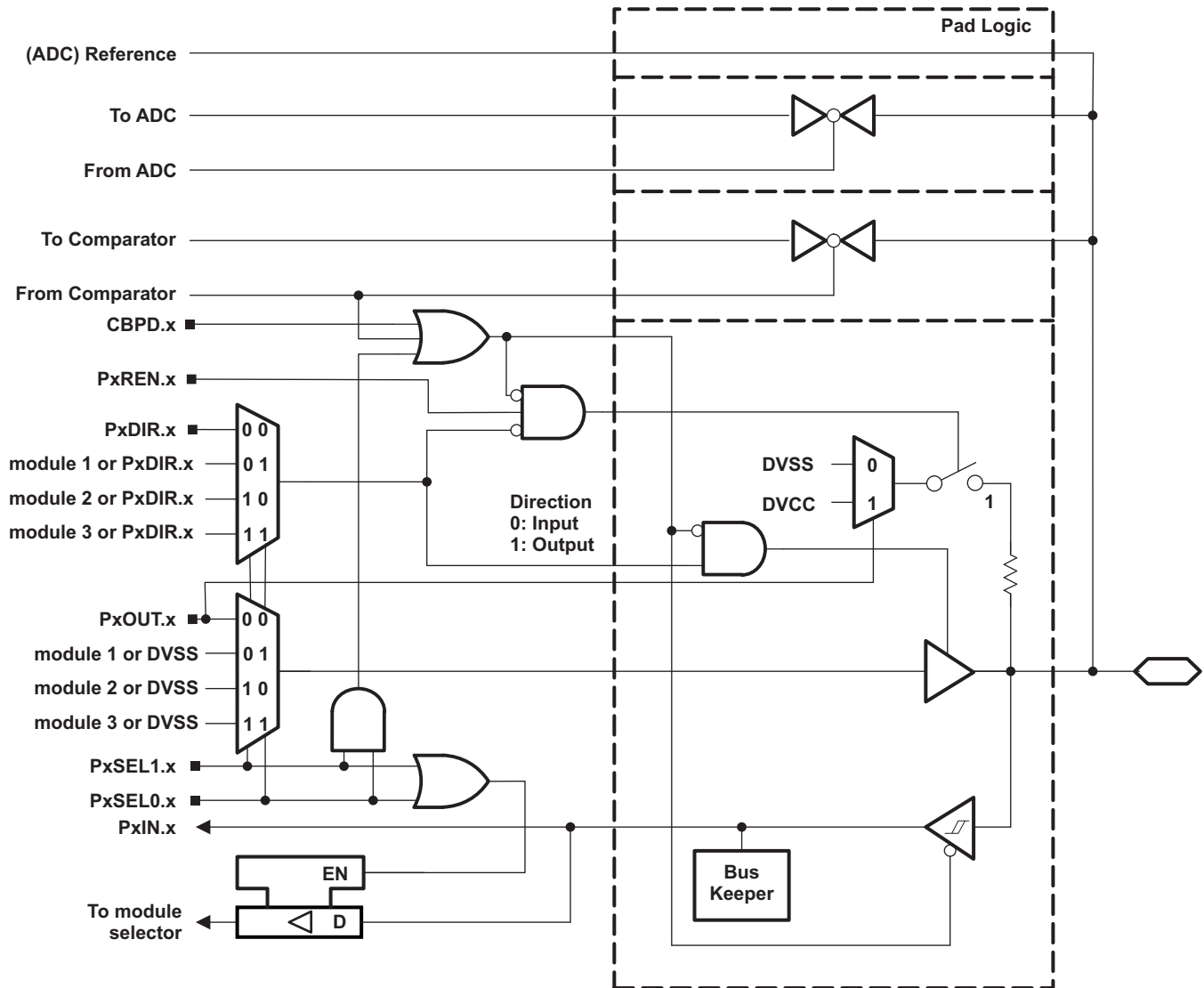
表 6-24. I/O Function Selection

I/O FUNCTIONS	PySEL1.x	PySEL1.x
General purpose I/O is selected	0	0
Primary module function is selected	0	1
Secondary module function is selected	1	0
Tertiary module function is selected	1	1

See the port pin function tables in the following section for the configurations of the function and direction for each pin.

6.14.2 Port P1 (P1.0 and P1.1) Input/Output With Schmitt Trigger

图 6-3 shows the port diagram. 表 6-25 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-3. Port P1 (P1.0 to P1.1) Diagram

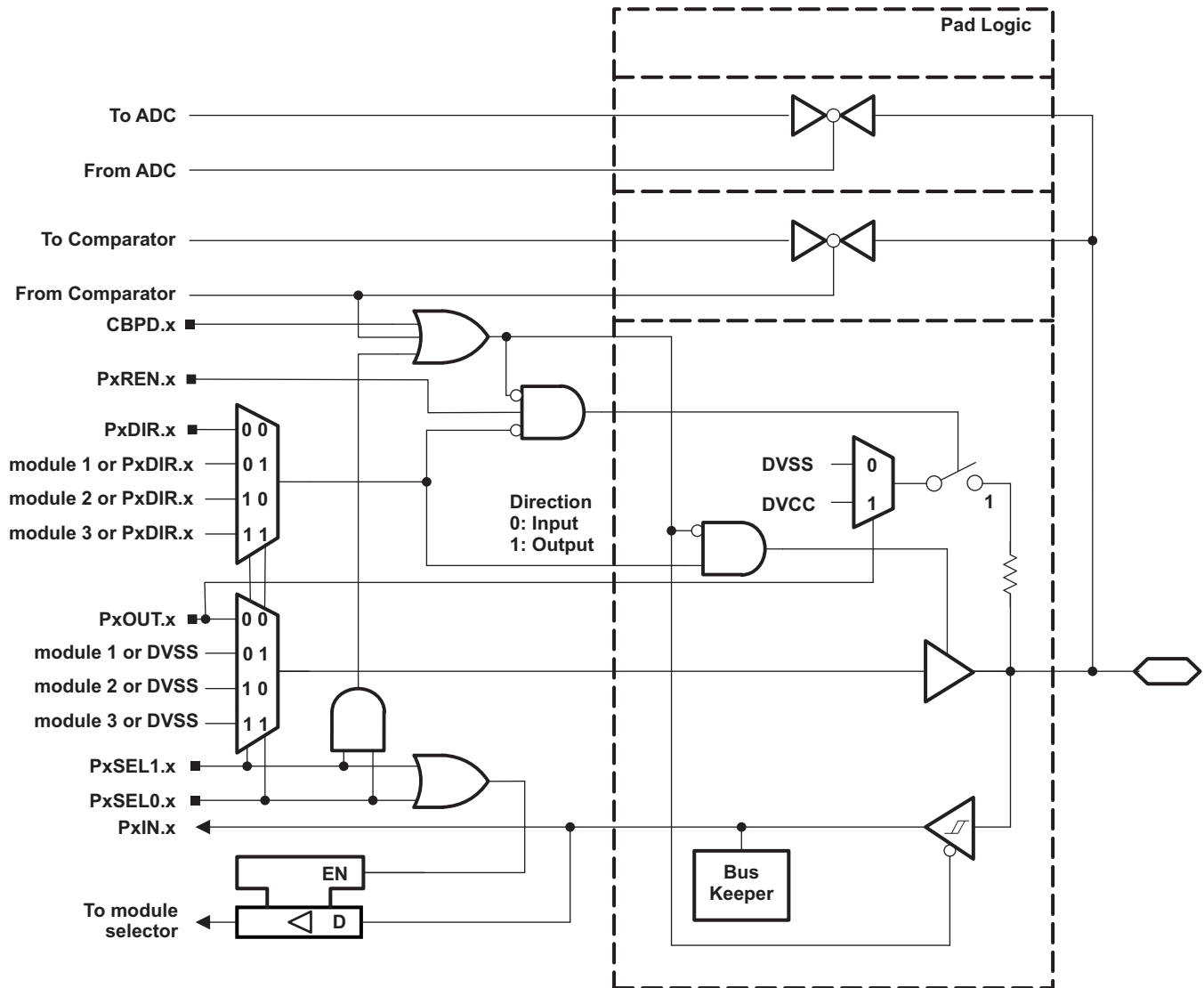
表 6-25. Port P1 (P1.0 to P1.1) Pin Functions

PIN NAME (P1.x)	P N 80	P M R G C 64	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾		
				P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/UCA1CLK/TA1.0/A0/C0/VREF-/VeREF-	4	3	P1.0 (I/O)	I: 0; O: 1	0	0
			UCA1CLK	X ⁽²⁾	0	1
			TA1.CCI0A	0	1	0
			TA1.0	1		
			A0, C0, VREF-, VeREF- ⁽³⁾⁽⁴⁾	X	1	1
P1.1/UCA1STE/TA4.0/A1/C1/VREF+/VeREF+	5	4	P1.1 (I/O)	I: 0; O: 1	0	0
			UCA1STE	X ⁽²⁾	0	1
			TA4.CCI0A	0	1	0
			TA4.0	1		
			A1, C1, VREF+, VeREF+ ⁽³⁾⁽⁴⁾	X	1	1

- (1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

6.14.3 Port P1 (P1.2 to P1.5) Input/Output With Schmitt Trigger

图 6-4 shows the port diagram. 表 6-26 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-4. Port P1 (P1.2 to P1.5) Diagram

表 6-26. Port P1 (P1.2 to P1.5) Pin Functions

PIN NAME (P1.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾		
				P1DIR.x	P1SEL1.x	P1SEL0.x
P1.2/UCA1SIMO/UCA1TXD/TA1.0/A8/C8	25	19	P1.2 (I/O)	I: 0; O: 1	0	0
			UCA1SIMO/UCA1TXD	X ⁽²⁾	0	1
			N/A	0	1	0
			TA1.0	1		
			A8, C8 ⁽³⁾⁽⁴⁾	X	1	1
P1.3/UCA1SOMI/UCA1RXD/TA1.1/A9/C9	26	20	P1.3 (I/O)	I: 0; O: 1	0	0
			UCA1SOMI/UCA1RXD	X ⁽²⁾	0	1
			N/A	0	1	0
			TA1.1	1		
			A9, C9 ⁽³⁾⁽⁴⁾	X	1	1
P1.4/TB0.4/UCB0STE/A2/C2	31	25	P1.4 (I/O)	I: 0; O: 1	0	0
			TB0.CCI4A	0	0	1
			TB0.4	1		
			UCB0STE	X ⁽⁵⁾	1	0
			A2, C2 ⁽³⁾⁽⁴⁾	X	1	1
P1.5/TB0.5/UCB0CLK/A3/C3	32	26	P1.5(I/O)	I: 0; O: 1	0	0
			TB0.CCI5A	0	0	1
			TB0.5	1		
			UCB0CLK	X ⁽⁵⁾	1	0
			A3, C3 ⁽³⁾⁽⁴⁾	X	1	1

(1) X = Don't care

(2) Direction controlled by eUSCI_A1 module.

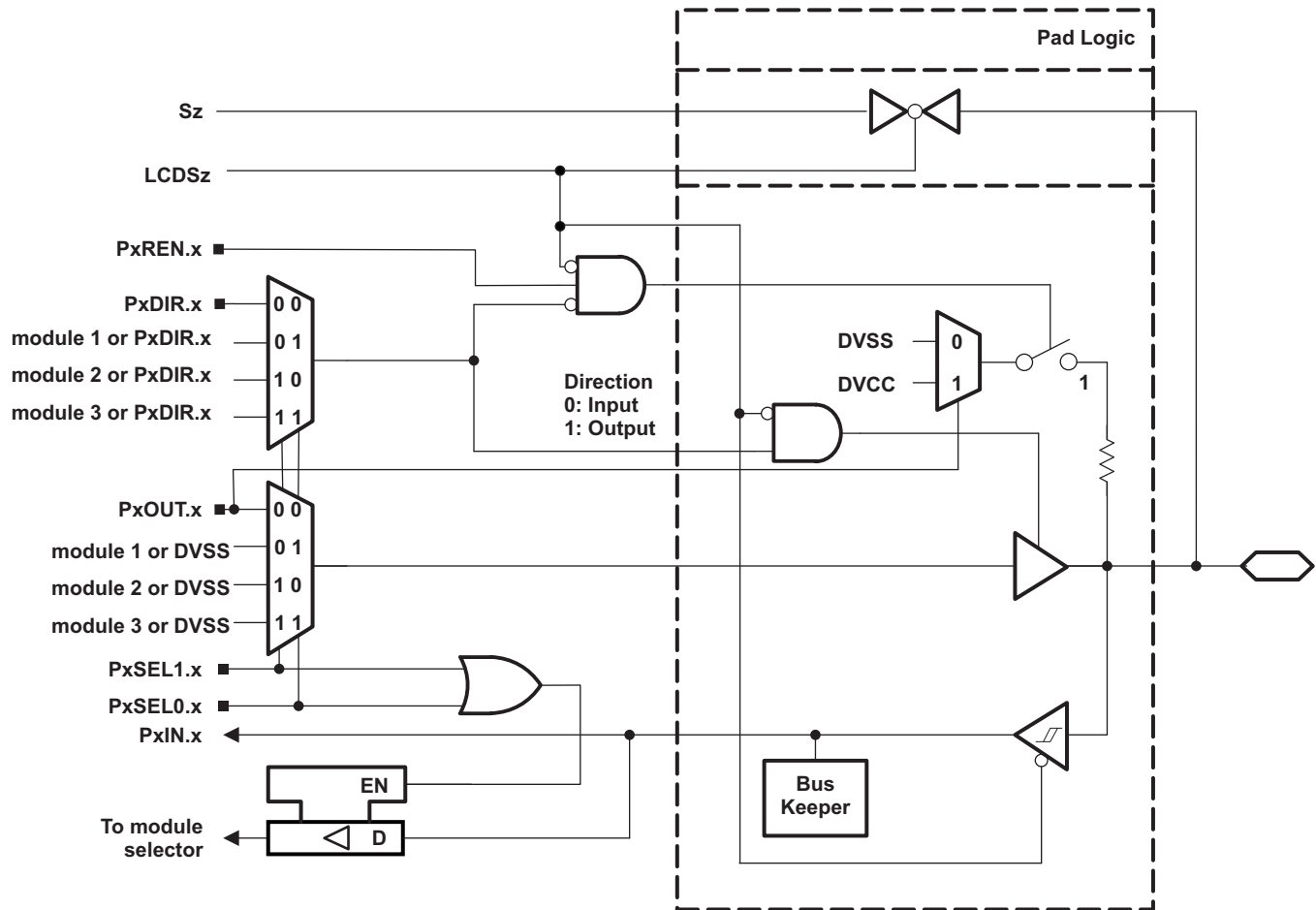
(3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

(5) Direction controlled by eUSCI_B0 module.

6.14.4 Port P1 (P1.6 to P1.7) Input/Output With Schmitt Trigger

图 6-5 shows the port diagram. 表 6-27 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-5. Port P1 (P1.6 to P1.7) Diagram

表 6-27. Port P1 (P1.6 to P1.7) Pin Functions

PIN NAME (P1.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P1DIR.x	P1SEL1. x	P1SEL0. x	LCDSz
P1.6/UCA3STE/UCB0SIMO/ UCB0SDA/LCDS17	29	23	P1.6(I/O)	I: 0; O: 1	0	0	0
			UCA3STE	X ⁽²⁾	0	1	0
			UCB0SIMO/UCB0SDA	X ⁽³⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1
P1.7/USSTRG/UCA3CLK/UC B0SOMI/UCB0SCL/LCDS16	30	24	P1.7(I/O)	I: 0; O: 1	0	0	0
			USSTRG (independent function)	0	X	1	X
					1	X	
			UCA3CLK	X ⁽²⁾	0	1	0
			UCB0SOMI/UCB0SCL	X ⁽³⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1

(1) X = Don't care

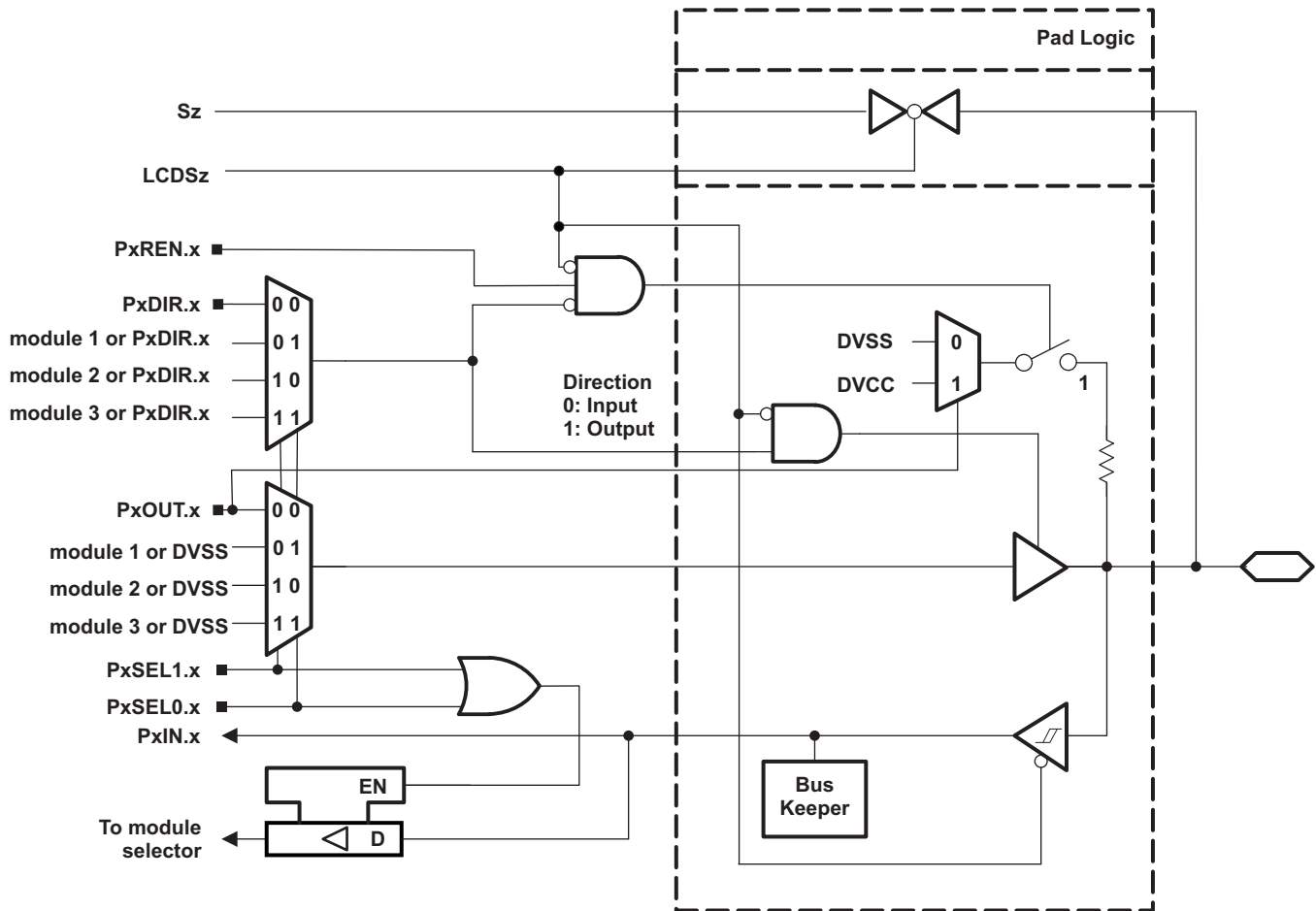
(2) Direction controlled by eUSCI_A3 module.

(3) Direction controlled by eUSCI_B0 module.

(4) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

6.14.5 Port P2 (P2.0 to P2.1) Input/Output With Schmitt Trigger

图 6-6 shows the port diagram. 表 6-28 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-6. Port P2 (P2.0 to P2.1) Diagram

表 6-28. Port P2 (P2.0 to P2.1) Pin Functions

PIN NAME (P2.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P2DIR.x	P2SEL1. x	P2SEL0. x	LCDSz
P2.0/UCA1CLK/UCA3SIMO/ UCA3TXD/LCDS19	27	21	P2.0(I/O)	I: 0; O: 1	0	0	0
			UCA1CLK	X ⁽²⁾	0	1	0
			UCA3SIMO/UCA3TXD	X ⁽³⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1
P2.1/UCA1STE/UCA3SOMI/ UCA3RXD/LCDS18	30	24	P2.1(I/O)	I: 0; O: 1	0	0	0
			UCA1STE	X ⁽²⁾	0	1	0
			UCA3SOMI/UCA3RXD	X ⁽³⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1

(1) X = Don't care

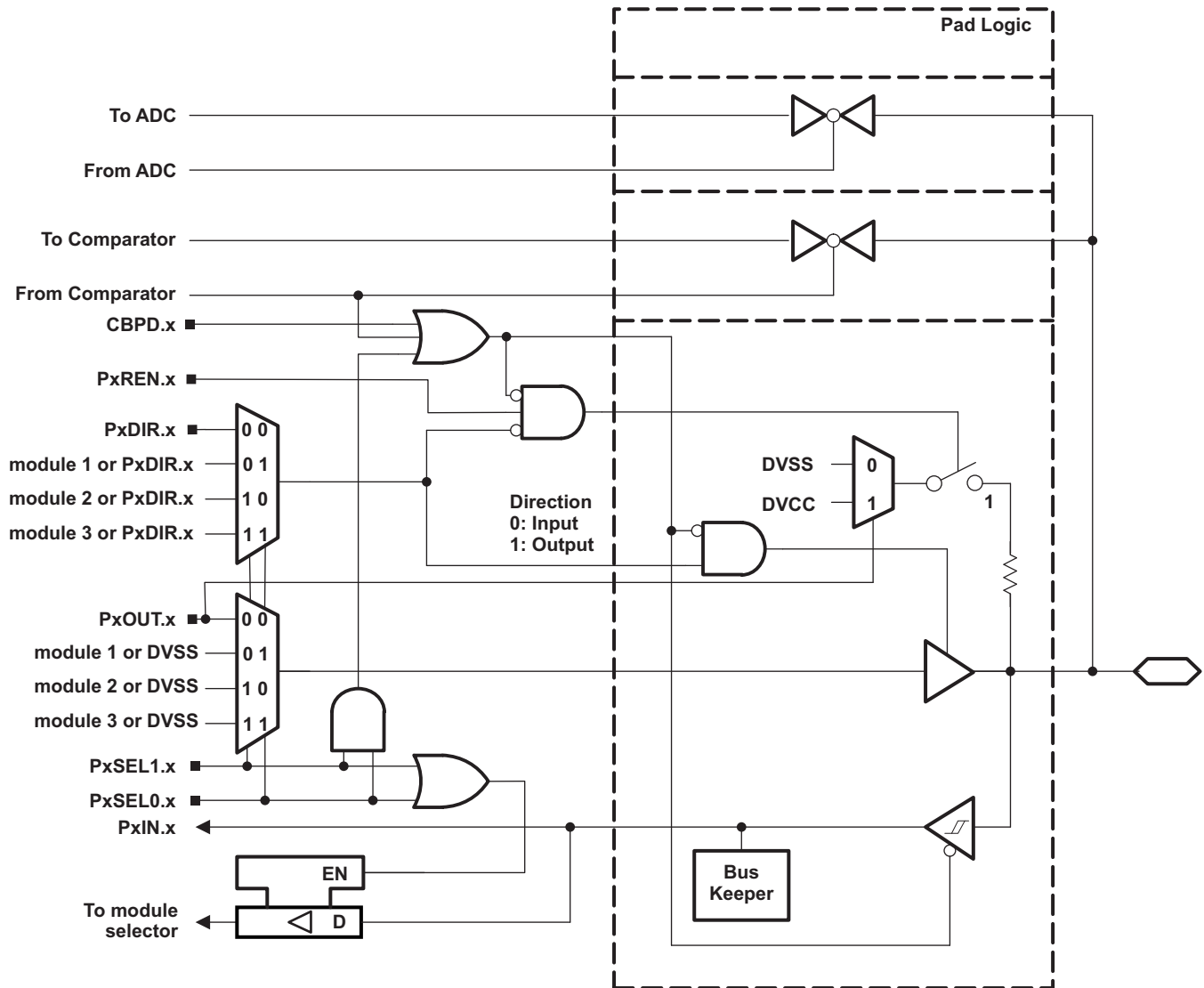
(2) Direction controlled by eUSCI_A1 module.

(3) Direction controlled by eUSCI_A3 module.

(4) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

6.14.6 Port P2 (P2.2 to P2.3) Input/Output With Schmitt Trigger

图 6-7 shows the port diagram. 表 6-29 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-7. Port P2 (P2.2 to P2.3) Diagram

表 6-29. Port P2 (P2.2 to P2.3) Pin Functions

PIN NAME (P2.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾		
				P2DIR.x	P2SEL1.x	P2SEL0.x
P2.2/COUT/UCA0CLK/A14/C14	2	2	P2.2 (I/O)	I: 0; O: 1	0	0
			N/A	0	0	1
			COUT	1		
			UCA0CLK	X ⁽²⁾	1	0
			A14, C14 ⁽³⁾⁽⁴⁾	X	1	1
P2.3/TA0.0/UCA0STE/A15/C15	3	--	P2.3(I/O)	I: 0; O: 1	0	0
			TA0.CCI0A	0	0	1
			TA0.0	1		
			UCA0STE	X ⁽²⁾	1	0
			A15, C15 ⁽³⁾⁽⁴⁾	X	1	1

(1) X = Don't care

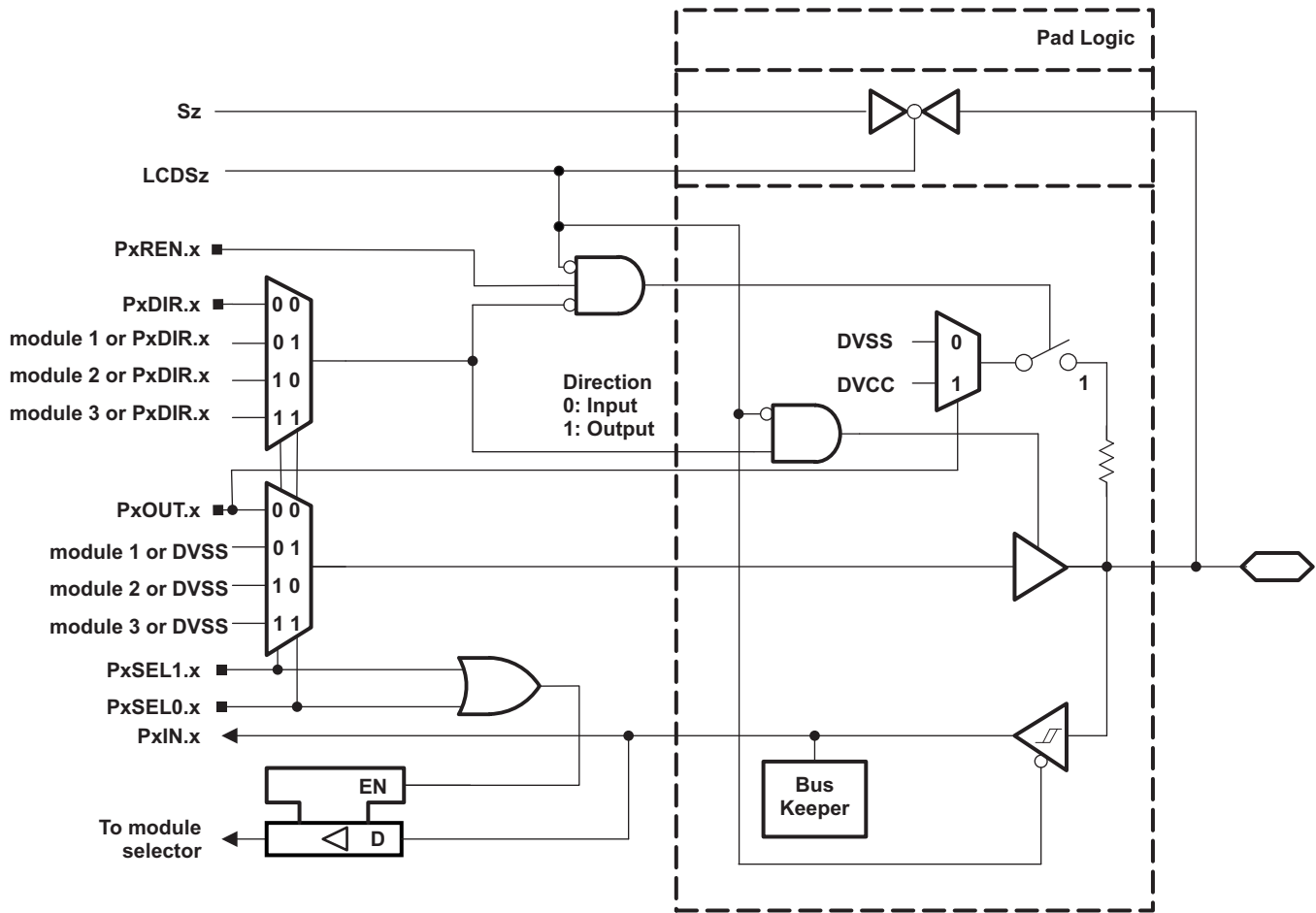
(2) Direction controlled by eUSCI_A0 module.

(3) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

6.14.7 Port P2 (P2.4 to P2.5) Input/Output With Schmitt Trigger

图 6-8 shows the port diagram. 表 6-30 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-8. Port P2 (P2.4 to P2.5) Diagram

表 6-30. Port P2 (P2.4 to P2.5) Pin Functions

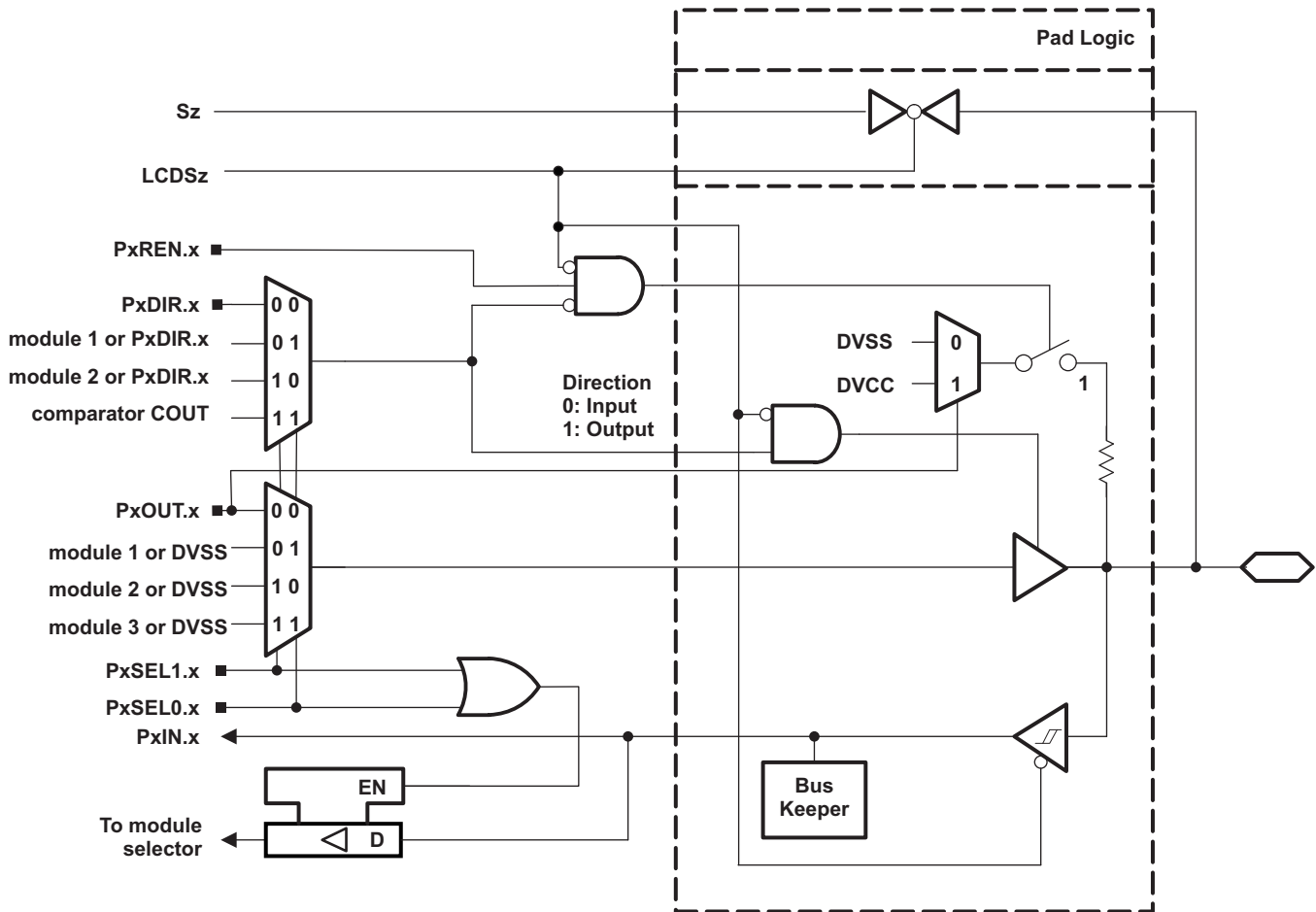
PIN NAME (P2.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P2DIR.x	P2SEL1. x	P2SEL0. x	LCDSz
P2.4/TA0CLK/TB0CLK/TA1CLK/LCDS24	12	--	P2.4 (I/O)	I: 0; O: 1	0	0	0
			TA0CLK	0	0	1	0
			Internally tied to DVSS	1			
			TB0CLK	0	1	0	0
			Internally tied to DVSS	1			
			TA1CLK	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽²⁾	X	X	X	1
P2.5/TA0.2/TA4.0/LCDS21	23	--	P2.5 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			TA0.2	1			
			TA4.CCI0B	0	1	0	0
			TA4.0	1			
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽²⁾	X	X	X	1

(1) X = Don't care

(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

6.14.8 Port P2 (P2.6 to P2.7) Input/Output With Schmitt Trigger

图 6-9 shows the port diagram. 表 6-31 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-9. Port P2 (P2.6 to P2.7) Diagram

表 6-31. Port P2 (P2.6 to P2.7) Pin Functions

PIN NAME (P2.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P2DIR.x	P2SEL1. x	P2SEL0. x	LCDSz
P2.6/UCA0SIMO/UCA0TXD/ TA1.2/TA1.2C/LCDS23	13	--	P2.6 (I/O)	I: 0; O: 1	0	0	0
			UCA0SIMO/UCA0TXD	X ⁽²⁾	0	1	0
			TA1.CCI2A	0	1	0	0
			TA1.2	1			
			TA1.2C	X ⁽³⁾	1	1	0
			Sz ⁽⁴⁾	X	X	X	1
P2.7/UCA0SOMI/UCA0RXD/ TA4.1/TA4.1C/LCDS22	14	--	P2.7 (I/O)	I: 0; O: 1	0	0	0
			UCA0SOMI/UCA0RXD	X ⁽²⁾	0	1	0
			TA4.CCI1B	0	1	0	0
			TA4.1	1			
			TA4.1C	X ⁽³⁾	1	1	0
			Sz ⁽⁴⁾	X	X	X	1

(1) X = Don't care

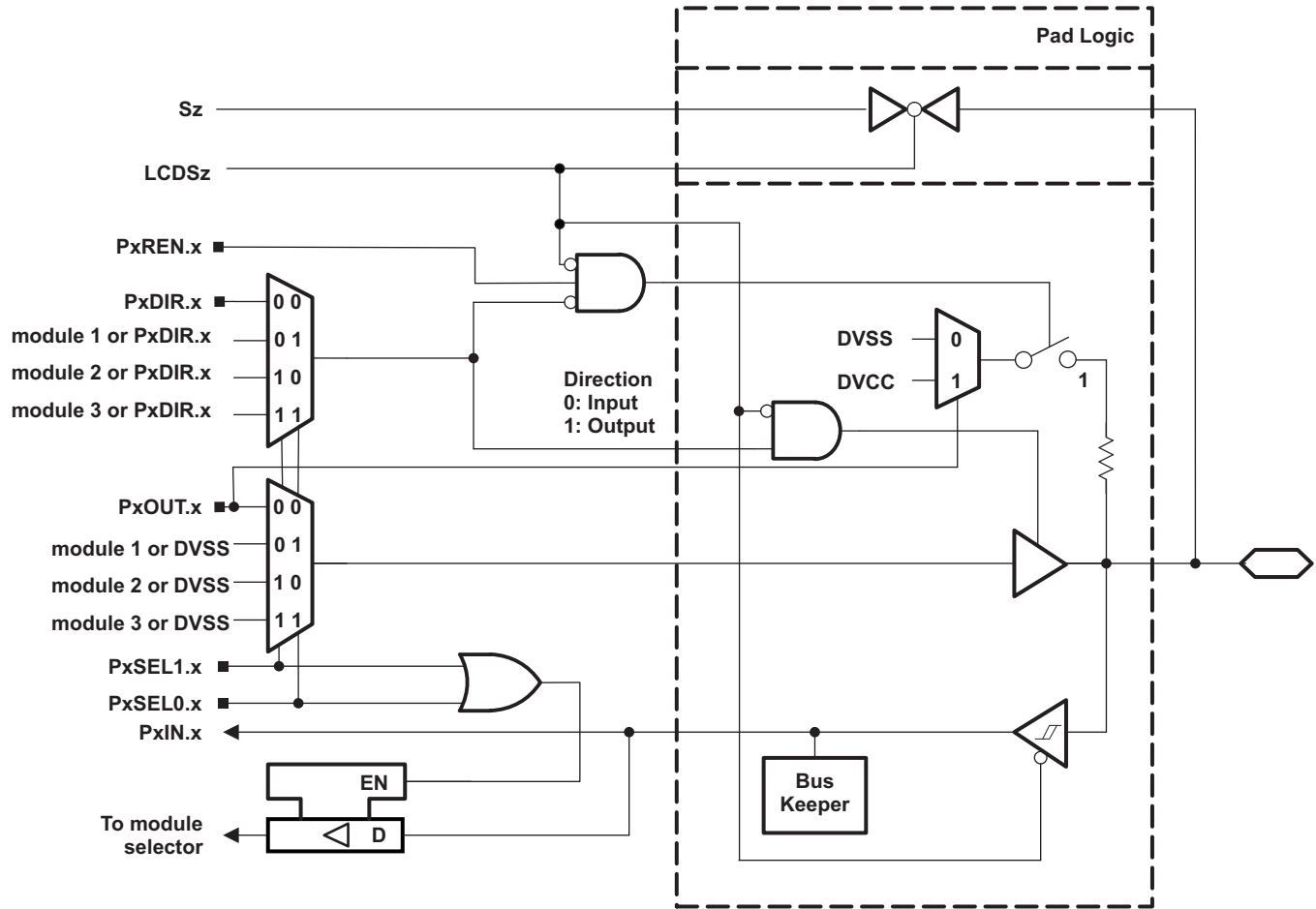
(2) Direction controlled by eUSCI_A0 module.

(3) Direction / HiZ controlled by comparator output COUT.

(4) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

6.14.9 Port P3 (P3.0) Input/Output With Schmitt Trigger

图 6-10 shows the port diagram. 表 6-32 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-10. Port P3 (P3.0) Diagram

表 6-32. Port P3 (P3.0) Pin Functions

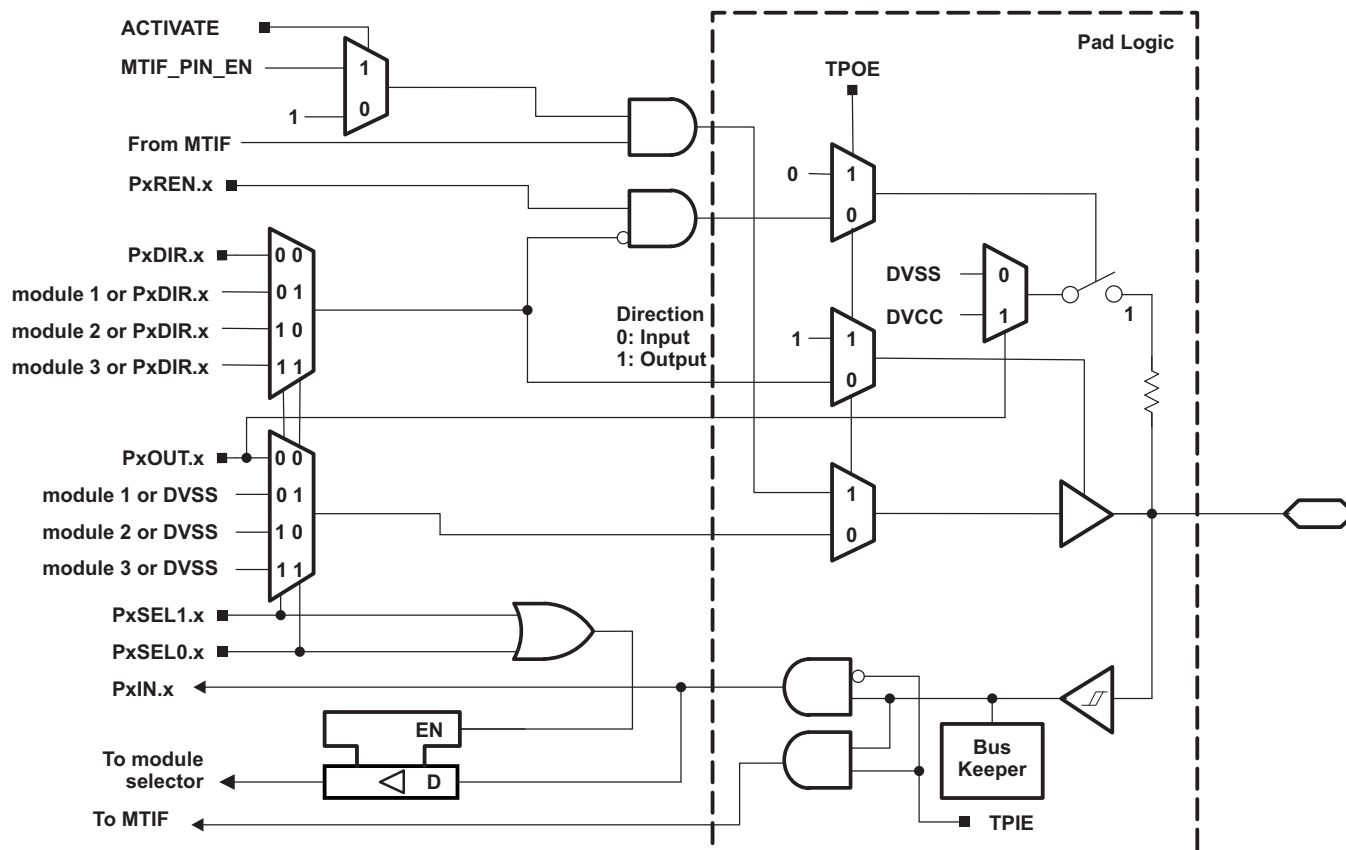
PIN NAME (P3.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P3DIR.x	P3SEL1. x	P3SEL0. x	LCDSz
P3.0/TB0.0/LCDS20	24	--	P3.0 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			Internally tied to DVSS	1	1	0	0
			TB0.CCI0A	0	1	0	0
			TB0.0	1	1	1	0
			N/A	0	1	1	0
			Internally tied to DVSS	1	1	1	0
			Sz ⁽²⁾	X	X	X	1

(1) X = Don't care

(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

6.14.10 Port P3 (P3.1) Input/Output With Schmitt Trigger

图 6-11 shows the port diagram. 表 6-33 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-11. Port P3 (P3.1) Diagram

表 6-33. Port P3 (P3.1) Pin Functions

PIN NAME (P3.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾						
				P3DIR.x	P3SEL1.x	P3SEL0.x	TPOE ⁽²⁾	TPIE ⁽²⁾	ACTIVATE ⁽²⁾	Signal on MTIF_PIN_EN pin ⁽³⁾
P3.1/TA1CLK/TB0.1/MTIF_OUT_IN	33	27	P3.1(I/O)	I: 0; O: 1	0	0	0	0	X	X
			TA1CLK	0	0	1	0	0	X	X
			Internally tied to DVSS	1						
			TB0.CCI1A	0	1	0	0	0	X	X
			TB0.1	1						
			N/A	0	1	1	0	0	X	X
			Internally tied to DVSS	1						
			MTIF_IN	X	X	X	0	1	X	X
			MTIF_OUT ⁽²⁾	X	X	X	1	X	0	X
			Internally tied to DVSS ⁽²⁾	X	X	X	1	X	1	0
			MTIF_OUT ⁽²⁾	X	X	X	1	X	1	1

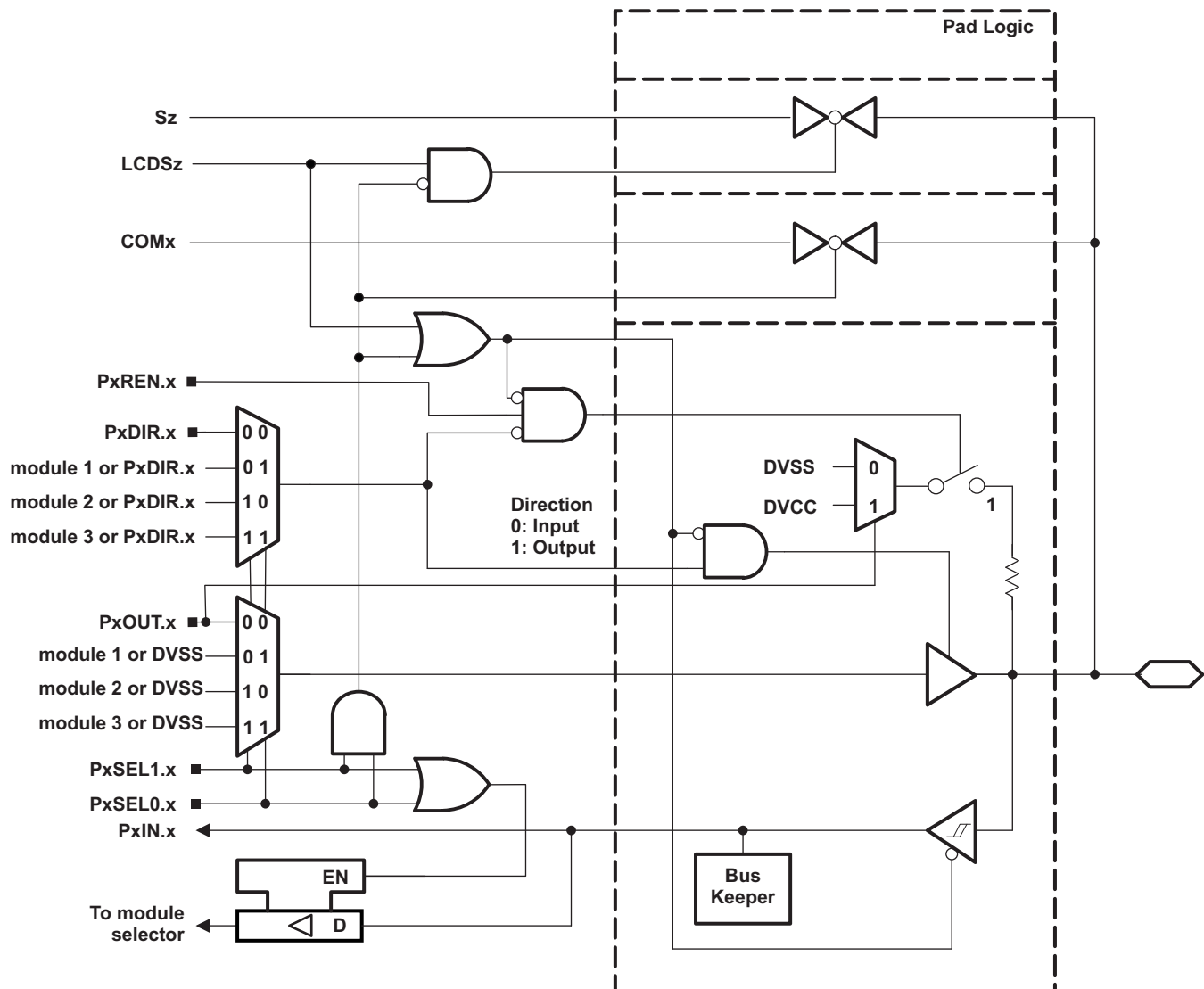
(1) X = Don't care

(2) See MTIF.TPCTL register

(3) When P3.1 pin is configured as MTIF_PIN_EN (See for details)

6.14.11 Port P3 (P3.2) Input/Output With Schmitt Trigger

图 6-12 shows the port diagram. 表 6-34 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-12. Port P3 (P3.2) Diagram

表 6-34. Port P3 (P3.2) Pin Functions

PIN NAME (P3.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P3DIR.x	P3SEL1. x	P3SEL0. x	LCDSz
P3.2/TA1.1/COM5/LCDS28	63	--	P3.2 (I/O)	I: 0; O: 1	0	0	0
			TA1.CCI1A	0	0	1	0
			TA1.1	1			
			DMAE0	0	1	0	0
			Internally tied to DVSS	1			
			COM5 ⁽²⁾		1	1	X
			Sz ⁽³⁾	X	X	0	1
					0	X	

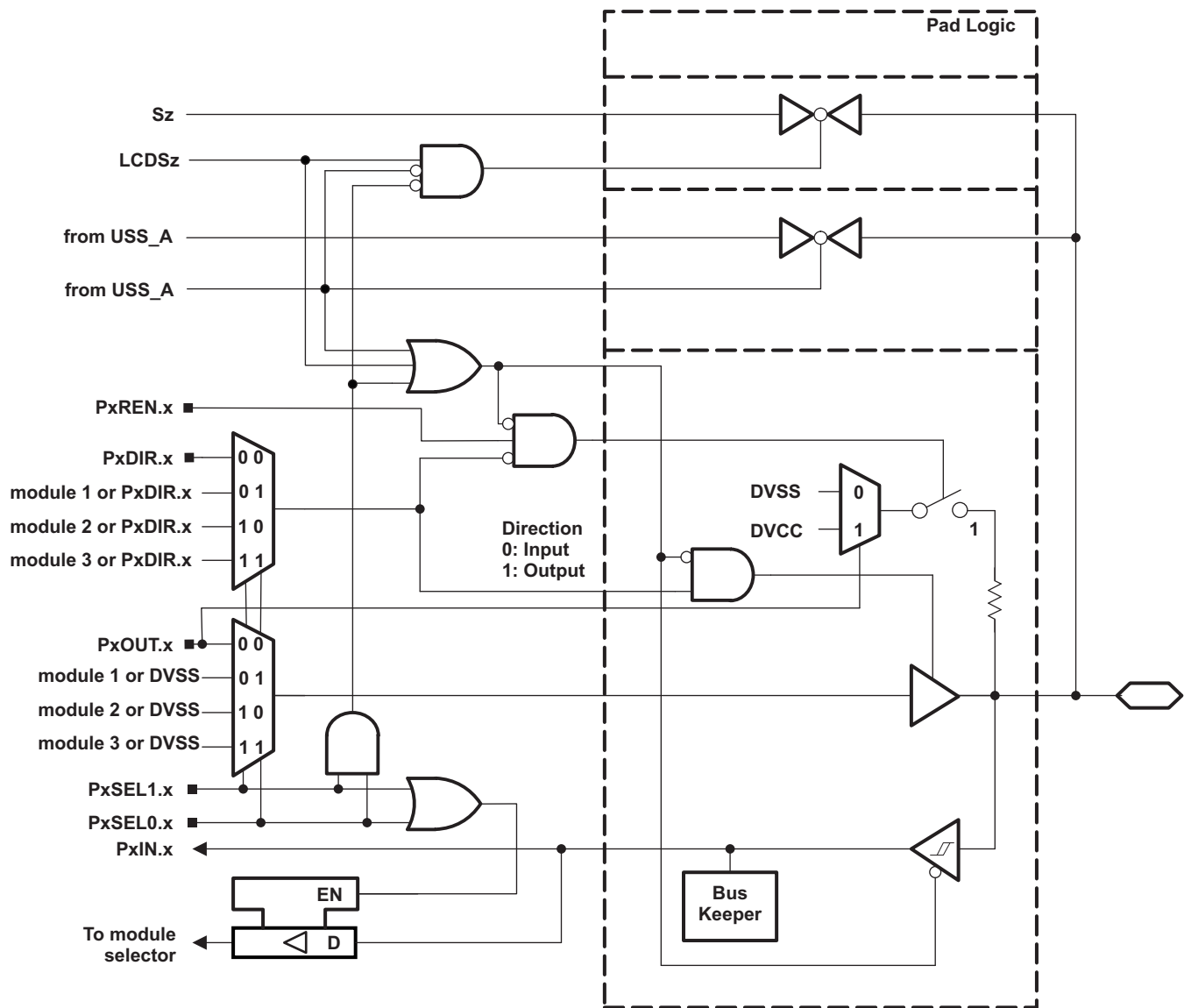
(1) X = Don't care

(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in [节 4](#).

6.14.12 Port P3 (P3.3) Input/Output With Schmitt Trigger

图 6-13 shows the port diagram. 表 6-35 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-13. Port P3 (P3.3) Diagram

表 6-35. Port P3 (P3.3) Pin Functions

PIN NAME (P3.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P3DIR.x	P3SEL1. x	P3SEL0. x	LCDSz
P3.3/MCLK/TB0.3/XPB1/LCD S25	64	50	P3.4 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			MCLK	1			
			TB0.CCI3B	0	1	0	0
			TB0.3	1			
			XPB1	X ⁽²⁾	X	X	X
			Sz ⁽³⁾	X	X	0	1
					0	X	

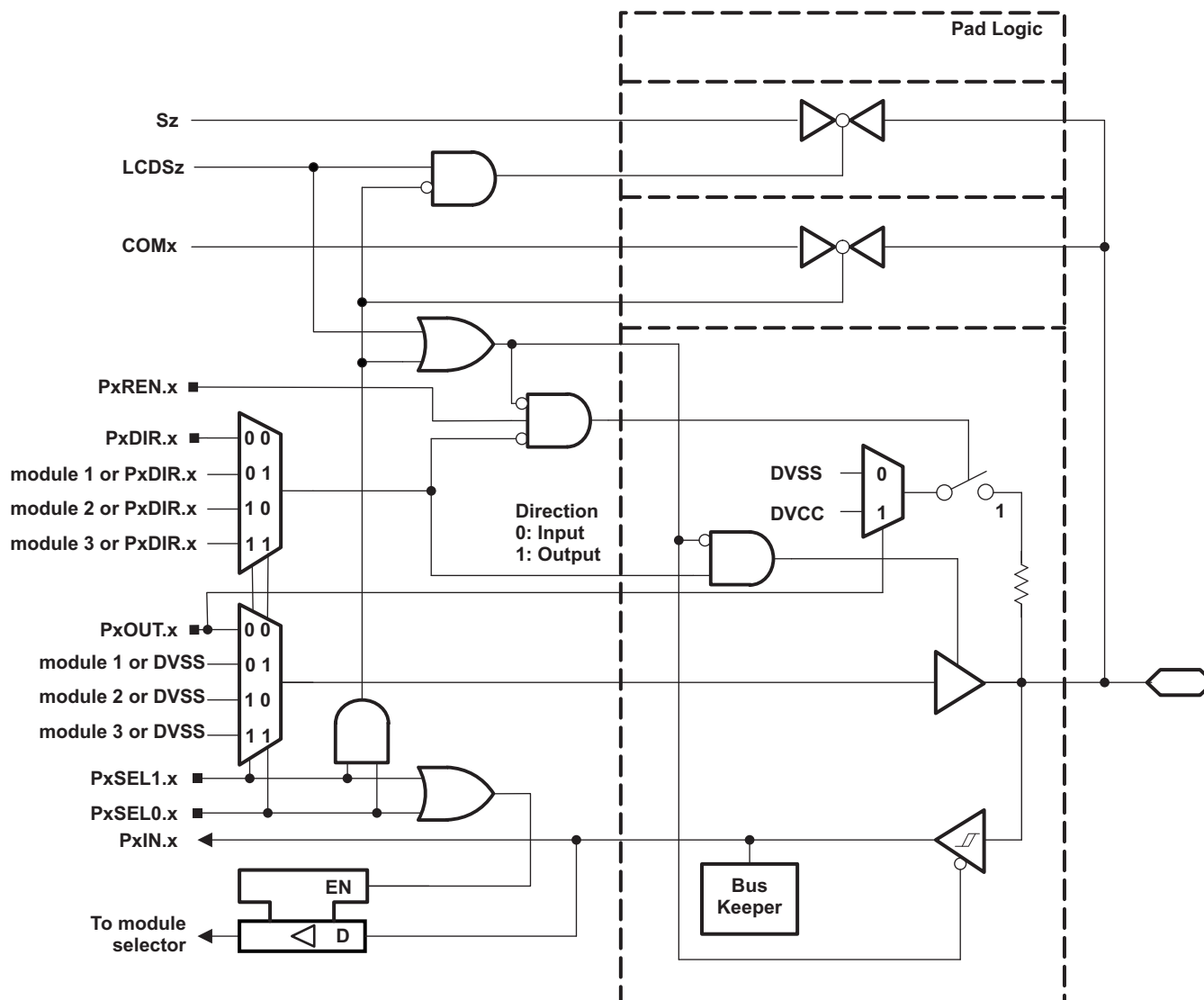
(1) X = Don't care

(2) XPB1 enable disables digital and LCD functions on this pin implicitly

(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in [节 4](#).

6.14.13 Port P3 (P3.4 to P3.5) Input/Output With Schmitt Trigger

图 6-14 shows the port diagram. 表 6-36 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-14. Port P3 (P3.4 to P3.5) Diagram

表 6-36. Port P3 (P3.4 to P3.5) Pin Functions

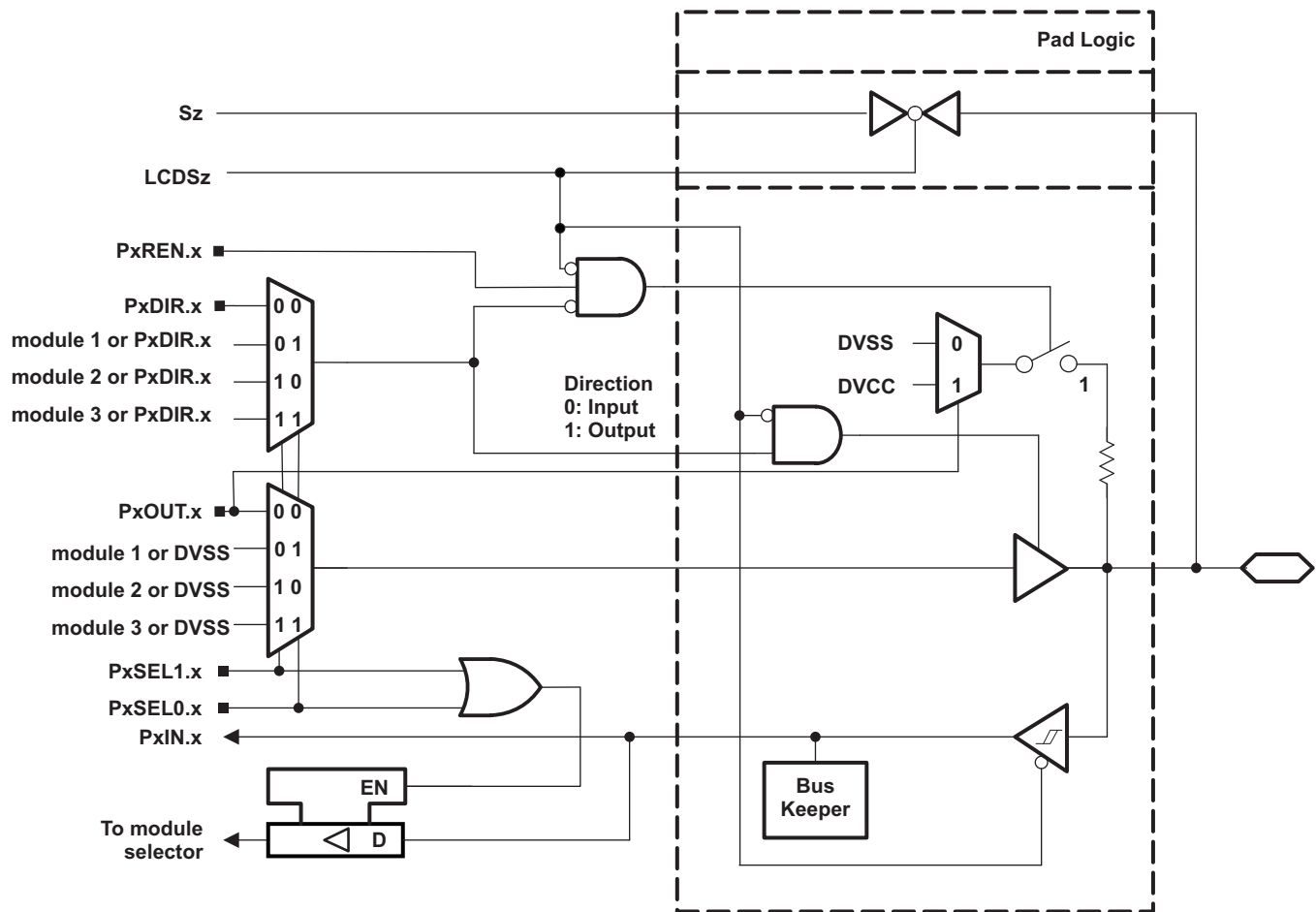
PIN NAME (P3.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P3DIR.x	P3SEL1. x	P3SEL0. x	LCDSz
P3.4/SMCLK/DMAE0/COM6/LCDS27	65	51	P3.4 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			SMCLK	1			
			DMAE0	0	1	0	0
			Internally tied to DVSS	1			
			COM6		1	1	X
			Sz	X	X 0	0 X	1
P3.5/ACLK/COU/COM3/LCDS26	66	52	P3.5 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			ACLK	1			
			N/A	0	1	0	0
			COU	1			
			COM3	X	1	1	X
			Sz ⁽²⁾	X	X 0	0 X	1

(1) X = Don't care

(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in [节 4](#).

6.14.14 Port P3 (P3.6 to P3.7) Input/Output With Schmitt Trigger

图 6-15 shows the port diagram. 表 6-37 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-15. Port P3 (P3.6 to P3.7) Diagram

表 6-37. Port P3 (P3.6 to P3.7) Pin Functions

PIN NAME (P3.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P3DIR.x	P3SEL1. x	P3SEL0. x	LCDSz
P3.6/UCB1SIMO/UCB1SDA/ TB0.6/USSXT_BOUT/LCDS35	75	--	P3.6 (I/O)	I: 0; O: 1	0	0	0
			UCB1SIMO/UCB1SDA	X ⁽²⁾	0	1	0
			TB0.CCI6B	0	1	0	0
			TB0.6	1			
			N/A	0	1	1	0
			USSXT_BOUT	1			
			Sz ⁽³⁾	X	X	X	1
P3.7/UCB1SOMI/UCB1SCL/ TB0.2/TB0OUTH/LCDS36	76	--	P3.7 (I/O)	I: 0; O: 1	0	0	0
			UCB1SOMI/UCB1SCL	X ⁽²⁾	0	1	0
			TB0.CCI2A	0	1	0	0
			TB0.2	1			
			TB0OUTH	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽³⁾	X	X	X	1

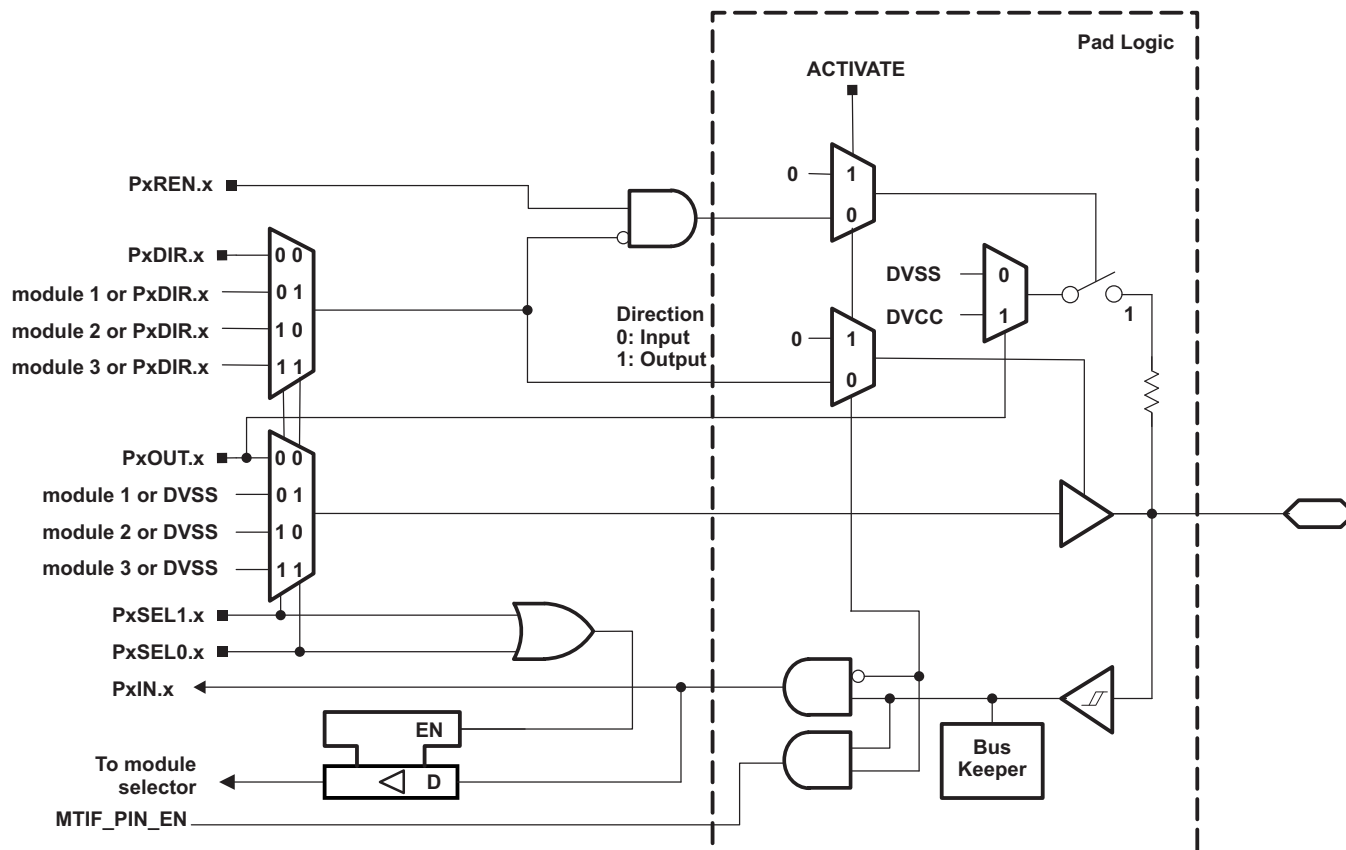
(1) X = Don't care

(2) Direction controlled by eUSCI_B1 module.

(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

6.14.15 Port P4 (P4.0) Input/Output With Schmitt Trigger

图 6-16 shows the port diagram. 表 6-38 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-16. Port P4 (P4.0) Diagram

表 6-38. Port P4 (P4.0) Pin Functions

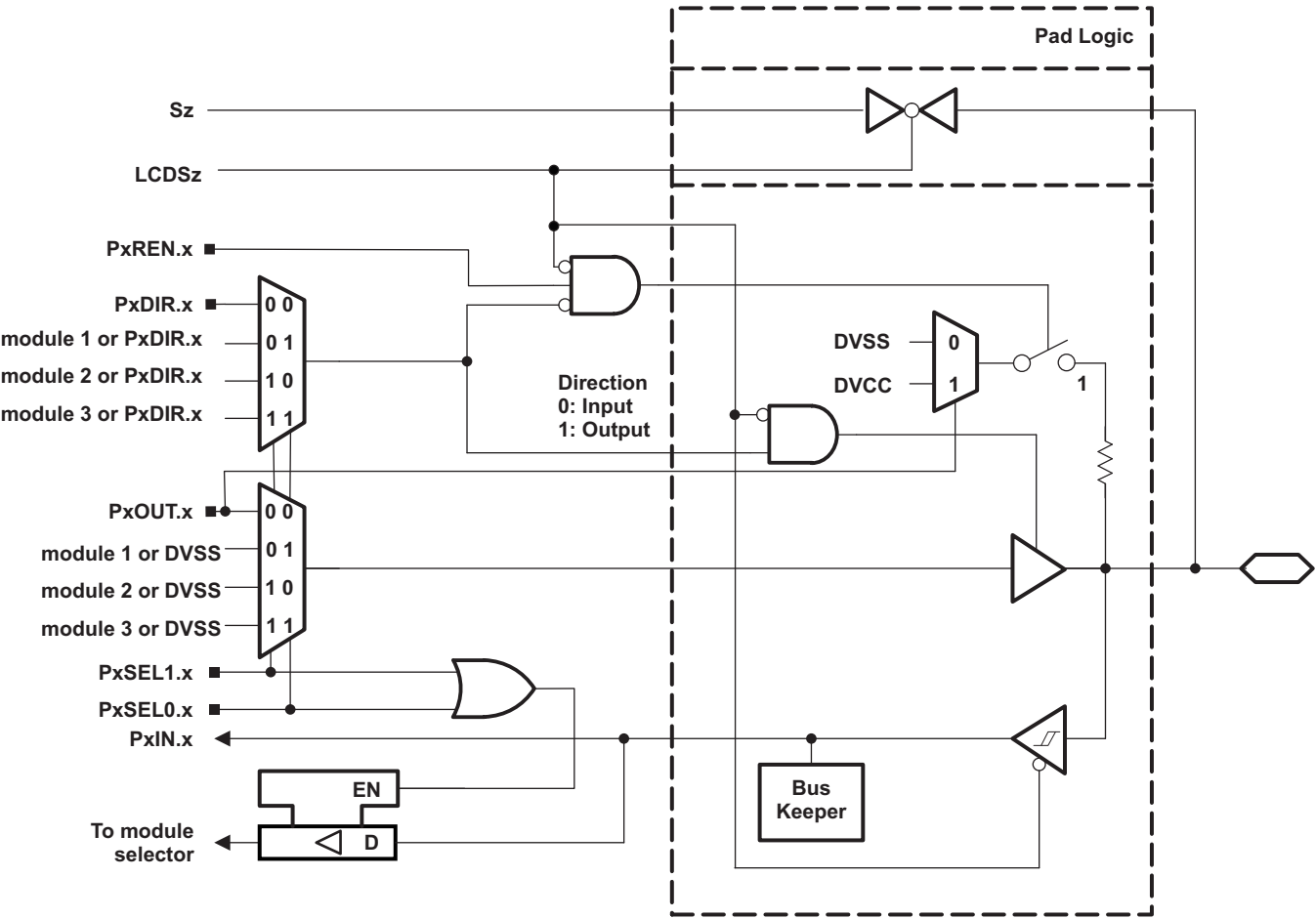
PIN NAME (P4.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P4DIR.x	P4SEL 1.x	P4SEL0. x	ACTIVATE ⁽²⁾
P4.0/RTCCLK/TA4.1/M TIF_PIN_EN	34	28	P4.0(I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			Internally tied to DVSS	1			
			N/A	0	1	0	0
			RTCCLK	1			
			N/A	0	1	1	0
			TA4.1	1			
			MTIF_PIN_EN	X	X	X	1

(1) X = Don't care

(2) See MTIF.TPCTL register

6.14.16 Port P4 (P4.1 to P4.7) Input/Output With Schmitt Trigger

图 6-17 shows the port diagram. 表 6-39 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-17. Port P4 (P4.1 to P4.7) Diagram

表 6-39. Port P4 (P4.1 to P4.7) Pin Functions

PIN NAME (P4.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P4DIR.x	P4SEL1. x	P4SEL0. x	LCDSz
P4.1/UCA0CLK/TB0.4/UCA3 SOMI/UCA3RXD/LCDS15	35	29	P4.1 (I/O)	I: 0; O: 1	0	0	0
			UCA0CLK	X ⁽²⁾	0	1	0
			TB0.CCI4B	0	1	0	0
			TB0.4	1			
			UCA3SOMI/UCA3RXD	X ⁽³⁾	1	1	0
			Sz ⁽⁴⁾	X	X	X	1

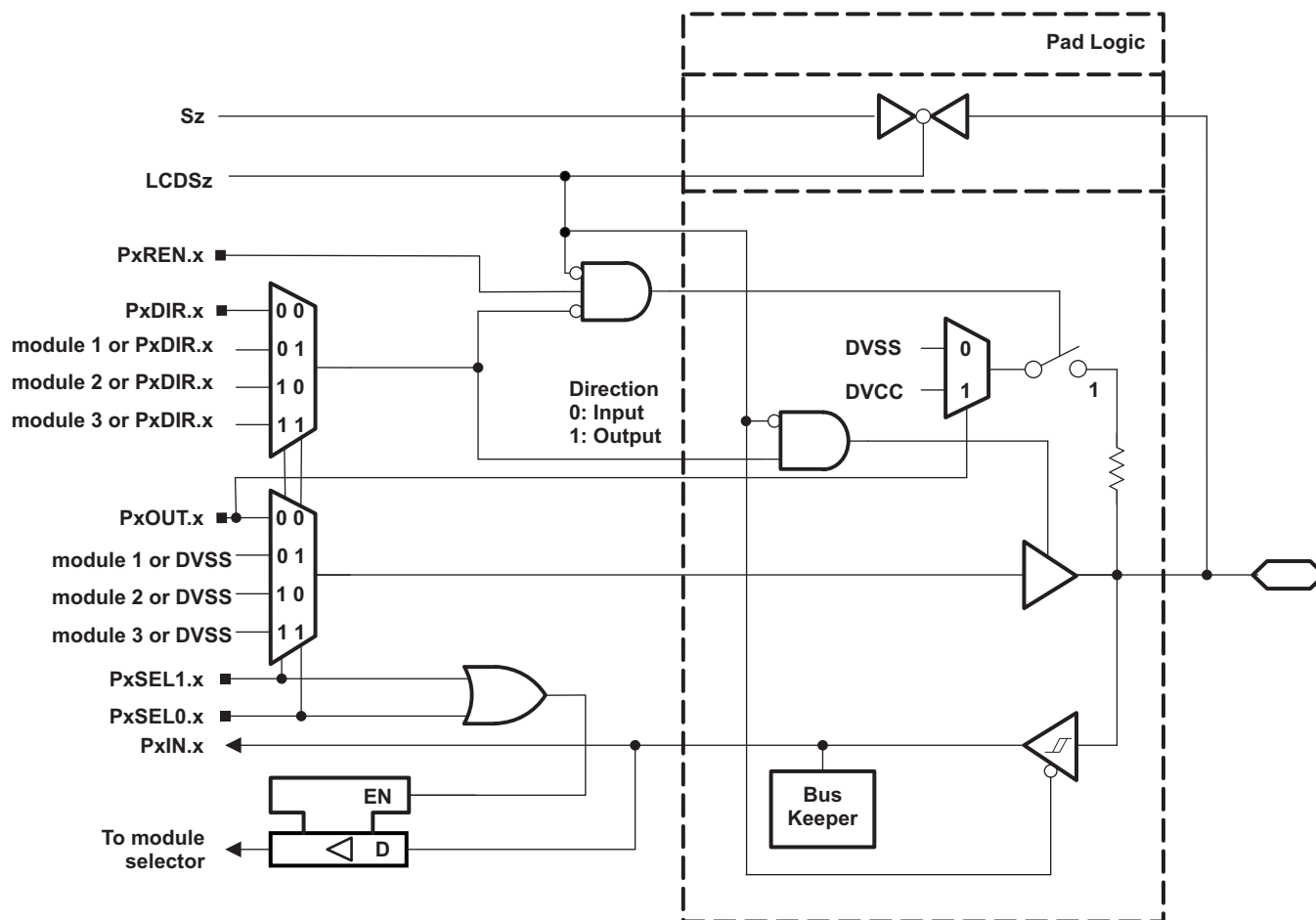
(1) X = Don't care
(2) Direction controlled by eUSCI_A0 module.
(3) Direction controlled by eUSCI_A3 module.
(4) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

表 6-39. Port P4 (P4.1 to P4.7) Pin Functions (continued)

PIN NAME (P4.x)	P N 80	P M R G C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P4DIR.x	P4SEL1. x	P4SEL0. x	LCDSz
P4.2/UCA0STE/TB0.5/UCA3 SIMO/UCA3TXD/LCDS14	36	30	P4.2 (I/O)	I: 0; O: 1	0	0	0
			UCA0STE	X ⁽²⁾	0	1	0
			TB0.CCI5B	0	1	0	0
			TB0.5	1			
			UCA3SIMO/UCA3TXD	X ⁽³⁾	1	1	0
			Sz ⁽⁴⁾	X	X	X	1
P4.3/UCA0SIMO/UCA0TXD/ LCDS13	37	31	P4.3 (I/O)	I: 0; O: 1	0	0	0
			UCA0SIMO/UCA0TXD	X ⁽²⁾	0	1	0
			N/A	0	1	0	0
			Internally tied to DVSS	1			
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1
P4.4/UCA0SOMI/UCA0RXD/ LCDS12	38	32	P4.4 (I/O)	I: 0; O: 1	0	0	0
			UCA0SOMI/UCA0RXD	X ⁽²⁾	0	1	0
			N/A	0	1	0	0
			Internally tied to DVSS	1			
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1
P4.5/TA0CLK/TA1CLK/LCDS 11	39	--	P4.5 (I/O)	I: 0; O: 1	0	0	0
			TA0CLK	0	0	1	0
			Internally tied to DVSS	1			
			TA1CLK	0	1	0	0
			Internally tied to DVSS	1			
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1
P4.6/TB0CLK/TA4CLK/LCDS 10	40	--	P4.6 (I/O)	I: 0; O: 1	0	0	0
			TB0CLK	0	0	1	0
			Internally tied to DVSS	1			
			TA4CLK	0	1	0	0
			Internally tied to DVSS	1			
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1
P4.7/DMAE0/LCDS9	42	--	P4.7 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			Internally tied to DVSS	1			
			DMAE0	0	1	0	0
			Internally tied to DVSS	1			
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽⁴⁾	X	X	X	1

6.14.17 Port P5 (P5.0 to P5.7) Input/Output With Schmitt Trigger

图 6-18 shows the port diagram. 表 6-40 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-18. Port P5 (P5.0 to P5.7) Diagram

表 6-40. Port P5 (P5.0 to P5.7) Pin Functions

PIN NAME (P5.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P5DIR.x	P5SEL1. x	P5SEL0. x	LCDSz
P5.0/TB0.0/UCA2SIMO/UCA2TXD/LCDS8	43	34	P5.0 (I/O)	I: 0; O: 1	0	0	0
			TB0.CCI0B	0	0	1	0
			TB0.0	1			
			UCA2SIMO/UCA2TXD	X ⁽²⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽³⁾	X	X	X	1
P5.1/TB0.1/UCA2SOMI/UCA2RXD/LCDS7	44	35	P5.1 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			TB0.1	1			
			UCA2SOMI/UCA2RXD	X ⁽²⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽³⁾	X	X	X	1
P5.2/TB0.2/UCA2CLK/LCDS6	45	36	P5.2 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			TB0.2	1			
			UCA2CLK	X ⁽²⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽³⁾	X	X	X	1
P5.3/TB0.3/UCA2STE/LCDS5	46	37	P5.3 (I/O)	I: 0; O: 1	0	0	0
			TB0.CCI3A	0	0	1	0
			TB0.3	1			
			UCA2STE	X ⁽²⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽³⁾	X	X	X	1
P5.4/TA0.0/UCB1CLK/TA4.0/LCDS4	47	38	P5.4 (I/O)	I: 0; O: 1	0	0	0
			TA0.CCI0B	0	0	1	0
			TA0.0	1			
			UCB1CLK	X ⁽⁴⁾	1	0	0
			N/A	0	1	1	0
			TA4.0	1			
			Sz ⁽³⁾	X	X	X	1
P5.5/TA4.1/UCB1SIMO/UCB1SDA/LCDS3	48	39	P5.5 (I/O)	I: 0; O: 1	0	0	0
			TA4.CCI1A	0	0	1	0
			TA4.1	1			
			UCB1SIMO/UCB1SDA	X ⁽⁴⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽³⁾	X	X	X	1

(1) X = Don't care

(2) Direction controlled by eUSCI_A2 module.

(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

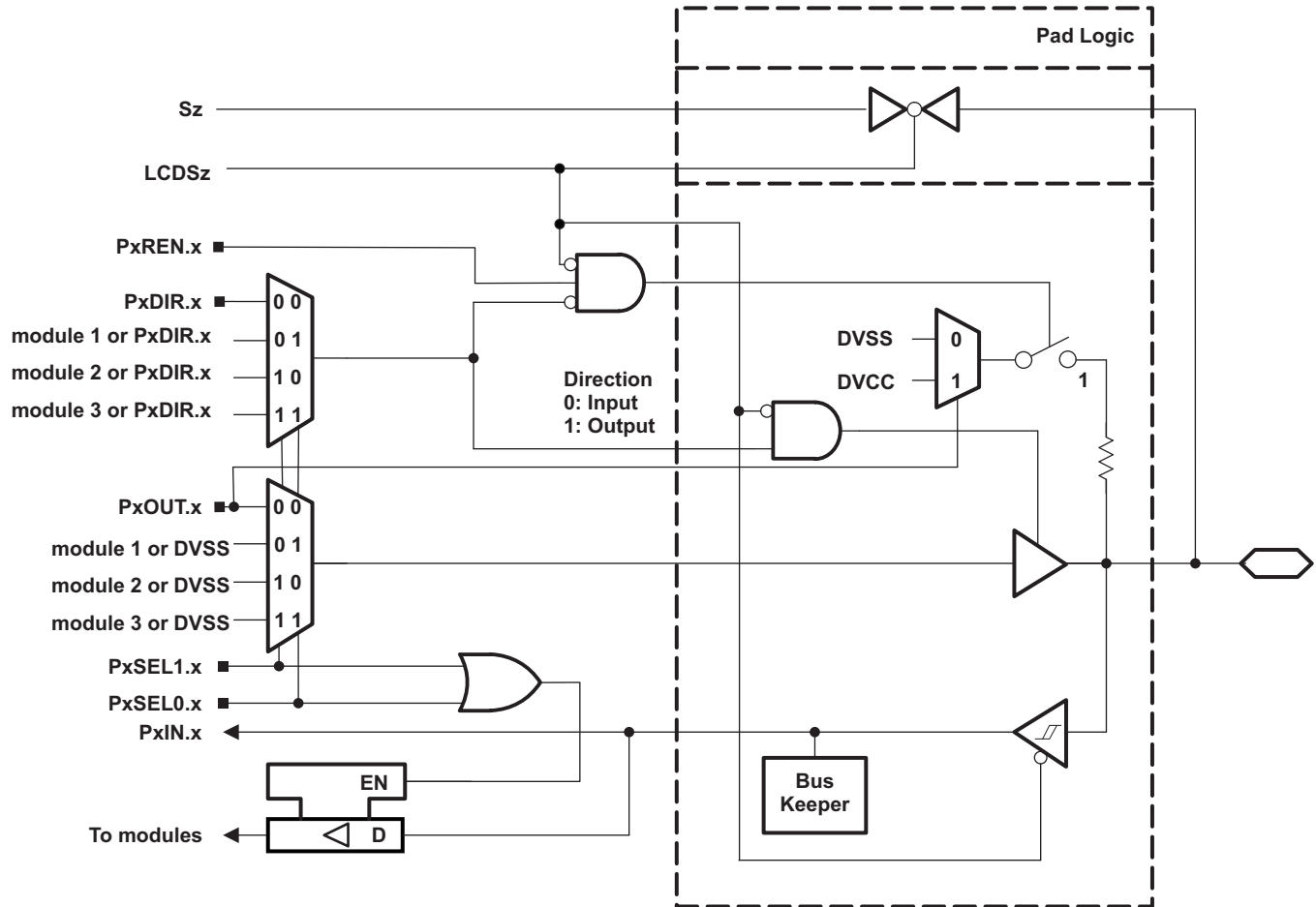
(4) Direction controlled by eUSCI_B1 module.

表 6-40. Port P5 (P5.0 to P5.7) Pin Functions (continued)

PIN NAME (P5.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P5DIR.x	P5SEL1. x	P5SEL0. x	LCDSz
P5.6/TB0OUTH/UCB1SOMI/ UCB1SCL/LCDS2	49	40	P5.6 (I/O)	I: 0; O: 1	0	0	0
			TB0OUTH	0	0	1	0
			Internally tied to DVSS	1			
			UCB1SOMI/UCB1SCL	X ⁽⁴⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽³⁾	X	X	X	1
P5.7/TA0.2/UCB1STE/LCDS 1	42	--	P5.7 (I/O)	I: 0; O: 1	0	0	0
			TA0.CCI2A	0	0	1	0
			TA0.2	1			
			UCB1STE	X ⁽⁴⁾	1	0	0
			N/A	0	1	1	0
			Internally tied to DVSS	1			
			Sz ⁽³⁾	X	X	X	1

6.14.18 Port P6 (P6.0) Input/Output With Schmitt Trigger

图 6-19 shows the port diagram. 表 6-41 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-19. Port P6 (P6.0) Diagram

表 6-41. Port P6 (P6.0) Pin Functions

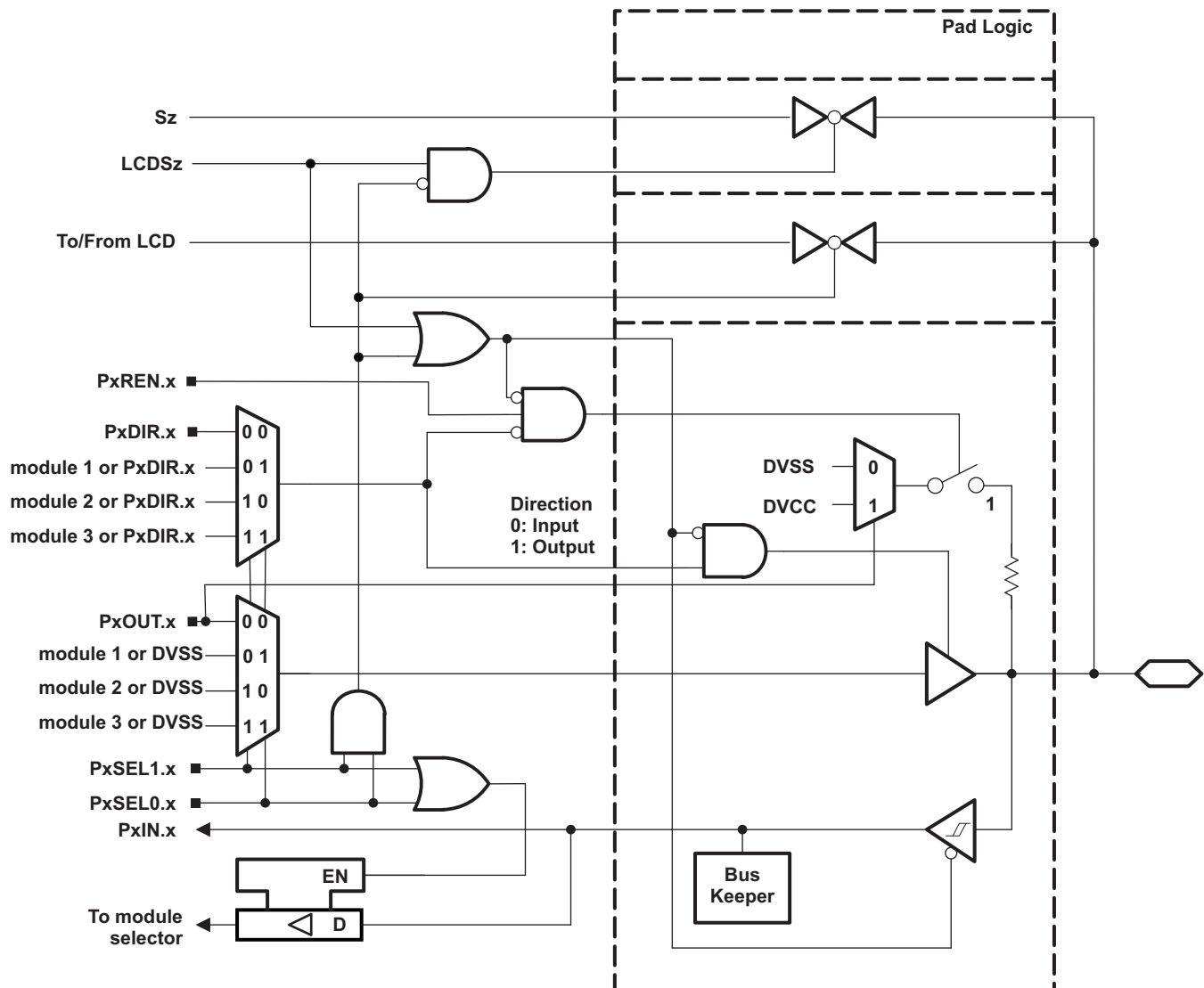
PIN NAME (P6.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P6DIR.x	P6SEL1. x	P6SEL0. x	LCDSz
P6.0/TA0CLK/COUT/LCDS0	51	41	P6.0 (I/O)	I: 0; O: 1	0	0	0
			TA0CLK	0	0	1	0
			Internally tied to DVSS	1	1	0	0
			N/A	0	1	0	0
			COUT	1	1	1	0
			N/A	0	1	1	0
			Internally tied to DVSS	1	1	1	0
			Sz ⁽²⁾	X	X	X	1

(1) X = Don't care

(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

6.14.19 Port P6 (P6.1 to P6.2) Input/Output With Schmitt Trigger

图 6-20 shows the port diagram. 表 6-42 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-20. Port P6 (P6.1 to P6.2) Diagram

表 6-42. Port P6 (P6.1 to P6.2) Pin Functions

PIN NAME (P6.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P6DIR.x	P6SEL1. x	P6SEL0. x	LCDSz
P6.1/RTCCLK/R03/LCDS3 3	56	--	P6.1 (I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			RTCCLK	1			
			N/A	0	1	0	0
			Internally tied to DVSS	1			
			R03 ⁽²⁾	X	1	1	X
			Sz ⁽³⁾	X	X	0	1
P6.2/TB0CLK/R13/LCDRE F/LCDS32	57	47	P6.2 (I/O)	I: 0; O: 1	0	0	0
			TB0CLK	0	0	1	0
			Internally tied to DVSS	1			
			N/A	0	1	0	0
			Internally tied to DVSS	1			
			R13/LCDREF ⁽²⁾	X	1	1	X
			Sz ⁽³⁾	X	X	0	1
					0	X	

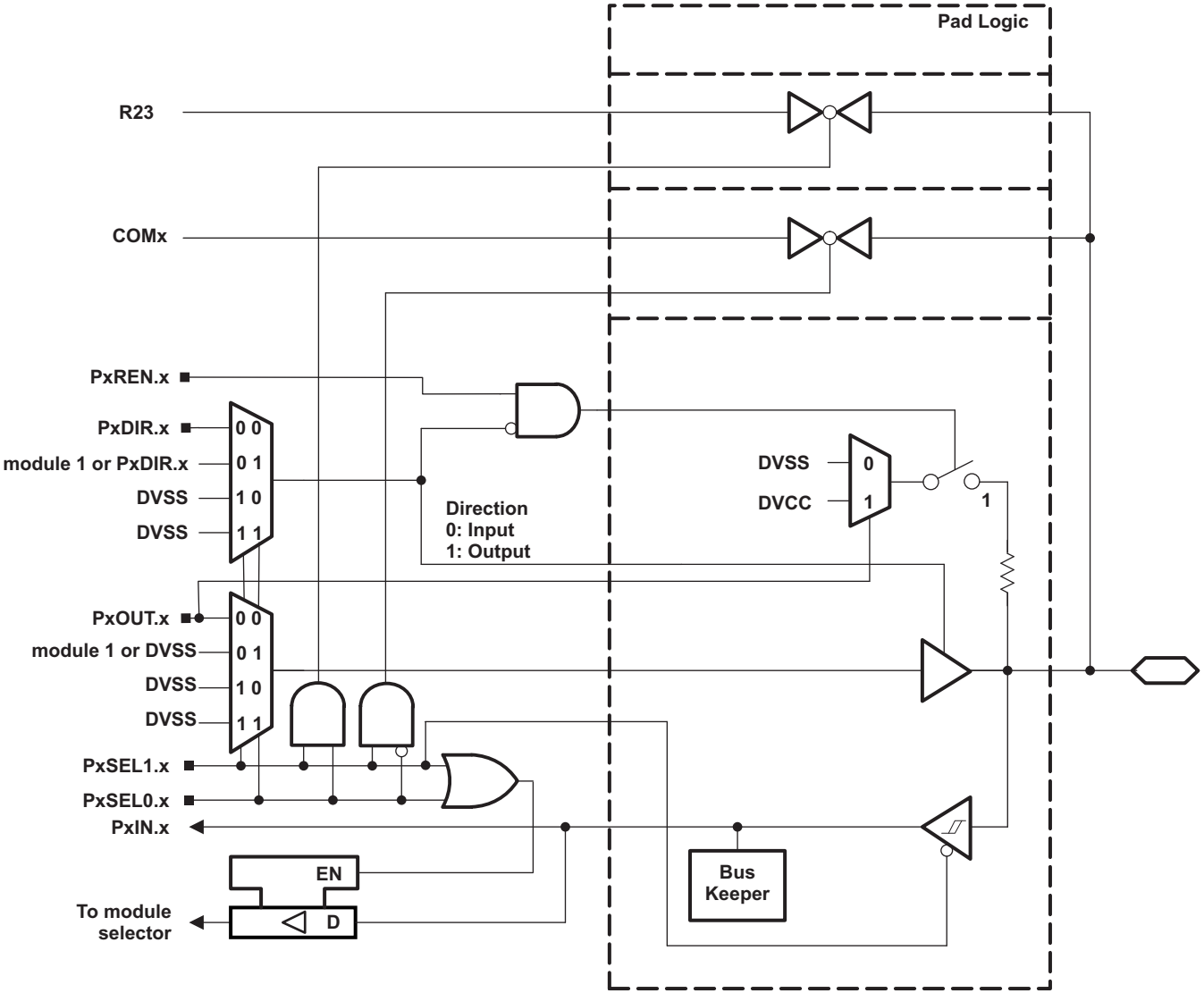
(1) X = Don't care

(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 节 4.

6.14.20 Port P6 (P6.3) Input/Output With Schmitt Trigger

图 6-21 shows the port diagram. 表 6-43 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-21. Port P6 (P6.3) Diagram

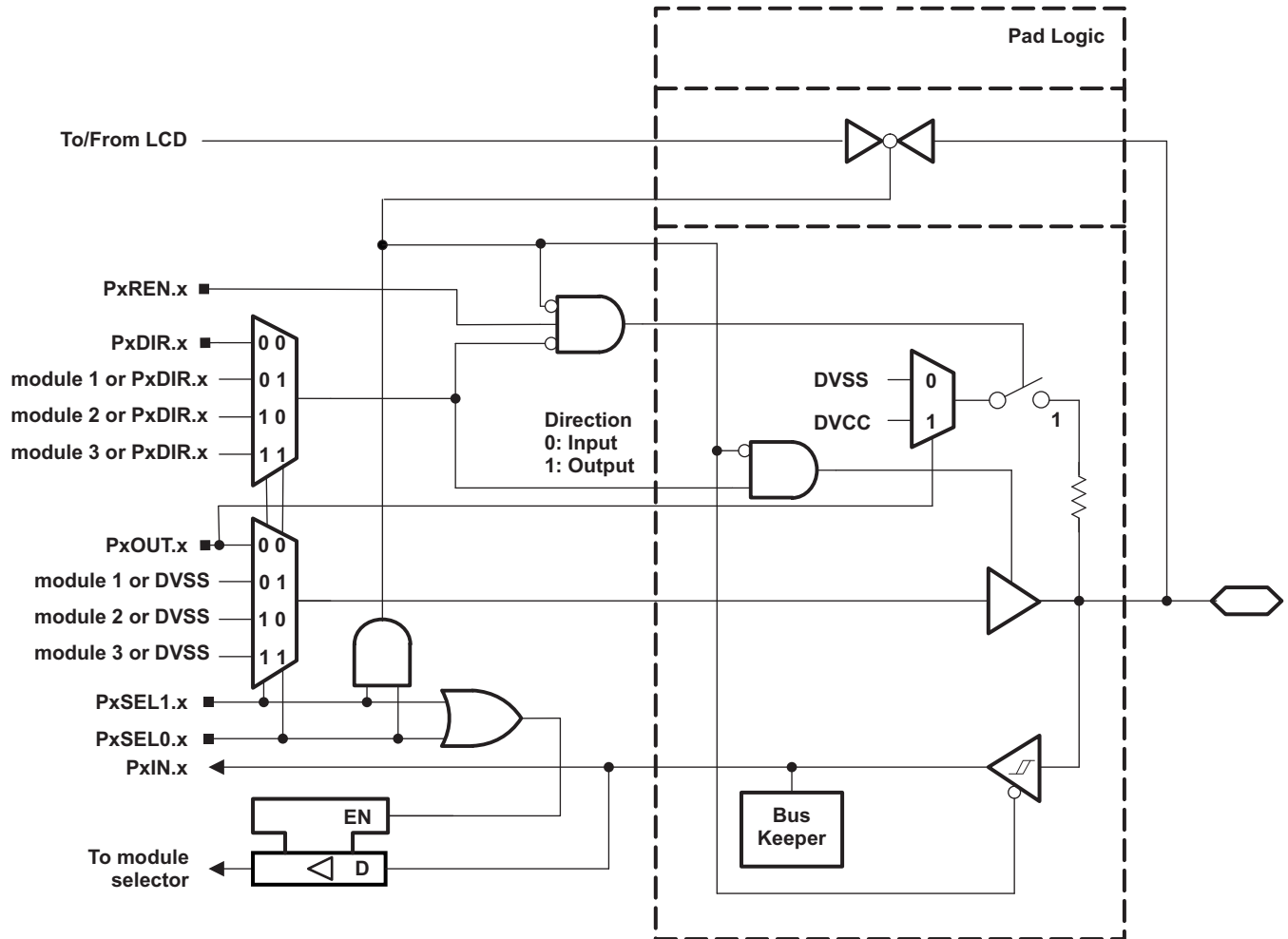
表 6-43. Port P6 (P6.3) Pin Functions

PIN NAME (P6.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
				P6DIR.x	P6SEL1.x	P6SEL0.x
P6.3/COM7/R23	60	--	P6.3 (I/O)	I: 0; O: 1	0	0
			N/A	0	0	1
			Internally tied to DVSS	1		
			COM7 ⁽²⁾	X	1	0
			R23 ⁽²⁾	X	1	1

(1) X = Don't care
(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.14.21 Port P6 (P6.4) Input/Output With Schmitt Trigger

图 6-22 shows the port diagram. 表 6-44 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-22. Port P6 (P6.4) Diagram

表 6-44. Port P6 (P6.4) Pin Functions

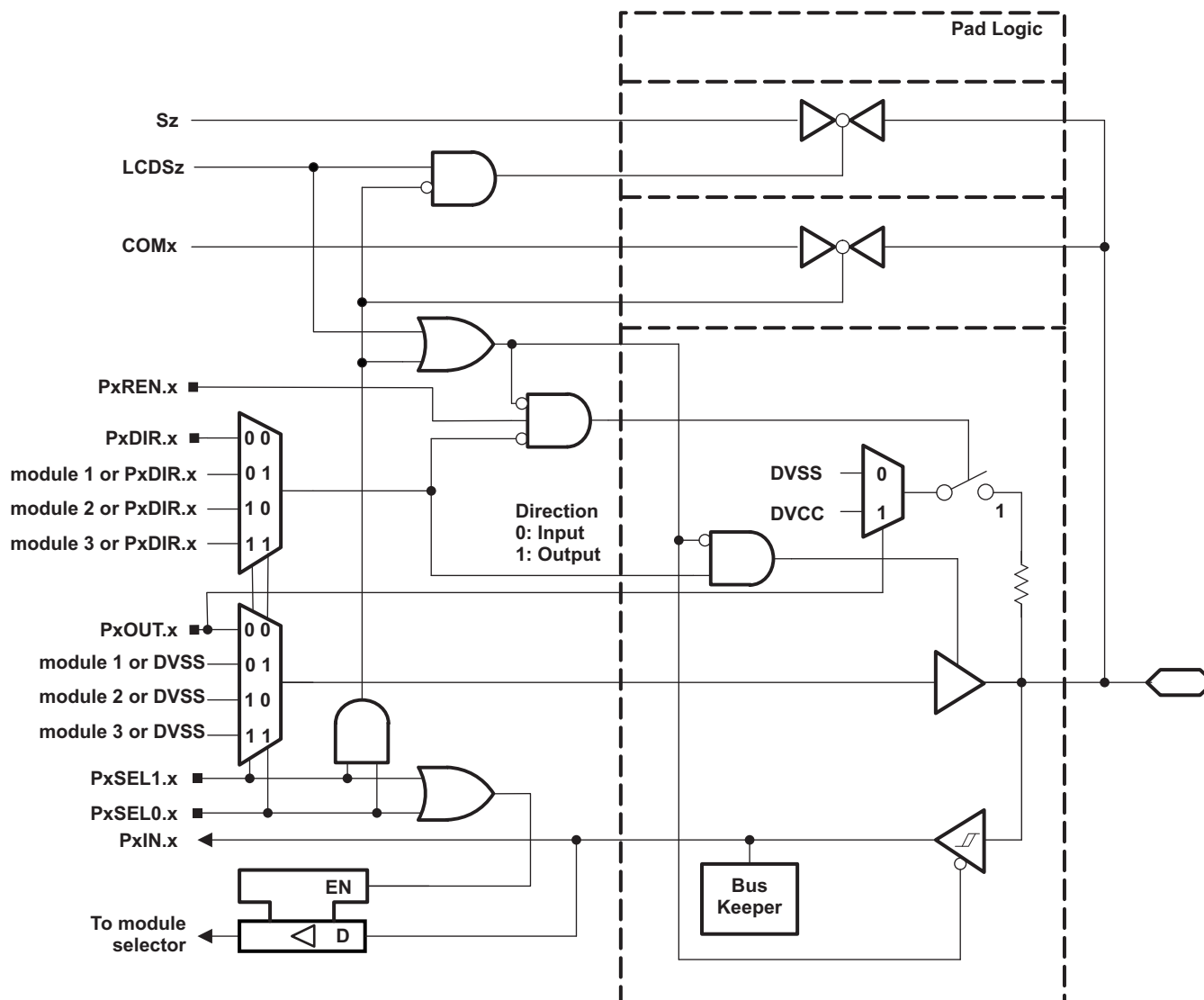
PIN NAME (P6.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
				P6DIR.x	P6SEL1.x	P6SEL0.x
P6.4/MCLK/COM0	52	43	P6.4 (I/O)	I: 0; O: 1	0	0
			N/A	0	0	1
			MCLK	1		
			N/A	0	1	0
			Internally tied to DVSS	1		
			COM0 ⁽²⁾	X	1	1

(1) X = Don't care

(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.14.22 Port P6 (P6.5 and P6.7) Input/Output With Schmitt Trigger

图 6-23 shows the port diagram. 表 6-45 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-23. Port P6 (P6.5 and P6.7) Diagram

表 6-45. Port P6 (P6.5 to P6.7) Pin Functions

PIN NAME (P6.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P6DIR.x	P6SEL1.x	P6SEL0.x	LCDSz
P6.5/SMCLK/COM1/LCDS34	53	44	P6.5(I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			SMCLK	1			
			N/A	0	1	0	0
			Internally tied to DVSS	1			
			COM1 ⁽²⁾	X	1	1	X
			Sz ⁽³⁾	X	X	0	1
P6.6/ACLK/COM2/LCDS31	54	45			0	X	
			P6.6(I/O)	I: 0; O: 1	0	0	0
			N/A	0	0	1	0
			ACLK	1			
			N/A	0	1	0	0
			Internally tied to DVSS	1			
			COM2 ⁽²⁾	X	1	1	X
P6.7/TA0.1/COM4/LCDS29	62	--	Sz ⁽³⁾	X	X	0	1
					0	X	
			P6.7(I/O)	I: 0; O: 1	0	0	0
			TA0.CCI1A	0	0	1	0
			TA0.1	1			
			N/A	0	1	0	0
			Internally tied to DVSS	1			
			COM4 ⁽²⁾	X	1	1	X
			Sz ⁽³⁾	X	X	0	1
					0	X	

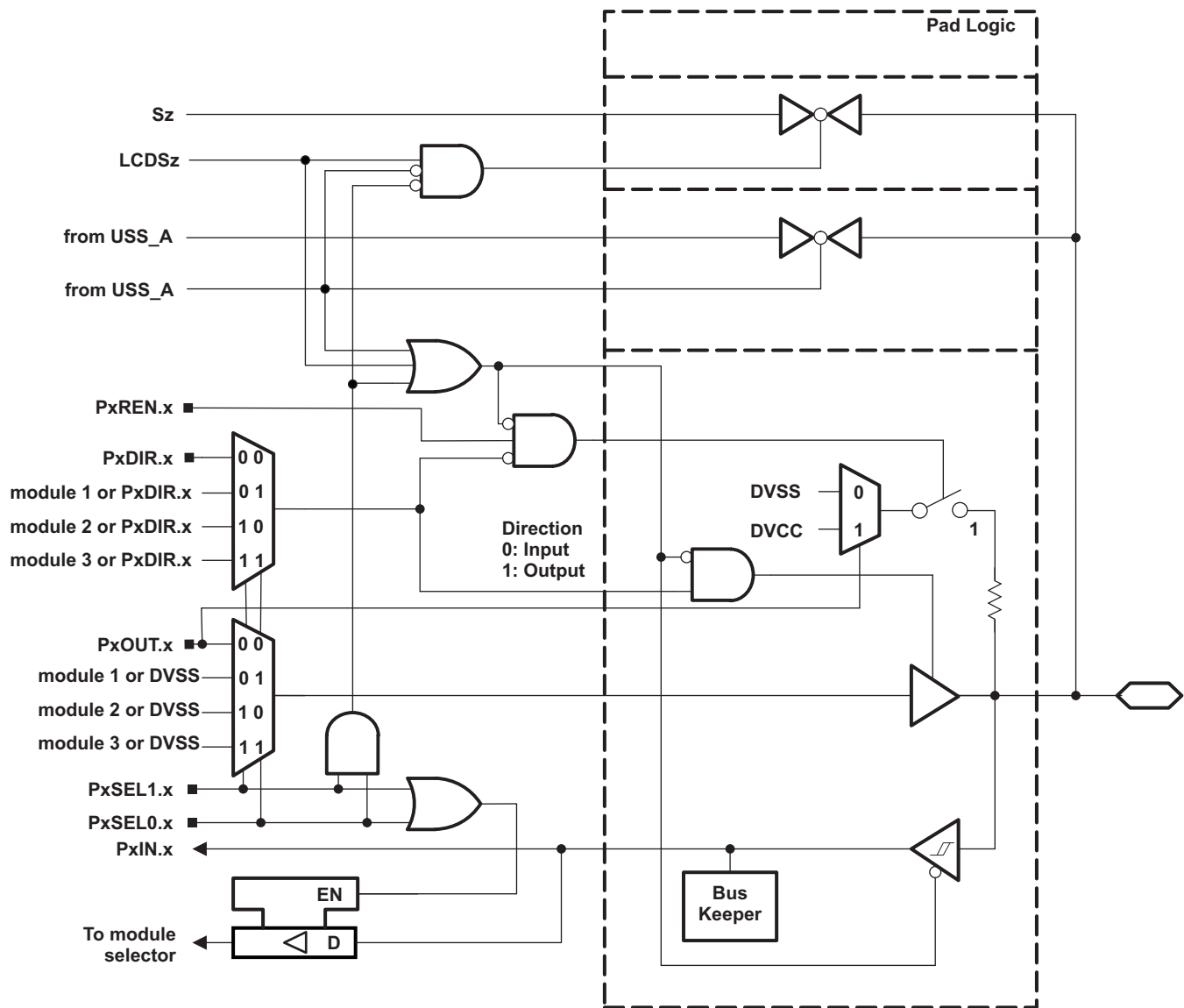
(1) X = Don't care

(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in [节 4](#).

6.14.23 Port P7 (P7.0) Input/Output With Schmitt Trigger

图 6-24 shows the port diagram. 表 6-46 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-24. Port P7 (P7.0) Diagram

表 6-46. Port P7 (P7.0) Pin Functions

PIN NAME (P7.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
				P7DIR.x	P7SEL1. x	P7EL0.x	LCDSz
P7.0/TA1.0/TA1.2/XPB0/LCD S30	55	46	P7.0 (I/O)	I: 0; O: 1	0	0	0
			TA1.CCI0B	0	0	1	0
			TA1.0	1			
			N/A	0	1	0	0
			TA1.2	1			
			XPB0	X ⁽²⁾	X	X	X
			Sz ⁽³⁾	X	X	0	1
					0	X	1

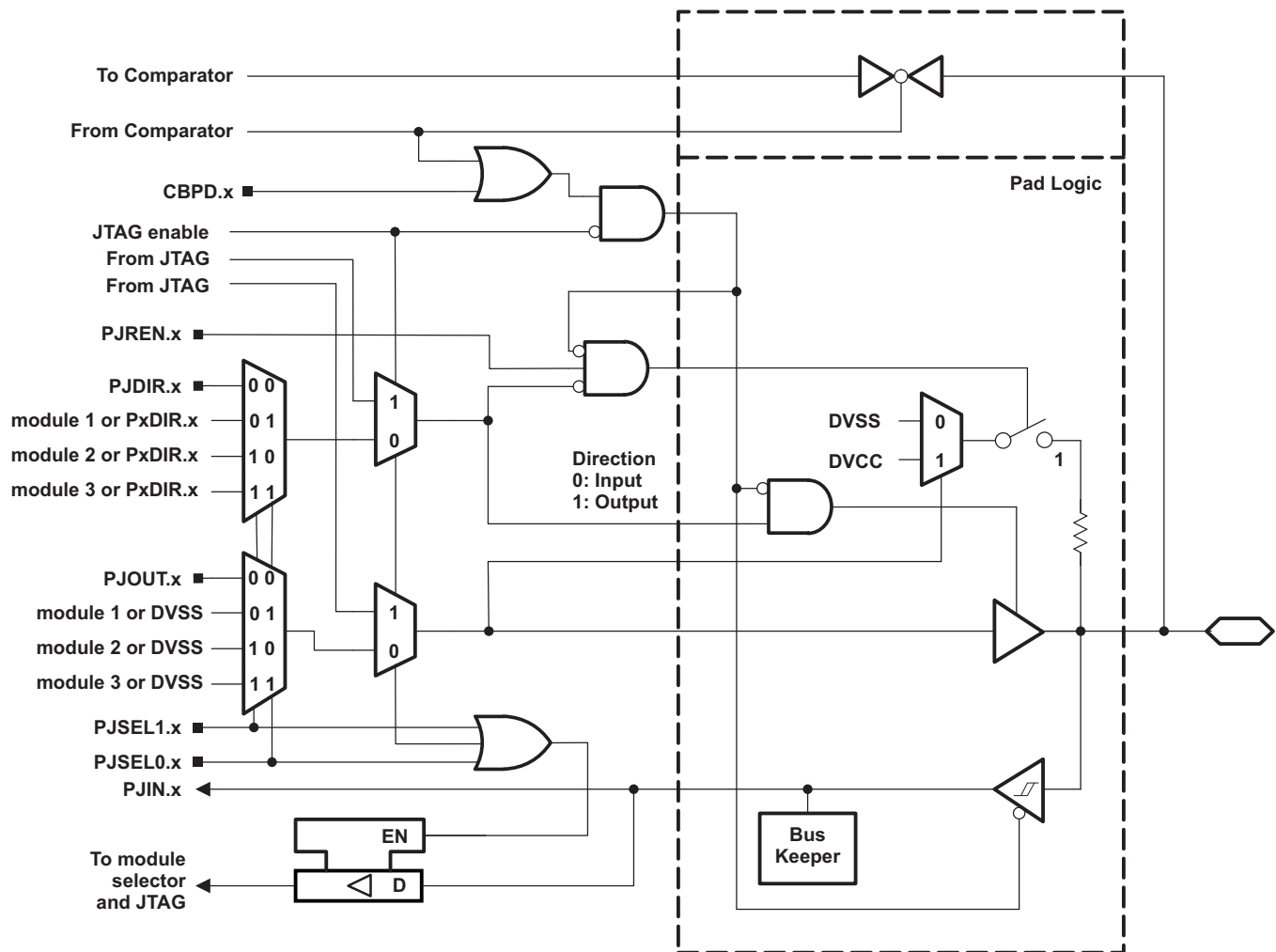
(1) X = Don't care

(2) XPB0 enable disables digital and LCD functions on this pin implicitly

(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in [节 4](#).

6.14.24 Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger

图 6-25 shows the port diagram. 表 6-47 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-25. Port PJ (PJ.0 to PJ.3) Diagram

表 6-47. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS/ SIGNALS ⁽¹⁾			
				PJDIR.x	PJSEL1.x	PJSEL0.x	CEPDx (Cx)
PJ.0/TDO/UCA2CLK/ SRSCG1/DMAE0/C10	17	13	PJ.0 (I/O) ⁽²⁾	I: 0; O: 1	0	0	0
			TDO ⁽³⁾	X	X	X	0
			UCA2CLK	X	0	1	0
			N/A	0	1	0	0
			CPU Status Register Bit SCG1	1			
			DMAE0	0	1	1	0
			Internally tied to DVSS	1			
			C10 ⁽⁴⁾	X	X	X	1
PJ.1/TDI/TCLK/UCA2 STE/SRSCG0/TA4CL K/C11	18	14	PJ.1 (I/O) ⁽²⁾	I: 0; O: 1	0	0	0
			TDI/TCLK ^{(3) (5)}	X	X	X	0
			UCA2STE	X	0	1	0
			N/A	0	1	0	0
			CPU Status Register Bit SCG0	1			
			TA4CLK	0	1	1	0
			Internally tied to DVSS	1			
			C11 ⁽⁴⁾	X	X	X	1
PJ.2/TMS/UCA2SIMO /UCA2TXD/SRSCOFF/TB0OUTH/C12	19	15	PJ.2 (I/O) ⁽²⁾	I: 0; O: 1	0	0	0
			TMS ^{(3) (5)}	X	X	X	0
			UCA2SIMO/UCA2TXD	X ⁽⁶⁾	0	1	0
			N/A	0	1	0	0
			CPU Status Register Bit OSCOFF	1			
			TB0OUTH	0	1	1	0
			Internally tied to DVSS	1			
			C12 ⁽⁴⁾	X	X	X	1
PJ.3/TCK/UCA2SOMI /UCA2RXD/SRCPUO FF/TB0.6/C13	20	16	PJ.3 (I/O) ⁽²⁾	I: 0; O: 1	0	0	0
			TCK ^{(3) (5)}	X	X	X	0
			UCA2SOMI/UCA2RXD	X ⁽⁶⁾	0	1	0
			N/A	0	1	0	0
			CPU Status Register Bit CPUOFF	1			
			TB0.CCI6A	0	1	1	0
			TB0.6	1			
			C13 ⁽⁴⁾	X	X	X	1

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made through the SYS module or by the Spy-Bi-Wire four-wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPDx bits have an effect in these cases.

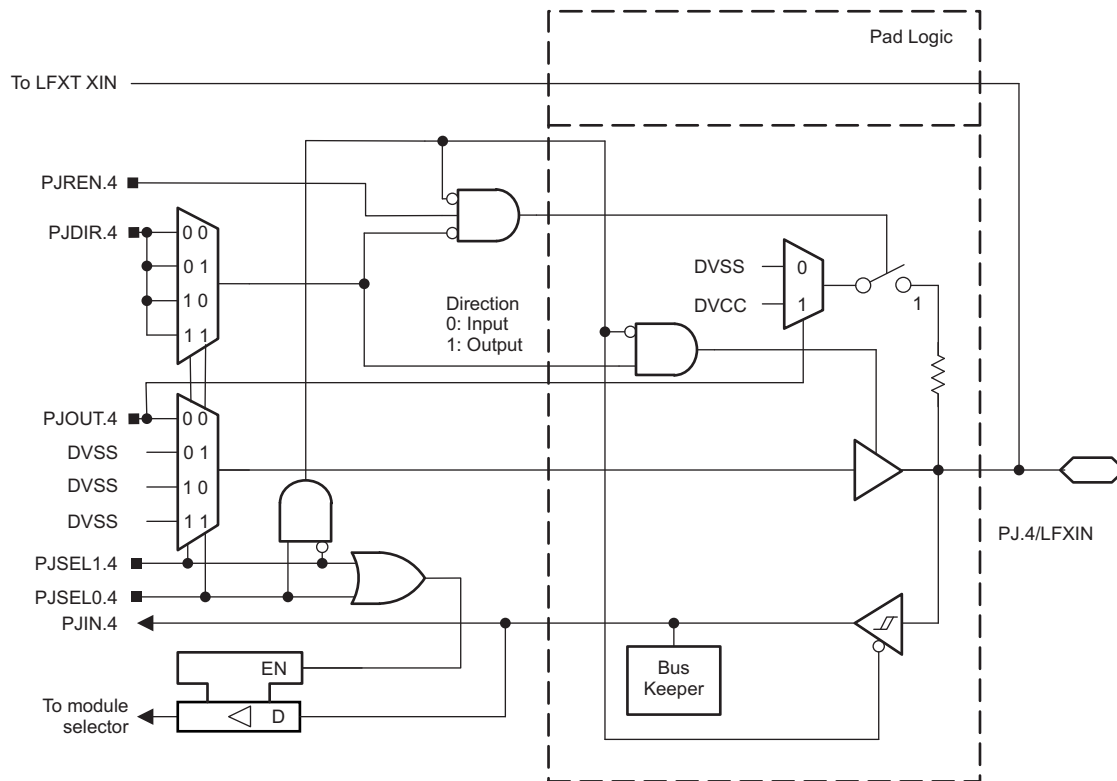
(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

(5) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

(6) Direction controlled by eUSCI_A2 module.

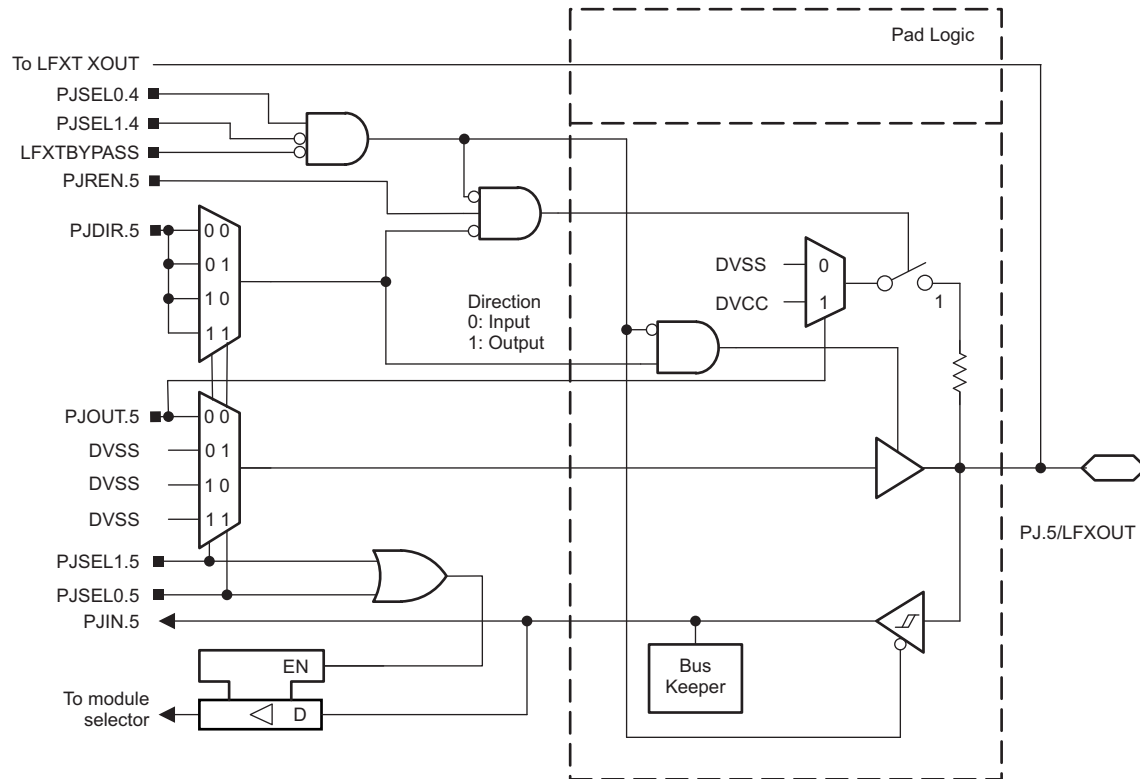
6.14.25 Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

图 6-26 and 图 6-27 show the port diagrams. 表 6-48 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-26. Port PJ (PJ.4) Diagram



NOTE: Functional representation only.

图 6-27. Port PJ (PJ.5) Diagram

表 6-48. Port PJ (PJ.4 and PJ.5) Pin Functions

PIN NAME (PJ.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾					
				PJDIR.x	PJSEL1. 5	PJSEL0.5	PJSEL1.4	PJSEL0. 4	LFXT BYPASS
PJ.4/LFXIN	7	6	PJ.4 (I/O)	I: 0; O: 1	X	X	0	0	X
			N/A	0	X	X	1	X	X
			Internally tied to DVSS	1					
			LFXIN crystal mode ⁽²⁾	X	X	X	0	1	0
			LFXIN bypass mode ⁽²⁾	X	X	X	0	1	1
PJ.5/LFXOUT	8	7	PJ.5 (I/O)	I: 0; O: 1	0	0	0	0	0
							1	X	
							X	X	1 ⁽³⁾
			N/A	0	see ⁽⁴⁾	see ⁽⁴⁾	0	0	0
							1	X	
							X	X	1 ⁽³⁾
			Internally tied to DVSS	1	see ⁽⁴⁾	see ⁽⁴⁾	0	0	0
							1	X	
							X	X	1 ⁽³⁾
			LFXOUT crystal mode ⁽²⁾	X	X	X	0	1	0

(1) X = Don't care

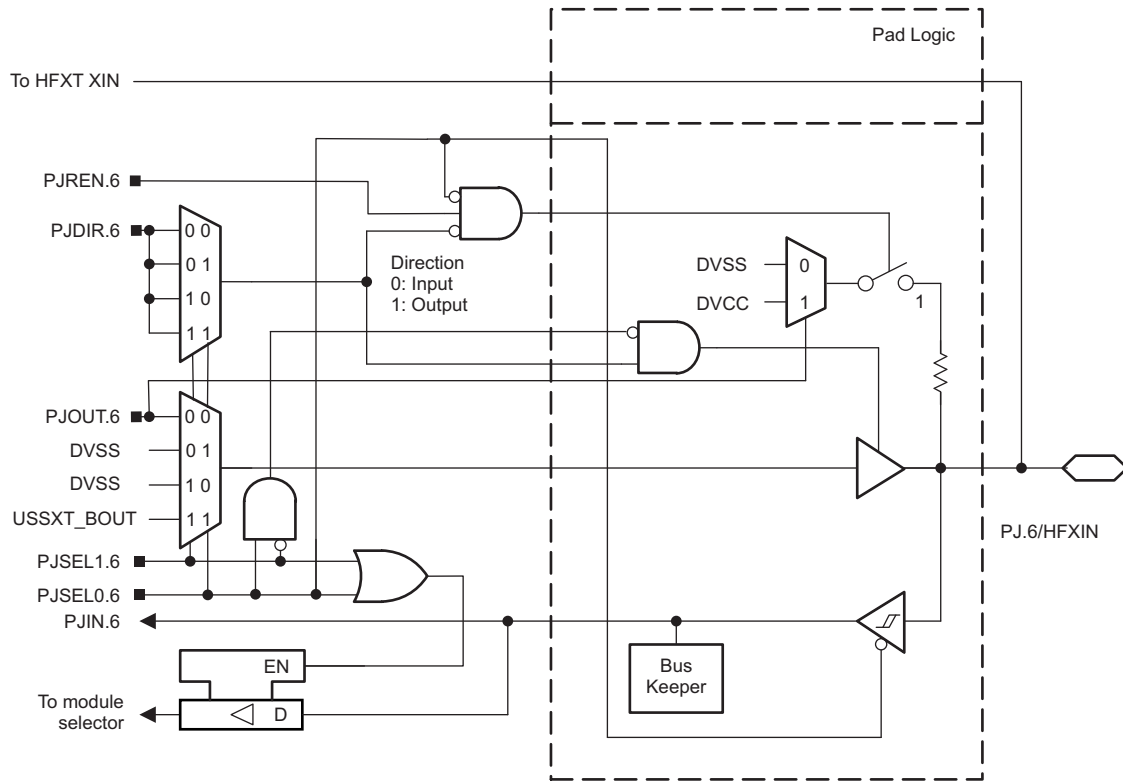
(2) If PJSEL1.4 = 0 and PJSEL0.4 = 1, the general-purpose I/O is disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.

(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.

(4) If PJSEL0.5 = 1 or PJSEL1.5 = 1, the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.

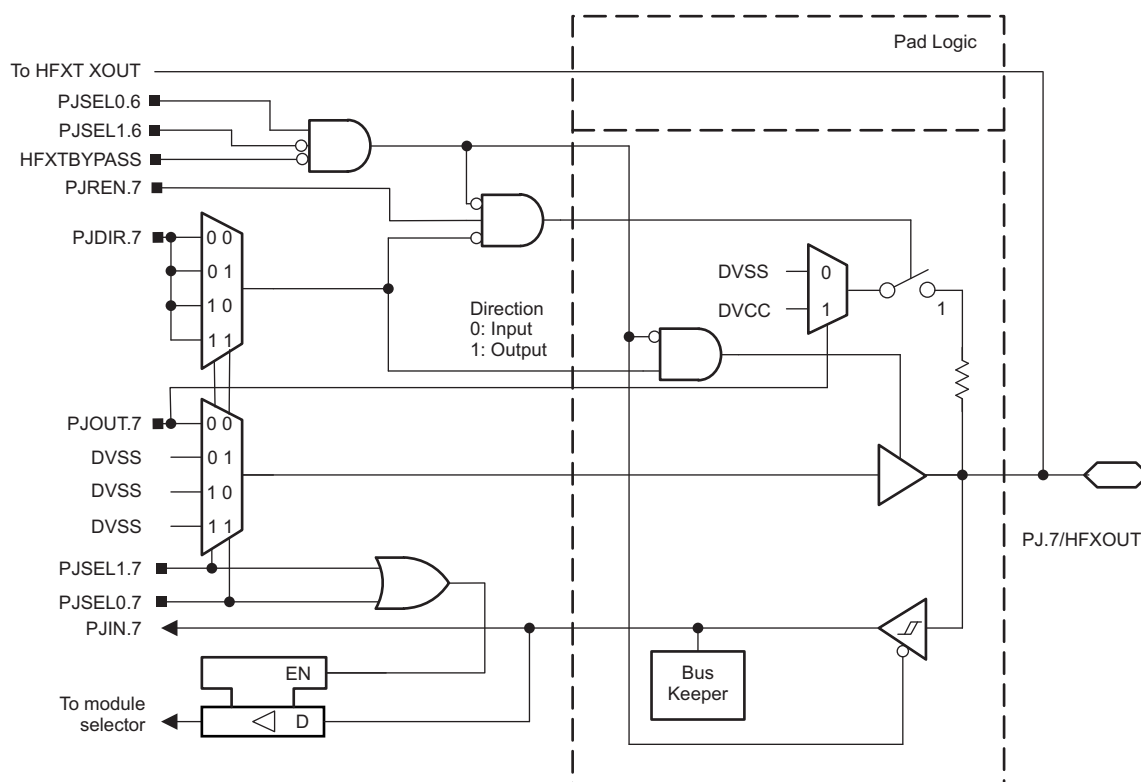
6.14.26 Port PJ (PJ.6 and PJ.7) Input/Output With Schmitt Trigger

图 6-28 和 图 6-29 show the port diagrams. 表 6-49 summarizes the selection of the pin function.



NOTE: Functional representation only.

图 6-28. Port PJ (PJ.6) Diagram



NOTE: Functional representation only.

图 6-29. Port PJ (PJ.7) Diagram

表 6-49. Port PJ (PJ.6 and PJ.7) Pin Functions

PIN NAME (PJ.x)	P N 80	PM RG C 64	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾					
				PJDIR.x	PJSEL1. 7	PJSEL0.7	PJSEL1. 6	PJSEL0.6	HFXTBYPASS
PJ.6/HFXIN/USSXT_BOUT	10	9	PJ.6 (I/O)	I: 0; O: 1	X	X	0	0	X
			HFXIN crystal mode ⁽²⁾	X	X	X	0	1	0
			HFXIN bypass mode ⁽²⁾	X	X	X	0	1	1
			N/A	0	X	X	1	0	X
			Internally tied to DVSS	0					
			N/A	0	X	X	1	1	X
			USSXT_BOUT ⁽³⁾	1					
PJ.7/HFXOUT	11	10	PJ.7 (I/O) ⁽⁴⁾	I: 0; O: 1	0	0	0	0	0
							1	X	
							X	X	
			N/A	0	see ⁽⁴⁾	see ⁽⁴⁾	0	0	0
							1	X	
							X	X	
			Internally tied to DVSS	1	see ⁽⁴⁾	see ⁽⁴⁾	0	0	0
							1	X	
							X	X	
			HFXOUT crystal mode ⁽²⁾	X	X	X	0	1	0

(1) X = Don't care

(2) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.7 and PJSEL0.7 are do not care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation and PJ.7 is configured as general-purpose I/O.

(3) HFXT is connected to USSXT_BOUT ; USSXT and HFXT operate at same frequency bur without phase control; PJ.6 acts as output

(4) With PJSEL0.7 = 1 or PJSEL1.7 =1 the general-purpose I/O functionality is disabled. No input function is available. Configured as output the pin is actively pulled to zero.

(5) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.

6.15 Device Descriptors (TLV)

表 6-50 lists the Device IDs. 表 6-51 lists the contents of the device descriptor tag-length-value (TLV) structure.

表 6-50. Device IDs

DEVICE	PACKAGE	DEVICE ID	
		01A05h	01A04h
MSP430FR6043	PN	83h	12h
MSP430FR60431	PN	83h	1Ah
MSP430FR6041	PN	83h	14h
MSP430FR5043	PM	83h	17h
MSP430FR50431	PM	83h	0Fh
MSP430FR5041	PM	83h	18h
MSP430FR5043	RGC	83h	17h
MSP430FR50431	RGC	83h	0Fh
MSP430FR5041	RGC	83h	18h

表 6-51. Device Descriptor Table⁽¹⁾

DESCRIPTION		ADDRESS	MSP430FR604x (UART BSL)	MSP430FR60431 (I ² C BSL)	MSP430FR504x (UART BSL)	MSP430FR50431 (I ² C BSL)
			VALUE	VALUE	VALUE	VALUE
Info Block	Info Length	01A00h	06h	06h	06h	06h
	CRC Length	01A01h	06h	06h	06h	06h
	CRC Value	01A02h	Per unit	Per unit	Per unit	Per unit
		01A03h	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	See 表 6-50.	See 表 6-50.	See 表 6-50.	See 表 6-50.
		01A05h				
	Hardware Revision	01A06h	Per unit	Per unit	Per unit	Per unit
	Firmware Revision	01A07h	Per unit	Per unit	Per unit	Per unit
Die Record	Die Record Tag	01A08h	08h	08h	08h	08h
	Die Record length	01A09h	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	Per unit	Per unit	Per unit	Per unit
		01A0Bh	Per unit	Per unit	Per unit	Per unit
		01A0Ch	Per unit	Per unit	Per unit	Per unit
		01A0Dh	Per unit	Per unit	Per unit	Per unit
	Die X Position	01A0Eh	Per unit	Per unit	Per unit	Per unit
		01A0Fh	Per unit	Per unit	Per unit	Per unit
	Die Y Position	01A10h	Per unit	Per unit	Per unit	Per unit
		01A11h	Per unit	Per unit	Per unit	Per unit
	Test Results	01A12h	Per unit	Per unit	Per unit	Per unit
		01A13h	Per unit	Per unit	Per unit	Per unit

(1) NA = Not applicable, Per unit = content can differ from device to device

表 6-51. Device Descriptor Table⁽¹⁾ (continued)

DESCRIPTION			MSP430FR604x (UART BSL)	MSP430FR60431 (I ² C BSL)	MSP430FR504x (UART BSL)	MSP430FR50431 (I ² C BSL)
		ADDRESS	VALUE	VALUE	VALUE	VALUE
ADC12 Calibration	ADC12 Calibration Tag	01A14h	11h	11h	11h	11h
	ADC12 Calibration Length	01A15h	10h	10h	10h	10h
	ADC Gain Factor ⁽²⁾	01A16h	Per unit	Per unit	Per unit	Per unit
		01A17h	Per unit	Per unit	Per unit	Per unit
	ADC Offset ⁽³⁾	01A18h	Per unit	Per unit	Per unit	Per unit
		01A19h	Per unit	Per unit	Per unit	Per unit
	ADC 1.2-V Reference Temperature Sensor 30°C	01A1Ah	Per unit	Per unit	Per unit	Per unit
		01A1Bh	Per unit	Per unit	Per unit	Per unit
	ADC 1.2-V Reference Temperature Sensor 85°C	01A1Ch	Per unit	Per unit	Per unit	Per unit
		01A1Dh	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V Reference Temperature Sensor 30°C	01A1Eh	Per unit	Per unit	Per unit	Per unit
		01A1Fh	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V Reference Temperature Sensor 85°C	01A20h	Per unit	Per unit	Per unit	Per unit
		01A21h	Per unit	Per unit	Per unit	Per unit
REF Calibration	ADC 2.5-V Reference Temperature Sensor 30°C	01A22h	Per unit	Per unit	Per unit	Per unit
		01A23h	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V Reference Temperature Sensor 85°C	01A24h	Per unit	Per unit	Per unit	Per unit
		01A25h	Per unit	Per unit	Per unit	Per unit
	REF Calibration Tag	01A26h	12h	12h	12h	12h
	REF Calibration Length	01A27h	06h	06h	06h	06h
	REF 1.2-V Reference	01A28h	Per unit	Per unit	Per unit	Per unit
		01A29h	Per unit	Per unit	Per unit	Per unit
	REF 2.0-V Reference	01A2Ah	Per unit	Per unit	Per unit	Per unit
		01A2Bh	Per unit	Per unit	Per unit	Per unit
	REF 2.5-V Reference	01A2Ch	Per unit	Per unit	Per unit	Per unit
		01A2Dh	Per unit	Per unit	Per unit	Per unit

(2) ADC Gain: the gain correction factor is measured at room temperature using a 2.5V external voltage reference without internal buffer (ADC12VRSEL=0x2, 0x4, or 0xE). Other settings (for example, using internal reference) can result in different correction factors.

(3) ADC Offset: the offset correction factor is measured at room temperature using ADC12VRSEL= 0x2 or 0x4, an external reference, VR+ = external 2.5V, VR- = AVSS.

表 6-51. Device Descriptor Table⁽¹⁾ (continued)

DESCRIPTION			MSP430FR604x (UART BSL)	MSP430FR60431 (I ² C BSL)	MSP430FR504x (UART BSL)	MSP430FR50431 (I ² C BSL)
		ADDRESS	VALUE	VALUE	VALUE	VALUE
Random Number	128-bit Random Number Tag	01A2Eh	15h	15h	15h	15h
	Random Number Length	01A2Fh	10h	10h	10h	10h
	128-Bit Random Number ⁽⁴⁾	01A30h	Per unit	Per unit	Per unit	Per unit
		01A31h	Per unit	Per unit	Per unit	Per unit
		01A32h	Per unit	Per unit	Per unit	Per unit
		01A33h	Per unit	Per unit	Per unit	Per unit
		01A34h	Per unit	Per unit	Per unit	Per unit
		01A35h	Per unit	Per unit	Per unit	Per unit
		01A36h	Per unit	Per unit	Per unit	Per unit
		01A37h	Per unit	Per unit	Per unit	Per unit
		01A38h	Per unit	Per unit	Per unit	Per unit
		01A39h	Per unit	Per unit	Per unit	Per unit
		01A3Ah	Per unit	Per unit	Per unit	Per unit
		01A3Bh	Per unit	Per unit	Per unit	Per unit
		01A3Ch	Per unit	Per unit	Per unit	Per unit
		01A3Dh	Per unit	Per unit	Per unit	Per unit
		01A3Eh	Per unit	Per unit	Per unit	Per unit
		01A3Fh	Per unit	Per unit	Per unit	Per unit
BSL Configur- ation	BSL Tag	01A40h	1Ch	1Ch	1Ch	1Ch
	BSL Length	01A41h	02h	02h	02h	02h
	BSL Interface	01A42h	00h	01h	00h	01h
	BSL Interface Configuration	01A43h	00h	48h	00h	48h

(4) 128-Bit Random Number: The random number is generated during production test using Microsoft's CryptGenRandom() function.

6.16 Memory Map

表 6-52 summarizes the memory map for all device variants.

表 6-52. Memory Organization⁽¹⁾

		MSP430FR5043(1), MSP430FR6043(1)	MSP430FR5041, MSP430FR6041
Memory (FRAM) Main: code memory Main: interrupt vectors and signatures	Total Size	64KB 015FFFh to 006000h 00FFFFh to 00FF80h	32KB 00FFFFh to 008000h 00FFFFh to 00FF80h
RAM (Shared with LEA) (Sector 2) Block 1 Block 0	Size	8KB (005FFFh to 004000h) 005FFFh to 005000h 004FFFh to 004000h	8KB (005FFFh to 004000h) 005FFFh to 005000h 004FFFh to 004000h
System RAM (Sector 1 base location) (Sector 0 base location) Mirrored location: 001FFFh to 001C00h Mirrored location: 002BFFh to 001C00h Main: base location Main: interrupt vectors	Size	4KB (002BFFh to 002400h) (0023FFh to 001C00h) 003FFFh to 003C00h 003BFFh to 002C00h 002BFFh to 001C00h 002BFFh to 002B80h	4KB (002BFFh to 002400h) (0023FFh to 001C00h) 003FFFh to 003C00h 003BFFh to 002C00h 002BFFh to 001C00h 002BFFh to 002B80h
Device descriptor info (TLV) (FRAM)	Size	256 B 001AFFh to 001A00h	256 B 001AFFh to 001A00h
TI calibration and configuration (FRAM)	Size	256 B 0019FFh to 001900h	256 B 0019FFh to 001900h
Bootloader (BSL) memory (ROM)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals	Size	4KB 000FFFh to 000020h	4KB 000FFFh to 000020h
Tiny RAM	Size	22 B 000001Fh to 00000Ah	22 B 000001Fh to 00000Ah
Reserved	Size	10 B 000009h to 000000h	10 B 000009h to 000000h

(1) All address space not listed is considered vacant memory.

6.16.1 Peripheral File Map

For complete module register descriptions, see the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#).

Table 6-53. Peripherals

MODULE NAME	BASE ADDRESS	END ADDRESS
Special Functions (see Table 6-54)	0100h	011Fh
PMM (see Table 6-55)	0120h	013Fh
FRAM Control (see Table 6-56)	0140h	014Fh
CRC (see Table 6-57)	0150h	0157h
RAM Control (see Table 6-58)	0158h	0159h
Watchdog (see Table 6-59)	015Ch	015Dh
CS (see Table 6-60)	0160h	016Fh
SYS (see Table 6-61)	0180h	019Fh
Shared Reference (see Table 6-62)	01B0h	01B1h
Digital I/O (see Table 6-63)	0200h	033Fh
TA0 (see Table 6-64)	0340h	036Fh
TA1 (see Table 6-65)	0380h	03AFh
TB0 (see Table 6-66)	03C0h	03EFh
TA2 (see Table 6-67)	0400h	042Fh
TA3 (see Table 6-68)	0440h	046Fh
RTC_C (see Table 6-69)	04A0h	04BFh
32-bit Hardware Multiplier (see Table 6-70)	04C0h	04EFh
DMA (see Table 6-71)	0500h	056Fh
MPU Control (see Table 6-72)	05A0h	05AFh
eUSCI_A0 (see Table 6-73)	05C0h	05DFh
eUSCI_A1 (see Table 6-74)	05E0h	05FFh
eUSCI_A2 (see Table 6-75)	0600h	061Fh
eUSCI_A3 (see Table 6-76)	0620h	063Fh
eUSCI_B0 (see Table 6-77)	0640h	066Fh
eUSCI_B1 (see Table 6-78)	0680h	06AFh
TA4 (see Table 6-79)	07C0h	07EFh
ADC12_B (see Table 6-80)	0800h	089Fh
Comparator E (see Table 6-81)	08C0h	08CFh
CRC32 (see Table 6-82)	0980h	09AFh
AES256 (see Table 6-83)	09C0h	09CFh
LEA (see Table 6-84)	0A80h	0AFFh
SAPH_A (see Table 6-85)	0E00h	0E7Fh
SDHS (see Table 6-86)	0E80h	0EBFh
UUPS (see Table 6-87)	0EC0h	0EDFh
HSPLL (see Table 6-88)	0EE0h	0EFFh
MTIF (see Table 6-89)	0F00h	0F1Fh

Table 6-54. Special Functions Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Enable	SFRIE1	0100h
Interrupt Flag	SFRIFG1	0102h

Table 6-54. Special Functions Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Reset Pin Control	SFRRPCR	0104h

Table 6-55. PMM Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
PMM control register 0	PMMCTL0	0120h
PMM interrupt flag register	PMMIFG	012Ah
Power mode 5 control register 0	PM5CTL0	0130h

Table 6-56. FRAM Control Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
FRAM Controller A Control Register 0	FRCTL0	0140h
General Control Register 0	GCCTL0	0144h
General Control Register 1	GCCTL1	0146h

Table 6-57. CRC Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
CRC Data In	CRCDI	0150h
CRC Data In Reverse Byte	CRCDIRB	0152h
CRC Initialization and Result	CRCINIRES	0154h
CRC Result Reverse	CRCRESR	0156h

Table 6-58. RAM Control Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
RAM Controller Control 0	RCCTL0	0158h
RAM Controller Control 1	RCCTL1	015Ah

Table 6-59. Watchdog Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Watchdog Timer Control Register	WDTCTL	015Ch

Table 6-60. CS Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Clock System Control 0	CSCTL0	0160h
Clock System Control 1	CSCTL1	0162h
Clock System Control 2	CSCTL2	0164h
Clock System Control 3	CSCTL3	0166h
Clock System Control 4	CSCTL4	0168h
Clock System Control 5	CSCTL5	016Ah
Clock System Control 6	CSCTL6	016Ch

Table 6-61. SYS Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
System Control	SYSCTL	0180h
JTAG Mailbox Control	SYSJMBC	0186h
JTAG Mailbox Input	SYSJMBIO	0188h

Table 6-61. SYS Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
JTAG Mailbox Input	SYSJMBI1	018Ah
JTAG Mailbox Output	SYSJMBO0	018Ch
JTAG Mailbox Output	SYSJMBO1	018Eh
User NMI Vector Generator	SYSUNIV	019Ah
System NMI Vector Generator	SYSSNIV	019Ch
Reset Vector Generator	SYSRSTIV	019Eh

Table 6-62. Shared Reference Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
REF Control Register 0	REFCTL0	01B0h

Table 6-63. Digital I/O Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Port A Input	PAIN	0200h
Port 1 Input	P1IN	0200h
Port 2 Input	P2IN	0201h
Port A Output	PAOUT	0202h
Port 1 Output	P1OUT	0202h
Port 2 Output	P2OUT	0203h
Port A Direction	PADIR	0204h
Port 1 Direction	P1DIR	0204h
Port 2 Direction	P2DIR	0205h
Port A Resistor Enable	PAREN	0206h
Port 1 Resistor Enable	P1REN	0206h
Port 2 Resistor Enable	P2REN	0207h
Port A Select 0	PASEL0	020Ah
Port 1 Select 0	P1SEL0	020Ah
Port 2 Select 0	P2SEL0	020Bh
Port A Select 1	PASEL1	020Ch
Port 1 Select 1	P1SEL1	020Ch
Port 2 Select 1	P2SEL1	020Dh
Port 1 Interrupt Vector Register	P1IV	020Eh
Port A Complement Select	PASELC	0216h
Port 1 Complement Select	P1SELC	0216h
Port 2 Complement Select	P2SELC	0217h
Port A Interrupt Edge Select	PAIES	0218h
Port 1 Interrupt Edge Select	P1IES	0218h
Port 2 Interrupt Edge Select	P2IES	0219h
Port A Interrupt Enable	PAIE	021Ah
Port 1 Interrupt Enable	P1IE	021Ah
Port 2 Interrupt Enable	P2IE	021Bh
Port A Interrupt Flag	PAIFG	021Ch
Port 1 Interrupt Flag	P1IFG	021Ch
Port 2 Interrupt Flag	P2IFG	021Dh
Port 2 Interrupt Vector Register	P2IV	021Eh
Port B Input	PBIN	0220h
Port 3 Input	P3IN	0220h

Table 6-63. Digital I/O Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Port 4 Input	P4IN	0221h
Port B Output	PBOUT	0222h
Port 3 Output	P3OUT	0222h
Port 4 Output	P4OUT	0223h
Port B Direction	PBDIR	0224h
Port 3 Direction	P3DIR	0224h
Port 4 Direction	P4DIR	0225h
Port B Resistor Enable	PBREN	0226h
Port 3 Resistor Enable	P3REN	0226h
Port 4 Resistor Enable	P4REN	0227h
Port B Select 0	PBSEL0	022Ah
Port 3 Select 0	P3SEL0	022Ah
Port 4 Select 0	P4SEL0	022Bh
Port B Select 1	PBSEL1	022Ch
Port 3 Select 1	P3SEL1	022Ch
Port 4 Select 1	P4SEL1	022Dh
Port 3 Interrupt Vector Register	P3IV	022Eh
Port B Complement Select	PBSELC	0236h
Port 3 Complement Select	P3SELC	0236h
Port 4 Complement Select	P4SELC	0237h
Port B Interrupt Edge Select	PBIES	0238h
Port 3 Interrupt Edge Select	P3IES	0238h
Port 4 Interrupt Edge Select	P4IES	0239h
Port B Interrupt Enable	PBIE	023Ah
Port 3 Interrupt Enable	P3IE	023Ah
Port 4 Interrupt Enable	P4IE	023Bh
Port B Interrupt Flag	PBIFG	023Ch
Port 3 Interrupt Flag	P3IFG	023Ch
Port 4 Interrupt Flag	P4IFG	023Dh
Port 4 Interrupt Vector Register	P4IV	023Eh
Port C Input	PCIN	0240h
Port 5 Input	P5IN	0240h
Port 6 Input	P6IN	0241h
Port C Output	PCOUT	0242h
Port 5 Output	P5OUT	0242h
Port 6 Output	P6OUT	0243h
Port C Direction	PCDIR	0244h
Port 5 Direction	P5DIR	0244h
Port 6 Direction	P6DIR	0245h
Port C Resistor Enable	PCREN	0246h
Port 5 Resistor Enable	P5REN	0246h
Port 6 Resistor Enable	P6REN	0247h
Port C Select 0	PCSEL0	024Ah
Port 5 Select 0	P5SEL0	024Ah
Port 6 Select 0	P6SEL0	024Bh
Port C Select 1	PCSEL1	024Ch
Port 5 Select 1	P5SEL1	024Ch

Table 6-63. Digital I/O Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Port 6 Select 1	P6SEL1	024Dh
Port 5 Interrupt Vector Register	P5IV	024Eh
Port C Complement Select	PCSELC	0256h
Port 5 Complement Select	P5SELC	0256h
Port 6 Complement Select	P6SELC	0257h
Port C Interrupt Edge Select	PCIES	0258h
Port 5 Interrupt Edge Select	P5IES	0258h
Port 6 Interrupt Edge Select	P6IES	0259h
Port C Interrupt Enable	PCIE	025Ah
Port 5 Interrupt Enable	P5IE	025Ah
Port 6 Interrupt Enable	P6IE	025Bh
Port C Interrupt Flag	PCIFG	025Ch
Port 5 Interrupt Flag	P5IFG	025Ch
Port 6 Interrupt Flag	P6IFG	025Dh
Port 6 Interrupt Vector Register	P6IV	025Eh
Port D Input	PDIN	0260h
Port 7 Input	P7IN	0260h
Port D Output	PDOUT	0262h
Port 7 Output	P7OUT	0262h
Port D Direction	PDDIR	0264h
Port 7 Direction	P7DIR	0264h
Port D Resistor Enable	PDREN	0266h
Port 7 Resistor Enable	P7REN	0266h
Port D Select 0	PDSEL0	026Ah
Port 7 Select 0	P7SEL0	026Ah
Port D Select 1	PDSEL1	026Ch
Port 7 Select 1	P7SEL1	026Ch
Port 7 Interrupt Vector Register	P7IV	026Eh
Port D Complement Select	PDSELC	0276h
Port 7 Complement Select	P7SELC	0276h
Port D Interrupt Edge Select	PDIES	0278h
Port 7 Interrupt Edge Select	P7IES	0278h
Port D Interrupt Enable	PDIE	027Ah
Port 7 Interrupt Enable	P7IE	027Ah
Port D Interrupt Flag	PDIFG	027Ch
Port 7 Interrupt Flag	P7IFG	027Ch
Port J Input	PJIN	0320h
Port J Output	PJOUT	0322h
Port J Direction	PJDIR	0324h
Port J Resistor Enable	PJREN	0326h
Port J Select 0	PJSEL0	032Ah
Port J Select 1	PJSEL1	032Ch
Port J Complement Select	PJSELC	0336h

Table 6-64. TA0 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A0 Control Register	TA0CTL	0340h
Timer_A0 Capture/Compare Control Register	TA0CCTL0	0342h
Timer_A0 Capture/Compare Control Register	TA0CCTL1	0344h
Timer_A0 Capture/Compare Control Register	TA0CCTL2	0346h
Timer_A0 register	TA0R	0350h
Timer_A0 Capture/Compare Register	TA0CCR0	0352h
Timer_A0 Capture/Compare Register	TA0CCR1	0354h
Timer_A0 Capture/Compare Register	TA0CCR2	0356h
Timer_A0 Expansion 0 Register	TA0EX0	0360h
Timer_A0 Interrupt Vector Register	TA0IV	036Eh

Table 6-65. TA1 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A1 Control Register	TA1CTL	0380h
Timer_A1 Capture/Compare Control Register	TA1CCTL0	0382h
Timer_A1 Capture/Compare Control Register	TA1CCTL1	0384h
Timer_A1 Capture/Compare Control Register	TA1CCTL2	0386h
Timer_A1 register	TA1R	0390h
Timer_A1 Capture/Compare Register	TA1CCR0	0392h
Timer_A1 Capture/Compare Register	TA1CCR1	0394h
Timer_A1 Capture/Compare Register	TA1CCR2	0396h
Timer_A1 Expansion 0 Register	TA1EX0	03A0h
Timer_A1 Interrupt Vector Register	TA1IV	03AEh

Table 6-66. TB0 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_B0 Control Register	TB0CTL	03C0h
Timer_B0 Capture/Compare Control Register	TB0CCTL0	03C2h
Timer_B0 Capture/Compare Control Register	TB0CCTL1	03C4h
Timer_B0 Capture/Compare Control Register	TB0CCTL2	03C6h
Timer_B0 Capture/Compare Control Register	TB0CCTL3	03C8h
Timer_B0 Capture/Compare Control Register	TB0CCTL4	03CAh
Timer_B0 Capture/Compare Control Register	TB0CCTL5	03CCh
Timer_B0 Capture/Compare Control Register	TB0CCTL6	03CEh
Timer_B0 count register	TB0R	03D0h
Timer_B0 Capture/Compare Register	TB0CCR0	03D2h
Timer_B0 Capture/Compare Register	TB0CCR1	03D4h
Timer_B0 Capture/Compare Register	TB0CCR2	03D6h
Timer_B0 Capture/Compare Register	TB0CCR3	03D8h
Timer_B0 Capture/Compare Register	TB0CCR4	03DAh
Timer_B0 Capture/Compare Register	TB0CCR5	03DCh
Timer_B0 Capture/Compare Register	TB0CCR6	03DEh
Timer_B0 Expansion Register 0	TB0EX0	03E0h
Timer_B0 Interrupt Vector Register	TB0IV	03EEh

Table 6-67. TA2 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A2 Control Register	TA2CTL	0400h
Timer_A2 Capture/Compare Control Register	TA2CCTL0	0402h
Timer_A2 Capture/Compare Control Register	TA2CCTL1	0404h
Timer_A2 register	TA2R	0410h
Timer_A2 Capture/Compare Register	TA2CCR0	0412h
Timer_A2 Capture/Compare Register	TA2CCR1	0414h
Timer_A2 Expansion 0 Register	TA2EX0	0420h
Timer_A2 Interrupt Vector Register	TA2IV	042Eh

Table 6-68. TA3 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A3 Control Register	TA3CTL	0440h
Timer_A3 Capture/Compare Control Register	TA3CCTL0	0442h
Timer_A3 Capture/Compare Control Register	TA3CCTL1	0444h
Timer_A3 register	TA3R	0450h
Timer_A3 Capture/Compare Register	TA3CCR0	0452h
Timer_A3 Capture/Compare Register	TA3CCR1	0454h
Timer_A3 Expansion 0 Register	TA3EX0	0460h
Timer_A3 Interrupt Vector Register	TA3IV	046Eh

Table 6-69. RTC_C Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
RTCCTL0 Register	RTCCTL0	04A0h
RTCCTL13 Register	RTCCTL13	04A2h
RTCOCAL Register	RTCOCAL	04A4h
RTCTCMP Register	RTCTCMP	04A6h
Real-Time Clock Prescale Timer 0 Control Register	RTCPS0CTL	04A8h
Real-Time Clock Prescale Timer 1 Control Register	RTCPS1CTL	04AAh
Real-Time Clock Prescale Timer Counter Register	RTCPS	04ACh
Prescale timer 0 counter value	RT0PS	04ACh
Prescale timer 1 counter value	RT1PS	04ADh
Real-Time Clock Interrupt Vector Register	RTCIV	04AEh
RTCTIM0 Register – Hexadecimal Format	RTCTIM0	04B0h
Real-Time Clock Hour, Day of Week	RTCTIM1	04B2h
RTCDATE - Hexadecimal Format	RTCDATE	04B4h
RTCYEAR Register – Hexadecimal Format	RTCYEAR	04B6h
RTCMINHR - Hexadecimal Format	RTCAMINHR	04B8h
RTCADOWDAY - Hexadecimal Format	RTCADOWDAY	04BAh
Binary-to-BCD Conversion Register	BIN2BCD	04BCh
BCD-to-Binary Conversion Register	BCD2BIN	04BEh

Table 6-70. 32-bit Hardware Multiplier Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
16-bit operand one – multiply	MPY	04C0h
16-bit operand one – signed multiply	MPYS	04C2h
16-bit operand one – multiply accumulate	MAC	04C4h

Table 6-70. 32-bit Hardware Multiplier Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
16-bit operand one – signed multiply accumulate	MACS	04C6h
16-bit operand two	OP2	04C8h
16x16-bit result low word	RESLO	04CAh
16x16-bit result high word	RESHI	04CCh
16x16-bit sum extension register	SUMEXT	04CEh
32-bit operand 1 – multiply – low word	MPY32L	04D0h
32-bit operand 1 – multiply – high word	MPY32H	04D2h
32-bit operand 1 – signed multiply – low word	MPYS32L	04D4h
32-bit operand 1 – signed multiply – high word	MPYS32H	04D6h
32-bit operand 1 – multiply accumulate – low word	MAC32L	04D8h
32-bit operand 1 – multiply accumulate – high word	MAC32H	04DAh
32-bit operand 1 – signed multiply accumulate – low word	MACS32L	04DCh
32-bit operand 1 – signed multiply accumulate – high word	MACS32H	04DEh
32-bit operand 2 – low word	OP2L	04E0h
32-bit operand 2 – high word	OP2H	04E2h
32x32-bit result 0 – least significant word	RES0	04E4h
32x32-bit result 1	RES1	04E6h
32x32-bit result 2	RES2	04E8h
32x32-bit result 3 – most significant word	RES3	04EAh
MPY32 control register 0	MPY32CTL0	04ECh

Table 6-71. DMA Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
DMA Control 0	DMACTL0	0500h
DMA Control 1	DMACTL1	0502h
DMA Control 2	DMACTL2	0504h
DMA Control 4	DMACTL4	0508h
DMA Interrupt Vector	DMAIV	050Eh
DMA Channel 0 Control	DMA0CTL	0510h
DMA Channel 0 Source Address	DMA0SA	0512h
DMA Channel 0 Destination Address	DMA0DA	0516h
DMA Channel 0 Transfer Size	DMA0SZ	051Ah
DMA Channel 1 Control	DMA1CTL	0520h
DMA Channel 1 Source Address	DMA1SA	0522h
DMA Channel 1 Destination Address	DMA1DA	0526h
DMA Channel 1 Transfer Size	DMA1SZ	052Ah
DMA Channel 2 Control	DMA2CTL	0530h
DMA Channel 2 Source Address	DMA2SA	0532h
DMA Channel 2 Destination Address	DMA2DA	0536h
DMA Channel 2 Transfer Size	DMA2SZ	053Ah
DMA Channel 3 Control	DMA3CTL	0540h
DMA Channel 3 Source Address	DMA3SA	0542h
DMA Channel 3 Destination Address	DMA3DA	0546h
DMA Channel 3 Transfer Size	DMA3SZ	054Ah
DMA Channel 4 Control	DMA4CTL	0550h
DMA Channel 4 Source Address	DMA4SA	0552h
DMA Channel 4 Destination Address	DMA4DA	0556h

Table 6-71. DMA Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
DMA Channel 4 Transfer Size	DMA4SZ	055Ah
DMA Channel 5 Control	DMA5CTL	0560h
DMA Channel 5 Source Address	DMA5SA	0562h
DMA Channel 5 Destination Address	DMA5DA	0566h
DMA Channel 5 Transfer Size	DMA5SZ	056Ah

Table 6-72. MPU Control Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Memory Protection Unit Control 0	MPUCTL0	05A0h
Memory Protection Unit Control 1	MPUCTL1	05A2h
Memory Protection Unit Segmentation Border 2 Register	MPUSEGB2	05A4h
Memory Protection Unit Segmentation Border 1 Register	MPUSEGB1	05A6h
Memory Protection Unit Segmentation Access Management Register	MPUSAM	05A8h
Memory Protection Unit IP Control 0 Register	MPUIPC0	05AAh
Memory Protection Unit IP Encapsulation Segment Border 2 Register	MPUIPSEGB2	05ACh
Memory Protection Unit IP Encapsulation Segment Border 1 Register	MPUIPSEGB1	05AEh

Table 6-73. eUSCI_A0 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A0 Control Word Register 0	UCA0CTLW0	05C0h
eUSCI_A0 Control Word Register 1	UCA0CTLW1	05C2h
eUSCI_A0 Baud Rate Control Word Register	UCA0BRW	05C6h
eUSCI_A0 Modulation Control Word Register	UCA0MCTLW	05C8h
eUSCI_A0 Status Register	UCA0STATW	05CAh
eUSCI_A0 Receive Buffer Register	UCA0RXBUF	05CCh
eUSCI_A0 Transmit Buffer Register	UCA0TXBUF	05CEh
eUSCI_A0 Auto Baud Rate Control Register	UCA0ABCTL	05D0h
eUSCI_A0 IrDA Control Word Register	UCA0IRCTL	05D2h
eUSCI_A0 Interrupt Enable Register	UCA0IE	05DAh
eUSCI_A0 Interrupt Flag Register	UCA0IFG	05DCh
eUSCI_A0 Interrupt Vector Register	UCA0IV	05DEh

Table 6-74. eUSCI_A1 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A1 Control Word Register 0	UCA1CTLW0	05E0h
eUSCI_A1 Control Word Register 1	UCA1CTLW1	05E2h
eUSCI_A1 Baud Rate Control Word Register	UCA1BRW	05E6h
eUSCI_A1 Modulation Control Word Register	UCA1MCTLW	05E8h
eUSCI_A1 Status Register	UCA1STATW	05EAh
eUSCI_A1 Receive Buffer Register	UCA1RXBUF	05ECh
eUSCI_A1 Transmit Buffer Register	UCA1TXBUF	05EEh
eUSCI_A1 Auto Baud Rate Control Register	UCA1ABCTL	05F0h
eUSCI_A1 IrDA Control Word Register	UCA1IRCTL	05F2h
eUSCI_A1 Interrupt Enable Register	UCA1IE	05FAh
eUSCI_A1 Interrupt Flag Register	UCA1IFG	05FCh
eUSCI_A1 Interrupt Vector Register	UCA1IV	05FEh

Table 6-75. eUSCI_A2 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A2 Control Word Register 0	UCA2CTLW0	0600h
eUSCI_A2 Control Word Register 1	UCA2CTLW1	0602h
eUSCI_A2 Baud Rate Control Word Register	UCA2BRW	0606h
eUSCI_A2 Modulation Control Word Register	UCA2MCTLW	0608h
eUSCI_A2 Status Register	UCA2STATW	060Ah
eUSCI_A2 Receive Buffer Register	UCA2RXBUF	060Ch
eUSCI_A2 Transmit Buffer Register	UCA2TXBUF	060Eh
eUSCI_A2 Auto Baud Rate Control Register	UCA2ABCTL	0610h
eUSCI_A2 IrDA Control Word Register	UCA2IRCTL	0612h
eUSCI_A2 Interrupt Enable Register	UCA2IE	061Ah
eUSCI_A2 Interrupt Flag Register	UCA2IFG	061Ch
eUSCI_A2 Interrupt Vector Register	UCA2IV	061Eh

Table 6-76. eUSCI_A3 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A3 Control Word Register 0	UCA3CTLW0	0620h
eUSCI_A3 Control Word Register 1	UCA3CTLW1	0622h
eUSCI_A3 Baud Rate Control Word Register	UCA3BRW	0626h
eUSCI_A3 Modulation Control Word Register	UCA3MCTLW	0628h
eUSCI_A3 Status Register	UCA3STATW	062Ah
eUSCI_A3 Receive Buffer Register	UCA3RXBUF	062Ch
eUSCI_A3 Transmit Buffer Register	UCA3TXBUF	062Eh
eUSCI_A3 Auto Baud Rate Control Register	UCA3ABCTL	0630h
eUSCI_A3 IrDA Control Word Register	UCA3IRCTL	0632h
eUSCI_A3 Interrupt Enable Register	UCA3IE	063Ah
eUSCI_A3 Interrupt Flag Register	UCA3IFG	063Ch
eUSCI_A3 Interrupt Vector Register	UCA3IV	063Eh

Table 6-77. eUSCI_B0 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_B0 Control Word Register 0	UCB0CTLW0	0640h
eUSCI_B0 Control Word Register 1	UCB0CTLW1	0642h
eUSCI_B0 Baud Rate Control Word Register	UCB0BRW	0646h
eUSCI_B0 Status Register	UCB0STATW	0648h
eUSCI_B0 Byte Counter Threshold Register	UCB0TBCNT	064Ah
eUSCI_B0 Receive Buffer Register	UCB0RXBUF	064Ch
eUSCI_B0 Transmit Buffer Register	UCB0TXBUF	064Eh
eUSCI_B0 I2C Own Address 0 Register	UCB0I2COA0	0654h
eUSCI_B0 I2C Own Address 1 Register	UCB0I2COA1	0656h
eUSCI_B0 I2C Own Address 2 Register	UCB0I2COA2	0658h
eUSCI_B0 I2C Own Address 3 Register	UCB0I2COA3	065Ah
eUSCI_B0 I2C Received Address Register	UCB0ADDRX	065Ch
eUSCI_B0 I2C Address Mask Register	UCB0ADDMASK	065Eh
eUSCI_B0 I2C Slave Address Register	UCB0I2CSA	0660h
eUSCI_B0 Interrupt Enable Register	UCB0IE	066Ah
eUSCI_B0 Interrupt Flag Register	UCB0IFG	066Ch
eUSCI_B0 Interrupt Vector Register	UCB0IV	066Eh

Table 6-78. eUSCI_B1 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_B1 Control Word Register 0	UCB1CTLW0	0680h
eUSCI_B1 Control Word Register 1	UCB1CTLW1	0682h
eUSCI_B1 Baud Rate Control Word Register	UCB1BRW	0686h
eUSCI_B1 Status Register	UCB1STATW	0688h
eUSCI_B1 Byte Counter Threshold Register	UCB1TBCNT	068Ah
eUSCI_B1 Receive Buffer Register	UCB1RXBUF	068Ch
eUSCI_B1 Transmit Buffer Register	UCB1TXBUF	068Eh
eUSCI_B1 I2C Own Address 0 Register	UCB1I2COA0	0694h
eUSCI_B1 I2C Own Address 1 Register	UCB1I2COA1	0696h
eUSCI_B1 I2C Own Address 2 Register	UCB1I2COA2	0698h
eUSCI_B1 I2C Own Address 3 Register	UCB1I2COA3	069Ah
eUSCI_B1 I2C Received Address Register	UCB1ADDRX	069Ch
eUSCI_B1 I2C Address Mask Register	UCB1ADDMASK	069Eh
eUSCI_B1 I2C Slave Address Register	UCB1I2CSA	06A0h
eUSCI_B1 Interrupt Enable Register	UCB1IE	06AAh
eUSCI_B1 Interrupt Flag Register	UCB1IFG	06ACh
eUSCI_B1 Interrupt Vector Register	UCB1IV	06AEh

Table 6-79. TA4 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A4 Control Register	TA4CTL	07C0h
Timer_A4 Capture/Compare Control Register	TA4CCTL0	07C2h
Timer_A4 Capture/Compare Control Register	TA4CCTL1	07C4h
Timer_A4 register	TA4R	07D0h
Timer_A4 Capture/Compare Register	TA4CCR0	07D2h
Timer_A4 Capture/Compare Register	TA4CCR1	07D4h
Timer_A4 Expansion 0 Register	TA4EX0	07E0h
Timer_A4 Interrupt Vector Register	TA4IV	07EEh

Table 6-80. ADC12_B Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
ADC12_B Control 0	ADC12CTL0	0800h
ADC12_B Control 1	ADC12CTL1	0802h
ADC12_B Control 2	ADC12CTL2	0804h
ADC12_B Control 3	ADC12CTL3	0806h
ADC12_B Window Comparator Low Threshold Register	ADC12LO	0808h
ADC12_B Window Comparator High Threshold Register	ADC12HI	080Ah
ADC12_B Interrupt Flag 0	ADC12IFGR0	080Ch
ADC12_B Interrupt Flag 1	ADC12IFGR1	080Eh
ADC12_B Interrupt Flag 2	ADC12IFGR2	0810h
ADC12_B Interrupt Enable 0	ADC12IER0	0812h
ADC12_B Interrupt Enable 1	ADC12IER1	0814h
ADC12_B Interrupt Enable 2	ADC12IER2	0816h
ADC12_B Interrupt Vector	ADC12IV	0818h
ADC12_B Memory Control 0 Register	ADC12MCTL0	0820h
ADC12_B Memory Control 1 Register	ADC12MCTL1	0822h
ADC12_B Memory Control 2 Register	ADC12MCTL2	0824h

Table 6-80. ADC12_B Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
ADC12_B Memory Control 3 Register	ADC12MCTL3	0826h
ADC12_B Memory Control 4 Register	ADC12MCTL4	0828h
ADC12_B Memory Control 5 Register	ADC12MCTL5	082Ah
ADC12_B Memory Control 6 Register	ADC12MCTL6	082Ch
ADC12_B Memory Control 7 Register	ADC12MCTL7	082Eh
ADC12_B Memory Control 8 Register	ADC12MCTL8	0830h
ADC12_B Memory Control 9 Register	ADC12MCTL9	0832h
ADC12_B Memory Control 10 Register	ADC12MCTL10	0834h
ADC12_B Memory Control 11 Register	ADC12MCTL11	0836h
ADC12_B Memory Control 12 Register	ADC12MCTL12	0838h
ADC12_B Memory Control 13 Register	ADC12MCTL13	083Ah
ADC12_B Memory Control 14 Register	ADC12MCTL14	083Ch
ADC12_B Memory Control 15 Register	ADC12MCTL15	083Eh
ADC12_B Memory Control 16 Register	ADC12MCTL16	0840h
ADC12_B Memory Control 17 Register	ADC12MCTL17	0842h
ADC12_B Memory Control 18 Register	ADC12MCTL18	0844h
ADC12_B Memory Control 19 Register	ADC12MCTL19	0846h
ADC12_B Memory Control 20 Register	ADC12MCTL20	0848h
ADC12_B Memory Control 21 Register	ADC12MCTL21	084Ah
ADC12_B Memory Control 22 Register	ADC12MCTL22	084Ch
ADC12_B Memory Control 23 Register	ADC12MCTL23	084Eh
ADC12_B Memory Control 24 Register	ADC12MCTL24	0850h
ADC12_B Memory Control 25 Register	ADC12MCTL25	0852h
ADC12_B Memory Control 26 Register	ADC12MCTL26	0854h
ADC12_B Memory Control 27 Register	ADC12MCTL27	0856h
ADC12_B Memory Control 28 Register	ADC12MCTL28	0858h
ADC12_B Memory Control 29 Register	ADC12MCTL29	085Ah
ADC12_B Memory Control 30 Register	ADC12MCTL30	085Ch
ADC12_B Memory Control 31 Register	ADC12MCTL31	085Eh
ADC12_B Memory 0 Register	ADC12MEM0	0860h
ADC12_B Memory 1 Register	ADC12MEM1	0862h
ADC12_B Memory 2 Register	ADC12MEM2	0864h
ADC12_B Memory 3 Register	ADC12MEM3	0866h
ADC12_B Memory 4 Register	ADC12MEM4	0868h
ADC12_B Memory 5 Register	ADC12MEM5	086Ah
ADC12_B Memory 6 Register	ADC12MEM6	086Ch
ADC12_B Memory 7 Register	ADC12MEM7	086Eh
ADC12_B Memory 8 Register	ADC12MEM8	0870h
ADC12_B Memory 9 Register	ADC12MEM9	0872h
ADC12_B Memory 10 Register	ADC12MEM10	0874h
ADC12_B Memory 11 Register	ADC12MEM11	0876h
ADC12_B Memory 12 Register	ADC12MEM12	0878h
ADC12_B Memory 13 Register	ADC12MEM13	087Ah
ADC12_B Memory 14 Register	ADC12MEM14	087Ch
ADC12_B Memory 15 Register	ADC12MEM15	087Eh
ADC12_B Memory 16 Register	ADC12MEM16	0880h
ADC12_B Memory 17 Register	ADC12MEM17	0882h

Table 6-80. ADC12_B Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
ADC12_B Memory 18 Register	ADC12MEM18	0884h
ADC12_B Memory 19 Register	ADC12MEM19	0886h
ADC12_B Memory 20 Register	ADC12MEM20	0888h
ADC12_B Memory 21 Register	ADC12MEM21	088Ah
ADC12_B Memory 22 Register	ADC12MEM22	088Ch
ADC12_B Memory 23 Register	ADC12MEM23	088Eh
ADC12_B Memory 24 Register	ADC12MEM24	0890h
ADC12_B Memory 25 Register	ADC12MEM25	0892h
ADC12_B Memory 26 Register	ADC12MEM26	0894h
ADC12_B Memory 27 Register	ADC12MEM27	0896h
ADC12_B Memory 28 Register	ADC12MEM28	0898h
ADC12_B Memory 29 Register	ADC12MEM29	089Ah
ADC12_B Memory 30 Register	ADC12MEM30	089Ch
ADC12_B Memory 31 Register	ADC12MEM31	089Eh

Table 6-81. Comparator E Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Comparator Control Register 0	CECTL0	08C0h
Comparator Control Register 1	CECTL1	08C2h
Comparator Control Register 2	CECTL2	08C4h
Comparator Control Register 3	CECTL3	08C6h
Comparator Interrupt Control Register	CEINT	08CCh
Comparator Interrupt Vector Word Register	CEIV	08CEh

Table 6-82. CRC32 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
CRC32 Data Input Word 0	CRC32DIW0	0980h
CRC32 Data Input Word 1	CRC32DIW1	0982h
CRC32 Data In Reverse Word 1	CRC32DIRBW1	0984h
CRC32 Data In Reverse Word 0	CRC32DIRBW0	0986h
CRC32 Initialization and Result Word 0	CRC32INIRESW0	0988h
CRC32 Initialization and Result Word 1	CRC32INIRESW1	098Ah
CRC32 Result Reverse Word 1	CRC32RESRW1	098Ch
CRC32 Result Reverse Word 0	CRC32RESRW0	098Eh
CRC16 Data Input	CRC16DIW0	0990h
CRC16 Data In Reverse	CRC16DIRBW0	0996h
CRC16 Init and Result	CRC16INIRESW0	0998h
CRC16 Result Reverse	CRC16RESRW0	099Eh

Table 6-83. AES256 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
AES Accelerator Control Register 0	AESACTL0	09C0h
AES Accelerator Control Register 1	AESACTL1	09C2h
AES Accelerator Status Register	AESASTAT	09C4h
AES Accelerator Key Register	AESAKEY	09C6h
AES Accelerator Data In Register	AESADIN	09C8h

Table 6-83. AES256 Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
AES Accelerator Data Out Register	AESADOUT	09CAh
AES Accelerator XORed Data In Register	AESAXDIN	09CCh
AES Accelerator XORed Data In Register	AESAXIN	09CEh

Table 6-84. LEA Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
LEA Capability Register	LEACAP	0A80h
Configuration Register 0	LEACNF0	0A84h
Configuration Register 1	LEACNF1	0A88h
Configuration Register 2	LEACNF2	0A8Ch
Memory Bottom Register	LEAMB	0A90h
Memory Top Register	LEAMT	0A94h
Code Memory Access Register	LEACMA	0A98h
Code Memory Control Register	LEACMCTL	0A9Ch
LEA Command Status Register	LEACMDSTAT	0AA8h
LEA Source 1 Status Register	LEAS1STAT	0AACCh
LEA Source 0 Status Register	LEAS0STAT	0AB0h
LEA Result Status Register	LEADSTSTAT	0AB4h
PM Control Register	LEAPMCTL	0AC0h
PM Result Register	LEAPMDST	0AC4h
PM Source 1 Register	LEAPMS1	0AC8h
PM Source 0 Register	LEAPMS0	0ACCCh
PM Command Buffer Register	LEAPMCB	0AD0h
Interrupt Flag and Set Register	LEAIFGSET	0AF0h
Interrupt Enable Register	LEAIE	0AF4h
Interrupt Flag and Clear Register	LEAIFG	0AF8h
Interrupt Vector Register	LEAIV	0AFCh

Table 6-85. SAPH_A Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Index	SAPH_AIIDX	0E00h
Masked Interrupt Satus	SAPH_AMIS	0E02h
Raw Interrupt Status	SAPH_ARIS	0E04h
Interrupt Mask	SAPH_AIMSC	0E06h
Interrupt Clear	SAPH_AICR	0E08h
Interrupt Set	SAPH_AISR	0E0Ah
Module-Descriptor Low Word	SAPH_ADESCLO	0E0Ch
Module-Descriptor High Word	SAPH_ADESCHI	0E0Eh
Key	SAPH_AKEY	0E10h
Physical Interface Output Control #0	SAPH_AOCTL0	0E12h
Physical Interface Output Control #1	SAPH_AOCTL1	0E14h
Physical Interface Output Function Select	SAPH_AOSEL	0E16h
Channel 0 Pull UpTrim Register	SAPH_ACH0PUT	0E20h
Channel 0 Pull DownTrim Register	SAPH_ACH0PDT	0E22h
Channel 0 Termination Trim	SAPH_ACH0TT	0E24h
Channel 1 Pull UpTrim	SAPH_ACH1PUT	0E26h
Channel 1 Pull DownTrim	SAPH_ACH1PDT	0E28h

Table 6-85. SAPH_A Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Channel 1 Termination Trim	SAPH_ACH1TT	0E2Ah
Mode Configuration	SAPH_AMCNF	0E2Ch
Trim Access Control	SAPH_ATACTL	0E2Eh
Physical Interface Input Control #0	SAPH_AICTL0	0E30h
Bias Control	SAPH_ABCTL	0E34h
PPG Count	SAPH_APGC	0E40h
Pulse Generator Low Period	SAPH_APGLPER	0E42h
Pulse Generator High Period	SAPH_APGHPER	0E44h
PPG Control	SAPH_APGCTL	0E46h
PPG Software Trigger	SAPH_APPGTRIG	0E48h
Extended Pulse Control Register	SAPH_AXPGLCTL	0E4Ah
Extra Pulse Low Period Register	SAPH_AXPGLPER	0E4Ch
Extra Pulse High Period Register	SAPH_AXPGHPER	0E4Eh
A-SEQ control register 0	SAPH_AASCTL0	0E60h
A-SEQ control register 1	SAPH_AASCTL1	0E62h
ASQ Software Trigger	SAPH_AASQTRIG	0E64h
ASQ ping output polarity	SAPH_AAPOL	0E66h
ASQ ping pause level	SAPH_AAPLEV	0E68h
ASQ ping pause impedance	SAPH_AAPHIZ	0E6Ah
A-SEQ start to 1st ping	SAPH_AATM_A	0E6Eh
ASQ start to ADC arm	SAPH_AATM_B	0E70h
Count for the TIMEMARK C Event	SAPH_AATM_C	0E72h
ASQ start to ADC trig	SAPH_AATM_D	0E74h
ASQ start to restart	SAPH_AATM_E	0E76h
ASQ start to timeout	SAPH_AATM_F	0E78h
Time Base Control	SAPH_ATBCTL	0E7Ah
Acquisition Timer Low Part	SAPH_AATIMLO	0E7Ch
Acquisition Timer High Part	SAPH_AATIMHI	0E7Eh

Table 6-86. SDHS Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Index Register	SDHSIIDX	0E80h
Masked Interrupt Status and Clear Register	SDHSMIS	0E82h
Raw Interrupt Status Register	SDHSRIS	0E84h
Interrupt Mask Register	SDHSIMSC	0E86h
Interrupt Clear Register.	SDHSICR	0E88h
Interrupt Set Register.	SDHSISR	0E8Ah
SDHS Descriptor Register L.	SDHSDESCLO	0E8Ch
SDHS Descriptor Register H.	SDHSDESCHI	0E8Eh
SDHS Control Register 0	SDHSCTL0	0E90h
SDHS Control Register 1	SDHSCTL1	0E92h
SDHS Control Register 2	SDHSCTL2	0E94h
SDHS Control Register 3	SDHSCTL3	0E96h
SDHS Control Register 4	SDHSCTL4	0E98h
SDHS Control Register 5	SDHSCTL5	0E9Ah
SDHS Control Register 6	SDHSCTL6	0E9Ch
SDHS Control Register 7	SDHSCTL7	0E9Eh

Table 6-86. SDHS Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
SDHS Data Conversion Register	SDHSDT	0EA2h
SDHS Window Comparator High Threshold Register.	SDHSWINHITH	0EA4h
SDHS Window Comparator Low Threshold Register.	SDHSWINLOTH	0EA6h
DTC destination address register	SDHSDTCDA	0EA8h

Table 6-87. UUPS Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Index Register	UUPSIIDX	0EC0h
Masked Interrupt Status Register	UUPSMIS	0EC2h
Raw Interrupt Status Register	UUPSRIS	0EC4h
Interrupt Mask Register	UUPSIMSC	0EC6h
Interrupt Clear Register.	UUPSICR	0EC8h
Interrupt Flag Set Register.	UUPSISR	0ECAh
UUPS Descriptor Register L.	UUPSDESCLO	0ECCh
UUPS Descriptor Register H.	UUPSDESCHI	0ECEh
UUPS Control	UUPSCTL	0ED0h

Table 6-88. HSPLL Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Index Register	HSPLLIIDX	0EE0h
Masked Interrupt Status Register.	HSPLLMIS	0EE2h
Raw Interrupt Status Register	HSPLLRIS	0EE4h
Interrupt Mask Register	HSPLLMSC	0EE6h
Interrupt Flag Clear Register.	HSPLLICR	0EE8h
Interrupt Flag Set Register.	HSPLLISR	0EEAh
HSPLL Descriptor Register L.	HSPLLDESCLO	0EECh
HSPLL Descriptor Register H.	HSPLLDESCHI	0EEeh
HSPLL Control Register	HSPLLCTL	0EF0h
USSXT Control Register	HSPLLUSSXTLCTL	0EF2h

Table 6-89. MTIF Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Pulse Generator Configuration Register	MTIFPGCNF	0F00h
Pulse Generator Value Register	MTIFPGKVAL	0F02h
Pulse Generator Control Register	MTIFPGCTL	0F04h
Pulse Generator Status Register	MTIFPGSR	0F06h
Pulse Counter Configuration Register	MTIFPCCNF	0F08h
Pulse Counter Value Register	MTIFPCR	0F0Ah
Pulse Counter Control Register	MTIFPCCTL	0F0Ch
Pulse Counter Status Register	MTIFPCSR	0F0Eh
Measurement Test Port Control Register	MTIFTPCTL	0F10h

表 6-90. LCD_C Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
LCD_C control register 0	LCDCCTL0	0A00h
LCD_C control register 1	LCDCCTL1	0A02h

表 6-90. LCD_C Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
LCD_C blinking control register	LCDCBLKCTL	0A04h
LCD_C memory control register	LCDCMEMCTL	0A06h
LCD_C voltage control register	LCDCVCTL	0A08h
LCD_C port control 0	LCDCPCTL0	0A0Ah
LCD_C port control 1	LCDCPCTL1	0A0Ch
LCD_C port control 2 (≥256 segments)	LCDCPCTL2	0A0Eh
LCD_C port control 3 (384 segments)	LCDCPCTL3	0A10h
LCD_C charge pump control register	LCDCCPCTL	0A12h
LCD_C interrupt vector	LCDCIV	0A1Eh
Static and 2 to 4 mux modes		
LCD_C memory 1	LCDM1	0A20h
LCD_C memory 2	LCDM2	0A21h
LCD_C memory 3	LCDM3	0A22h
LCD_C memory 4	LCDM4	0A23h
LCD_C memory 5	LCDM5	0A24h
LCD_C memory 6	LCDM6	0A25h
LCD_C memory 7	LCDM7	0A26h
LCD_C memory 8	LCDM8	0A27h
LCD_C memory 9	LCDM9	0A28h
LCD_C memory 10	LCDM10	0A29h
LCD_C memory 11	LCDM11	0A2Ah
LCD_C memory 12	LCDM12	0A2Bh
LCD_C memory 13	LCDM13	0A2Ch
LCD_C memory 14	LCDM14	0A2Dh
LCD_C memory 15	LCDM15	0A2Eh
LCD_C memory 16	LCDM16	0A2Fh
LCD_C memory 17	LCDM17	0A30h
LCD_C memory 18	LCDM18	0A31h
LCD_C memory 19	LCDM19	0A32h
LCD_C memory 20	LCDM20	0A33h
Reserved		0A34h to 0A3Bh
LCD_C blinking memory 1	LCDBM1	0A40h
LCD_C blinking memory 2	LCDBM2	0A41h
LCD_C blinking memory 3	LCDBM3	0A42h
LCD_C blinking memory 4	LCDBM4	0A43h
LCD_C blinking memory 5	LCDBM5	0A44h
LCD_C blinking memory 6	LCDBM6	0A45h
LCD_C blinking memory 7	LCDBM7	0A46h
LCD_C blinking memory 8	LCDBM8	0A47h
LCD_C blinking memory 9	LCDBM9	0A48h
LCD_C blinking memory 10	LCDBM10	0A49h
LCD_C blinking memory 11	LCDBM11	0A4Ah
LCD_C blinking memory 12	LCDBM12	0A4Bh
LCD_C blinking memory 13	LCDBM13	0A4Ch
LCD_C blinking memory 14	LCDBM14	0A4Dh
LCD_C blinking memory 15	LCDBM15	0A4Eh
LCD_C blinking memory 16	LCDBM16	0A4Fh

表 6-90. LCD_C Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
LCD_C blinking memory 17	LCDBM17	0A50h
LCD_C blinking memory 18	LCDBM18	0A51h
LCD_C blinking memory 19	LCDBM19	0A52h
LCD_C blinking memory 20	LCDBM20	0A53h
Reserved		0A54h to 0A5Bh
5 to 8 mux modes		
LCD_C memory 1	LCDM1	0A20h
LCD_C memory 2	LCDM2	0A21h
LCD_C memory 3	LCDM3	0A22h
LCD_C memory 4	LCDM4	0A23h
LCD_C memory 5	LCDM5	0A24h
LCD_C memory 6	LCDM6	0A25h
LCD_C memory 7	LCDM7	0A26h
LCD_C memory 8	LCDM8	0A27h
LCD_C memory 9	LCDM9	0A28h
LCD_C memory 10	LCDM10	0A29h
LCD_C memory 11	LCDM11	0A2Ah
LCD_C memory 12	LCDM12	0A2Bh
LCD_C memory 13	LCDM13	0A2Ch
LCD_C memory 14	LCDM14	0A2Dh
LCD_C memory 15	LCDM15	0A2Eh
LCD_C memory 16	LCDM16	0A2Fh
LCD_C memory 17	LCDM17	0A30h
LCD_C memory 18	LCDM18	0A31h
LCD_C memory 19	LCDM19	0A32h
LCD_C memory 20	LCDM20	0A33h
LCD_C memory 21	LCDM21	0A34h
LCD_C memory 22	LCDM22	0A35h
LCD_C memory 23	LCDM23	0A36h
LCD_C memory 24	LCDM24	0A37h
LCD_C memory 25	LCDM25	0A38h
LCD_C memory 26	LCDM26	0A39h
LCD_C memory 27	LCDM27	0A3Ah
LCD_C memory 28	LCDM28	0A3Bh
LCD_C memory 29	LCDM29	0A3Ch
LCD_C memory 30	LCDM30	0A3Dh
LCD_C memory 31	LCDM31	0A3Eh
LCD_C memory 32	LCDM32	0A3Fh
LCD_C memory 33	LCDM33	0A40h
LCD_C memory 34	LCDM34	0A41h
LCD_C memory 35	LCDM35	0A42h
LCD_C memory 36	LCDM36	0A43h
Reserved		0A44h to 0A53h

LDC memory is implemented for groups of segments. Memory for non-existent segment lines is accessible but cannot be used.

6.17 Identification

6.17.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [节 8.4](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in the Device Descriptor structure.

6.17.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [节 8.4](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in the Device Descriptor structure.

6.17.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in [MSP430 Programming With the JTAG Interface](#).

7 Applications, Implementation, and Layout

注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP MCU. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply and Bulk Capacitors

TI recommends connecting a combination of a 1- μ F plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital to analog circuits on the board and to achieve high analog accuracy.

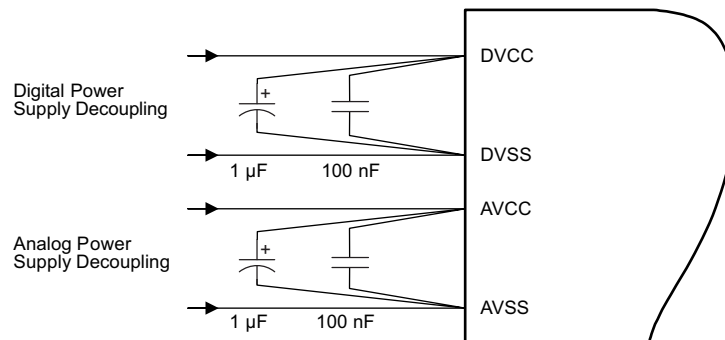


图 7-1. Power Supply Decoupling

For PVCC and PVSS, TI recommends connecting a combination of a 1- μ F plus a 22- μ F low-ESR ceramic decoupling capacitor between the PVCC and PVSS pins and a serial 22- Ω resistor to filter low-frequency noise on the supply line (see 图 7-2).

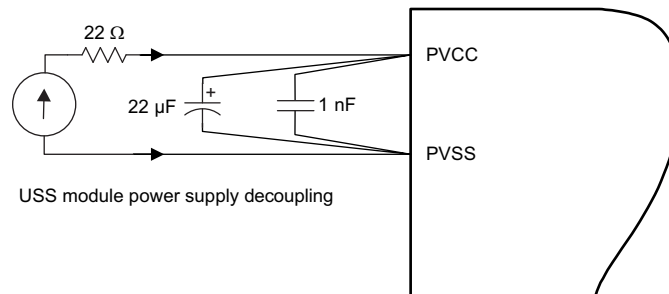


图 7-2. Power Supply Decoupling for PVCC and PVSS

7.1.2 External Oscillator (HFXT and LFXT)

Depending on the device variant (see 节 3), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, they must be terminated according to 节 4.6.

图 7-3 shows a typical connection diagram.

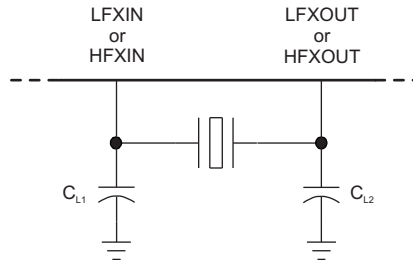


图 7-3. Typical Crystal Connection

See [MSP430 32-kHz Crystal Oscillators](#) for more information on selecting, testing, and designing a crystal oscillator with the MSP MCUs.

7.1.3 USS Oscillator (USSXT)

Depending on the device variant (see), the device with USS module supports a high-frequency crystal on the USSXT pins. External bypass capacitors for the crystal oscillator pins are required. A 22-Ω resistor is required to be serially connected closely to the USSXTOUT pin as shown in 图 7-4. The USSXT does not support bypass mode, so it is not possible to apply digital clock signals to the USSXTIN pin. Never connect the USSXTIN pin to a power supply line (AVCC, DVCC, or PVCC). If the USSXT pins are not used, terminate them according to 节 4.6.

图 7-4 shows a typical connection diagram.

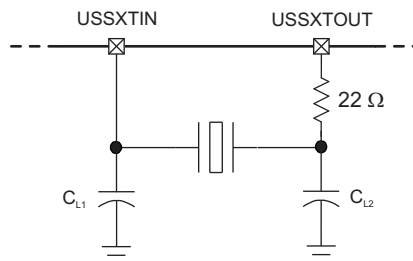


图 7-4. Typical Crystal Connection

Consider the following items for the USSXT layout:

- Keep the trace of USSXTIN and USSXTOUT as short as possible. In case one must be longer than the other, keep USSXTIN shorter because USSXTIN is more sensitive to EMI
- Make ground shield open ended without making a loop
- Use ground plane to reduce the impedance of ground trace
- In case USSXT_BOUT is used, keep coupling to USSXTIN and CH0_IN to a minimum
- In case USSXT_BOUT is feeding other clock or device inputs, apply a small capacitor (10 pF) as the line termination load at end of line. This avoids reflection artifacts on sensitive inputs (for example, HFXIN).

图 7-5 shows recommended PCB layout.

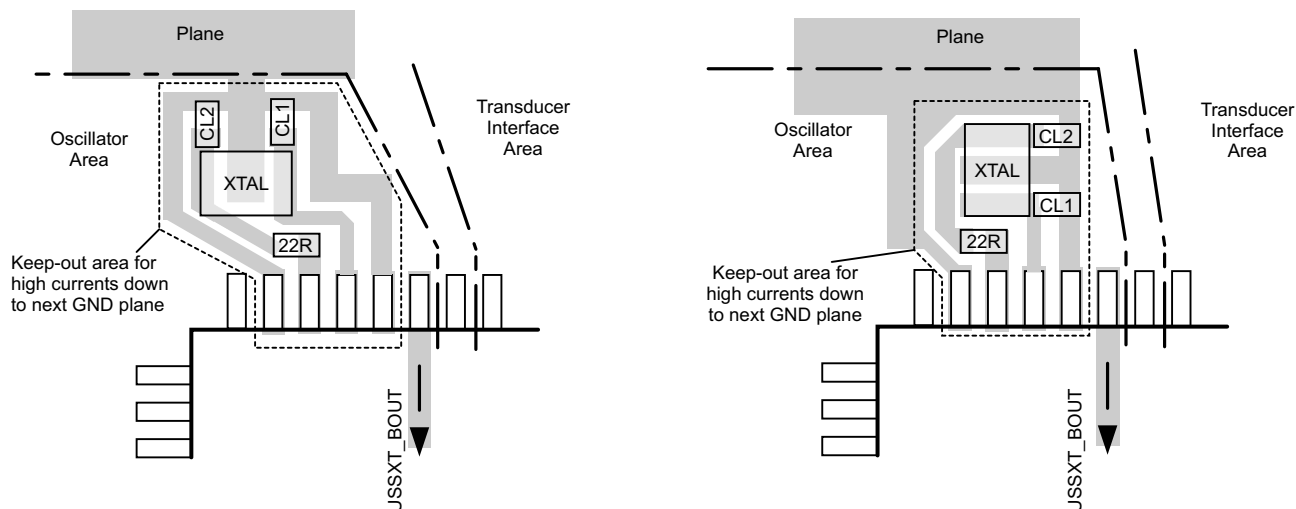


图 7-5. USSXT PCB Layout Recommendation

7.1.4 Transducer Connection to the USS Module

图 7-6 shows a typical connection of two transducers to the USS output and input pins. TI recommends 1% error tolerance for the external termination resistors (R_{term0} and R_{term1}) and the AC coupling capacitors (C_{ac0} and C_{ac1}). Typical value of the termination resistors is in the range of 150 to 400 Ω , the AC coupling capacitors are 1 to 2 nF. Actual values should be determined to meet the requirements of each application.

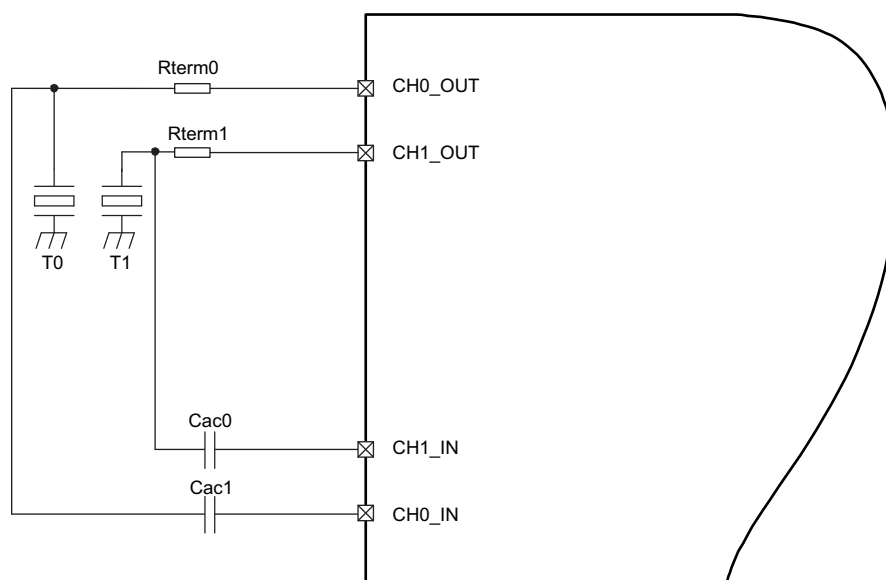


图 7-6. Typical Transducer Connection

7.1.5 Charge Pump Control of Input Multiplexer

图 7-7 shows the control logic of the charge pump control of the input multiplexer of CHx_IN . The charge pump is enabled as long the $SAPH_AMCNF.CPEO$ is high and during the arming of the SDHS. Use the CPDA bit to control the CP during data acquisition.

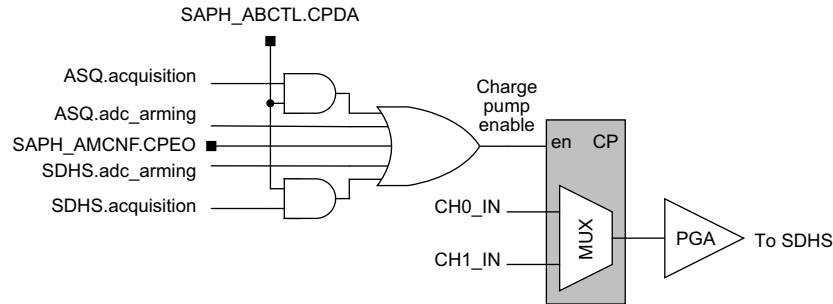


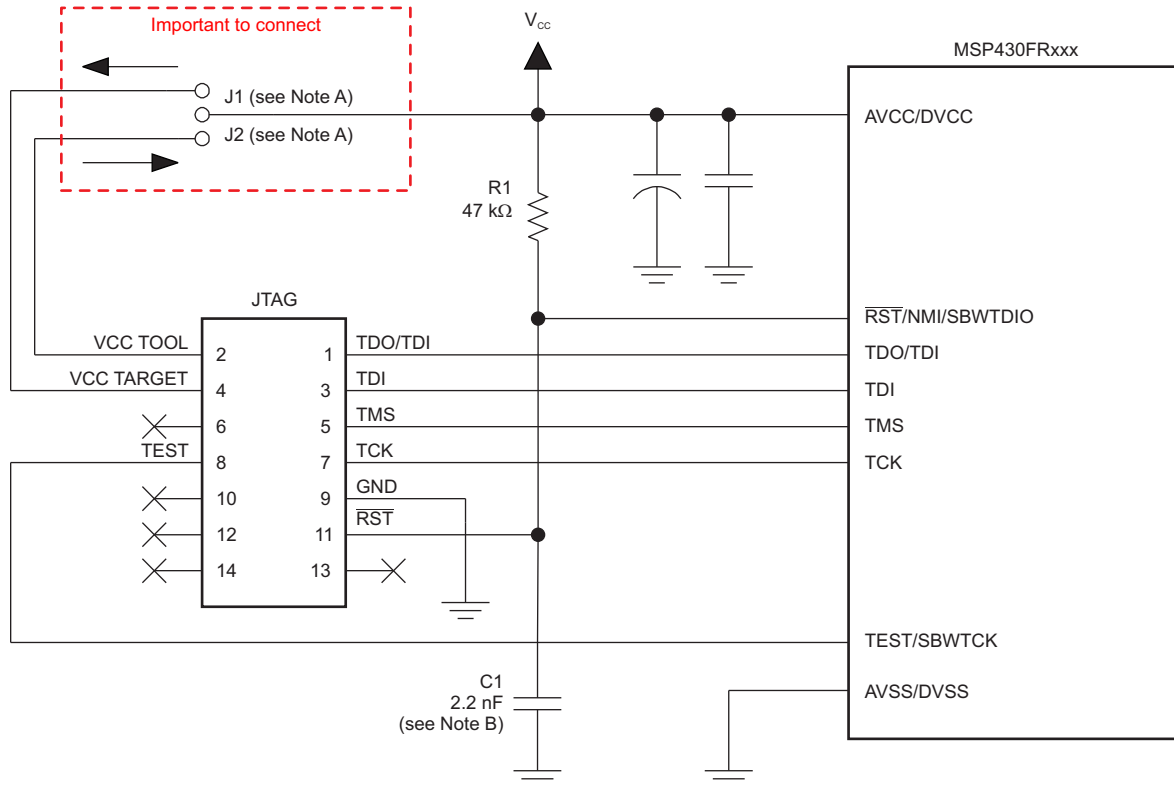
图 7-7. Control Of Input Multiplexer

7.1.6 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. 图 7-8 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. 图 7-9 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply V_{CC} to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a V_{CC} -sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The V_{CC} -sense feature senses the local V_{CC} present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. 图 7-8 and 图 7-9 show a jumper block that supports both scenarios of supplying V_{CC} to the target board. If this flexibility is not required, the desired V_{CC} connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

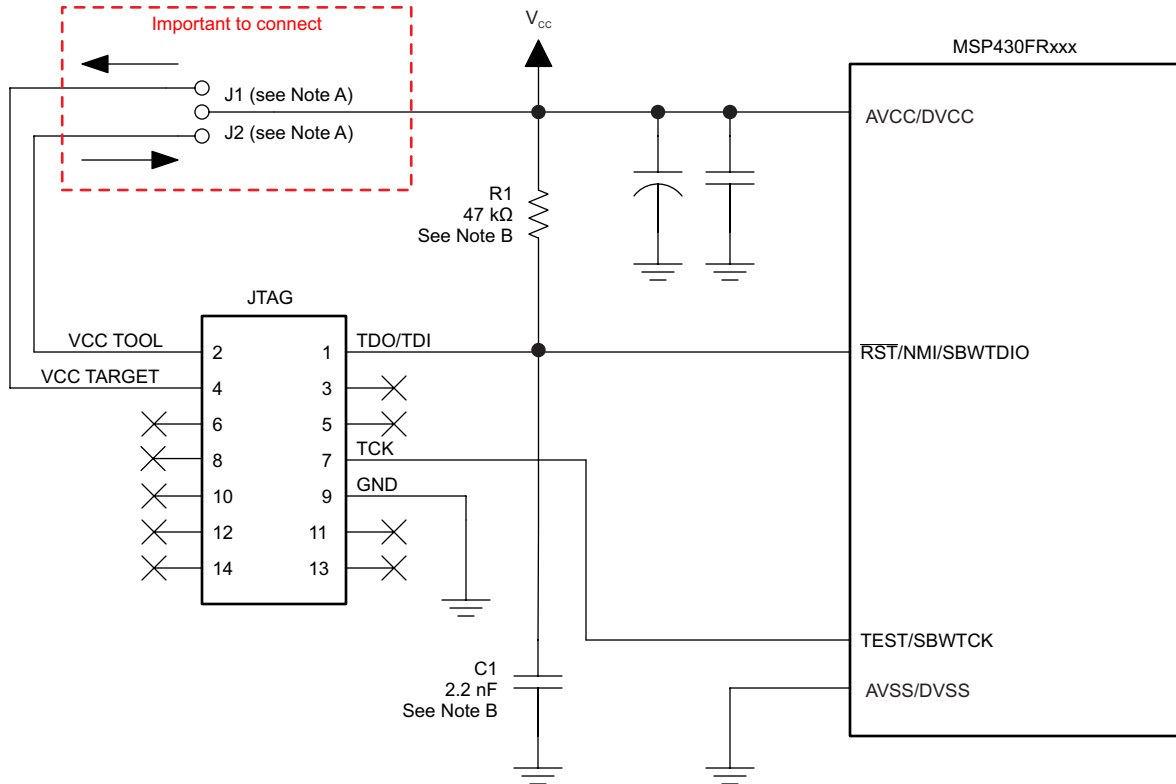
For additional design information regarding the JTAG interface, see the [MSP430 Hardware Tools User's Guide](#).



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- If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- The upper limit for C1 is 2.2 nF when using current TI tools.

图 7-8. Signal Connections for 4-Wire JTAG Communication



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- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device $\overline{\text{RST}}/\text{NMI}/\text{SBWDIO}$ pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

图 7-9. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.7 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the SFRRPCR register.

In reset mode, the $\overline{\text{RST}}/\text{NMI}$ pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}/\text{NMI}$ pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}/\text{NMI}$ pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}/\text{NMI}$ pin is unused, either select and enable the internal pullup or connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}/\text{NMI}$ pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the [MSP430FR58xx](#), [MSP430FR59xx](#), and [MSP430FR6xx Family User's Guide](#) for more information on the referenced control registers and bits.

7.1.8 Unused Pins

For details on the connection of unused pins, see 节 4.6.

7.1.9 General Layout Recommendations

- Use proper grounding and short traces for the external crystal to reduce parasitic capacitance. See [MSP430 32-kHz Crystal Oscillators](#) for recommended layout guidelines.
- Place the proper bypass capacitors on DVCC, AVCC, and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals (for example, PWM or JTAG signals) away from the oscillator circuit.
- Design for proper ESD level protection to protect the device from unintended high-voltage electrostatic discharge. See [MSP430 System-Level ESD Considerations](#) for guidelines.

7.1.10 Do's and Don'ts

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in . Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC12_B Peripheral

7.2.1.1 Partial Schematic

图 7-10 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the $I_{O(VREF+)}$ specification of the REF module.

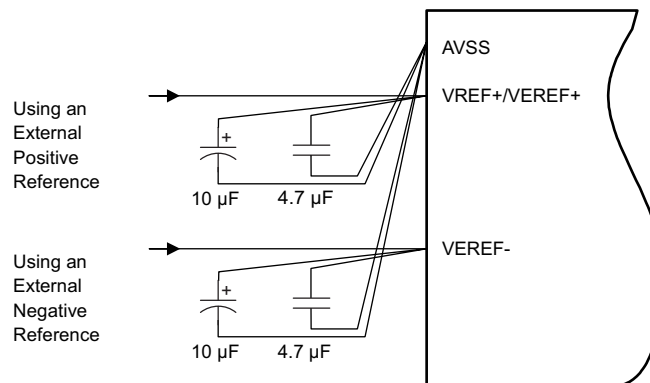


图 7-10. ADC12_B Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, follow appropriate PCB layout and grounding techniques to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in 节 7.1.1 combined with the connections shown in 节 7.2.1.1 prevent these offsets.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10- μ F capacitor buffers the reference pin and filters low-frequency ripple. A 4.7- μ F bypass capacitor filters out high-frequency noise.

7.2.1.3 Detailed Design Procedure

For additional design information, see the application report [Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC](#).

7.2.1.4 Layout Guidelines

Component that are shown in the partial schematic (see [图 7-10](#)) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12_B, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

7.2.2 LCD_C Peripheral

7.2.2.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and whether the on-chip charge pump is employed. Also, there is a fair amount of flexibility as to how the segment (Sx) and common (COMx) signals are connected to the MCU which can provide unique benefits. Since LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However, for examples and how-to circuit-design guidance, see [Designing With MSP430™ MCUs and Segment LCDs](#).

7.2.2.2 Design Requirements

Due to the flexibility of the LCD_C peripheral module to accommodate various segment-based LCDs, selecting the right display for the application in combination with determining specific design requirements is often an iterative process. TI strongly recommends reviewing the LCD_C peripheral module chapter in the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#) and [Designing With MSP430™ MCUs and Segment LCDs](#) during the initial design requirements and decision process.

7.2.2.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD_C peripheral module and the display itself. Two basic design processes can be employed for this step, although in reality often a balanced co-design approach is recommended:

- PCB layout-driven design, optimizing signal routing
- Software-driven design, focusing on optimizing computational overhead

For a detailed discussion of the design procedure as well as for design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, see [Designing With MSP430™ MCUs and Segment LCDs](#) and the LCD_C Controller chapter in the [MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide](#).

7.2.2.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP pin should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace and also have a solid connection to the ground plane that is supplying the VSS pins of the MCU.

For an example layouts and a more in-depth discussion of this topic, see [Designing With MSP430™ MCUs and Segment LCDs](#).

8 器件和文档支持

8.1 入门和后续步骤

有关 MSP 系列微控制器以及有助于开发的工具和库的更多信息，请访问 [MSP430 概述页面](#)。

8.2 器件命名规则

为了标示产品开发周期所处的阶段，TI 为所有 MSP MCU 器件的部件号分配了前缀。每个 MSP MCU 商用系列产品成员都具有以下两个前缀之一：MSP 或 XMS。这些前缀代表了产品开发的发展阶段，即从工程原型 (XMS) 直到完全合格的生产器件 (MSP)。

XMS - 实验器件，不一定代表最终器件的电气规格

MSP - 完全合格的生产器件

XMS 器件在供货时附带如下免责声明：

“开发中的产品用于内部评估用途。”

MSP 器件的特性已经全部明确，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书对该器件适用。

预测显示原型器件 (XMS) 的故障率大于标准生产器件。由于这些器件的预计最终使用故障率尚不确定，德州仪器 (TI) 建议不要将它们用于任何生产系统。请仅使用合格的生产器件。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。此后缀表示温度范围、封装类型和配送形式。图 8-1 提供了解读完整器件名称的图例。

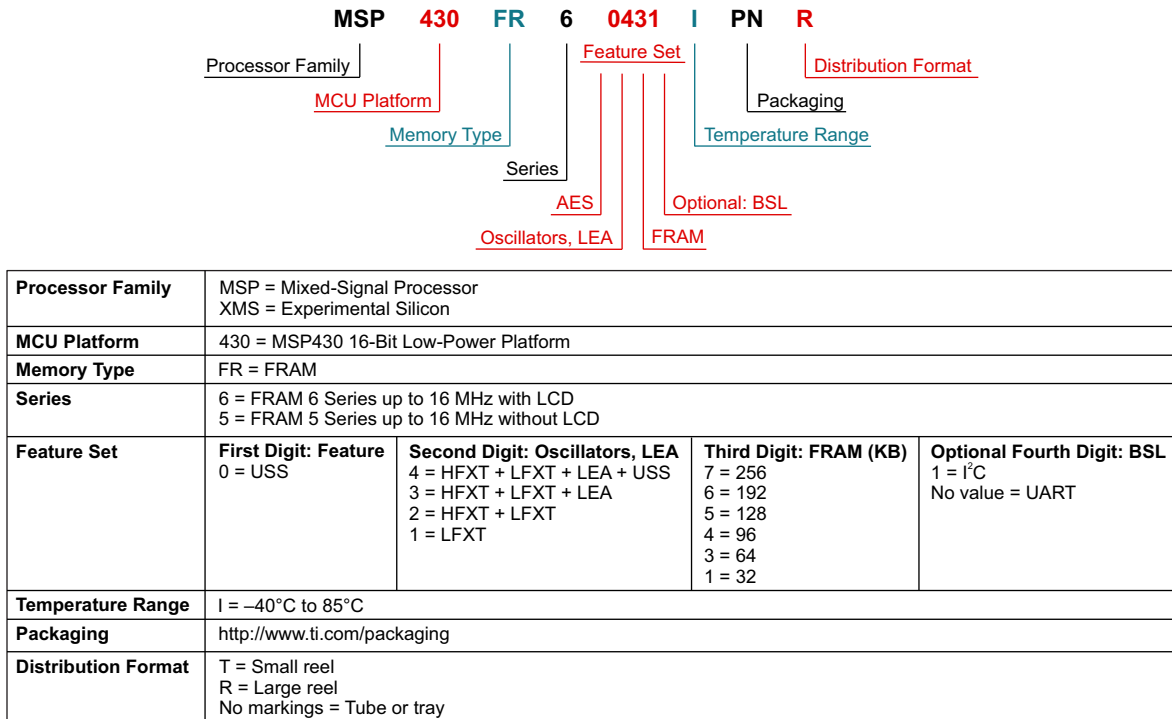


图 8-1. 器件命名规则

8.3 工具和软件

表 8-1 列出 调试 的调试功能。

有关可用 功能的详细信息，请参阅《适用于 MSP430 的 Code Composer Studio IDE 用户指南》。

有关详细使用信息，请参阅以下应用报告：

《使用 Code Composer Studio 与增强型仿真模块 (EEM) 进行高级调试》

《MSP430™ 高级功耗优化：ULP Advisor™ 和 EnergyTrace™ 技术》

表 8-1. 硬件 特性

MSP 架构	4 线 JTAG	两线制 JTAG	断点 (N)	范围断点	时钟控制	状态序列发生器	跟踪缓冲器	LPMx.5 调试支持	EnergyTrace++™
MSP430xv2	有	有	3	有	是	否	否	有	有

设计套件与评估模块

EVM430-FR6043 EVM430-FR6043 是一款开发平台，可用于在超声波传感应用中评估 MSP430FR6043 MCU 的性能。

MSP-TS430PN80C MSP-TS430PN80C 是一款独立的 80 引脚 ZIF 插座目标板，用于通过 JTAG 接口或 Spy Bi-Wire (2 线 JTAG) 协议对 MSP430 MCU 系统内置器件进行编程和调试。

适用于气流测量的超声波传感子系统参考设计 此参考设计可帮助设计人员使用集成的超声波传感解决方案 (USS) 模块开发超声波气体计量子系统，从而提供卓越的计量性能、低功耗和最大集成度。

软件

MSP430Ware™ 软件 MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

MSP430FR604x、MSP430FR504x 代码示例 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

MSP 驱动程序库 MSP 驱动程序库的抽象 API 提供易用的函数调用，无需直接操纵 MSP430 硬件的位与字节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可以使用驱动程序库功能，以最低开销编写完整项目。

MSP EnergyTrace™ 技术 适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，适用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

ULP (超低功耗) Advisor ULP Advisor™ 软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP430 和 MSP432 微控制器 独特 的超低 功耗™ 特性。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地减少应用程序的能耗。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

适用于 MSP 超低功耗微控制器的 FRAM 嵌入式软件实用程序 FRAM 实用程序旨在作为不断扩充的嵌入式软件实用程序集合，其中的实用程序充分利用 FRAM 的超低功耗和近乎无限次的写入寿命。这些实用程序适用于 MSP430FRxx FRAM 微控制器并提供示例代码协助应用程序开发。其中的实用程序包含功耗计算实用程序 (CTPL)。CTPL 是一套实用程序 API 集，通过 CTPL 能够轻松使用 LPMx.5 低功耗模式以及强大的关断模式，允许应用程序在检测到功率损耗时节约能耗并恢复关键的系统元件。

IEC60730 软件包 IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010 (家用及类似用途的自动化电气控制 - 第 1 部分：一般要求) B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 MCU 中 运行的客户应用，从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

适用于 MSP 的定点数学库 MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时 应用，而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 MSP430 的浮点数学运算库 TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。此标量函数的浮点数学运算库，能够充分利用器件的智能外设，使速度最高达到标准 MSP430 数学函数的 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio IDE 和 IAR Embedded Workbench IDE 中。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境 Code Composer Studio (CCS) 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。CCS 包含一整套用于开发和调试嵌入式应用的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种功能。

IAR Embedded Workbench® IDE 适用于 MSP430 MCU 的 IAR Embedded Workbench IDE 是一套用于构建和调试基于 MSP430 微控制器的嵌入式应用的完整 C/C++ 编译器工具链。该调试器可用于源代码和反汇编代码，而且支持复杂代码和数据断点。它还提供了硬件仿真器，可在未连接实际目标的情况下进行调试。

Uniflash 独立闪存工具 CCS Uniflash 是一个独立的工具，用于在 TI MCU 上对片上闪存进行编程。Uniflash 具有 GUI、命令行和脚本界面。Uniflash 软件工具支持两种使用方式：TI 云工具或者从 TI 网页下载的桌面应用。

MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

MSP-GANG 生产编程器 MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

TIREX Resource Explorer (TIRex) 用于查找器件和开发板的示例、库、可执行代码和文档的在线门户。您可以直接在 Code Composer Studio IDE 内访问 TIRex，也可以在“TI 云工具”中访问 TIRex。

TI 云工具 快速在 dev.ti.com 上开始开发。首先使用 Resource Explorer 界面快速找到您需要的所有文件。然后使用行业领先的 Code Composer Studio Cloud IDE 在云中编辑、生成和调试嵌入式应用。

GCC - 适用于 MSP 的编译器 MSP430 和 MSP432 GCC 开源包是一个完整的调试器和开源 C/C++ 编译器工具链，用于基于 MSP430 和 MSP432 微控制器构建和调试嵌入式应用。这些免费的 GCC 编译器支持所有 MSP430 和 MSP432 器件且没有代码大小限制。此外，这些编译器可以通过命令行独立使用，也可在 Code Composer Studio v6.0 或更高版本中使用。不管您使用的是 Windows®、Linux® 还是 OS X® 环境，马上开始吧。

8.4 文档支持

以下文档介绍了 MSP430FR6043 MCU。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 8.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《MSP430FR6043 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR60431 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR6041 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5043 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR50431 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5041 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

用户指南

《MSP430FR58xx、MSP430FR59xx 和 MSP430FR6xx 系列用户指南》 该器件系列提供的所有模块和外设的详细说明。

《MSP430 FRAM 器件引导加载程序 (BSL) 用户指南》 MSP430 MCU 上的引导加载程序 (BSL) 允许用户在原型设计、投产和维护等各阶段与 MSP430 MCU 中的嵌入式存储器进行通信。可编程存储器 (FRAM 存储器) 和数据存储器 (RAM) 均可按要求予以修改。

《通过 JTAG 接口对 MSP430 进行编程》 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。

《MSP430 硬件工具用户指南》 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

《MSP430 32kHz 晶体振荡器》 选择合适的晶体、正确的负载电路和适当的电路板布局是实现稳定的晶体振荡器的关键。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

《MSP430 系统级 ESD 注意事项》 随着硅晶技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了三个不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。另外还介绍了若干实际应用系统级 ESD 保护设计示例及其结果。

8.5 相关链接

表 8-2 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具与软件，以及立即订购快速访问。

表 8-2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
MSP430FR6043	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR60431	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR6041	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5043	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR50431	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5041	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

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Linux is a registered trademark of Linus Torvalds.

Windows is a registered trademark of Microsoft Corporation.

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8.9 Export Control Notice

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9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR5041IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5041	Samples
MSP430FR5041IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5041	Samples
MSP430FR5041IRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5041	Samples
MSP430FR5041IRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5041	Samples
MSP430FR50431IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR50431	Samples
MSP430FR50431IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR50431	Samples
MSP430FR50431IRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR50431	Samples
MSP430FR50431IRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR50431	Samples
MSP430FR5043IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5043	Samples
MSP430FR5043IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5043	Samples
MSP430FR5043IRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5043	Samples
MSP430FR5043IRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5043	Samples
MSP430FR6041IPN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6041	Samples
MSP430FR6041IPNR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6041	Samples
MSP430FR60431IPN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60431	Samples
MSP430FR60431IPNR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60431	Samples
MSP430FR6043IPN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6043	Samples
MSP430FR6043IPNR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6043	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

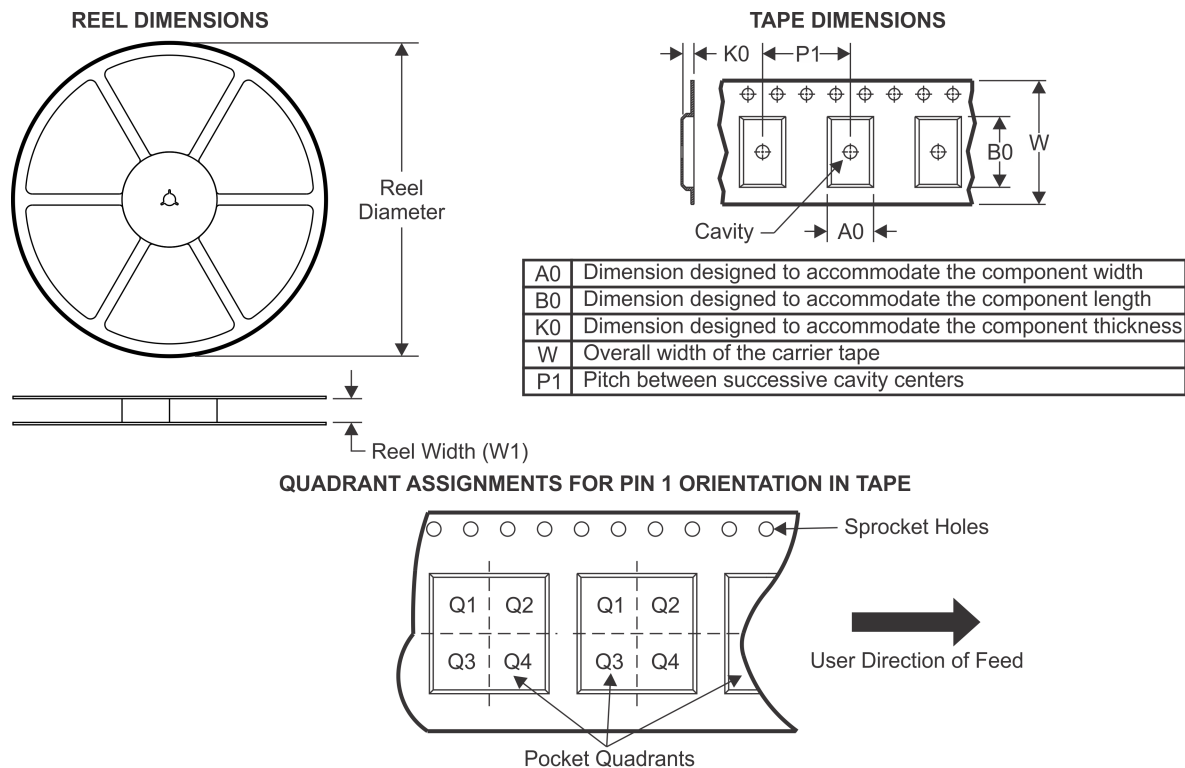
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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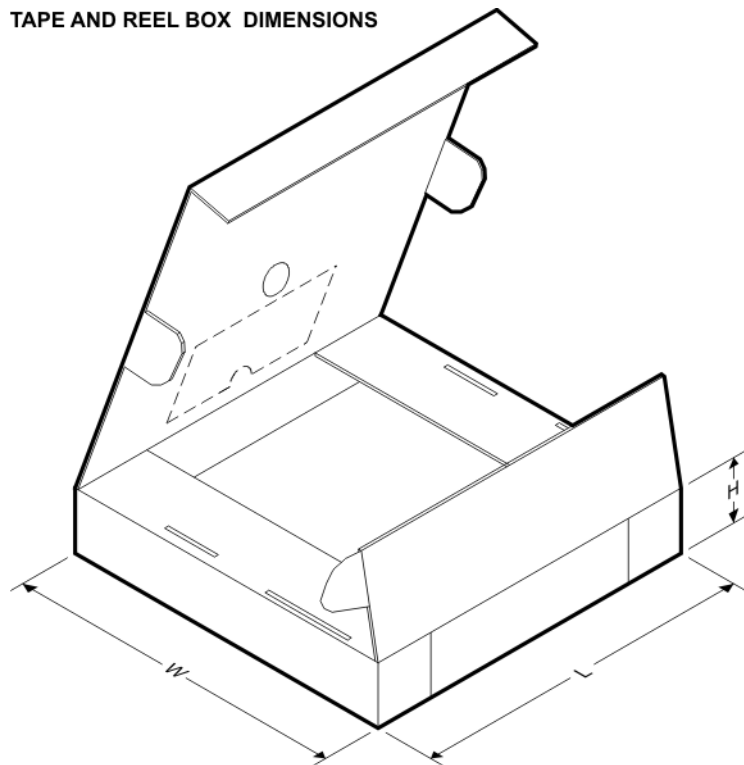
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TAPE AND REEL INFORMATION


*All dimensions are nominal

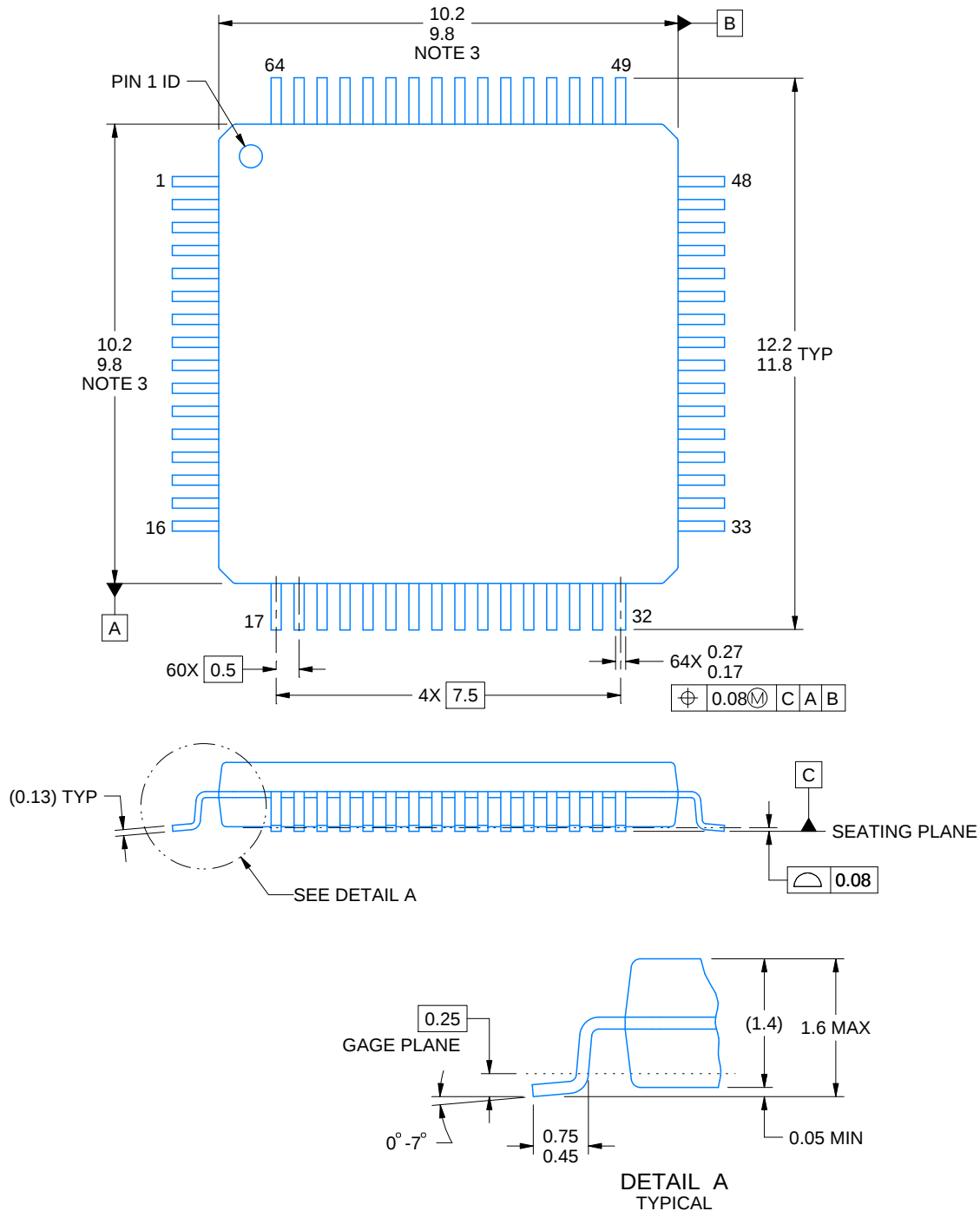
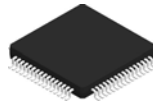
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR5041IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR5041IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR5041IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR50431IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR50431IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR50431IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR5043IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR5043IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR5043IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR6043IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR5041IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR5041IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR5041IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430FR50431IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR50431IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR50431IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430FR5043IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR5043IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR5043IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430FR6043IPNR	LQFP	PN	80	1000	350.0	350.0	43.0



4215162/A 03/2017

NOTES:

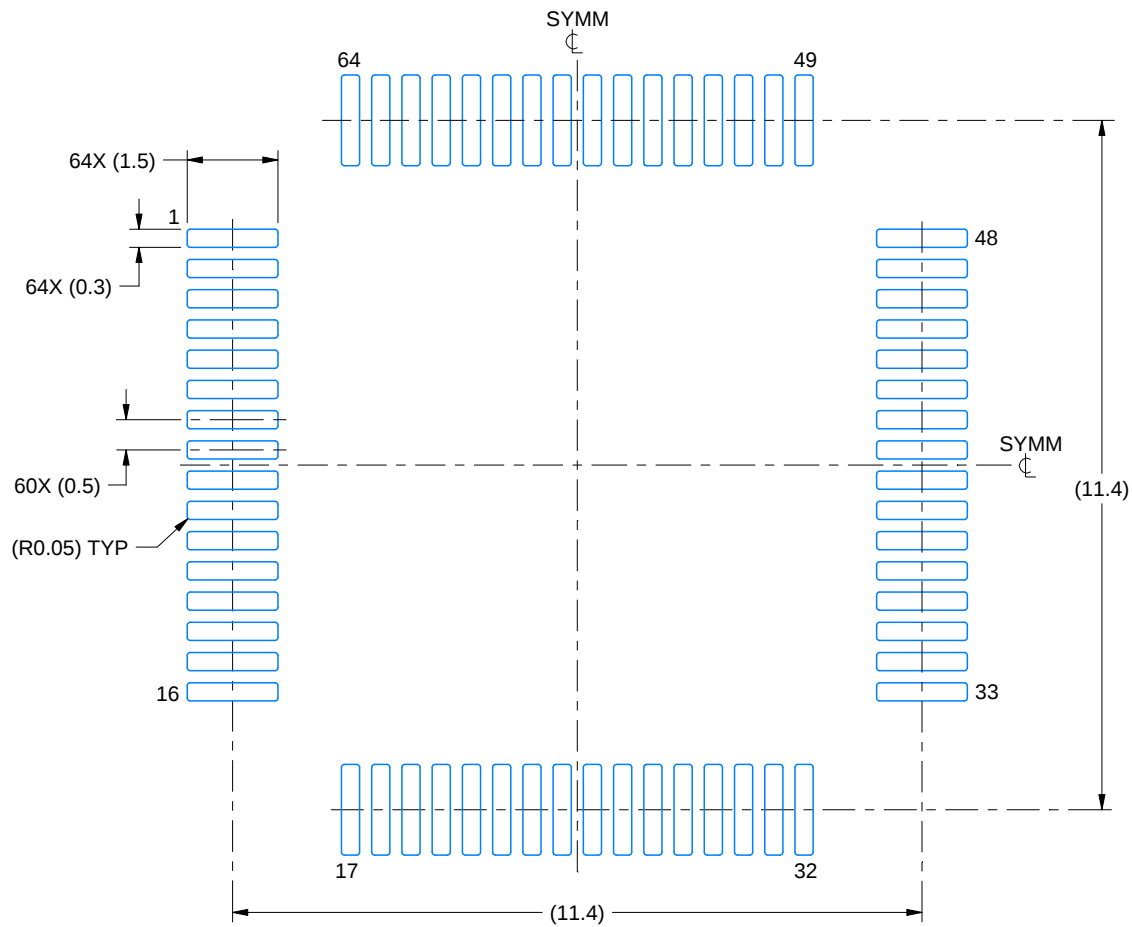
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

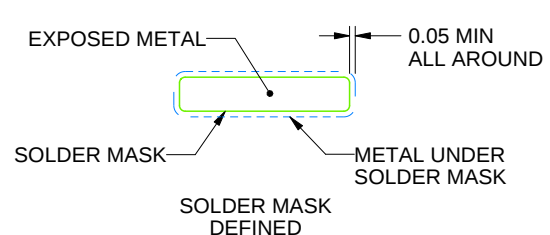
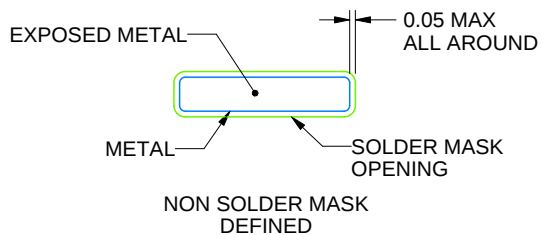
PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

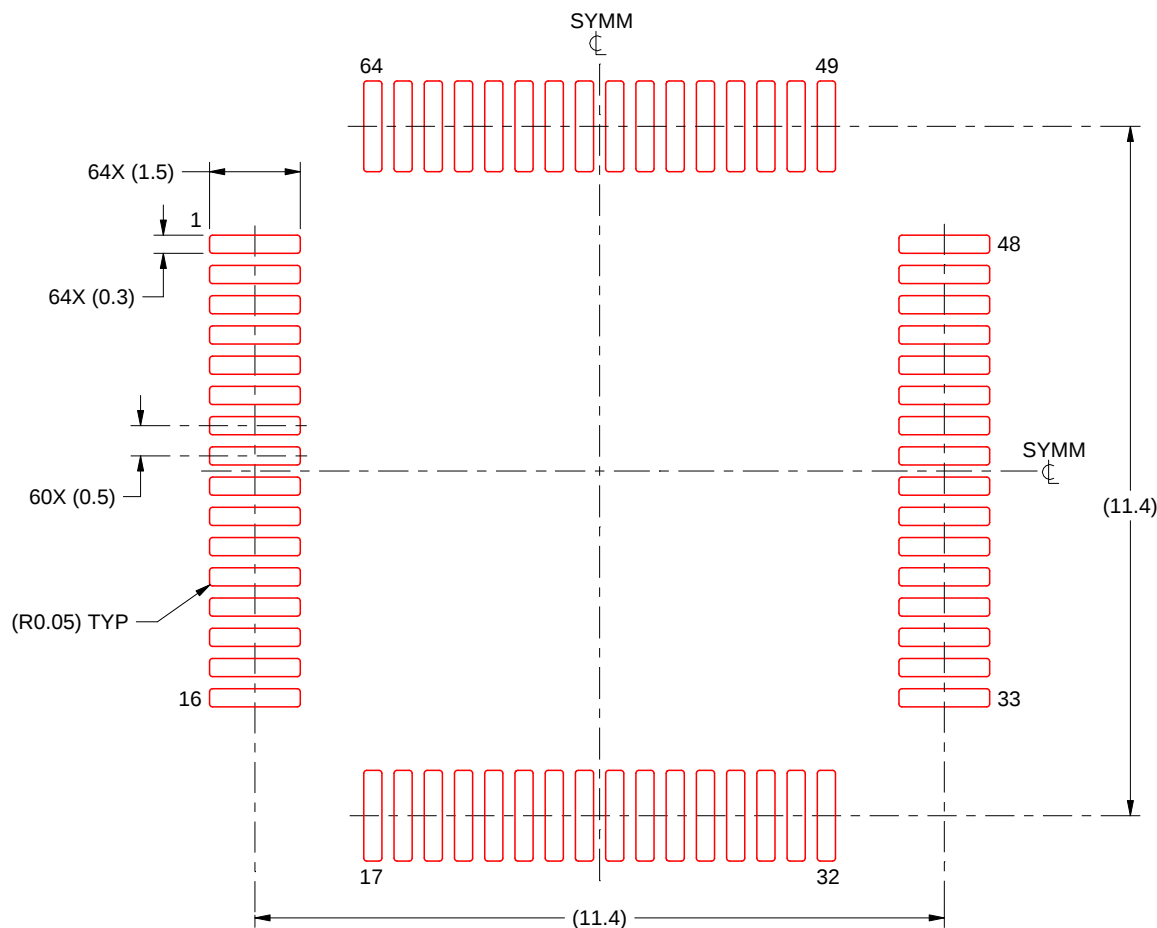
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

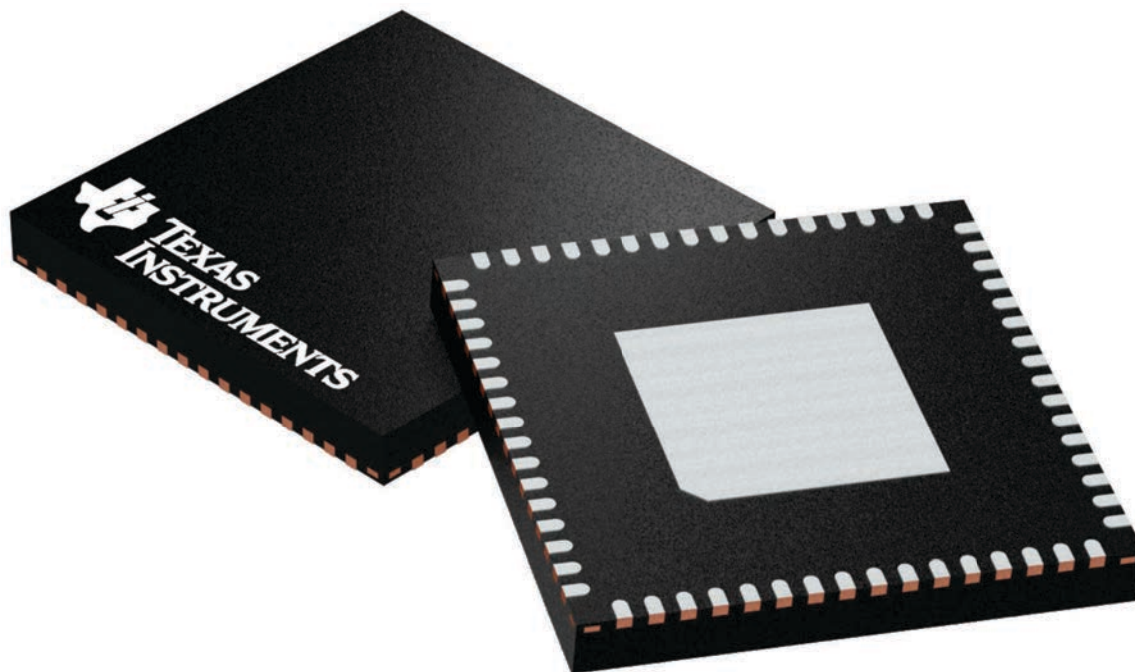
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

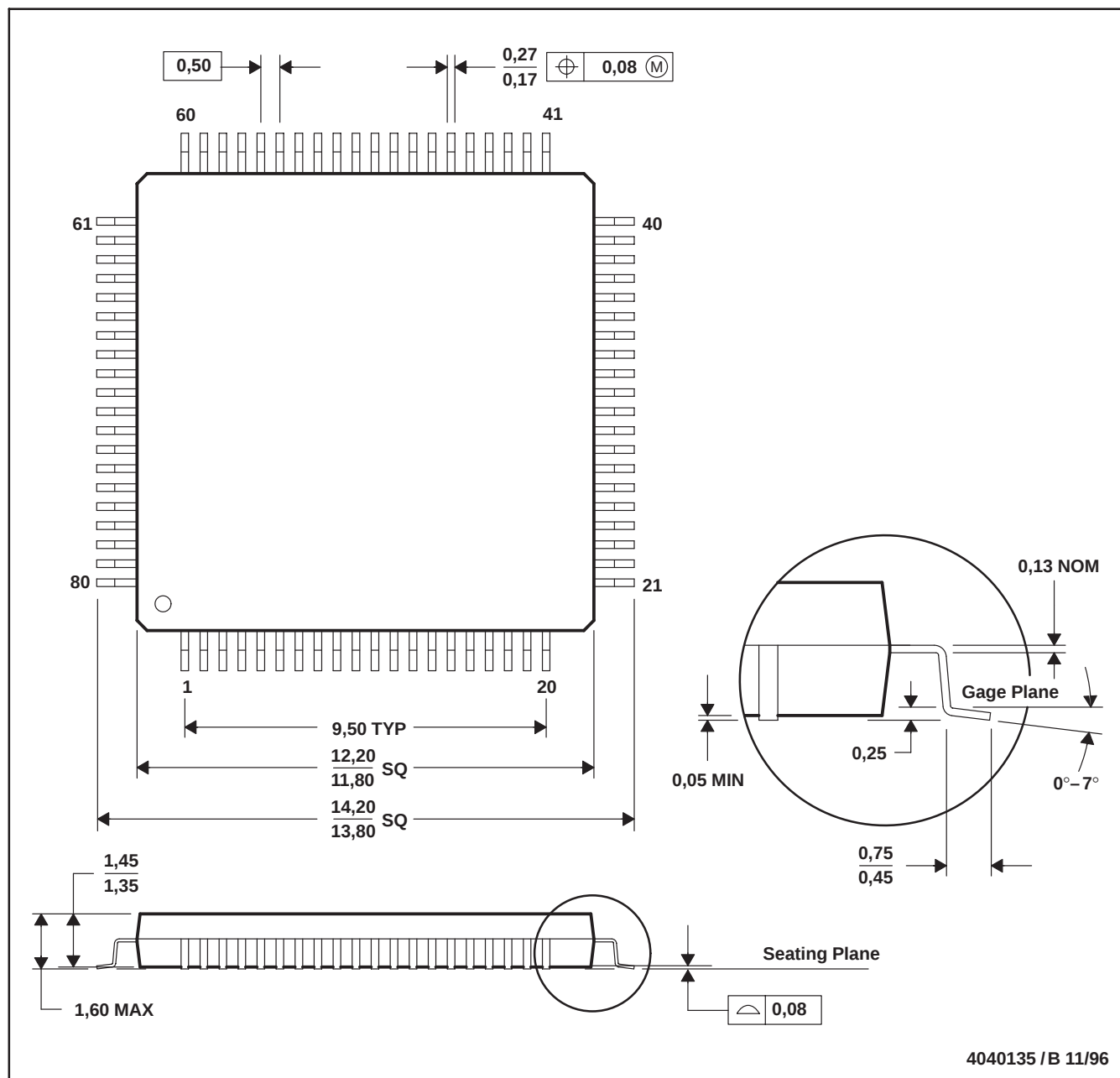


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

PN (S-PQFP-G80)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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