混合信号微控制器

特性

- 低电源电压范围: **1.8 V** 至 **3.6 V**
- 超低功耗
  - 运行模式： **220 µA** （在 **1 MHz** 频率和 **2.2 V** 电压条件下）
  - 待机模式： **0.5 µA**
  - 关闭模式 （**RAM** 保持）： **0.1 µA**
- **5** 种节能模式
- 可在不到 **1 µs** 的时间里超快速地从待机模式唤醒
- **16** 位 **RISC** 架构、**62.5-ns** 指令周期时间
- 基本时钟模块配置
  - 高达 **16 MHz** 的内部频率并具有**4** 种浮动范围在 **±1%** 之内的校准频率
  - 内部超低功耗低频振荡器
- 具有 **2** 个捕捉**/**比较寄存器的 **16** 位 **Timer_A**
- 用于模拟信号比较功能或者斜率模数 **(A/D)** 转换的片载比较器 （只适用于 **MSP430G2210**）
- **10** 位 **200-ksps** 具有内部基准、取样保持、和自动扫描的模数 **(A/D)** 转换器 （只适用于 **MSP430G2230**）
- 支持 **SPI** 和 **I2C** 的通用串行接口 **(USI) (**仅适用于 **MSP430G2230)**
- 欠压检测器
- 串行板上编程时，无需外部编程电压，由安全熔丝 **(Security Fuse)** 对可编程代码进行保护
- 具有两线制 **(Spy-Bi-Wire)** 接口的片上仿真逻辑电路
- 系列成员：
  - **MSP430G22x0**
    - **2KB + 256B** 闪存
    - **128B RAM**
- 采用 **8** 引脚塑料封装 **(D)**
- 要获得完整的模块说明， 请参见 ***MSP430x2xx*** *系列产品用户指南* **(SLAU144)**

说明

德州仪器公司 MSP430™ 系列超低功率微控制器包含几个器件，这些器件特有针对多种应用的不同的外设集。 这种架构与 5 种低功耗模式相组合，专为在便携式测量应用中延长电池使用寿命而优化。 该器件具有一个强大的 16 位 RISC CPU、16 位寄存器和有助于获得最大编码效率的常数发生器。 数字控制振荡器 (DCO) 可在不到 1µs 的时间里完成从低功耗模式至运行模式的唤醒。

MSP430G22x0 系列产品是一款超低功率混合信号微控制器，此微控制器装有一个内置的 16 位定时器和 4 个 I/O 引脚。 除此之外， MSP430G2230 还有使用同步协议 （SPI 或者 I2C） 的内置通信功能和一个 10 位 A/D 转换器。 MSP430G2210 装有一个多用途模拟比较器。

表 **1.** 提供的选项[(1)]

T_A	封装的器件[(2)]
	塑料 **8** 引脚 **(D)**
-40°C 至 85°C	MSP430G2230ID MSP430G2210ID

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者登录 TI 的网站 www.ti.com.

(2) 封装图样、热数据和符号可登录 www.ti.com/packaging 获取。

English Data Sheet: SLAS753

Device Pinout and Functional Block Diagram, MSP430G2210

See Application Information for detailed I/O information.

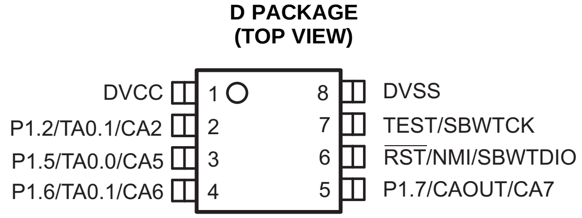


Figure 1. Device Pinout, MSP430G2210

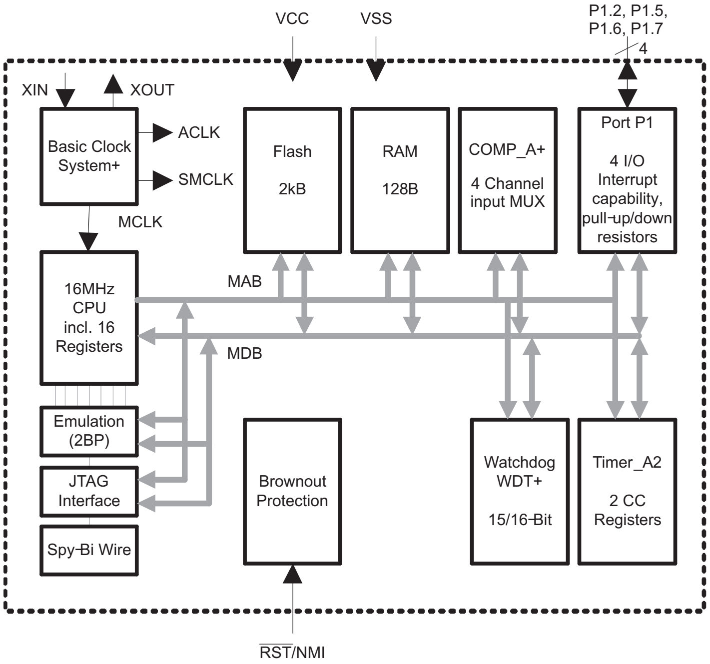


Figure 2. Functional Block Diagram, MSP430G2210

Device Pinout and Functional Block Diagram, MSP430G2230

See Application Information for detailed I/O information.

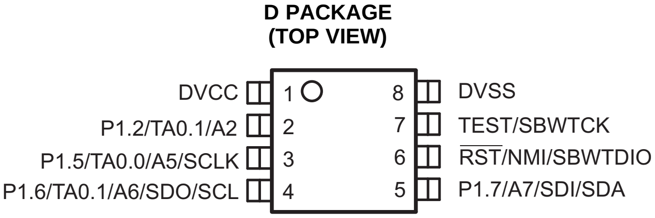


Figure 3. Device Pinout, MSP430G2230

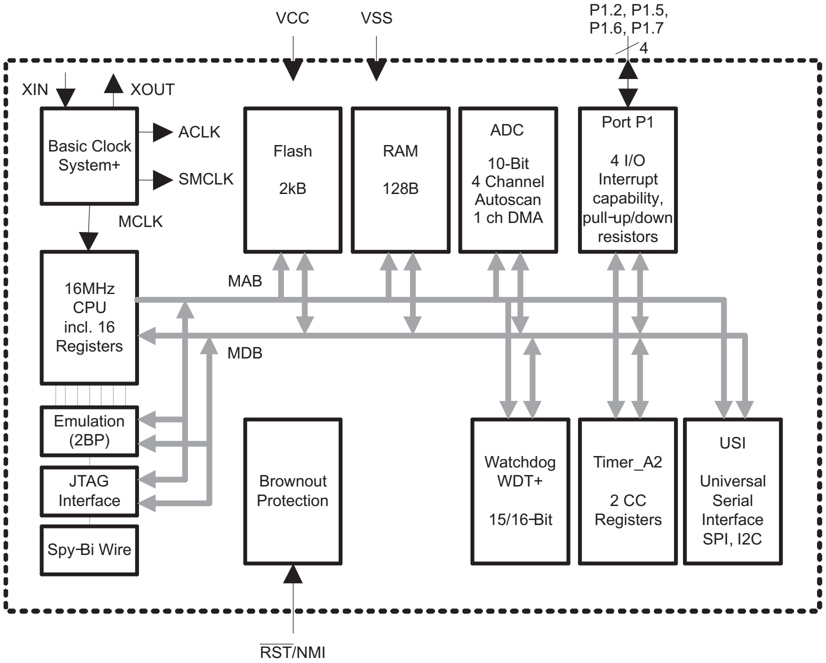


Figure 4. Functional Block Diagram, MSP430G2230

Table 2. Terminal Functions, MSP430G2210[1]

TERMINAL			DESCRIPTION
NAME	NO. D	I/O	
P1.2/ TA0.1/ CA2	2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare Out1 output Comparator_A+, CA2 input
P1.5/ TA0.0/ CA5	3	I/O	General-purpose digital I/O pin Timer_A, compare Out0 output Comparator_A+, CA5 input
P1.6/ TA0.1/ CA6	4	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A+, CA6 input
P1.7/ CAOUT/ CA7	5	I/O	General-purpose digital I/O pin Comparator_A+, output Comparator_A+, CA7 input
RST/ NMI/ SBWTDIO	6	I	Reset input Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	7	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DVCC	1		Digital supply voltage
DVSS	8		Digital ground reference

(1) The GPIOs P1.0, P1.1, P1.3, P1.4, P2.6, and P2.7 are implemented but not available on the device pinout. To avoid floating inputs, these digital I/Os should be properly configured. The pullup or pulldown resistors of the unbounded P1.x GPIOs should be enabled, and the VLO should be selected as the ACLK source (see the *MSP430x2xx Family User's Guide* (SLAU144)).

Table 3. Terminal Functions, MSP430G2230[1]

TERMINAL			DESCRIPTION
NAME	NO. D	I/O	
P1.2/ TA0.1/ A2	2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare Out1 output ADC10 analog input A2
P1.5/ TA0.0/ A5/ SCLK	3	I/O	General-purpose digital I/O pin Timer_A, compare Out0 output ADC10 analog input A5 USI: clock input in I2C mode; clock input/output in SPI mode
P1.6/ TA0.1/ A6/ SDO/ SCL	4	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1B input, compare: Out1 output ADC10 analog input A6 USI: Data output in SPI mode USI: I2C clock in I2C mode
P1.7/ A7/ SDI/ SDA	5	I/O	General-purpose digital I/O pin ADC10 analog input A7 USI: Data input in SPI mode USI: Data input in I2C mode
RST/ NMI/ SBWTDIO	6	I	Reset input Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	7	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DVCC	1		Digital supply voltage
DVSS	8		Digital ground reference

(1) The GPIOs P1.0, P1.1, P1.3, P1.4, P2.6, and P2.7 are implemented but not available on the device pinout. To avoid floating inputs, these digital I/Os should be properly configured. The pullup or pulldown resistors of the unbounded P1.x GPIOs should be enabled, and the VLO should be selected as the ACLK source (see the *MSP430x2xx Family User's Guide* (SLAU144)).

SHORT-FORM DESCRIPTION

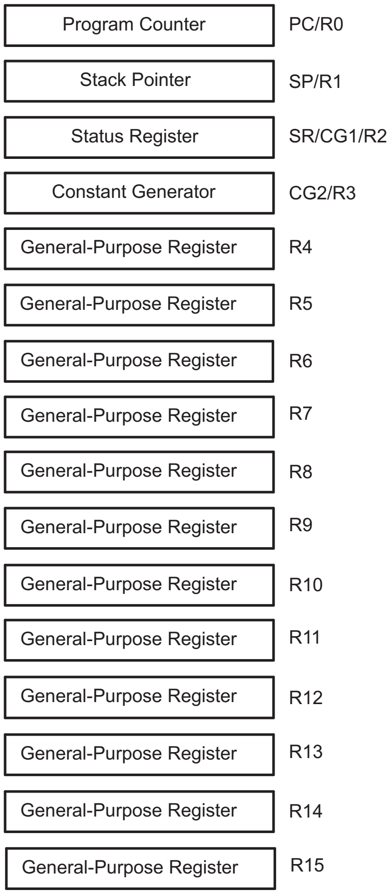
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 4 shows examples of the three types of instruction formats; Table 5 shows the address modes.

Table 4. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 5. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 --> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) --> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0x0FFFF to 0x0FFC0. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0x0FFFE) contains 0x0FFFF (for example, flash is not programmed) the CPU goes into LPM4 immediately after power-up.

Table 6. Interrupt Sources

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0xFFFE	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable, (non)-maskable, (non)-maskable	0xFFFC	30
			0xFFFA	29
			0xFFF8	28
Comparator_A+ (MSP430G2210 Only)	CAIFG (4)		0xFFF6	27
Watchdog Timer+	WDTIFG	maskable	0xFFF4	26
Timer_A2	TACCR0 CCIFG(4)	maskable	0xFFF2	25
Timer_A2	TACCR1 CCIFG, TAIFG(2)(4)	maskable	0xFFF0	24
			0xFFEE	23
			0xFFEC	22
ADC10 (MSP430G2230 Only)	ADC10IFG(4)	maskable	0xFFEA	21
USI (MSP430G2230 Only)	USIIFG, USISTTIFG(2)(4)	maskable	0xFFE8	20
			0xFFE6	19
I/O Port P1(four flags)	P1IFG.2, P1IFG.5, P1IFG.6, and P1IFG.7(2)(4)(5)	maskable	0xFFE4	18
			0xFFE2	17
			0xFFE0	16
See (6)			0xFFDE to 0xFFC0	15 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) All eight interrupt flags P1IFG.0 to P1IFG.7 are implemented while four are connected to pins.
(6) The interrupt vectors at addresses 0xFFDE to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend	**rw:**	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
	▨	SFR bit is not present in device.

Table 7. Interrupt Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
00h	▨	▨	**ACCVIE**	**NMIIE**	▨	▨	**OFIE**	**WDTIE**
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable. Set to 0.
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	▨	▨	▨	▨	▨	▨	▨	▨

Table 8. Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	▨	▨	▨	**NMIIFG**	**RSTIFG**	**PORIFG**	**OFIFG**	**WDTIFG**
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-on or a reset condition at the $\overline{\text{RST}}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault. The XIN/XOUT pins are not available as device terminals.
PORIFG	Power-On Reset interrupt flag. Set on V_{CC} power-up.
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{\text{RST}}$/NMI pin in reset mode. Reset on V_{CC} power-up.
NMIIFG	Set by $\overline{\text{RST}}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h	▨	▨	▨	▨	▨	▨	▨	▨

Memory Organization

Table 9. Memory Organization

		MSP430G22x0
Memory Main: interrupt vector Main: code memory	Size Flash Flash	2KB Flash 0xFFFF-0xFFC0 0xFFFF-0xF800
Information memory	Size Flash	256 Byte 0x10FF - 0x1000
RAM	Size	128 Byte 0x027F - 0x0200
Peripherals	16-bit 8-bit 8-bit SFR	0x01FF - 0x0100 0x00FF - 0x0010 0x000F - 0x0000

Flash Memory

The flash memory can be programmed by the Spy-Bi-Wire or JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF (VLOCLK) oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

NOTE

The LFXT1 oscillator is not available. LFXT1Sx bits of the BCSCTL3 register should be configured to use VLOCLK (see the *MSP430x2xx Family User's Guide* (SLAU144)).

Table 10. DCO Calibration Data (Provided From Factory in Flash Information Memory Segment A)

DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh
16 MHz	CALBC1_16MHZ	byte	010F9h
	CALDCO_16MHZ	byte	010F8h

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There are four pins of one 8-bit I/O port implemented—port P1:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the four bits of port P1.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A2

Timer_A2 is a 16-bit timer/counter with two capture/compare registers. Timer_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 11. Timer_A2 Signal Connections - MSP430G2210

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
D					D
-	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
-	TACLK	INCLK			
-	TA0	CCI0A	CCR0	TA0	3 - P1.5
	ACLK (internal)	CCI0B			
	V_{SS}	GND			
	V_{CC}	V_{CC}			
2 - P1.2	TA1	CCI1A	CCR1	TA1	2 - P1.2
	CAOUT (internal)	CCI1B			4 - P1.6
	V_{SS}	GND			
	V_{CC}	V_{CC}			

Table 12. Timer_A2 Signal Connections - MSP430G2230

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
D					D
-	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
-	TACLK	INCLK			
-	TA0	CCI0A	CCR0	TA0	
	ACLK (internal)	CCI0B			
	V_{SS}	GND			
	V_{CC}	V_{CC}			
2 - P1.2	TA1	CCI1A	CCR1	TA1	2 - P1.2
4 - P1.6	TA1	CCI1B			4 - P1.6
	V_{SS}	GND			
	V_{CC}	V_{CC}			

USI (MSP430G2230 Only)

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

ADC10 (MSP430G2230 Only)

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

Comparator_A+ (MSP430G2210 Only)

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals

Peripheral File Map

Table 13. Peripherals With Word Access

ADC10 (MSP430G2230 Only)	ADC control 0 ADC10 control 1 ADC memory	ADC10CTL0 ADC10CTL1 ADC10MEM	01B0h 01B2h 01B4h
Timer_A	Capture/compare register Capture/compare register Timer_A register Capture/compare control Capture/compare control Timer_A control Timer_A interrupt vector	TACCR1 TACCR0 TAR TACCTL1 TACCTL0 TACTL TAIV	0174h 0172h 0170h 0164h 0162h 0160h 012Eh
Flash Memory	Flash control 3 Flash control 2 Flash control 1	FCTL3 FCTL2 FCTL1	012Ch 012Ah 0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

Table 14. Peripherals With Byte Access

ADC10 (MSP430G2230 Only)	Analog Enable	ADC10AE	04Ah
USI (MSP430G2230 Only)	USI control 0 USI control 1 USI clock control USI bit counter USI shift register	USICTL0 USICTL1 USICKCTL USICNT USISR	078h 079h 07Ah 07Bh 07Ch
Comparator_A+ (MSP430G2210 Only)	Comparator_A+ port disable Comparator_A+ control 2 Comparator_A+ control 1	CAPD CACTL2 CACTL1	05Bh 05Ah 059h
Basic Clock System+	Basic clock system control 3 Basic clock system control 2 Basic clock system control 1 DCO clock frequency control	BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL	053h 058h 057h 056h
Port P1	Port P1 resistor enable Port P1 selection Port P1 interrupt enable Port P1 interrupt edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input	P1REN P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	027h 026h 025h 024h 023h 022h 021h 020h
Special Function	SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1	IFG2 IFG1 IE2 IE1	003h 002h 001h 000h

Absolute Maximum Ratings[1]

	Voltage applied at V_{CC} to V_{SS}		-0.3 V to 4.1 V
	Voltage applied to any pin[2]		-0.3 V to V_{CC} + 0.3 V
	Diode current at any device terminal		±2 mA
T_{stg}	Storage temperature[3]	Unprogrammed device	-55°C to 150°C
		Programmed device	-40°C to 150°C

[1] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

[3] Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

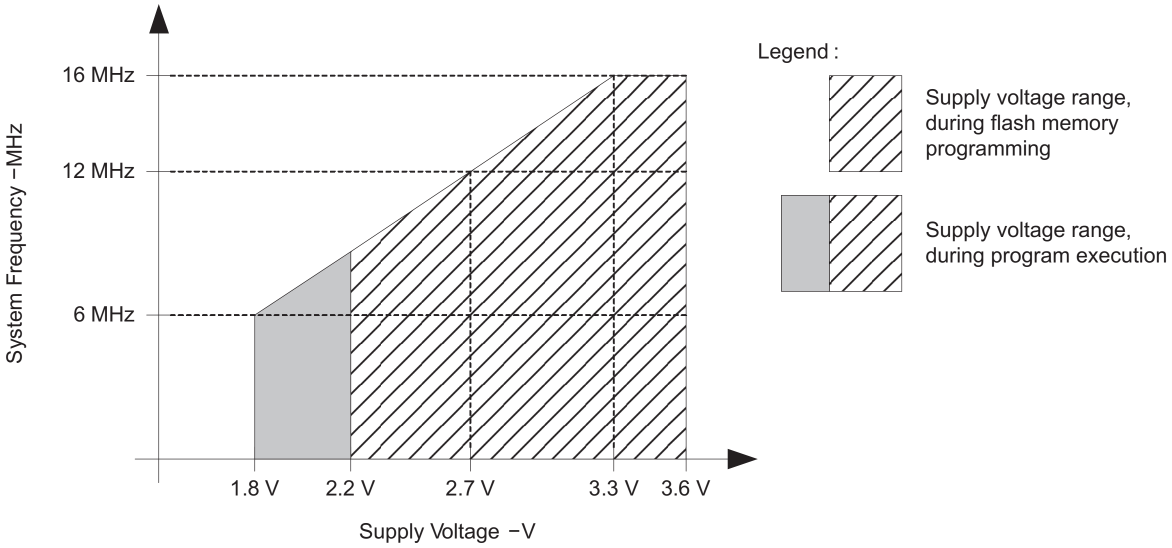
Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution	1.8		3.6	V
		During flash program or erase	2.2		3.6	
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature		-40		85	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)[1][2]	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc		12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ± 10%	dc		16	

[1] The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.

[2] Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 5. Safe Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 0 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		220		µA
				3 V		300	370	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.

Typical Characteristics – Active Mode Supply Current (Into V_{CC})

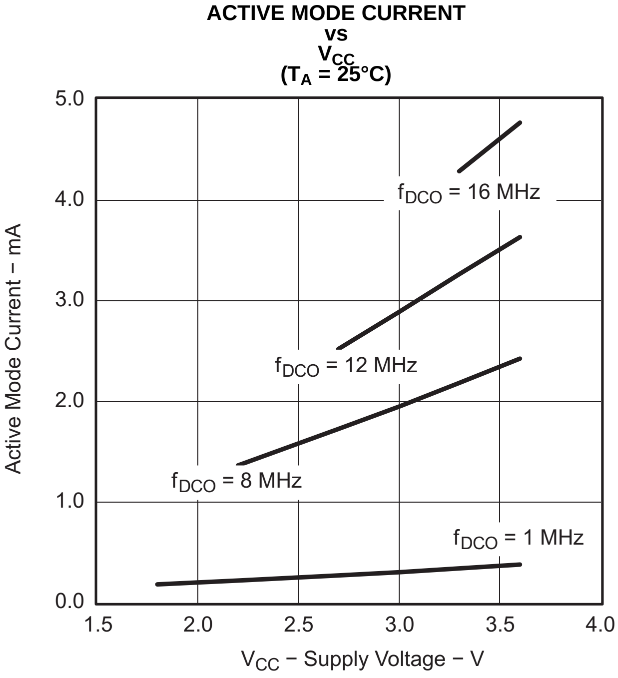


Figure 6.

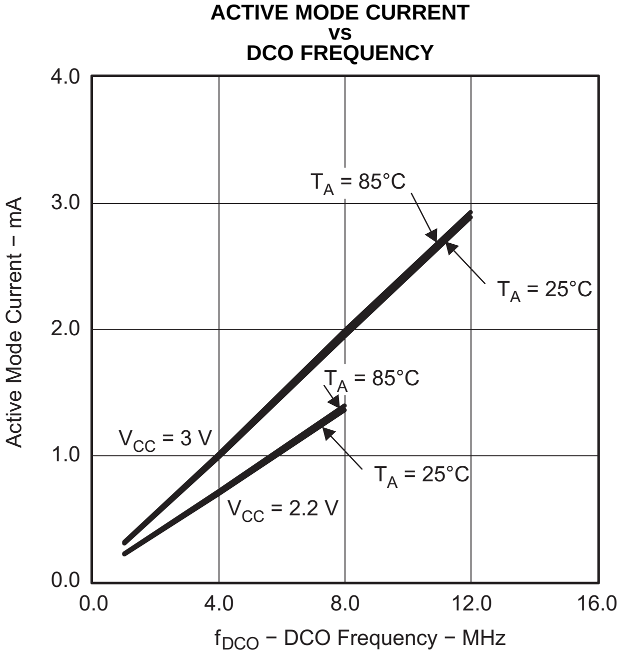


Figure 7.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current[2]	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		65		µA
I_{LPM2}	Low-power mode 2 (LPM2) current[3]	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22	29	µA
$I_{LPM3,VLO}$	Low-power mode 3 (LPM3) current[3]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	0.7	µA
I_{LPM4}	Low-power mode 4 (LPM4) current[4]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	0.5	µA
			85°C			0.8	1.5	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for brownout and WDT clocked by SMCLK included.
(3) Current for brownout and WDT clocked by ACLK included.
(4) Current for brownout included.

Schmitt-Trigger Inputs (Port P1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})		3 V	0.3		1.0	V
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

Leakage Current (Port P1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	/3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs (Port P1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = -6 mA (1)	3 V	V_{CC} - 0.6		V_{CC}	V
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 6 mA (1)	3 V	V_{SS}		V_{SS} + 0.6	V

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Port P1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	C_L = 20 pF, R_L = 1 kΩ (1) (2)	3 V			12	MHz
$f_{Port°CLK}$	Clock output frequency	C_L = 20 pF (2)	3 V			16	MHz

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

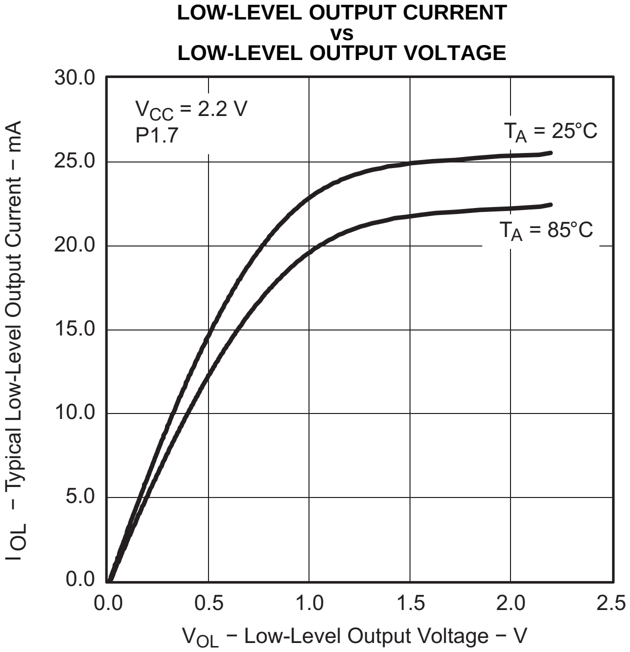


Figure 8.

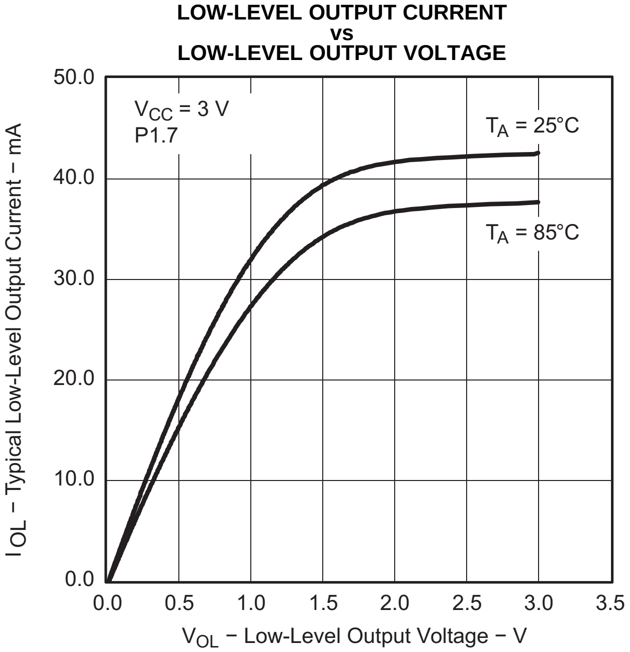


Figure 9.

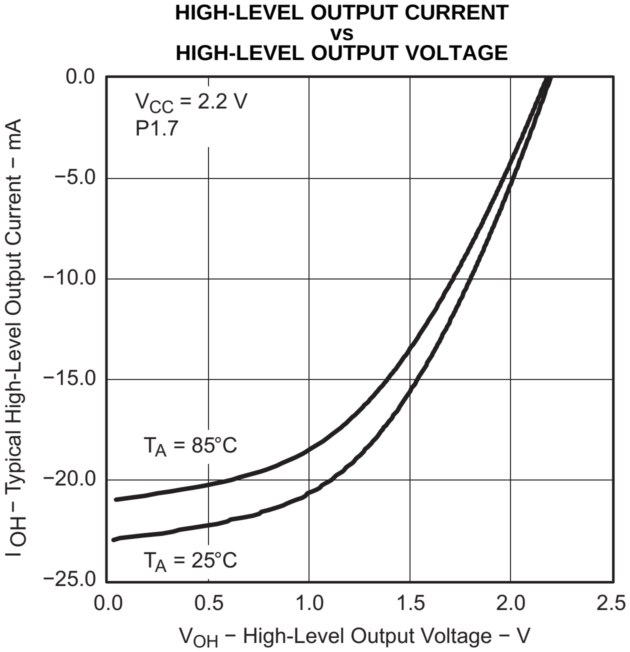


Figure 10.

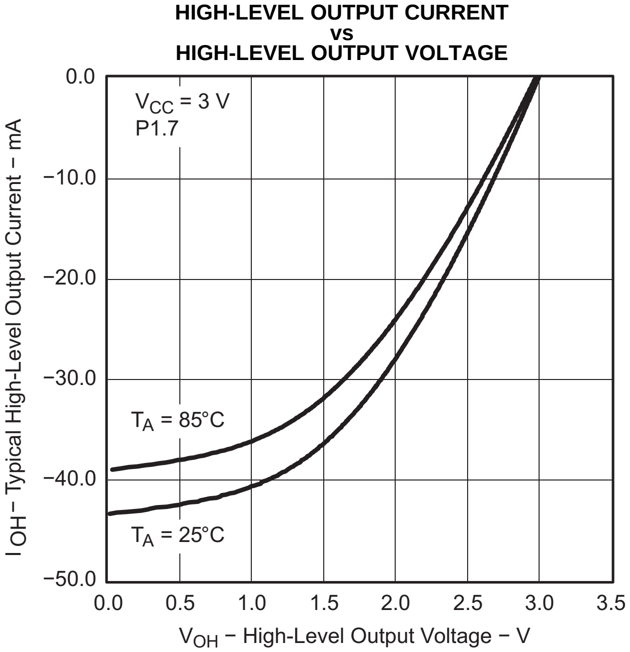


Figure 11.

POR and BOR[1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 12	$dV_{CC}/dt \leq 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 12 through Figure 14	$dV_{CC}/dt \leq 3$ V/s			1.35	1	V
$V_{hys(B\_IT-)}$	See Figure 12	$dV_{CC}/dt \leq 3$ V/s			140		mV
$t_{d(BOR)}$	See Figure 12					2000	µs
$t_{(reset)}$	Pulse duration needed at $\overline{RST}$/NMI pin to accept reset internally		3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

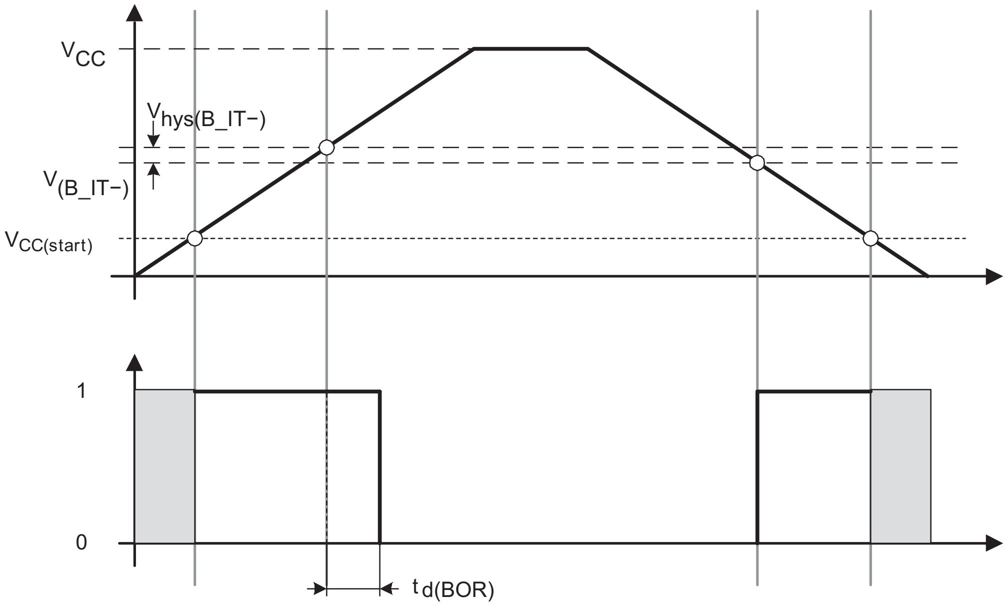


Figure 12. POR and BOR vs Supply Voltage

Typical Characteristics – POR and BOR

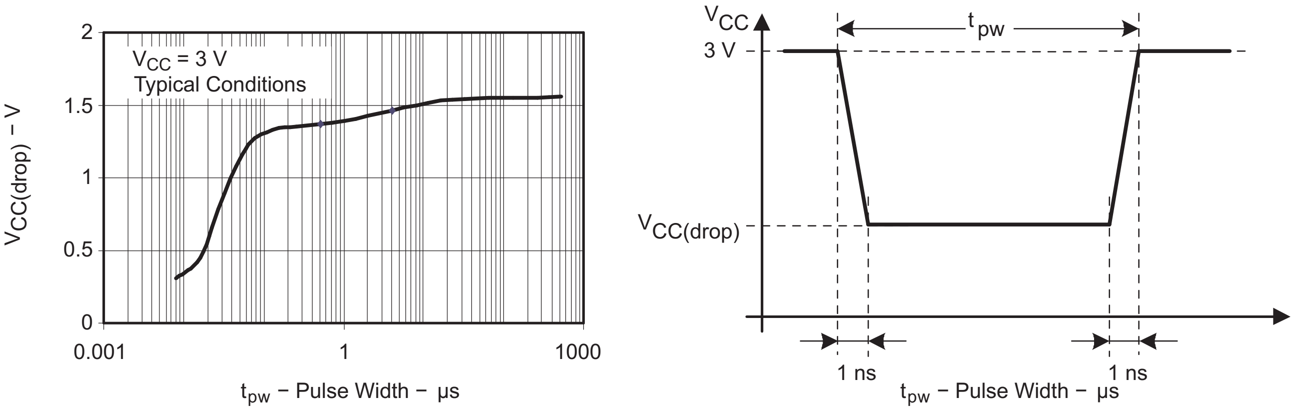


Figure 13. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR or BOR Signal

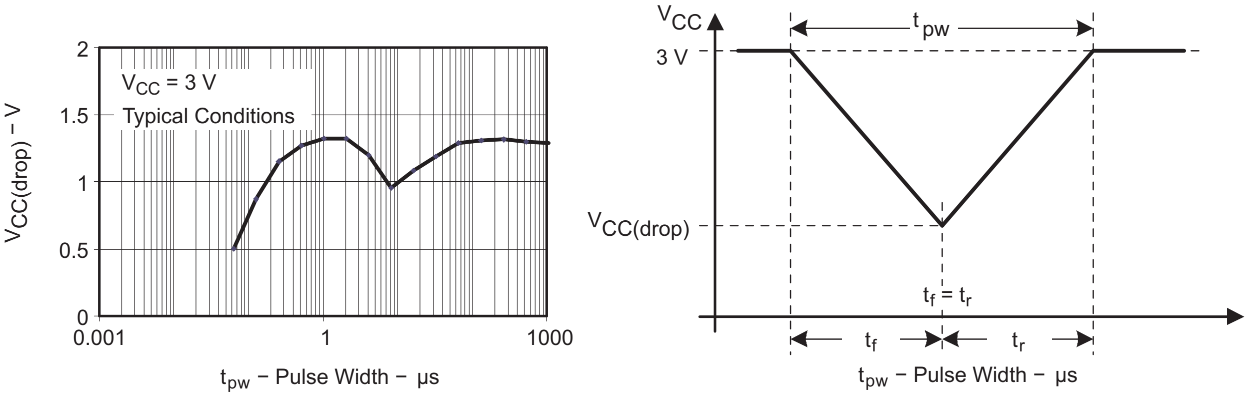


Figure 14. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3 V		0.12		MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3 V		0.15		MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3 V		0.21		MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3 V		0.30		MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3 V		0.41		MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3 V		0.58		MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3 V		0.80		MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3 V		1.6		MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3 V		2.3		MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3 V		3.4		MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3 V		4.25		MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3 V	4.3		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3 V		7.8		MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3 V	8.6		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V		15.25		MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V		21		MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	3 V		1.35		ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	3 V		1.08		ratio
	Duty cycle		3 V		50		%

Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	3	%
8-MHz tolerance over temperature	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±1.0	3	%
12-MHz tolerance over temperature	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±1.0	3	%
16-MHz tolerance over temperature	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±2.0	3	%

Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	25°C	1.8 V to 3.6 V	-3	±2	+3	%
8-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	25°C	1.8 V to 3.6 V	-3	±2	+3	%
12-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	25°C	2.2 V to 3.6 V	-3	±2	+3	%
16-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	25°C	3 V to 3.6 V	-6	±2	+3	%

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance overall	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	I: -40°C to 85°C	1.8 V to 3.6 V	-5	±2	+5	%
8-MHz tolerance overall	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	I: -40°C to 85°C	1.8 V to 3.6 V	-5	±2	+5	%
12-MHz tolerance overall	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	I: -40°C to 85°C	2.2 V to 3.6 V	-5	±2	+5	%
16-MHz tolerance overall	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	I: -40°C to 85°C	3 V to 3.6 V	-6	±3	+6	%

Wake-Up From Lower-Power Modes (LPM3, LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3 or LPM4 (1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V, 3 V		2		µs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ			1.5		
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ			1		
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V		1		
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3 or LPM4 (2)				$1 / f_{MCLK} + t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).

(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4

DCO WAKE-UP TIME FROM LPM3
vs
DCO FREQUENCY

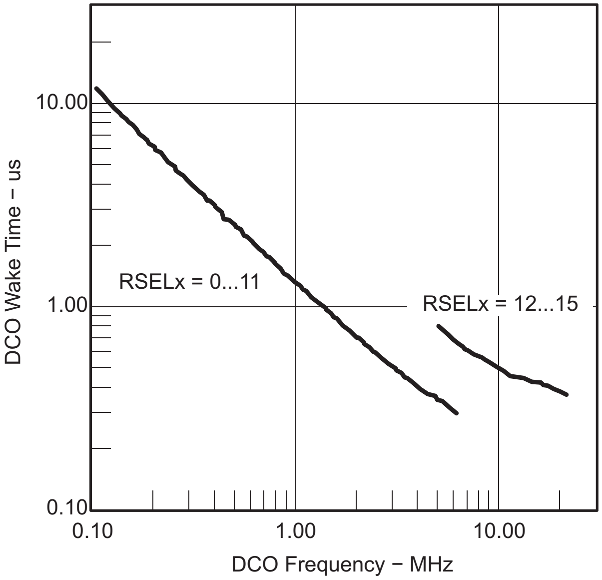


Figure 15.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	3 V	4	12	20	kHz
df_{VLO}/dT	VLO frequency temperature drift(1)	-40°C to 85°C	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(2)	25°C	1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK External: TACLK, INCLK Duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$t_{TA,cap}$	Timer_A capture timing	TAx	3 V	20			ns

USI, Universal Serial Interface (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USI}	USI clock frequency	External: SCLK, Duty cycle = 50% ±10%, SPI slave mode USI module in I^2C mode, $I_{(OLmax)}$ = 1.5 mA			f_{SYSTEM}		MHz
$V_{OL,I2C}$	Low-level output voltage on SDA and SCL		3 V	V_{SS}		V_{SS} + 0.4	V

Typical Characteristics, USI Low-Level Output Voltage on SDA and SCL (MSP430G2230 Only)

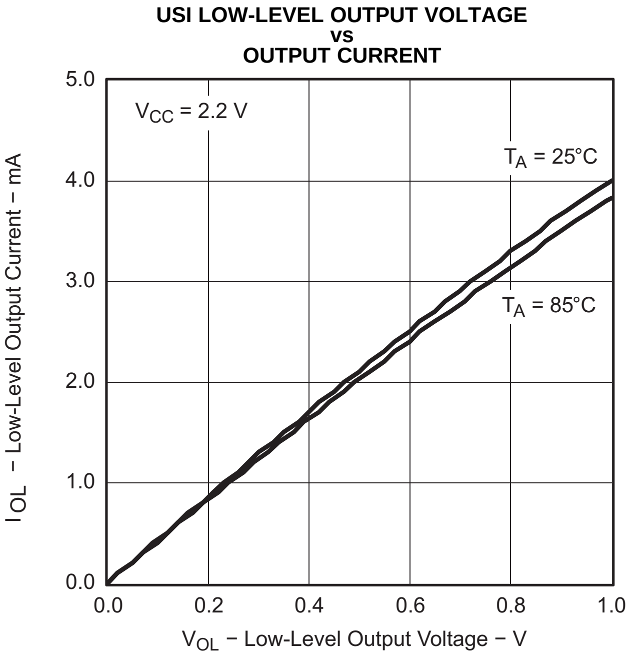


Figure 16.

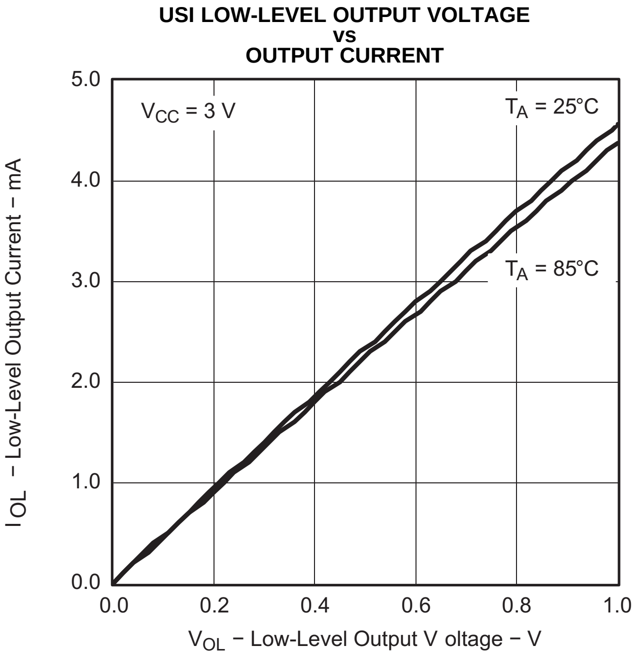


Figure 17.

Comparator_A+ (MSP430G2210 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$ [1]		CAON = 1, CARSEL = 0, CAREF = 0	3 V		45		µA
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at CA0 and CA1	3 V		45		µA
$V_{(IC)}$	Common–mode input voltage	CAON = 1	3 V	0		V_{CC}-1	V
$V_{(Ref025)}$	(Voltage at 0.25 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at CA0 and CA1	3 V		0.24		
$V_{(Ref050)}$	(Voltage at 0.5 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at CA0 and CA1	3 V		0.48		
$V_{(RefVT)}$	See Figure 18 and Figure 19	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at CA0 and CA1, TA = 85°C	3 V		490		mV
$V_{(offset)}$	Offset voltage [2]		3 V		±10		mV
V_{hys}	Input hysteresis	CAON = 1	3 V		0.7		mV
$t_{(response)}$	Response time (low-to-high and high-to-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	3 V		120		ns
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1			1.5		µs

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.

Typical Characteristics – Comparator_A+ (MSP430G2210 Only)

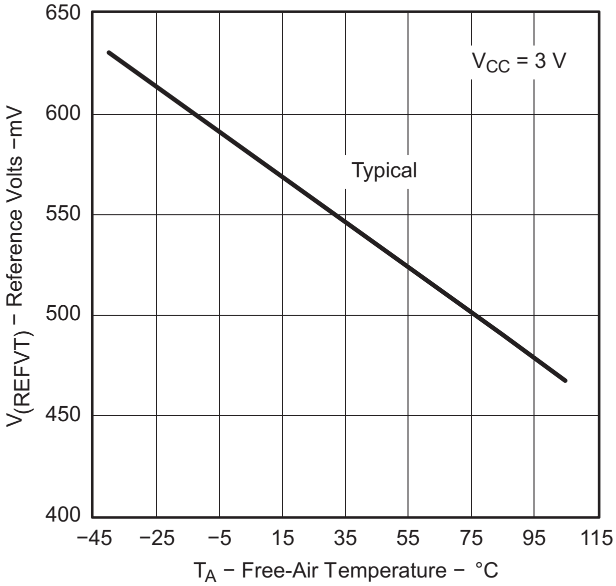


Figure 18. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

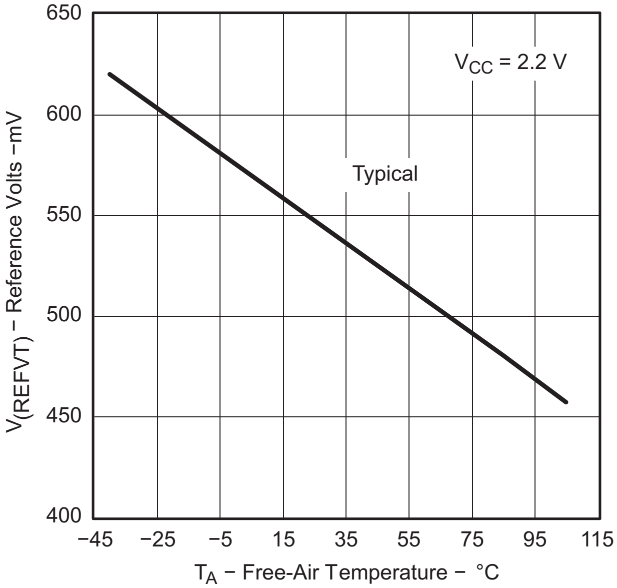


Figure 19. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

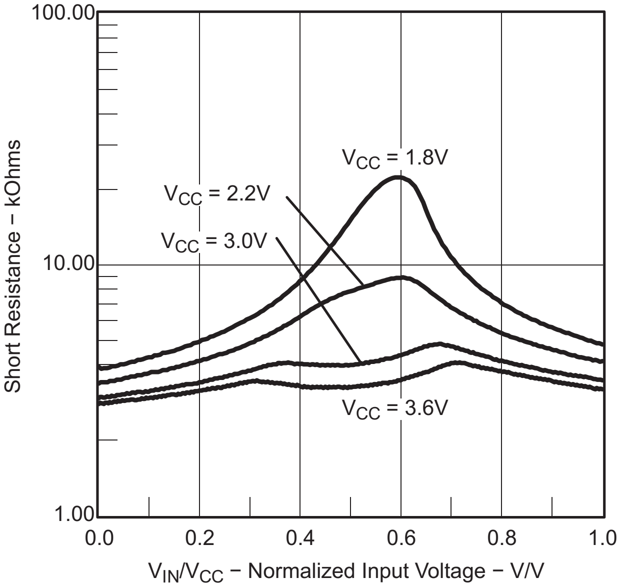


Figure 20. Short Resistance vs V_{IN}/V_{CC}

10-Bit ADC, Power Supply and Input Range Conditions (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage(2)	All Ax terminals, Analog inputs selected in ADC10AE register		3 V	0		V_{CC}	V
I_{ADC10}	ADC10 supply current(3)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	25°C	3 V		0.6		mA
I_{REF+}	Reference supply current, reference buffer disabled(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	25°C	3 V		0.25		mA
		$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0				0.25		
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	25°C	3 V		1.1		mA
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	25°C	3 V		0.5		mA
C_I	Input capacitance	Only one terminal Ax can be selected at one time	25°C	3 V			27	pF
R_I	Input MUX ON resistance	0 V ≤ V_{Ax} ≤ V_{CC}	25°C	3 V		1000		Ω

(1) The leakage current is defined in the leakage current table with Px.y/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
(4) The internal reference current is supplied by terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	I_{VREF+} ≤ 1 mA, REF2_5V = 0		2.2			V
		I_{VREF+} ≤ 1 mA, REF2_5V = 1		2.9			
V_{REF+}	Positive built-in reference voltage	I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 0	3 V	1.41	1.5	1.59	V
		I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 1		2.35	2.5	2.65	
$I_{LD,VREF+}$	Maximum VREF+ load current		3 V			±1	mA
	VREF+ load regulation	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage V_{Ax} ≈ 0.75 V, REF2_5V = 0	3 V			±2	LSB
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage V_{Ax} ≈ 1.25 V, REF2_5V = 1				±2	
	V_{REF+} load regulation response time	I_{VREF+} = 100 µA→900 µA, V_{Ax} ≈ 0.5 × VREF+, Error of conversion result ≤ 1 LSB, ADC10SR = 0	3 V			400	ns
C_{VREF+}	Maximum capacitance at pin VREF+	I_{VREF+} ≤ ±1 mA, REFON = 1, REFOUT = 1	3 V			100	pF
TC_{REF+}	Temperature coefficient[1]	I_{VREF+} = const with 0 mA ≤ I_{VREF+} ≤ 1 mA	3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1	3.6 V			30	µs
$t_{REFBURST}$	Settling time of reference buffer to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0	3 V			2	µs

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))

10-Bit ADC, External Reference (MSP430G2230 Only)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
VEREF+	Positive external reference input voltage range (2)	VEREF+ > VEREF–, SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		VEREF– ≤ VEREF+ ≤ V_{CC} – 0.15 V, SREF1 = 1, SREF0 = 1 (3)		1.4		3	
VEREF–	Negative external reference input voltage range (4)	VEREF+ > VEREF–		0		1.2	V
ΔVEREF	Differential external reference input voltage range, ΔVEREF = VEREF+ – VEREF–	VEREF+ > VEREF– (5)		1.4		V_{CC}	V
I_{VEREF+}	Static input current into VEREF+	0 V ≤ VEREF+ ≤ V_{CC}, SREF1 = 1, SREF0 = 0	3 V		±1		µA
		0 V ≤ VEREF+ ≤ V_{CC} – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1(3)	3 V		0		
$I_{VEREF–}$	Static input current into VEREF–	0 V ≤ VEREF– ≤ V_{CC}	3 V		±1		µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.

(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

(3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.

(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.

(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45		6.3	MHz
			ADC10SR = 1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0				13 × ADC10DIV × $1/f_{ADC10CLK}$		
$t_{ADC10ON}$	Turn-on settling time of the ADC	(1)					100	ns

(1) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		3 V			±1	LSB
E_D	Differential linearity error		3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	3 V			±1	LSB
E_G	Gain error		3 V		±1.1	±2	LSB
E_T	Total unadjusted error		3 V		±2	±5	LSB

10-Bit ADC, Temperature Sensor and Built-In V_{MID} (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current (1)	REFON = 0, INCHx = 0Ah, T_A = 25°C	3 V		60		µA
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah (2)	3 V		3.55		mV/°C
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected (3)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	3 V	30			µs
I_{VMID}	Current into divider at channel 11	ADC10ON = 1, INCHx = 0Bh	3 V			(4)	µA
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, $V_{MID} \approx 0.5 \times V_{CC}$	3 V		1.5		V
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (5)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	3 V	1220			ns

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).

(2) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]

(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.

(4) No additional current is needed. The V_{MID} is used during sampling.

(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V, 3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V, 3.6 V		1	7	mA
t_{CPT}	Cumulative program time (1)		2.2 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V, 3.6 V	20			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			30		t_{FTG}
$t_{Block,\ 0}$	Block program time for first byte or word	(2)			25		t_{FTG}
$t_{Block,\ 1-63}$	Block program time for each additional byte or word	(2)			18		t_{FTG}
$t_{Block,\ End}$	Block program end-sequence wait time	(2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	(2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	(2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
(2) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge (1))	2.2 V, 3 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time	2.2 V, 3 V	15		100	µs
$R_{Internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.

JTAG Fuse (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) After the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION

Port (P1.2 and P1.5) Pin Schematics - MSP430G2210

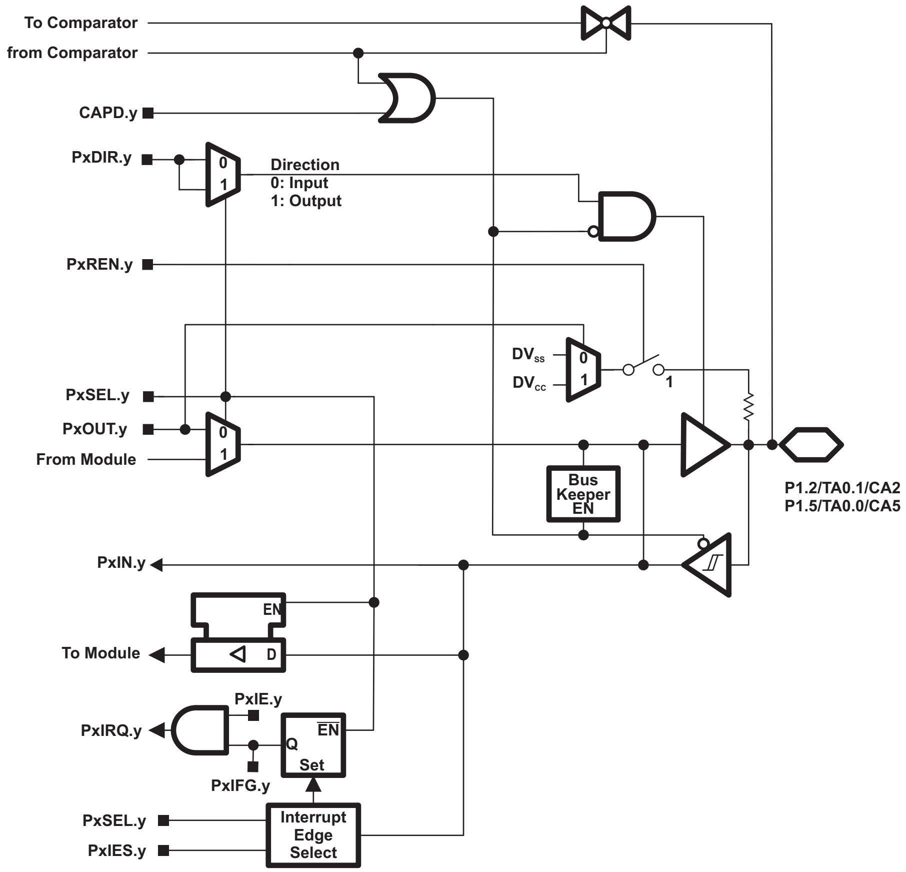


Figure 21.

Table 15. Port P1 (P1.2 to P1.5) Pin Functions - MSP430G2210

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P1DIR.x	P1SEL.x	CAPD.y
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0
TA0.1/		TA0.1	1	1	0
		TA0.CCI1A	0	1	0
CA2		CA2	X	X	1 (y = 2)
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0
TA0.0/		TA0.0	1	1	0
CA5		CA5	X	Xx	1 (y = 5)

---

(1) X = don't care

Port P1 (P1.6 and 1.7) Pin Schematic - MSP430G2210

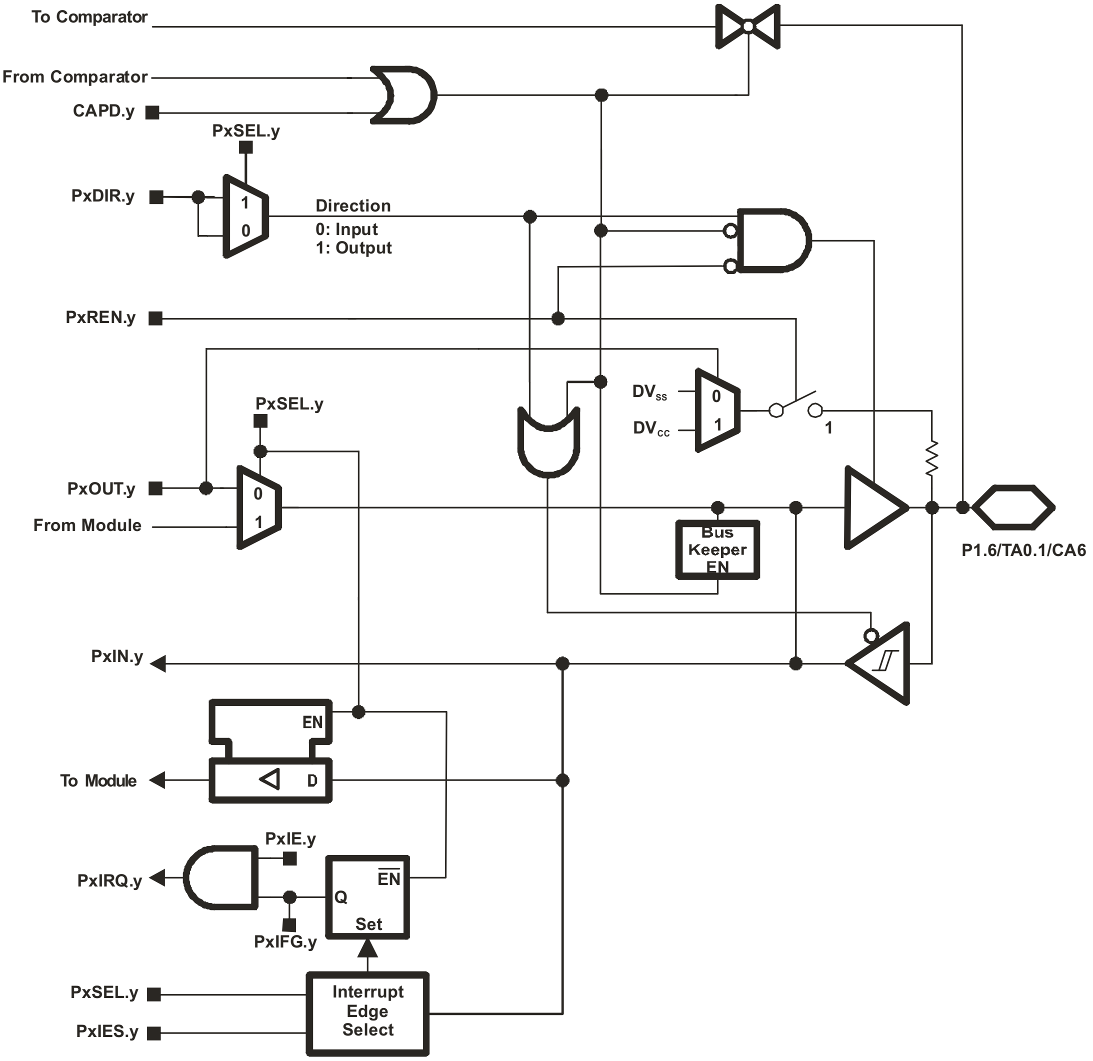


Figure 22.

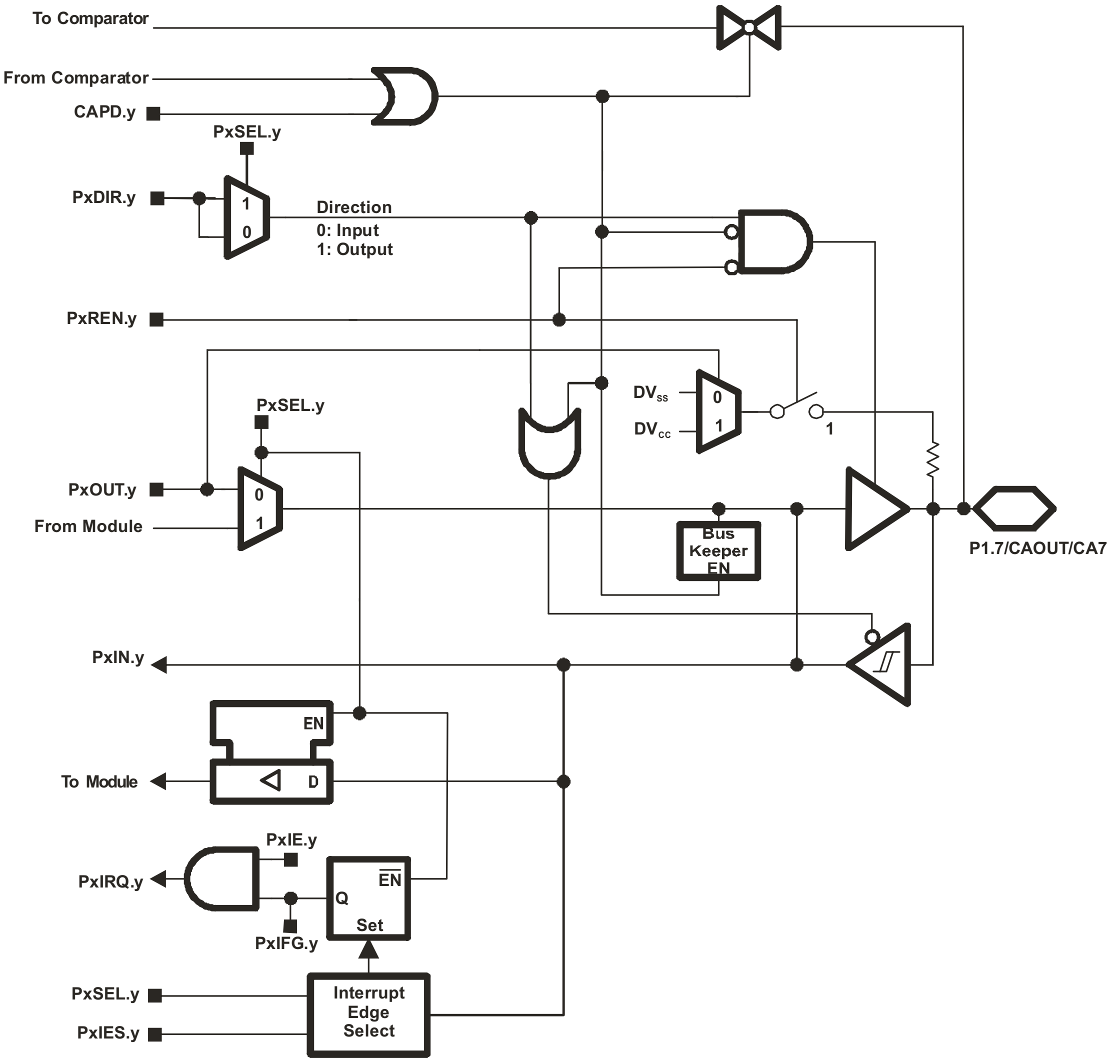


Figure 23.

Table 16. Port P1 (P1.6 and P1.7) Pin Functions - MSP430G2210

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P1DIR.x	P1SEL.x	CAPD.y
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0
TA0.1/		TA0.1	1	1	0
CA6		CA6	X	X	1 (y = 6)
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0
CA7/		CA7	X	X	1 (y = 7)
CAOUT		CAOUT	1	1	0

(1) X = don't care

Port P1 (P1.2) Pin Schematics - MSP430G2230

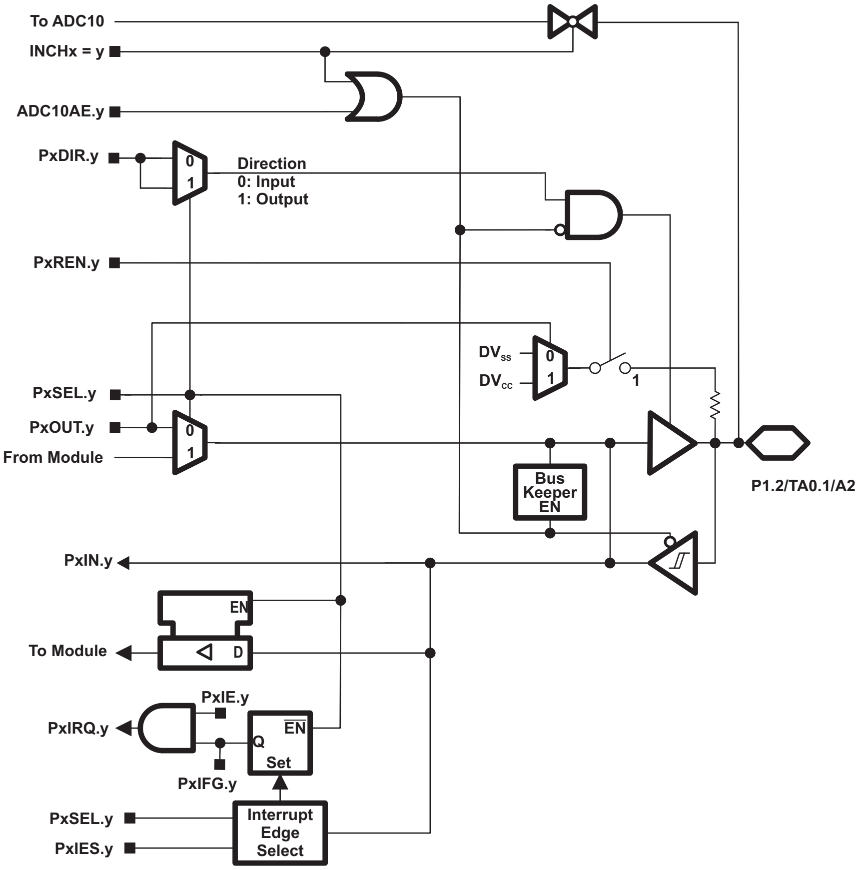


Figure 24.

Table 17. Port P1 (P1.2) Pin Functions - MSP430G2230

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P1DIR.x	P1SEL.x	ADC10AE.x (INCH.y = 1)
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0
TA0.1/		TA0.1	1	1	0
		TA0.CCI1A	0	1	0
A2		A2	X	X	1 (y = 2)

(1) X = don't care

Port P1 (P1.5) Pin Schematics - MSP430G2230

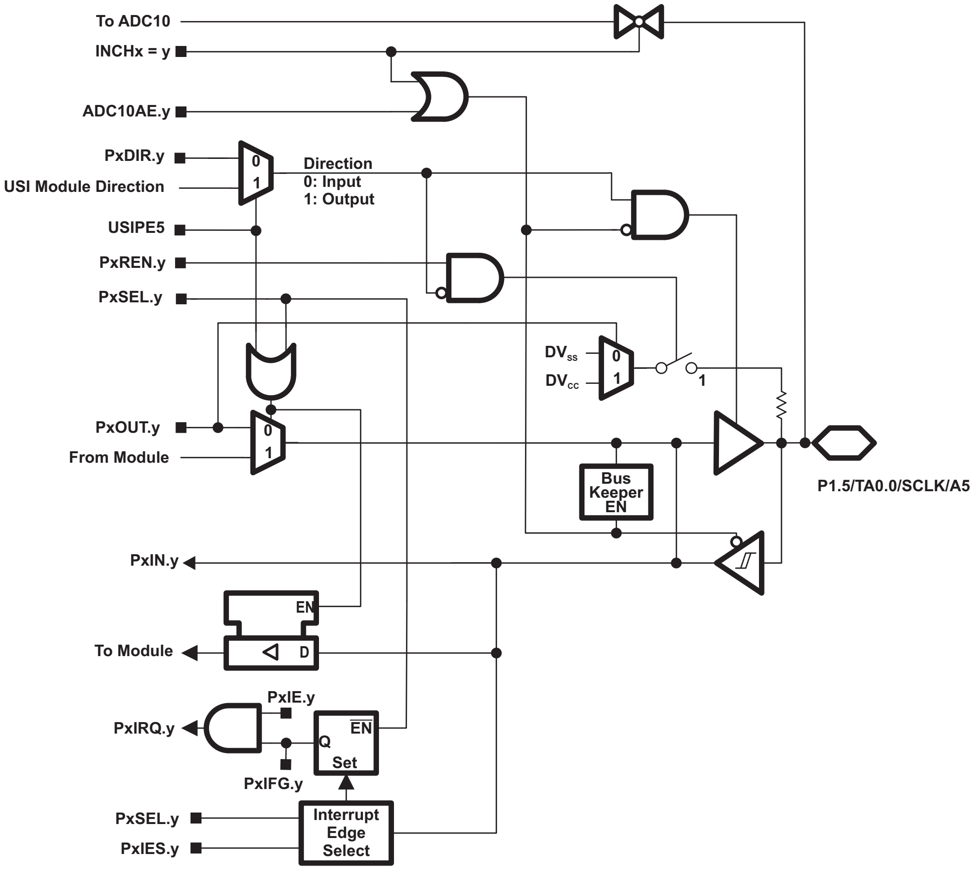


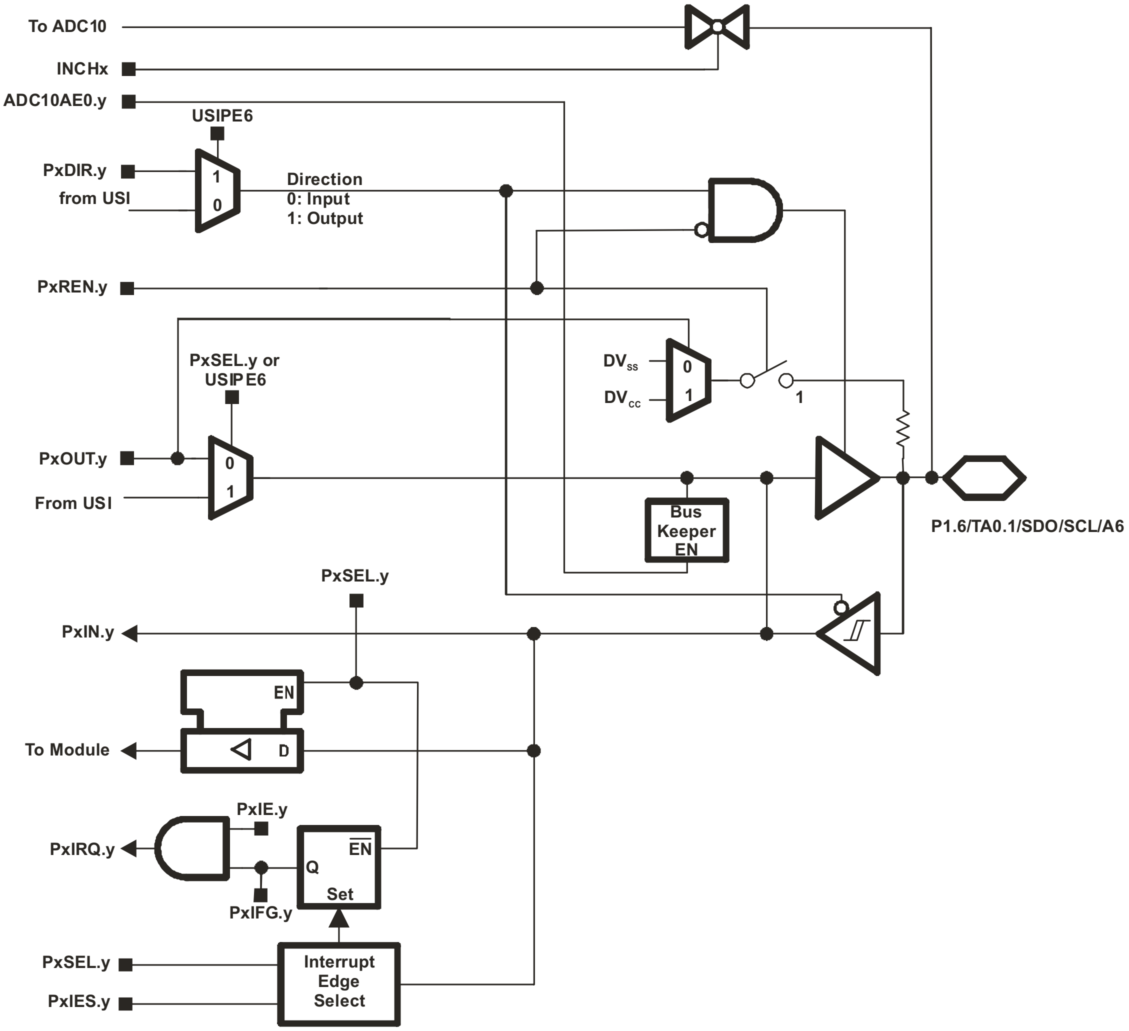
Figure 25.

Table 18. Port P1 (P1.5) Pin Functions - MSP430G2230

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)				
			P1DIR.x	P1SEL.x	USIP.x	ADC10AE.x (INCH.y = 1)	INCHx
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0	X
TA0.0/		TA0.0	1	1	0	0	X
SCLK/		SCLK	X	X	1	X	X
A5		A5	X	X	X	1 (y = 5)	5

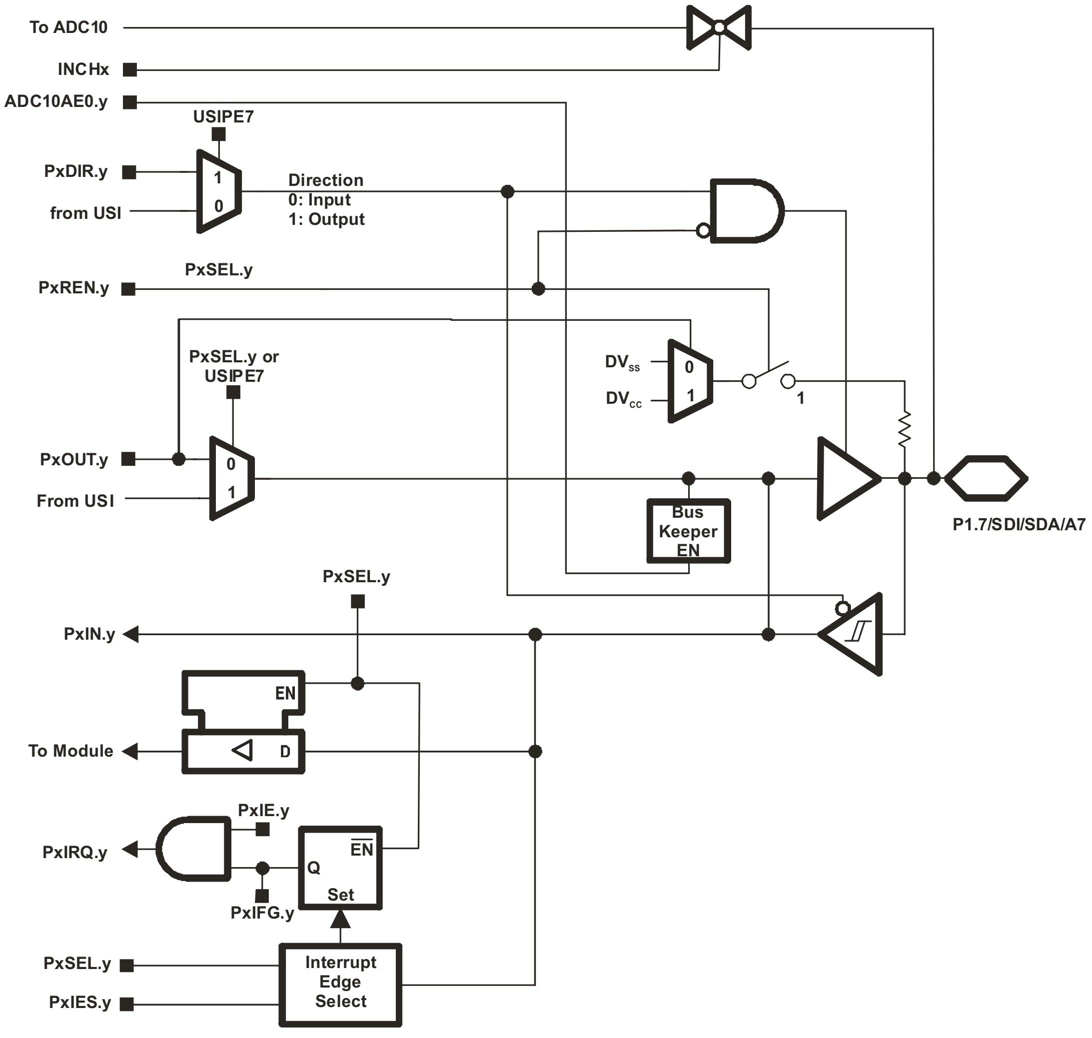
(1) X = don't care

Port P1 (P1.6 and 1.7) Pin Schematic - MSP430G2230



USI in I2C mode: Output driver drives low level only.

Figure 26.



USI in I2C mode: Output driver drives low level only.

Figure 27.

Table 19. Port P1 (P1.6 and P1.7) Pin Functions - MSP430G2230

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]			
			P1DIR.x	P1SEL.x	USIP.x	ADC10AE.x (INCH.y = 1)
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0
TA0.1/		TA0.CCI1A	0	1	0	0
		TA0.1	1	1	0	0
SDO/		SPI Mode	from USI	1	1	0
SCL/		I2C Mode	from USI	1	1	0
A6		A6	X	X	0	1 (y = 6)
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0
SDI/		SDI	X	1	1	0
SDA/		SDA	X	1	1	0
A7		A7	X	X	0	1 (y = 7)

(1) X = don't care

REVISION HISTORY

Literature Number	Comments
SLAS753	Production Data release
SLAS753A	Changed Table 11. Added Table 12.
SLAS753B	Corrected "Basic Clock Module Configurations" list in 特性. Added note to TC_{REF+} in 10-Bit ADC, Built-In Voltage Reference (MSP430G2230 Only).
SLAS753C	Added Flash Memory.
SLAS753D	Table 15, Removed ADC10AE.x column and removed A2 and A5 rows (no ADC on this device). Table 18, Added USIP.x column. Table 19, Added "(INCH.y = 1)" to ADC10AE.x column header.
SLAS753E	Recommended Operating Conditions, Added test conditions for typical values. POR and BOR, Added note (2).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2210ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	G2210	Samples
MSP430G2210IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	G2210	Samples
MSP430G2230ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	G2230	Samples
MSP430G2230IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	G2230	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430G2230 :

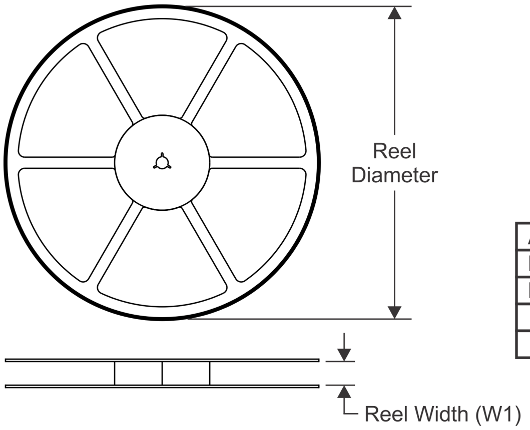
- Enhanced Product: MSP430G2230-EP

NOTE: Qualified Version Definitions:

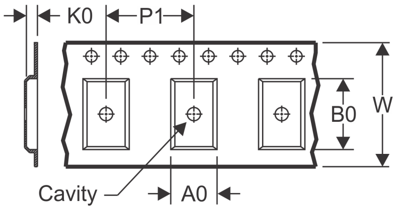
  - Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

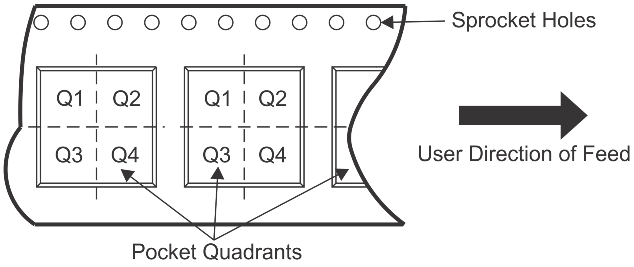


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

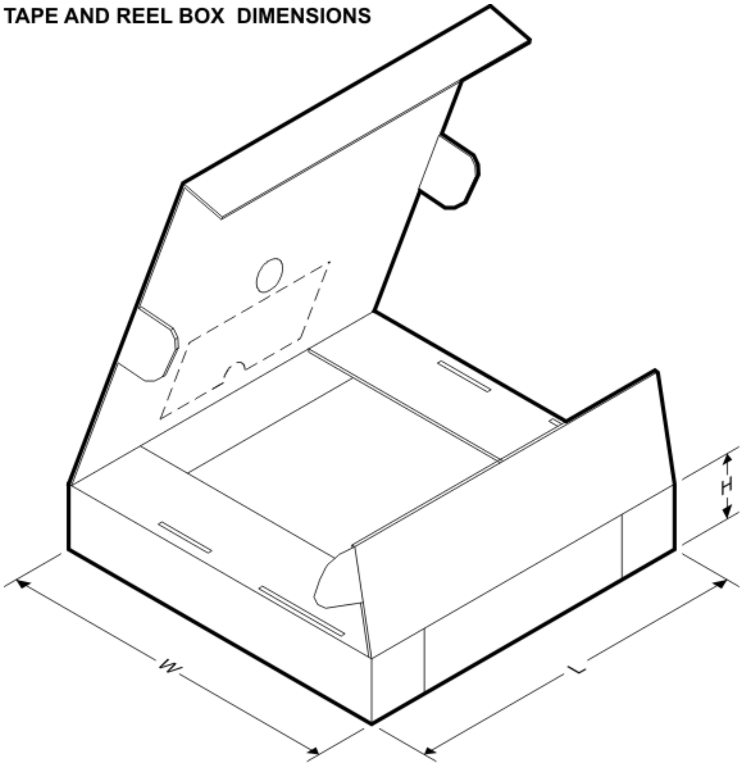
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430G2210IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MSP430G2230IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

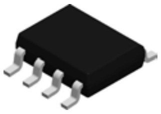


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430G2210IDR	SOIC	D	8	2500	853.0	449.0	35.0
MSP430G2230IDR	SOIC	D	8	2500	853.0	449.0	35.0

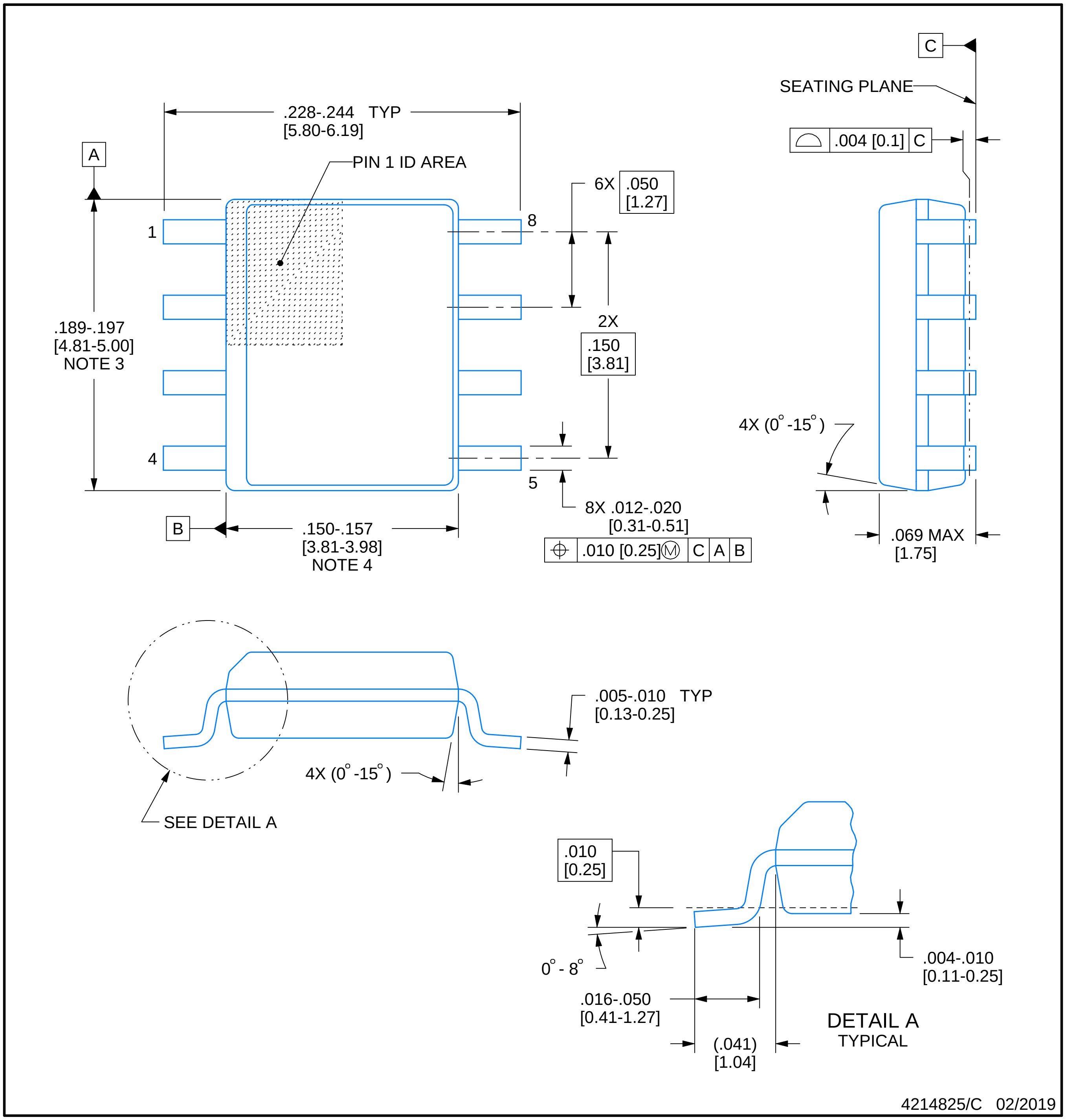
PACKAGE OUTLINE

D0008A



SOIC - 1.75 mm max height

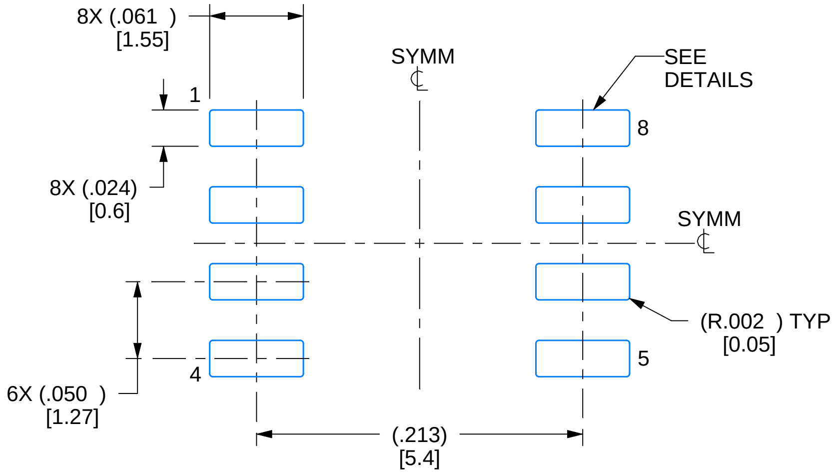
SMALL OUTLINE INTEGRATED CIRCUIT



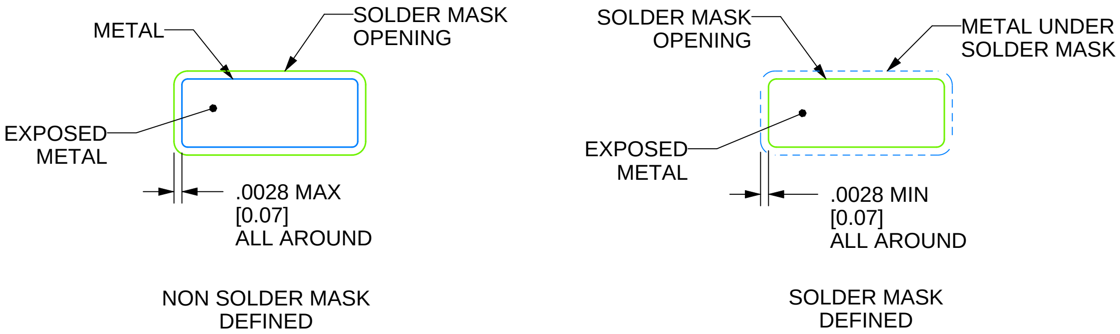
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

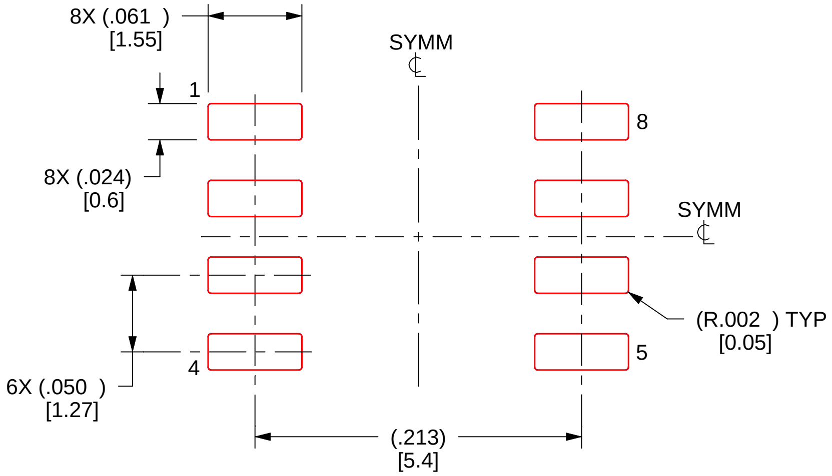


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122