

SCAN90CP02 1.5 Gbps 2x2 LVDS Crosspoint Switch with Pre-Emphasis and IEEE 1149.6

Check for Samples: [SCAN90CP02](#)

FEATURES

- 1.5 Gbps per Channel
- Low Power: 70 mA in Dual Repeater Mode @1.5 Gbps
- Low Output Jitter
- Configurable 0/25/50/100% Pre-Emphasis Drives Lossy Backplanes and Cables
- Non-Blocking Architecture Allows 1:2 Splitter, 2:1 Mux, Crossover, and Dual Buffer Configurations
- Flow-Through Pinout
- LVDS/BLVDS/CML/LVPECL Inputs, LVDS Outputs
- IEEE 1149.1 and 1149.6 Compliant
- Single 3.3V Supply
- Separate Control of Inputs and Outputs Allows for Power Savings
- Industrial -40 to +85°C Temperature Range
- 28-Lead UQFN Package, or 32-Lead LQFP Package

DESCRIPTION

The SCAN90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch. High speed data paths and flow-through pinout minimize internal device jitter, while configurable 0/25/50/100% pre-emphasis overcomes external ISI jitter effects of lossy backplanes and cables. The differential inputs interface to LVDS and Bus LVDS signals such as those on TI's 10-, 16-, and 18-bit Bus LVDS SerDes, as well as CML and LVPECL. The SCAN90CP02 can also be used with ASICs and FPGAs. The non-blocking crosspoint architecture is pin-configurable as a 1:2 clock or data splitter, 2:1 redundancy mux, crossover function, or dual buffer for signal booster and stub hider applications.

Integrated IEEE 1149.1 (JTAG) and 1149.6 circuitry supports testability of both single-ended LVTTL/CMOS and differential LVDS PCB interconnect. The 3.3V supply, CMOS process, and LVDS I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

Block Diagram

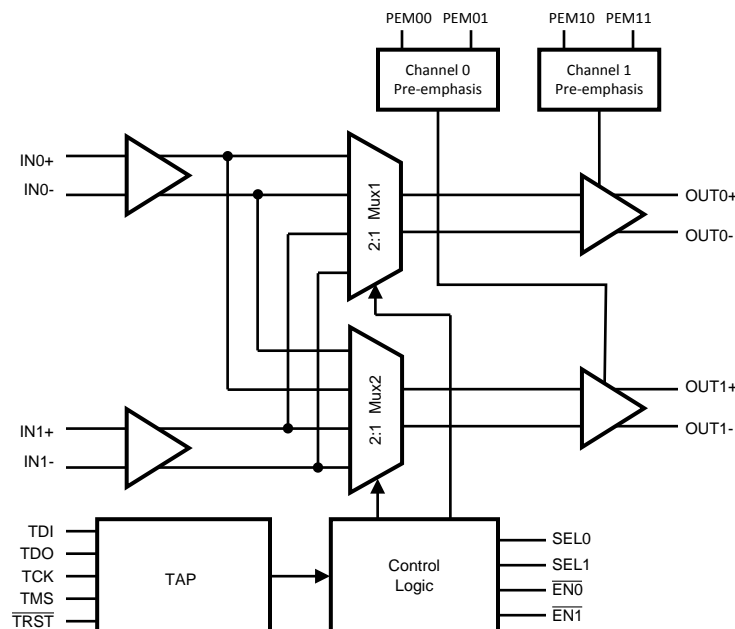


Figure 1. SCAN90CP02 Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2013, Texas Instruments Incorporated

PIN DESCRIPTIONS

Pin Name	UQFN Pin Number	LQFP Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS COMMON TO ALL MUXES				
IN0+ IN0–	9 10	9 10	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
IN1+ IN1–	12 13	13 14	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SWITCHED DIFFERENTIAL OUTPUTS				
OUT0+ OUT0–	27 26	32 31	O, LVDS	Inverting and non-inverting differential outputs. OUT0± can be connected to any one pair IN0±, or IN1±. LVDS compatible ⁽¹⁾ .
OUT1+ OUT1–	24 23	28 27	O, LVDS	Inverting and non-inverting differential outputs. OUT1± can be connected to any one pair IN0±, or IN1±. LVDS compatible ⁽¹⁾ .
DIGITAL CONTROL INTERFACE				
SEL0, SEL1	6 5	7 6	I, LVTTTL	Select Control Inputs
EN0, EN1	7 15	8 17	I, LVTTTL	Output Enable Inputs
PEM00, PEM01	4 3	4 3	I, LVTTTL	Channel 0 Output Pre-emphasis Control Inputs
PEM10, PEM11	2 1	2 1	I, LVTTTL	Channel 1 Output Pre-emphasis Control Inputs
TDI	19	22	I, LVTTTL	Test Data Input to support IEEE 1149.1 features
TDO	20	23	O, LVTTTL	Test Data Output to support IEEE 1149.1 features
TMS	18	21	I, LVTTTL	Test Mode Select to support IEEE 1149.1 features
TCK	17	19	I, LVTTTL	Test Clock to support IEEE 1149.1 features
TRST	21	24	I, LVTTTL	Test Reset to support IEEE 1149.1 features
N/C	8, 28			Not Connected
POWER				
V _{DD}	11, 14, 16, 22, 25	12, 16, 18, 25, 29	I, Power	V _{DD} = 3.3V ±0.3V. At least 4 low ESR 0.01 µF bypass capacitors should be connected from V _{DD} to GND plane.
GND	See ⁽²⁾	5, 11, 15, 20, 26, 30		Ground reference to LVDS and CMOS circuitry. For the UQFN package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the UQFN-28 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

(1) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.

(2) Note that for the UQFN package GND is not an actual pin on the package, the GND is connected thru the DAP on the back side of the UQFN package.

Connection Diagrams

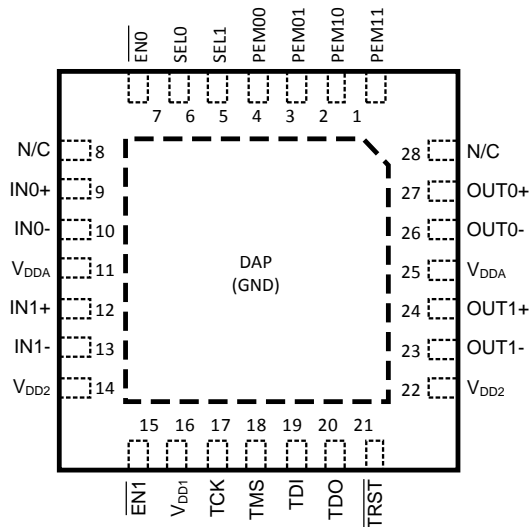


Figure 2. UQFN Top View
DAP = GND

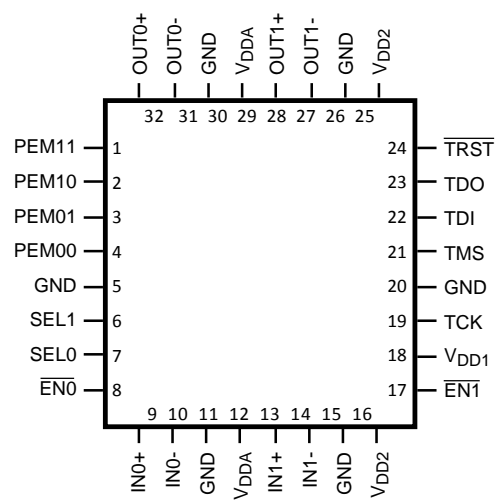


Figure 3. LQFP Top View

CONFIGURATION SELECT TRUTH TABLE⁽¹⁾

SEL0	SEL1	EN0	EN1	OUT0	OUT1	Mode
0	0	0	0	IN0	IN0	1:2 Splitter (IN1 powered down)
0	1	0	0	IN0	IN1	Dual Channel Repeater
1	0	0	0	IN1	IN0	Dual Channel Switch
1	1	0	0	IN1	IN1	1:2 Splitter (IN0 powered down)
0	1	0	1	IN0	PD	Single Channel Repeater (Channel 1 powered down)
1	1	0	1	IN1	PD	Single Channel Switch (IN0 and OUT1 powered down)
0	0	1	0	PD	IN0	Single Channel Switch (IN1 and OUT0 powered down)
0	1	1	0	PD	IN1	Single Channel Repeater (Channel 0 powered down)
X	X	1	1	PD	PD	Both Channels in Power Down Mode
0	0	0	1			Invalid State ⁽²⁾
1	0	0	1			Invalid State ⁽²⁾
1	0	1	0			Invalid State ⁽²⁾
1	1	1	0			Invalid State ⁽²⁾

(1) PD = Power Down mode to minimize power consumption

X = Don't Care

(2) Entering these states is not forbidden, however device operation is not defined in these states.

PRE-EMPHASIS

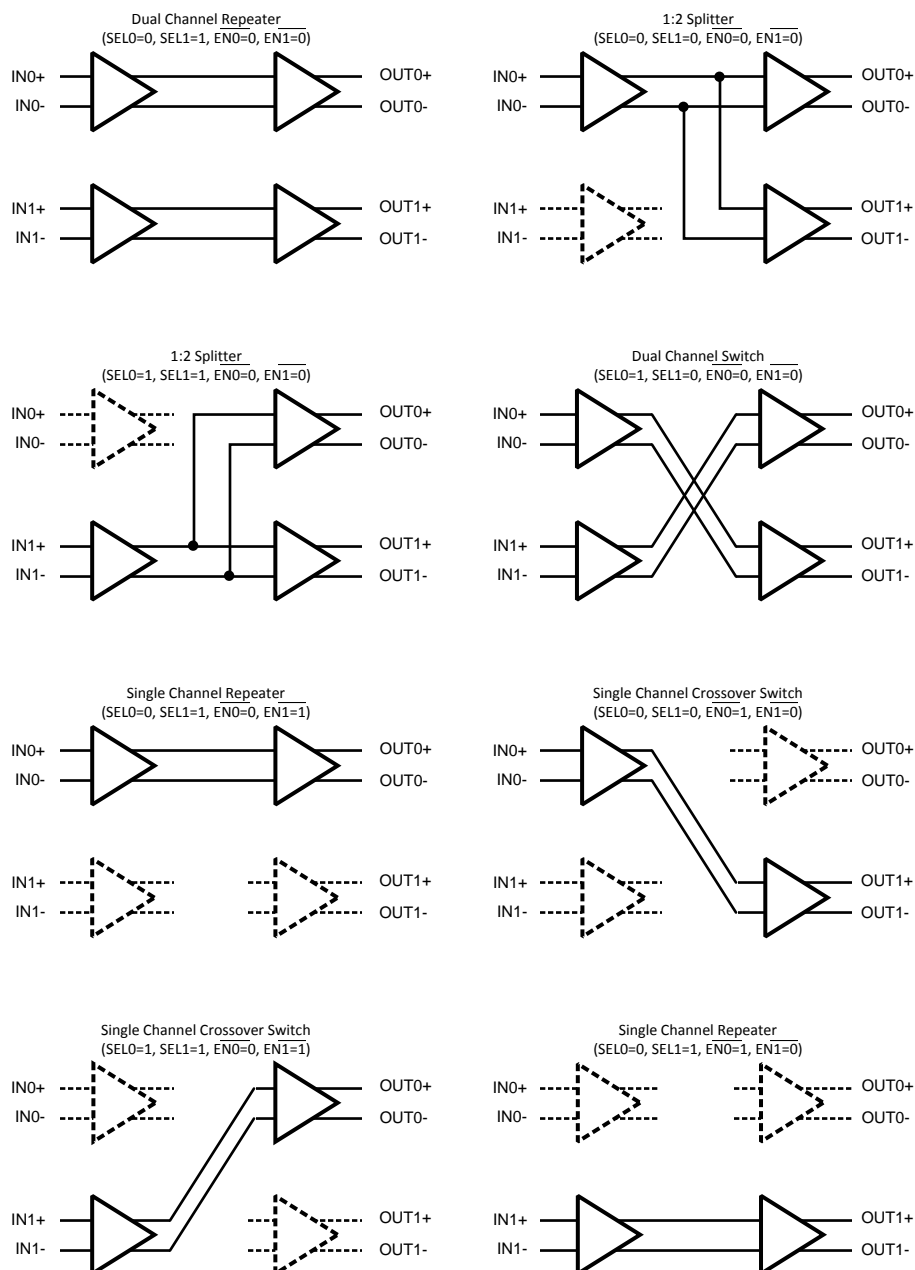
The pre-emphasis is used to compensate for long or lossy transmission media. Separate pins are provided for each output to minimize power consumption. Pre-emphasis is programmable to be off or to preset values per [Table 1](#).

Output Characteristics

The output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.

Table 1. Pre-emphasis Control Selection Table

Channel 0		Channel 1		Pre-emphasis
PEM01	PEM00	PEM11	PEM10	
0	0	0	0	0%
0	1	0	1	25%
1	0	1	0	50%
1	1	1	1	100%

Applications Information**Figure 4. SCAN90CP02 Configuration Select Decode**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage (V_{DD})		-0.3V to +4.0V
CMOS Input Voltage		-0.3V to ($V_{DD} + 0.3V$)
LVDS Receiver Input Voltage		-0.3V to +3.6V
LVDS Driver Output Voltage		-0.3V to +3.6V
LVDS Output Short Circuit Current		40mA
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Lead Temperature (Soldering, 4sec.)		+260°C
Maximum Package Power Dissipation at 25°C	UQFN-28	4.31 W
	LQFP-32	1.47 W
Derating above 25°C	UQFN-28	34.5 mW/°C
	LQFP-32	11.8 mW/°C
Thermal Resistance, θ_{JA}	UQFN-28	29°C/W
	LQFP-32	85°C/W
ESD Rating	HBM, 1.5 k Ω , 100 pF	6.5 kV
	EIAJ, 0 Ω , 200 pF	>250V

- (1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be specified. They are not meant to imply that the device should be operated at these limits.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Unit
Supply Voltage (V_{DD} – GND)	3.0	3.3	3.6	V
Receiver Input Voltage	0		3.6	V
Operating Free Air Temperature	-40	25	85	°C
Junction Temperature			150	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Units
LVTTL DC SPECIFICATIONS (SEL0, SEL1, $\overline{EN1}$, $\overline{EN2}$, PEM00, PEM01, PEM10, PEM11, TDI, TCK, TMS, \overline{TRST})						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	-10		+10	μ A
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	-10		+10	μ A
I_{ILR}	Low Level Input Current	TDI, TMS, \overline{TRST}	-40		-200	μ A
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		3.5		pF
C_{OUT1}	Output Capacitance	Any Digital Output Pin to V_{SS}		5.5		pF
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA	-1.5	-0.8		V
V_{OH}	High Level Output Voltage (TDO)	$I_{OH} = -12$ mA, $V_{DD} = 3.0$ V	2.4			V
		$I_{OH} = -100$ μ A, $V_{DD} = 3.0$ V	$V_{DD}-0.2$			V
V_{OL}	Low Level Output Voltage (TDO)	$I_{OL} = 12$ mA, $V_{DD} = 3.0$ V			0.5	V
		$I_{OL} = 100$ μ A, $V_{DD} = 3.0$ V			0.2	V
I_{OS}	Output Short Circuit Current	TDO	-15		-125	mA

- (1) Typical parameters are measured at $V_{DD} = 3.3V$, $T_A = 25^\circ C$. They are for reference purposes, and are not production-tested.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Units
LVDS INPUT DC SPECIFICATIONS (IN0±, IN1±)						
V _{TH}	Differential Input High Threshold ⁽²⁾	V _{CM} = 0.8V or 1.2V or 3.55V, V _{DD} = 3.6V		0	100	mV
V _{TL}	Differential Input Low Threshold	V _{CM} = 0.8V or 1.2V or 3.55V, V _{DD} = 3.6V	−100	0		mV
V _{ID}	Differential Input Voltage	V _{CM} = 0.8V to 3.55V, V _{DD} = 3.6V	100			mV
V _{CMR}	Common Mode Voltage Range	V _{ID} = 150 mV, V _{DD} = 3.6V	0.05		3.55	V
C _{IN2}	Input Capacitance	IN+ or IN− to V _{SS}		3.5		pF
I _{IN}	Input Current	V _{IN} = 3.6V, V _{DD} = V _{DDMAX} or 0V	−10		+10	μA
		V _{IN} = 0V, V _{DD} = V _{DDMAX} or 0V	−10		+10	μA
LVDS OUTPUT DC SPECIFICATIONS (OUT0±, OUT1±)						
V _{OD}	Differential Output Voltage, 0% Pre-emphasis ⁽²⁾	R _L = 100Ω between OUT+ and OUT−	250	400	575	mV
ΔV _{OD}	Change in V _{OD} between Complementary States		−35		35	mV
V _{OS}	Offset Voltage ⁽³⁾		1.09	1.25	1.475	V
ΔV _{OS}	Change in V _{OS} between Complementary States		−35		35	mV
I _{OS}	Output Short Circuit Current, One Complementary Output	OUT+ or OUT− Short to GND		−60	−90	mA
C _{OUT2}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE		5.5		pF
SUPPLY CURRENT (Static)						
I _{CC0}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT−.		42	60	mA
I _{CC1}	Supply Current - one channel powered down	Single channel crossover switch or single channel repeater modes (1 channel active, one channel in power down mode)		22	30	mA
I _{CC2}	Supply Current - one input powered down	Splitter mode (One input powered down, both outputs active)		30	40	mA
I _{CCZ}	TRI-STATE Supply Current	Both input/output Channels in Power Down Mode		1.4	2.5	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS (Figure 5, Figure 6)						
t _{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V _{OD} .	70	150	215	ps
t _{HLT}	Differential High to Low Transition Time		50	135	180	ps
t _{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V _{OD} between input to output.	0.5	2.4	3.5	ns
t _{PHLD}	Differential High to Low Propagation Delay		0.5	2.4	3.5	ns
t _{SKD1}	Pulse Skew	t _{PLHD} −t _{PHLD}		55	120	ps
t _{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t _{PLHD} or t _{PHLD}) among all output channels in Splitter mode (any one input to all outputs).	0	130	315	ps

(2) Differential output voltage V_{OD} is defined as ABS(OUT+–OUT–). Differential input voltage V_{ID} is defined as ABS(IN+–IN–).

(3) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Units
t_{JIT}	Jitter (0% Pre-emphasis) ⁽⁴⁾	RJ - Alternating 1/0 @ 750 MHz ⁽⁵⁾		1.4	2.5	psrms
		DJ - K28.5 Pattern 1.5 Gbps ⁽⁶⁾	LQFP	110	140	psp-p
			UQFN	42	75	psp-p
		TJ - PRBS 2 ²³ -1 Pattern 1.5 Gbps ⁽⁷⁾	LQFP	113	148	psp-p
			UQFN	93	126	psp-p
t_{ON}	LVDS Output Enable Time	Time from \overline{ENx} to OUT \pm change from TRI-STATE to active.	50	110	150	ns
t_{OFF}	LVDS Output Disable Time	Time from \overline{ENx} to OUT \pm change from active to TRI-STATE.		5	12	ns
t_{SW}	LVDS Switching Time SELx to OUT \pm	Time from configuration select (SELx) to new switch configuration effective for OUT \pm .		110	150	ns

(4) Jitter is not production tested, but specified through characterization on a sample basis.

(5) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = $V_{ID} = 500\text{mV}$, 50% duty cycle at 750MHz, $t_r = t_f = 50\text{ps}$ (20% to 80%).

(6) Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = $V_{ID} = 500\text{mV}$, K28.5 pattern at 1.5 Gbps, $t_r = t_f = 50\text{ps}$ (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

(7) Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = $V_{ID} = 500\text{mV}$, 2²³-1 PRBS pattern at 1.5 Gbps, $t_r = t_f = 50\text{ps}$ (20% to 80%).

SCAN CIRCUITRY TIMING REQUIREMENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Maximum TCK Clock Frequency	$R_L = 500\Omega$, $C_L = 35\text{ pF}$	25.0			MHz
t_S	TDI to TCK, H or L		1.0			ns
t_H	TDI to TCK, H or L		2.0			ns
t_S	TMS to TCK, H or L		2.0			ns
t_H	TMS to TCK, H or L		1.5			ns
t_W	TCK Pulse Width, H or L		10.0			ns
t_W	\overline{TRST} Pulse Width, L		2.5			ns
t_{REC}	Recovery Time, \overline{TRST} to TCK		2.0			ns

TIMING DIAGRAMS

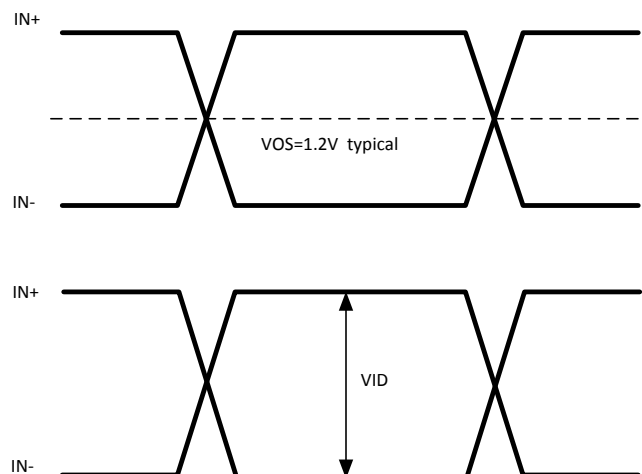


Figure 5. LVDS Signals

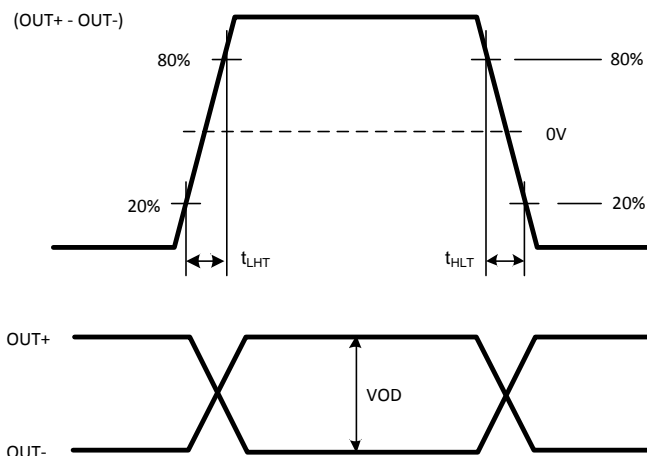


Figure 6. LVDS Output Transition Time

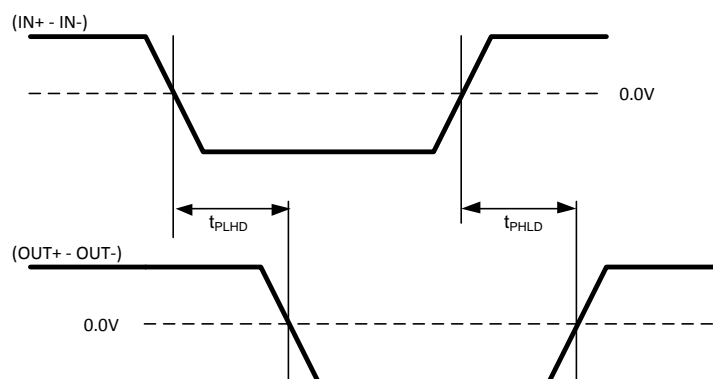


Figure 7. LVDS Output Propagation Delay

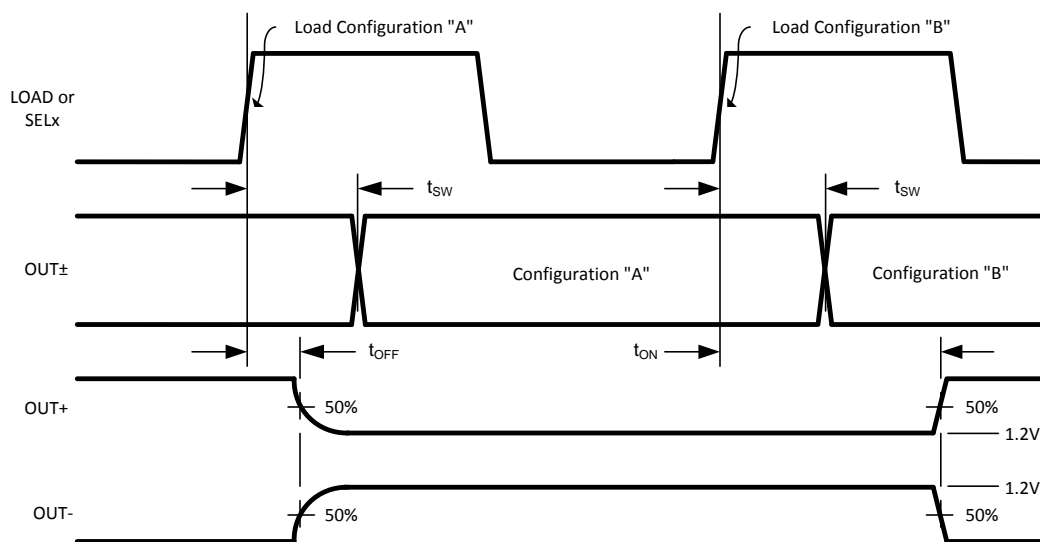


Figure 8. Configuration and Output Enable/Disable Timing

Input Interfacing

The SCAN90CP02 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the SCAN90CP02 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers.

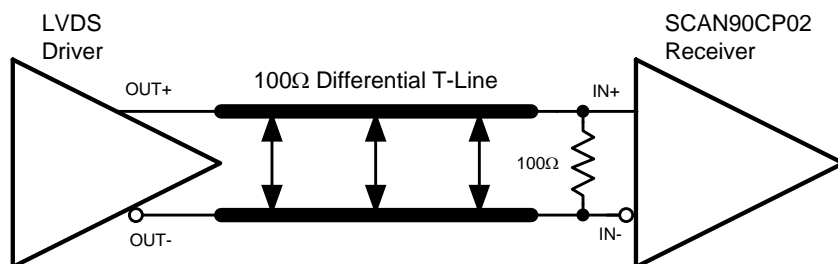


Figure 9. Typical LVDS Driver DC-Coupled Interface to SCAN90CP02 Input

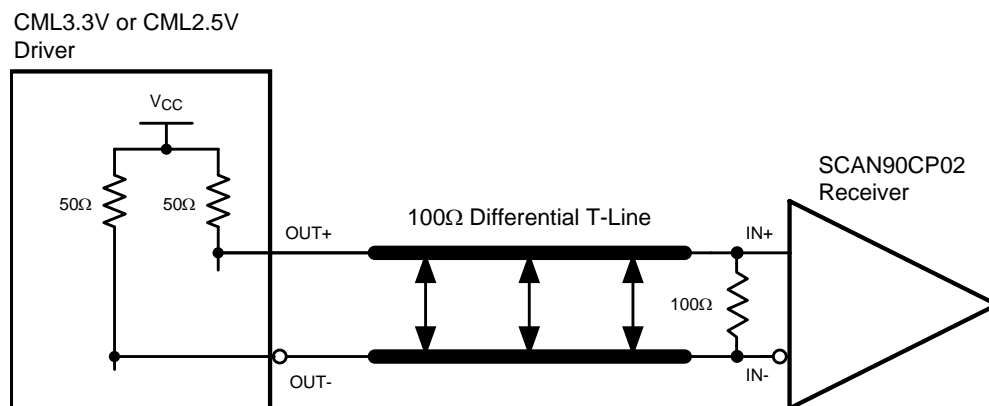


Figure 10. Typical CML Driver DC-Coupled Interface to SCAN90CP02 Input

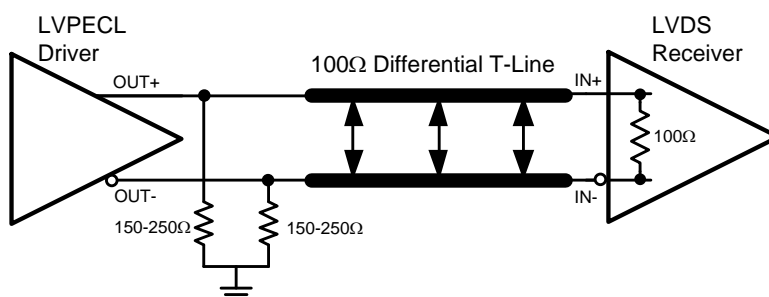


Figure 11. Typical LVPECL Driver DC-Coupled Interface to SCAN90CP02 Input

Output Interfacing

The SCAN90CP02 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. Figure 12 illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

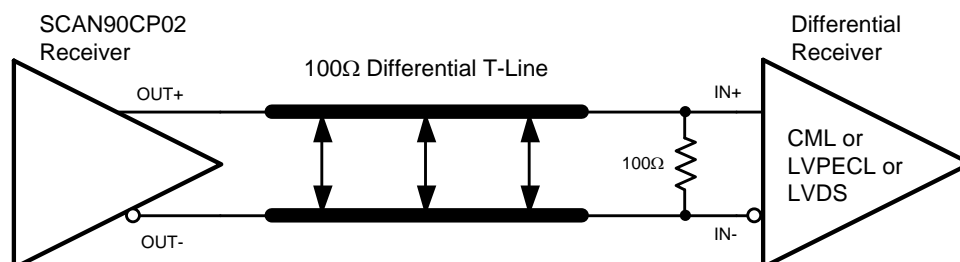
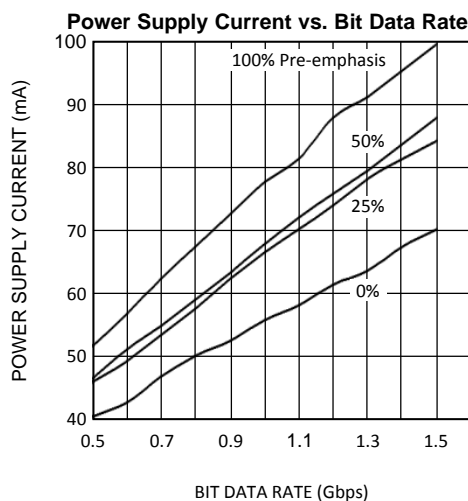


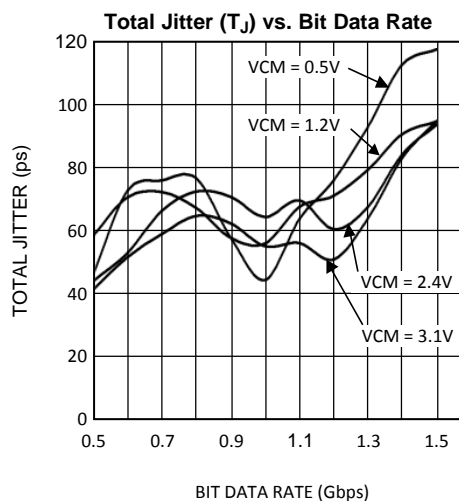
Figure 12. Typical SCAN90CP02 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

TYPICAL PERFORMANCE CHARACTERISTICS FOR UQFN PACKAGE



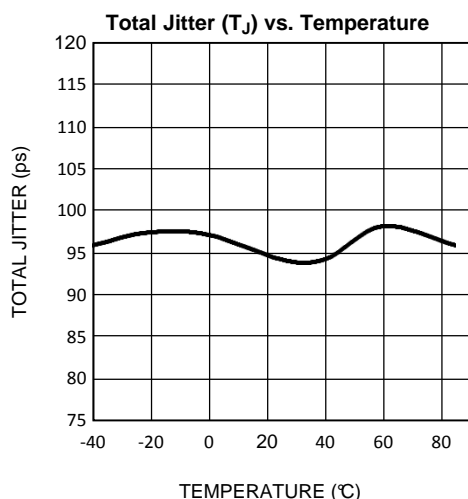
Dynamic power supply current was measured while running a PRBS $2^{23}-1$ pattern in dual channel repeater mode. $V_{CC} = 3.3V$, $T_A = +25^\circ C$, $V_{ID} = 0.5V$, $V_{CM} = 1.2V$

Figure 13.



Total Jitter measured at 0V differential while running a PRBS $2^{23}-1$ pattern in single channel repeater mode. $V_{CC} = 3.3V$, $T_A = +25^\circ C$, $V_{ID} = 0.5V$, 0% Pre-emphasis

Figure 14.



Total Jitter measured at 0V differential while running a PRBS $2^{23}-1$ pattern in dual channel repeater mode. $V_{CC} = 3.3V$, $V_{ID} = 0.5V$, $V_{CM} = 1.2V$, 1.5 Gbps data rate, 0% Pre-emphasis

Figure 15.

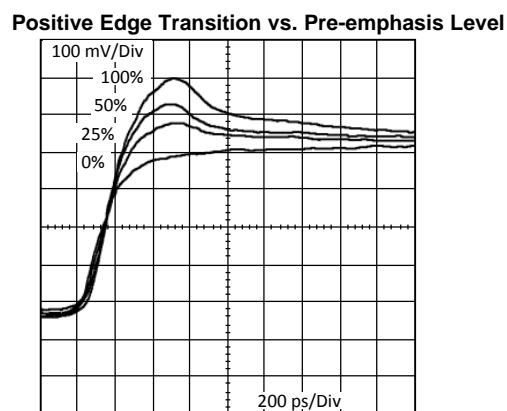


Figure 16.

DESIGN-FOR-TEST (DFT) FEATURES

IEEE 1149.1 SUPPORT

The SCAN90CP02 supports a fully compliant IEEE 1149.1 interface. The Test Access Port (TAP) provides access to boundary scan cells at each LVTTTL I/O on the device for interconnect testing. Differential pins are included in the same boundary scan chain but instead contain IEEE1149.6 cells. IEEE1149.6 is the improved IEEE standard for testing high-speed differential signals.

Refer to the BSDL file located on TI's website for the details of the SCAN90CP02 IEEE 1149.1 implementation.

IEEE 1149.6 SUPPORT

AC-coupled differential interconnections on very high speed (1+ Gbps) data paths are not testable using traditional IEEE 1149.1 techniques. The IEEE 1149.1 structures and methods are intended to test static (DC-coupled), single ended networks. IEEE1149.6 is specifically designed for testing high-speed differential, including AC coupled networks.

The SCAN90CP02 is intended for high-speed signaling up to 1.5 Gbps and includes IEEE1149.6 on all differential inputs and outputs.

FAULT INSERTION

Fault Insertion is a technique used to assist in the verification and debug of diagnostic software. During system testing faults are "injected" to simulate hardware failure and thus help verify the monitoring software can detect and diagnose these faults. In the SCAN90004 an IEEE1149.1 "stuck-at" instruction can create a stuck-at condition, either high or low, on any pin or combination of pins.

A more detailed description of the stuck-at feature can be found in Texas Instruments Applications note AN-1313([SNLA060](#)).

REVISION HISTORY

Changes from Revision L (April 2013) to Revision M

Page

- Changed layout of National Data Sheet to TI format [12](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SCAN90CP02SP/NOPB	ACTIVE	UQFN	NJD	28	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	SCP02SP	Samples
SCAN90CP02VY/NOPB	ACTIVE	LQFP	NEY	32	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	SCAN90 CP02VY	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SCAN90CP02SP/NOPB	UQFN	NJD	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

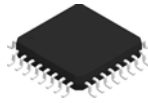
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SCAN90CP02SP/NOPB	UQFN	NJD	28	1000	210.0	185.0	35.0

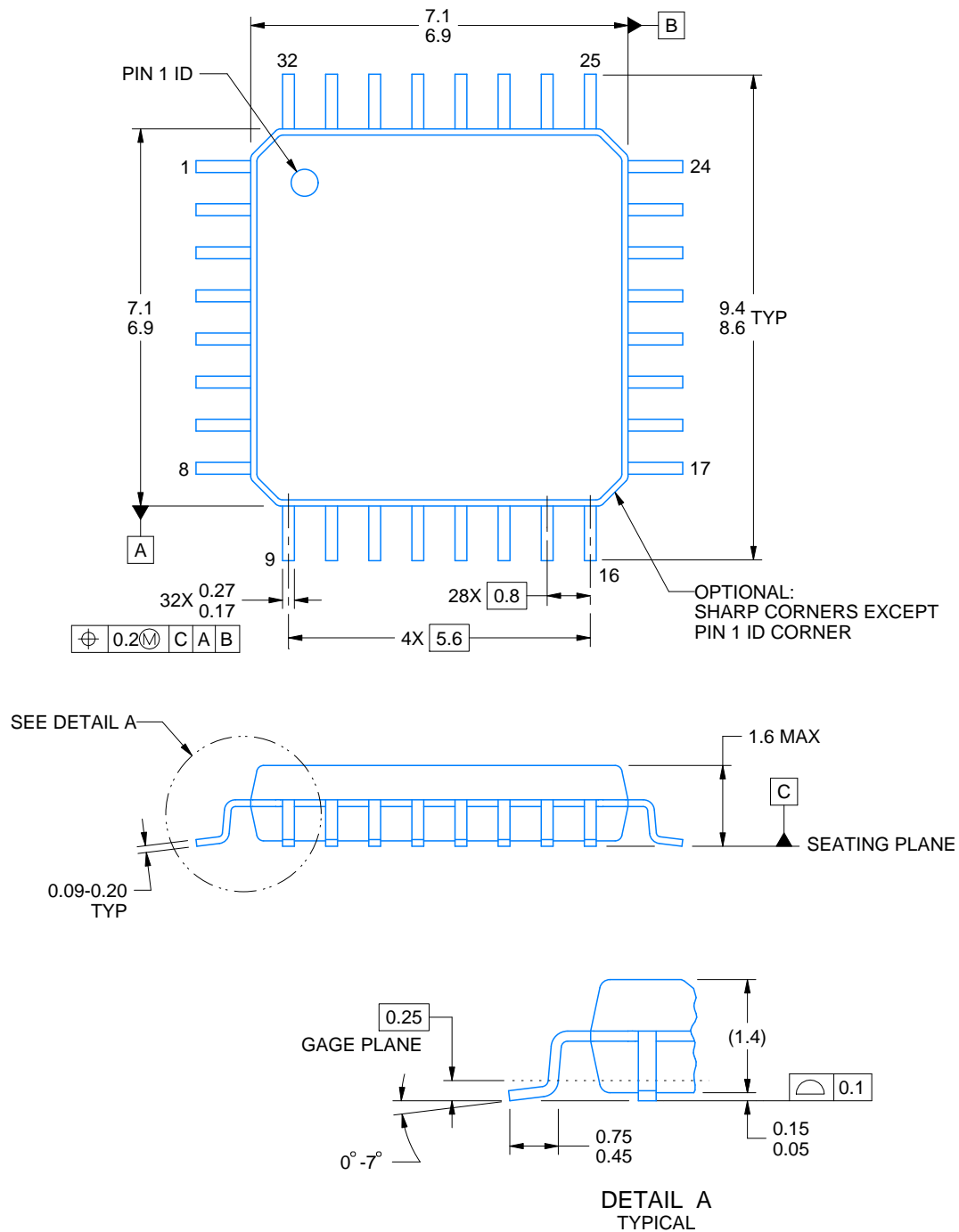
NEY0032A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4219901/A 10/2016

NOTES:

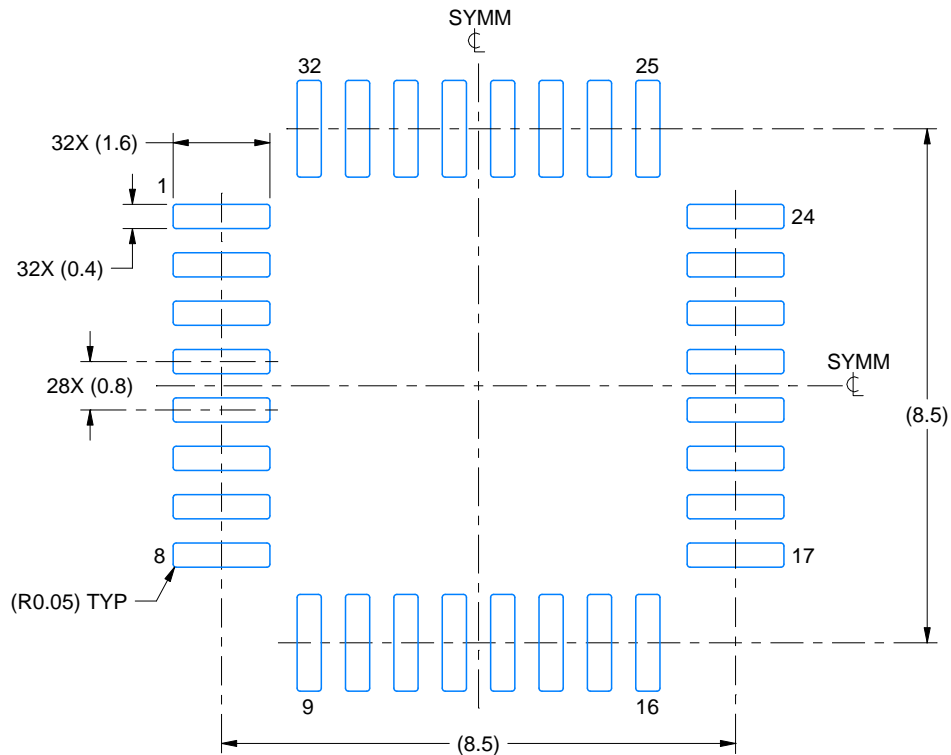
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

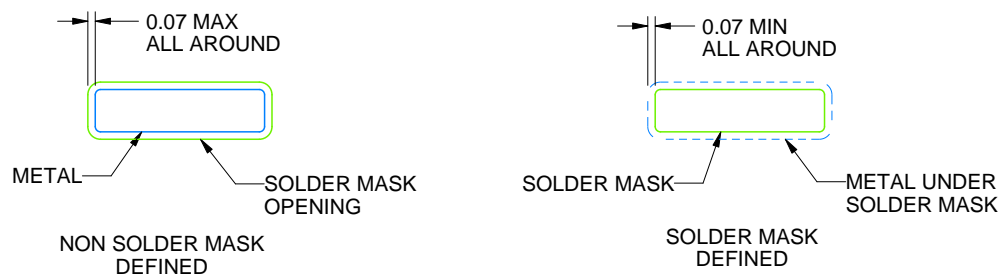
NEY0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4219901/A 10/2016

NOTES: (continued)

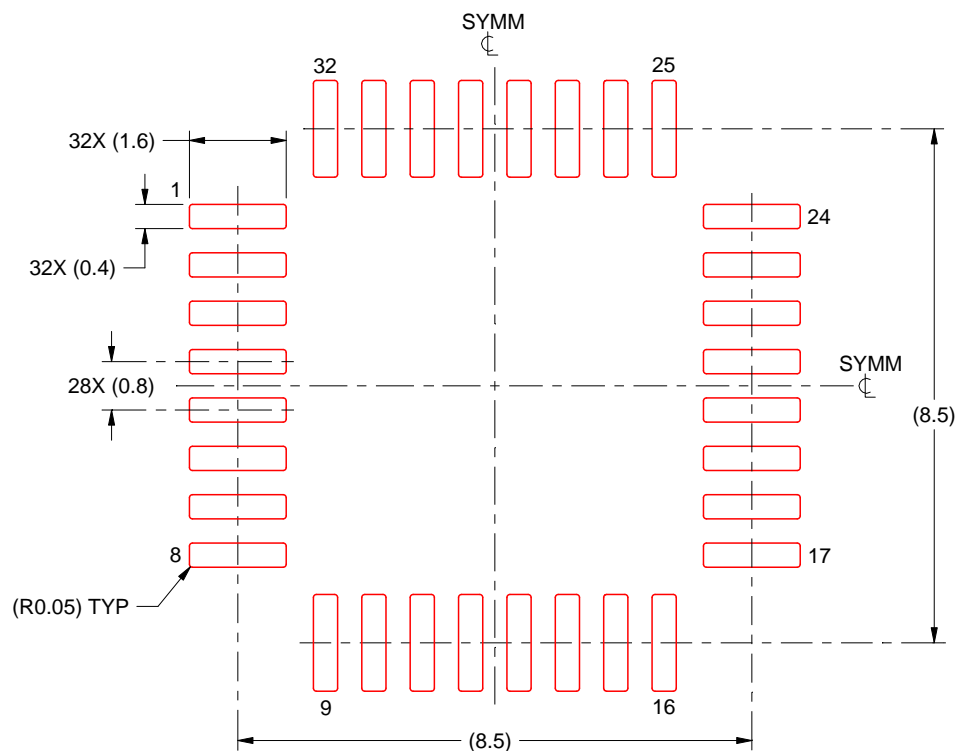
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NEY0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

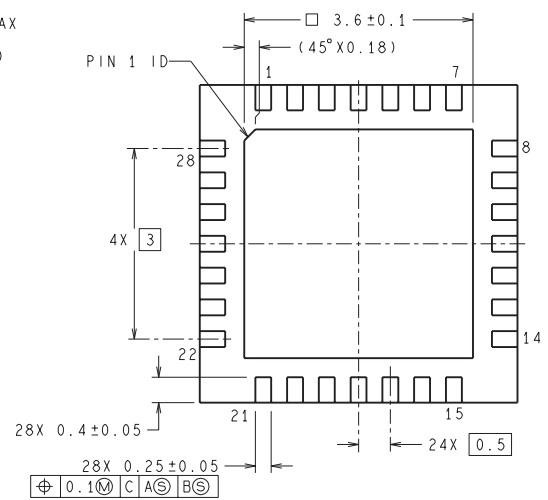


SOLDER PASTE EXAMPLE
SCALE 8X

4219901/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated