DS42MB100 4.25-Gbps 2:1/1:2 CML MUX/Buffer With Transmit Pre-Emphasis and Receive Equalization

1 Features

- 2:1 Multiplexer and 1:2 Buffer
- 0.25-Gbps to 4.25-Gbps Fully Differential Data Paths
- Fixed Input Equalization
- Programmable Output Pre-Emphasis
- Independent Pre-Emphasis Controls
- Programmable Loopback Modes
- On-Chip Terminations
- ESD Rating of 6-kV HBM
- 3.3-V Supply
- Lead-Less WQFN-36 Package
- –40°C to +85°C Operating Temperature Range

2 Applications

- Backplane Drivers or Cable Drivers
- Redundancy and Signal Conditioning Applications
- CPRI/OBSAI

3 Description

The DS42MB100 device is a signal conditioning 2:1 multiplexer and 1:2 fan-out buffer designed for use in backplane-redundancy or cable driving applications. Signal conditioning features include continuous time linear equalization (CTLE) and programmable output pre-emphasis that enable data communication in FR4 backplane up to 4.25 Gbps. Each input stage has a fixed equalizer to reduce ISI distortion from board traces.

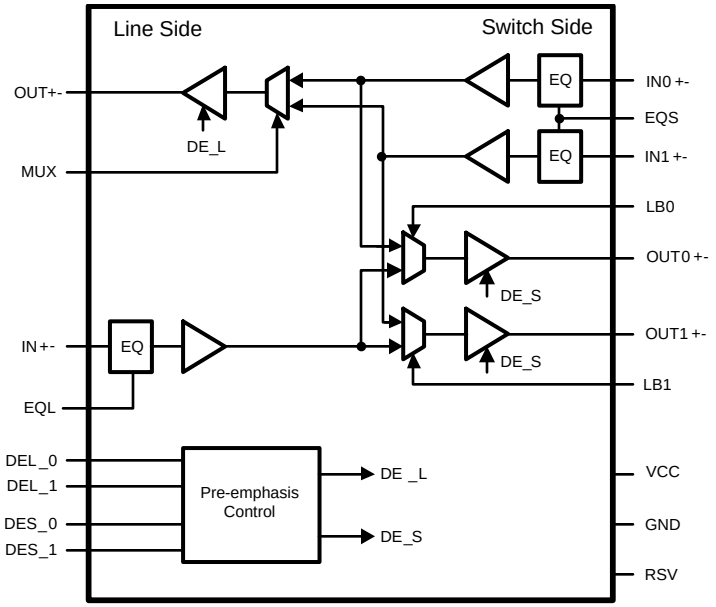
All output drivers have four selectable levels of pre-emphasis to compensate for transmission losses from long FR4 backplane or cable attenuation reducing deterministic jitter. The pre-emphasis levels can be independently controlled for the line-side and switch-side drivers. The internal loopback paths from switch-side input to switch-side output enable at-speed system testing. All receiver inputs are internally terminated with 100-Ω differential terminating resistors. All driver outputs are internally terminated with 50-Ω terminating resistors to V_{CC}.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS42MB100	WQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2013) to Revision H **Page**

- Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Thermal Information* table, *Parameter Measurement Information* section, *Feature Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed thermal information per latest modeling results ... 5
- Changed board trace attenuation estimate, per recent measurement ... 14

Changes from Revision F (April 2013) to Revision G **Page**

- Changed layout of National Data Sheet to TI format ... 12

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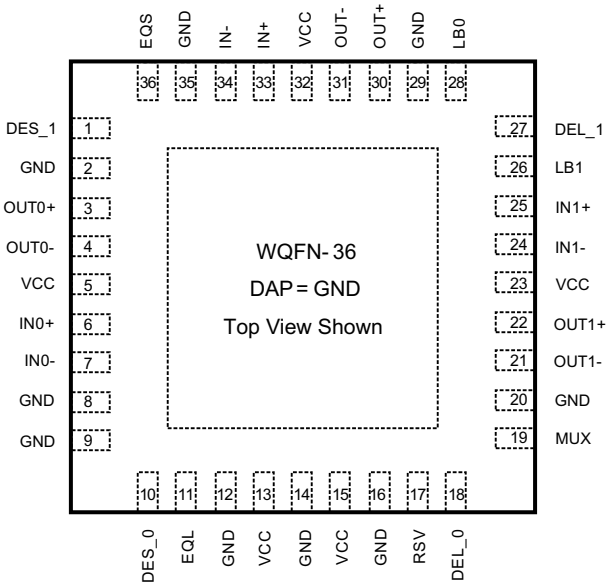
5 Pin Configuration and Functions

NJK Package
36-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
LINE SIDE HIGH SPEED DIFFERENTIAL I/Os			
IN+ IN−	33 34	I	Inverting and non-inverting differential inputs at the line side. IN+ and IN− have an internal 50 Ω connected to an internal reference voltage. See Figure 8.
OUT+ OUT−	30 31	O	Inverting and non-inverting differential outputs at the line side. OUT+ and OUT− have an internal 50 Ω connected to V_{CC}.
SWITCH SIDE HIGH SPEED DIFFERENTIAL I/Os			
IN0+ IN0−	6 7	I	Inverting and non-inverting differential inputs to the MUX at the switch side. IN0+ and IN0− have an internal 50 Ω connected to an internal reference voltage. See Figure 8.
IN1+ IN1−	25 24	I	Inverting and non-inverting differential inputs to the MUX at the switch side. IN1+ and IN1− have an internal 50 Ω connected to an internal reference voltage. See Figure 8.
OUT0+ OUT0−	3 4	O	Inverting and non-inverting differential outputs at the switch side. OUT0+ and OUT0− have an internal 50 Ω connected to V_{CC}.
OUT1+ OUT1−	22 21	O	Inverting and non-inverting differential outputs at the switch side. OUT1+ and OUT1− have an internal 50 Ω connected to V_{CC}.
CONTROL (3.3-V LVCMOS)			
DEL_0 DEL_1	18 27	I	DEL_0 and DEL_1 select the output pre-emphasis of the line side drivers (OUT±). DEL_0 and DEL_1 are internally pulled high.
DES_0 DES_1	10 1	I	DES_0 and DES_1 select the output pre-emphasis of the switch side drivers (OUT0±, OUT1±). DES_0 and DES_1 are internally pulled high.
EQL	11	I	A logic low enables the input equalizer on the line side. EQL is internally pulled high. Default is with EQ disabled.
EQS	36	I	A logic low enables the input equalizer on the switch side. EQS is internally pulled high. Default is with EQ disabled.
LB0	28	I	A logic low at LB0 enables the internal loopback path from IN0± to OUT0±. LB0 is internally pulled high.
LB1	26	I	A logic low at LB1 enables the internal loopback path from IN1± to OUT1±. LB1 is internally pulled high.
MUX	19	I	A logic low at MUX selects IN1±. MUX is internally pulled high. Default state for MUX is IN0±.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RSV	17	I	Reserve pin to support factory testing. This pin can be left open, or tied to GND, or tied to GND through an external pull-down resistor.
POWER			
GND	2, 8, 9, 12, 14, 16, 20, 29, 35	P	Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin.
GND	DAP	P	DAP is the metal contact at the bottom side, located at the center of the WQFN package. It should be connected to the GND plane with at least 16 via to lower the ground impedance and improve the thermal performance of the package.
V_{CC}	5, 13, 15, 23, 32	P	V_{CC} = 3.3 V ± 5%. Each V_{CC} pin should be connected to the V_{CC} plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V_{CC} pin. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each V_{CC} pin to ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)(2)

	MIN	MAX	UNIT
Supply voltage (V_{CC})	–0.3	4	V
CMOS/TTL input voltage	–0.3	V_{CC} + 0.3	V
CML input/output voltage	–0.3	V_{CC} + 0.3	V
Junction temperature		150	°C
Lead temperature (soldering, 4 seconds)		260	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), 1.5 kΩ, 100 pF, per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1250	
		Machine model	±350	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Ratings

	MIN	NOM	MAX	UNIT
Supply voltage (V_{CC} – GND)	3.135	3.3	3.465	V
Supply noise amplitude (10 Hz to 2 GHz)			100	mV_{PP}
Ambient temperature	–40		85	°C
Case temperature			100	°C

6.4 Thermal Information

THERMAL METRIC[1]		DS42MB100 NJK (WQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	32.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistances are based on having 16 thermal relief vias on the DAP pad under the 0 airflow condition.

6.5 Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
LVCMOS DC SPECIFICATIONS							
V_{IH}	High level input voltage			2		V_{CC} + 0.3	V
V_{IL}	Low level input voltage			–0.3		0.8	V
I_{IH}	High level input current	$V_{IN} = V_{CC}$		–10		10	µA
I_{IL}	Low level input current	V_{IN} = GND		75	94	124	µA
R_{PU}	Pull-high resistance				35		kΩ
RECEIVER SPECIFICATIONS							
V_{ID}	Differential input voltage range[2]	AC coupled differential signal. This parameter is not tested at production.	Below 1.25 Gbps	100		1750	mV_{P-P}
			Between 1.25 Gbps–3.125 Gbps	100		1560	
			Above 3.125 Gbps	100		1200	
V_{ICM}	Common-mode voltage at receiver inputs	Measured at receiver inputs reference to ground.			1.3		V
R_{ITD}	Input differential termination[3]	On-chip differential termination between IN+ or IN−.		84	100	116	Ω

(1) Typical parameters measured at V_{CC} = 3.3 V, T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(2) This parameter is specified by design and/or characterization. It is not tested in production.
(3) IN+ and IN− are generic names refer to one of the many pairs of complimentary inputs of the DS42MB100. OUT+ and OUT− are generic names refer to one of the many pairs of the complimentary outputs of the DS42MB100. Differential input voltage V_{ID} is defined as |IN+–IN−|. Differential output voltage V_{OD} is defined as |OUT+–OUT−|.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER SPECIFICATIONS							
V_{ODB}	Output differential voltage swing without pre-emphasis(4)	R_L = 100 Ω ±1% DES_1 = DES_0 = 0 DEL_1 = DEL_0 = 0 Driver pre-emphasis disabled. Running K28.7 pattern at 4.25 Gbps. See Figure 6 for test circuit.		1100	1300	1500	mV_{P-P}
V_{PE}	Output pre-emphasis voltage ratio 20 × log (VODPE / VODB)	R_L = 100 Ω ±1% Running K28.7 pattern at 4.25 Gbps x = S for switch side pre-emphasis control x = L for line side pre-emphasis control See Figure 9 on waveform. See Figure 6 for test circuit.	DEx_[1:0] = 00		0		dB
			DEx_[1:0] = 01		–3		
			DEx_[1:0] = 10		–6		
			DEx_[1:0] = 11		–9		
T_{PE}	Pre-emphasis width	Tested at −9-dB pre-emphasis level, DEx[1:0] = 11 x = S for switch side pre-emphasis control x = L for line side pre-emphasis control See Figure 3 on measurement condition.		125	188	250	ps
R_{OTSE}	Output termination(3)	On-chip termination from OUT+ or OUT− to V_{CC}		42	50	58	Ω
R_{OTD}	Output differential termination	On-chip differential termination between OUT+ and OUT−			100		Ω
ΔR_{OTSE}	Mismatch in output termination resistors	Mismatch in output terminations at OUT+ and OUT−				5%	
V_{OCM}	Output common mode voltage				2.7		V
POWER DISSIPATION							
P_D	Power dissipation	V_{DD} = 3.3 V at 25°C All outputs terminated by 100 Ω ±1%. DEL_[1:0] = 0, DES_[1:0] = 0 Running PRBS 2^7 – 1 pattern at 4.25 Gbps			0.45		W
AC CHARACTERISTICS							
RJ	Device random jitter(5)	See Figure 6 for test circuit. Alternating 1-0 pattern. EQ and pre-emphasis disabled.	At 0.25 Gbps			2	ps_{rms}
			At 1.25 Gbps			2	
			At 4.25 Gbps			2	
DJ	Device deterministic jitter(6)	See Figure 6 for test circuit. EQ and pre-emphasis disabled	Between 0.25 and 4.25 Gbps with PRBS7 pattern for DS42MB100 at –40°C to 85°C			35	ps_{p-p}
DR	Data rate(2)	Tested with alternating 1-0 pattern		0.25		4.25	Gbps

(4) K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000} K28.5 pattern is a 20-bit repeating pattern of +K28.5 and −K28.5 code groups {110000 0101 001111 1010}

(5) Device output random jitter is a measurement of the random jitter contribution from the device. It is derived by the equation $sqrt(RJ_{OUT}^2 – RJ_{IN}^2)$, where RJ_{OUT} is the total random jitter measured at the output of the device in ps_{rms}, RJ_{IN} is the random jitter of the pattern generator driving the device.

(6) Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation $(DJ_{OUT} – DJ_{IN})$, where DJ_{OUT} is the total peak-to-peak deterministic jitter measured at the output of the device in ps_{p-p}, DJ_{IN} is the peak-to-peak deterministic jitter of the pattern generator driving the device.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Differential low to high transition time	Measured with a clock-like pattern at 4.25 Gbps, between 20% and 80% of the differential output voltage. Pre-emphasis disabled. Transition time is measured with fixture as shown in Figure 6, adjusted to reflect the transition time at the output pins.		85		ps
t_F	Differential high to low transition time			85		ps
t_{PLH}	Differential low to high propagation delay	Measured at 50% differential voltage from input to output.			1	ns
t_{PHL}	Differential high to low propagation delay				1	ns
t_{SKP}	Pulse skew	$\lvert t_{PHL} - t_{PLH} \rvert$			20	ps
t_{SKO}	Output skew(1)	Difference in propagation delay among data paths in the same device.			100	ps
t_{SKPP}	Part-to-part skew	Difference in propagation delay between the same output from devices operating under identical condition.			100	ps
t_{SM}	MUX switch time	Measured from V_{IH} or V_{IL} of the MUX-control or loopback control to 50% of the valid differential output.		1.8	6	ns

(1) t_{SKO} is the magnitude difference in the propagation delays among data paths. An example is the output skew among data paths from IN0± to OUT± and IN1± to OUT±.. Another example is the output skew among data paths from IN± to OUT0± and IN± to OUT1±. t_{SKO} also refers to the delay skew of the loopback paths of the same port and between similar data paths. An example is the output skew among data paths IN0± to OUT0± and IN1± to OUT1±.

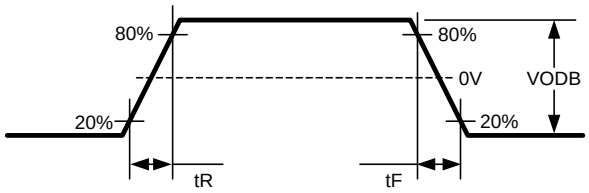

Figure 1. Driver Output Transition Time

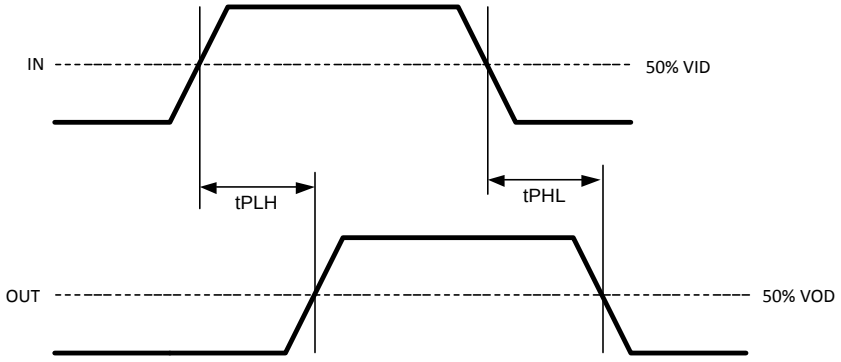

Figure 2. Propagation Delay From Input To Output

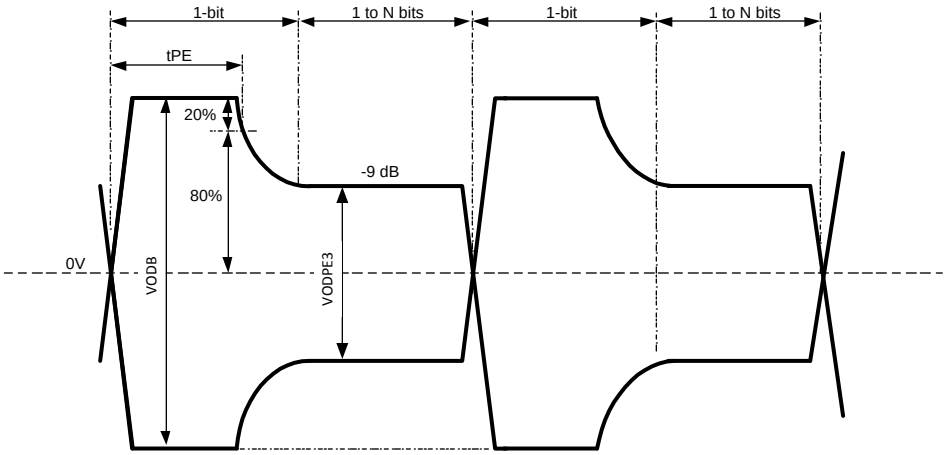

Figure 3. Test Condition For Output Pre-Emphasis Duration

6.7 Typical Characteristics

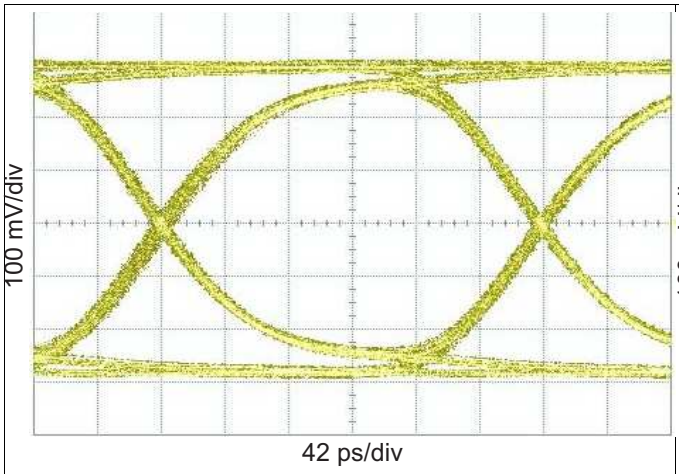

Figure 4. PRBS-7, Pre-Emphasis = 0 dB at 4 Gbps

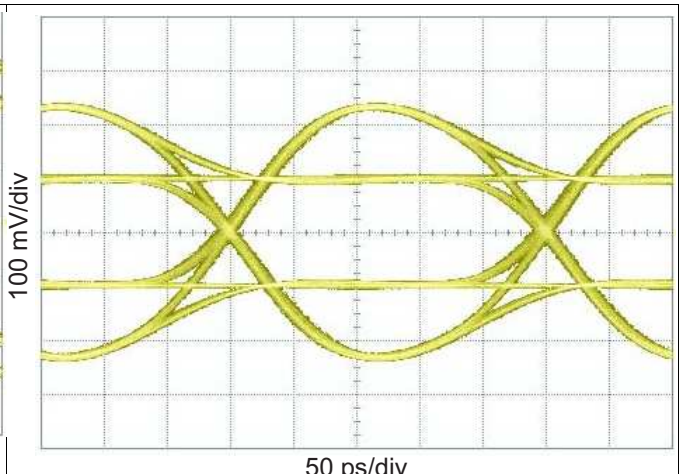

Figure 5. PRBS-7, Pre-Emphasis = –9 dB at 4 Gbps

7 Parameter Measurement Information

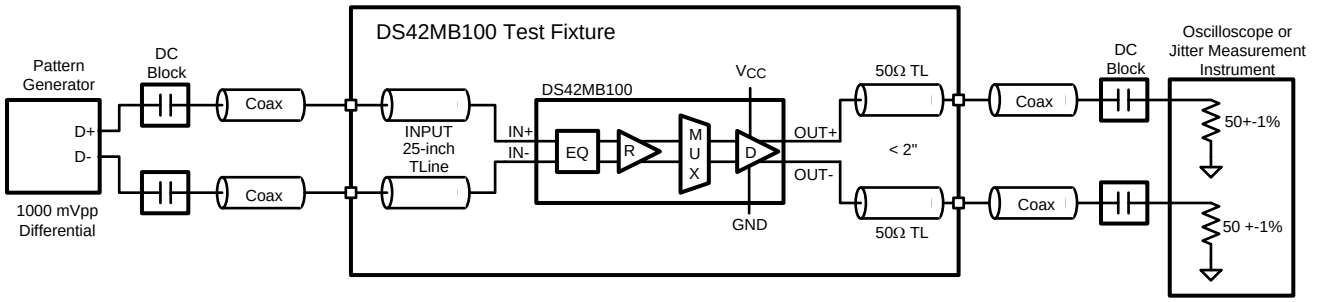

Figure 6. AC Test Circuit

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8 Detailed Description

8.1 Overview

The DS42MB100 is a signal conditioning 2:1 multiplexer and a 1:2 buffer designed to support port redundancy with encoded or scrambled data rates between 0.25 and 4.25 Gbps. The DS42MB100 provides fixed equalization at the receive input and pre-emphasis control on the output in order to support signal reach extension.

8.2 Functional Block Diagram

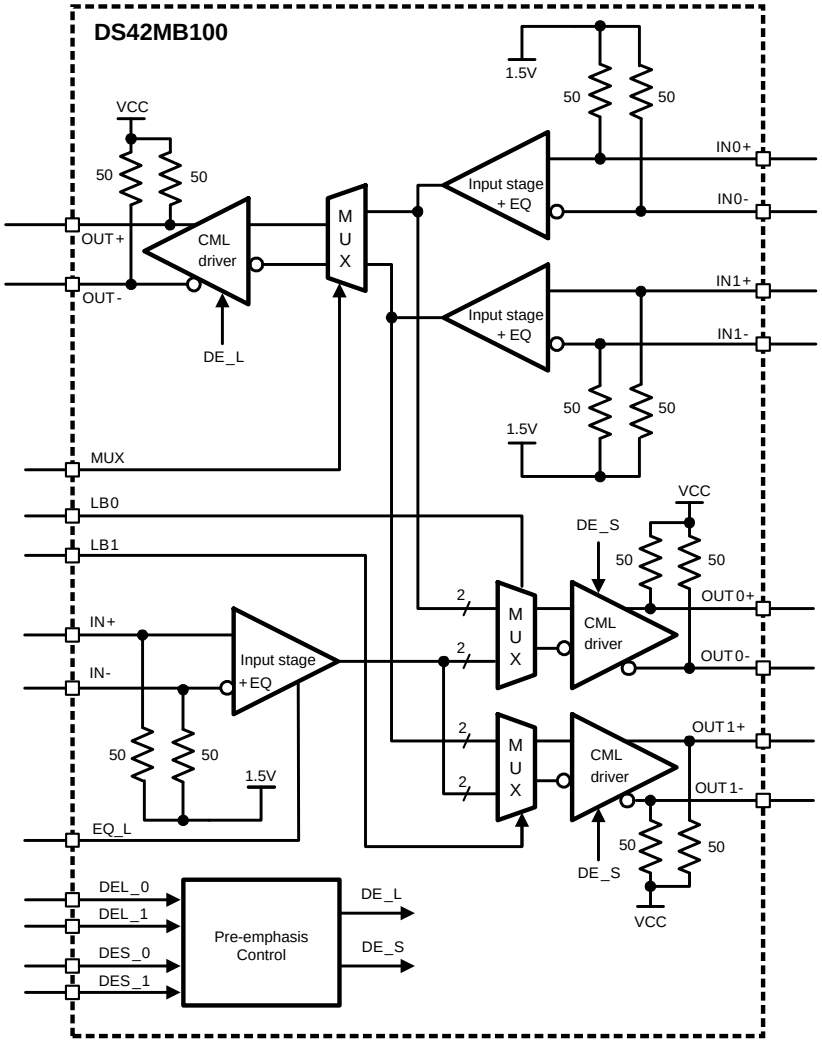

Figure 7. Simplified Block Diagram

8.3 Feature Description

The DS42MB100 MUX buffer consists of several key blocks:

- CML Inputs and EQ
- Multiplexer and Loopback Control
- CML Drivers and Pre-Emphasis Control

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Feature Description (continued)

8.3.1 CML inputs and EQ

The high speed inputs are self-biased to about 1.3 V at IN+ and IN- and are designed for AC coupling, allowing the DS42MB100 to be inserted directly into the datapath without any limitation. See Figure 8 for details about the internal receiver input termination and bias circuit.

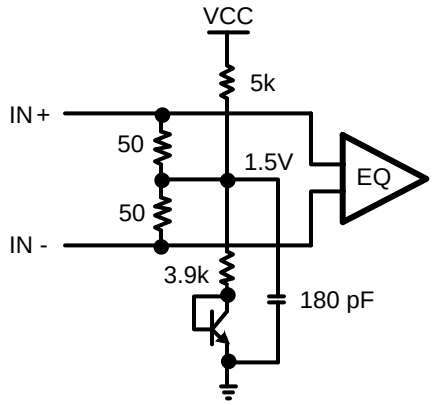

Figure 8. Receiver Input Termination and Bias Circuit

The inputs are compatible to most AC coupling differential signals such as LVDS, LVPECL, and CML. The ideal AC coupling capacitor value is often based on the lowest frequency component embedded within the serial link. A typical AC coupling capacitor value ranges between 100 and 1000 nF. Some specifications with scrambled data may require a larger coupling capacitor for optimal performance. To reduce unwanted parasitics around and within the AC coupling capacitor, a body size of 0402 is recommended. Figure 6 shows the AC coupling capacitor placement in an AC test circuit.

Each input stage has a fixed equalizer that provides equalization to compensate about 5 dB (at 2 GHz) of transmission loss from a short backplane trace (about 10 inches backplane). EQ can be enabled or disabled with the EQL and EQS pins.

Table 1. EQ Controls for Line and Switch Inputs

PIN	PIN VALUE	EQUALIZER FUNCTION
EQL, EQS	0	Enable equalization.
	1 (default)	Normal mode. Equalization disabled.

8.3.2 Multiplexer and Loopback Control

Table 2 and Table 3 provide details about how to configure the DS42MB100 multiplexer and loopback settings.

Table 2. Logic Table for Multiplex Controls

PIN	PIN VALUE	MUX FUNCTION
MUX	0	MUX select switch input IN1±.
	1 (default)	MUX select switch input IN0±.

Table 3. Logic Table for Loopback Controls

PIN	PIN VALUE	LOOPBACK FUNCTION
LB0	0	Enable loopback from IN0± to OUT0±.
	1 (default)	Normal mode. Loopback disabled.
LB1	0	Enable loopback from IN1± to OUT1±.
	1 (default)	Normal mode. Loopback disabled.

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8.3.3 CML Drivers and Pre-Emphasis Control

The output driver has pre-emphasis (driver-side equalization) to compensate the transmission loss of the backplane that it is driving. The driver conditions the output signal such that the lower frequency and higher frequency pulses reach approximately the same amplitude at the end of the backplane and minimize the deterministic jitter caused by the amplitude disparity. The DS42MB100 provides four steps of user-selectable pre-emphasis ranging from 0, –3, –6 and –9 dB to handle different lengths of backplane. Figure 9 shows a driver pre-emphasis waveform. The pre-emphasis duration is 188 ps nominal, corresponding to 0.8 unit intervals (UI) at 4.25 Gbps. The pre-emphasis levels of switch-side and line-side can be individually programmed.

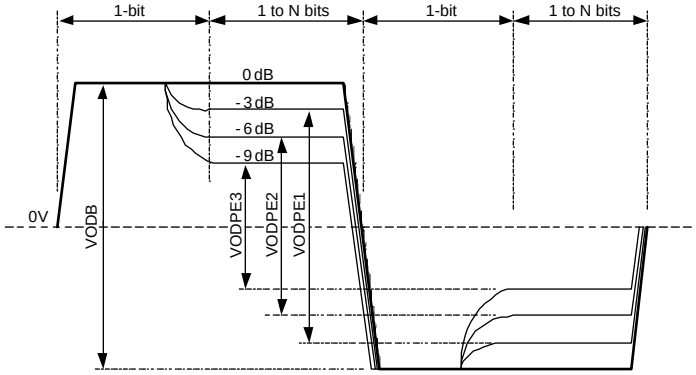

Figure 9. Driver Pre-Emphasis Differential Waveform (Showing All 4 Pre-Emphasis Steps)

Table 4. Line-Side Pre-Emphasis Controls

DEL_[1:0]	PRE-EMPHASIS LEVEL IN mV_{PP} (VODB)	PRE-EMPHASIS LEVEL IN mV_{PP} (VODPE)	PRE-EMPHASIS IN dB (VODPE/VODB)	TYPICAL FR4 BOARD TRACE
0 0	1300	1300	0	10 inches
0 1	1300	920	−3	20 inches
1 0	1300	650	−6	30 inches
1 1 (default)	1300	461	−9	40 inches

Table 5. Switch-Side Pre-Emphasis Controls

DES_[1:0]	PRE-EMPHASIS LEVEL IN mV_{PP} (VODB)	PRE-EMPHASIS LEVEL IN mV_{PP} (VODPE)	PRE-EMPHASIS IN dB (VODPE/VODB)	TYPICAL FR4 BOARD TRACE
0 0	1300	1300	0	10 inches
0 1	1300	920	−3	20 inches
1 0	1300	650	−6	30 inches
1 1 (default)	1300	461	−9	40 inches

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS42MB100 is a 2:1 MUX and 1:2 buffer that equalizes input data up to 4.25 Gbps and provides transmit pre-emphasis controls to improve overall signal reach. As a MUX buffer, the DS42MB100 is ideal for designs where there is a need for port sharing or redundancy as well as on-the-fly reorganization of routes and data connections.

9.2 Typical Application

A typical application for the DS42MB100 is shown in Figure 10 and Figure 11.

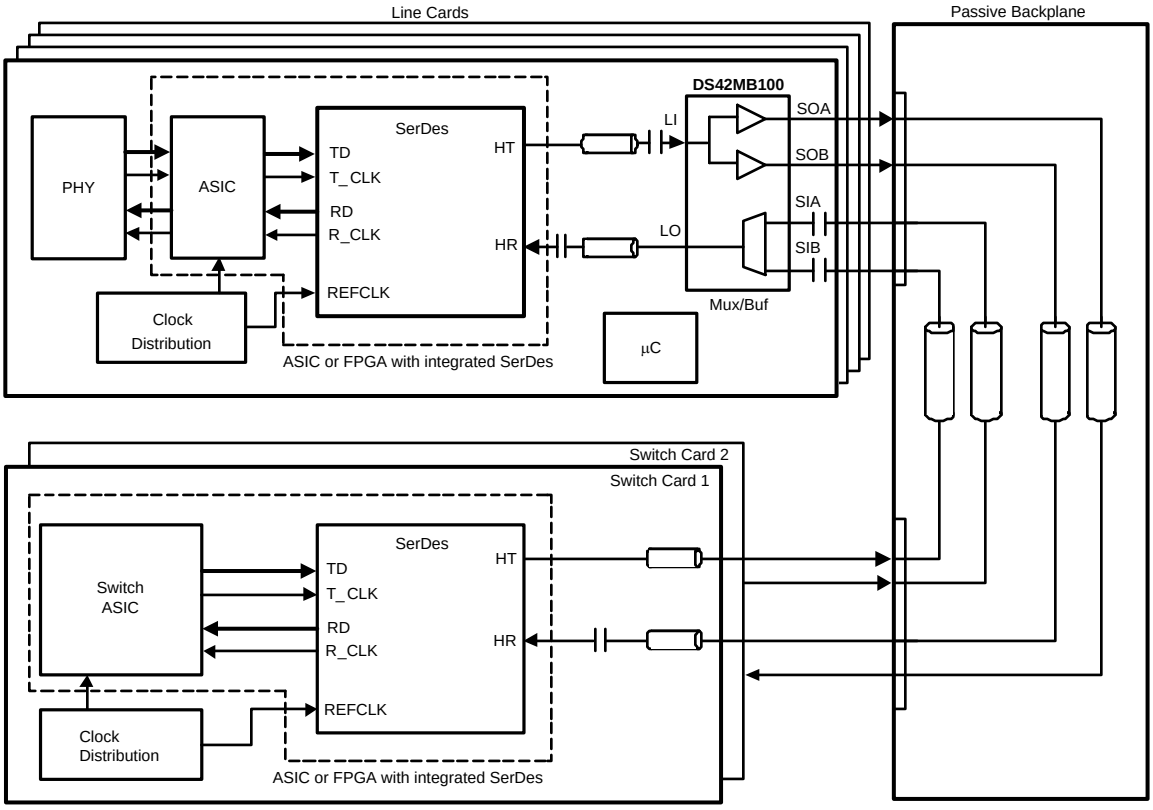

Figure 10. Network Switch System With Redundancy

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Typical Application (continued)

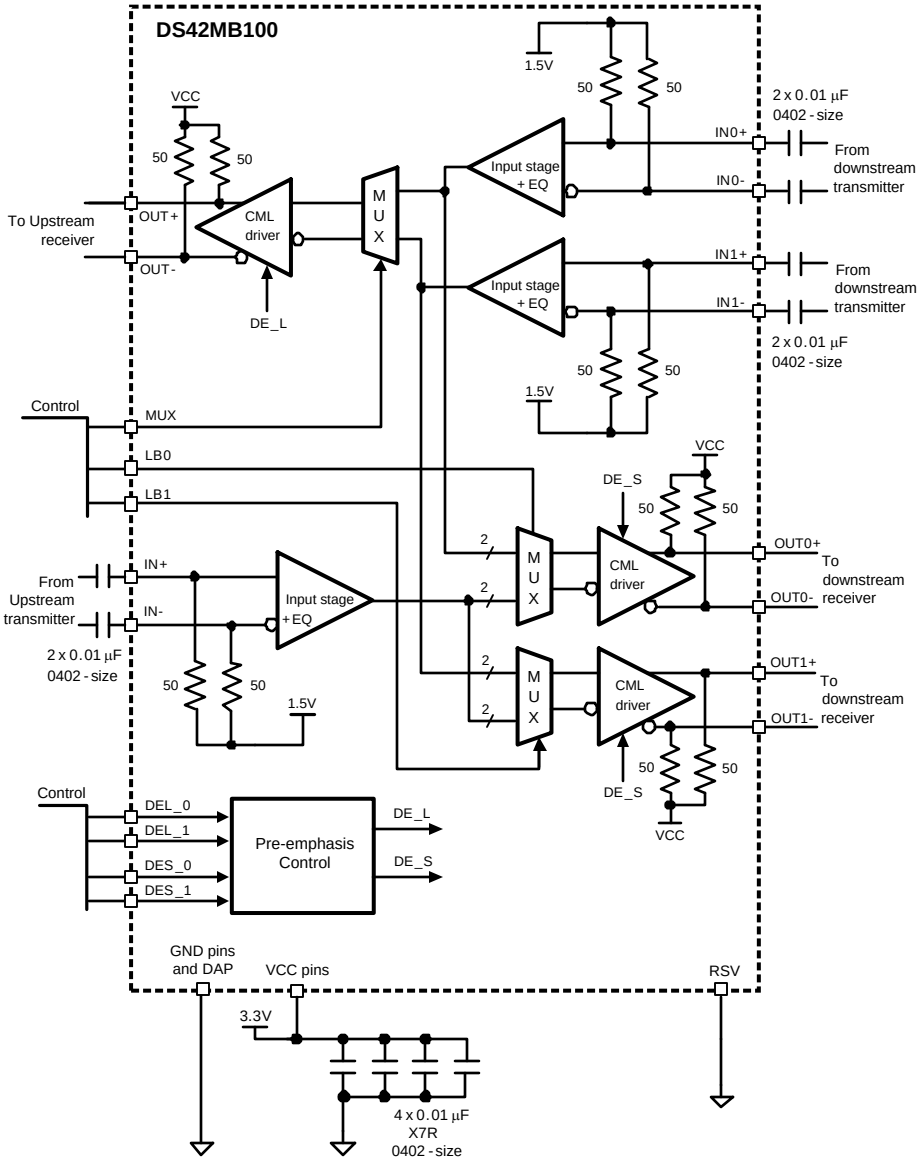

Figure 11. DS42MB100 Connection Block Diagram

9.2.1 Design Requirements

In a typical design, the DS42MB100 equalizes a short backplane trace on its input, followed by a longer trace at the DS42MB100 output. In this application example, a 25-inch FR4 coupled micro-strip board trace is used in place of the short backplane link. A block diagram of this example is shown in Figure 12.

Typical Application (continued)

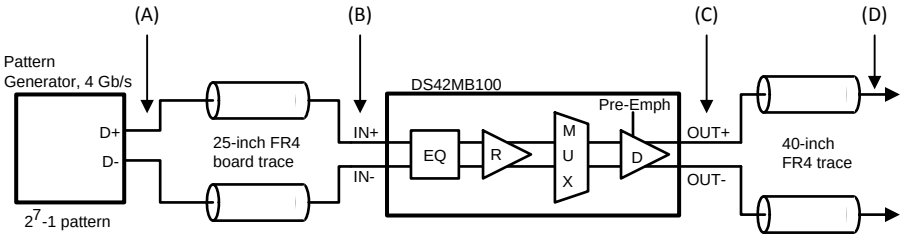

Figure 12. Block Diagram of DS42MB100 Application Example

The 25-inch microstrip board trace has approximately 6 dB of attenuation between 375 MHz and 1.875 GHz, representing closely the transmission loss of the short backplane transmission line. The 25-inch microstrip is connected between the pattern generator and the differential inputs of the DS42MB100 for AC measurements.

Table 6. Input Trace Parameters

TRACE LENGTH	FINISHED TRACE WIDTH W	SEPARATION BETWEEN TRACES	DIELECTRIC HEIGHT H	DIELECTRIC CONSTANT ε_R	LOSS TANGENT
25 inches	8.5 mil	11.5 mil	6 mil	3.8	0.022

The length of the output trace may vary based on system requirements. In this example, a 40-inch FR4 trace with similar trace width, separation, and dielectric characteristics, is placed at the DS42MB100 output.

As with any high speed design, there are many factors which influence the overall performance. Following is a list of critical areas for consideration and study during design.

- Use 100-Ω impedance traces. Generally these are very loosely coupled to ease routing length differences.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- The maximum body size for AC-coupling capacitors is 0402.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

9.2.2 Detailed Design Procedure

For optimal design, the DS42MB100 must be configured to route incoming data correctly as well as provide the best signal quality. The following design procedures should be observed:

1. The DS42MB100 should be configured to provide the correct MUX and buffer routes in order to satisfy system requirements. In order to set the appropriate MUX control settings, refer to Table 2. To configure the buffer control settings, refer to Table 3. For example, consider the case where the designer wishes to route the input from Switch Card 0 (IN0±) to the output for the line card (OUT±). To accomplish this, set MUX = 1 (select IN0±). For the other direction from line card output to switch card, set LB0 = 1 and LB1 = 1 so that the input from the line card is buffered to both Switch Card 0 (OUT0±) and Switch Card 1 (OUT1±).
2. The DS42MB100 is designed to be placed at an offset location with respect to the overall channel attenuation. To optimize performance, determine whether input and output equalization is required. Set EQL = 0 and EQS = 0 to enable input equalization. The MUX buffer transmit pre-emphasis can be tuned to extend the trace length reach while also recovering a solid eye opening. To tune transmit pre-emphasis on either the line card side or switch card side, refer to Table 4 and Table 5 for recommended pre-emphasis control settings according to the length of FR4 board trace connected at the DS42MB100 output. For example, if 40 inches of FR4 trace is connected to the switch card output, set DES_[1:0] = (1, 1) for VOD = 1200 mVpp and –9 dB of transmit pre-emphasis.

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9.2.3 Application Curves

Figure 13 through Figure 18 show how the signal integrity varies at different places in the data path. These measured locations can be referenced back to the labeled points provided in Figure 12.

- Point (A): Output signal of source pattern generator
- Point (B): Input to DS42MB100 after 25 inches of FR4 trace from source
- Point (C): Output of DS42MB100 driver
- Point (D): Signal after 40 inches of FR4 trace from DS42MB100 driver

The source signal is a PRBS-7 pattern at 4 Gbps. For the long output traces, the eye after 40 inches of output FR4 trace is significantly improved by adding –9 dB of pre-emphasis.

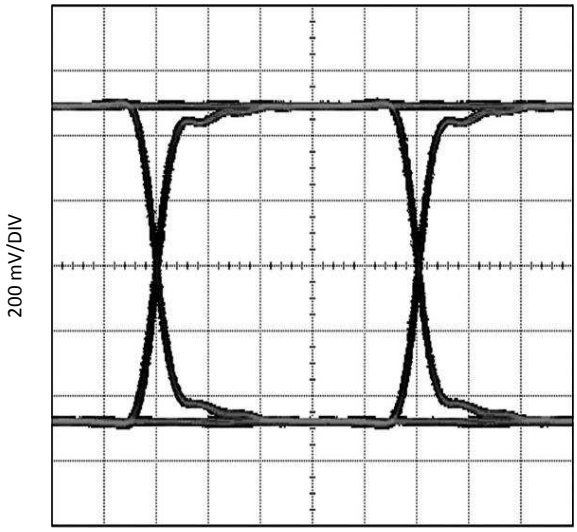

Figure 13. Eye Measured at Point (A)

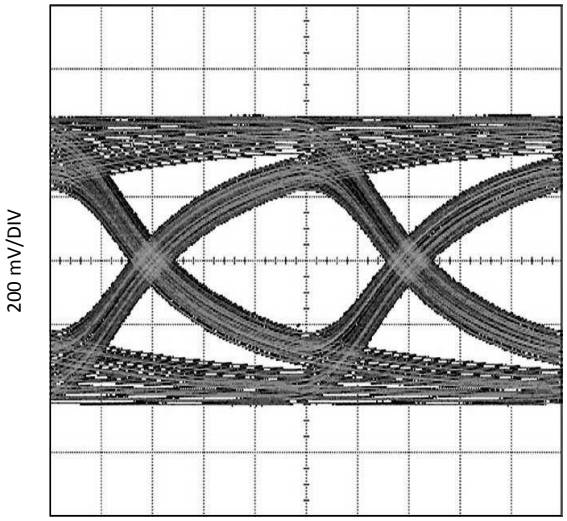

Figure 14. Eye Measured at Point (B)

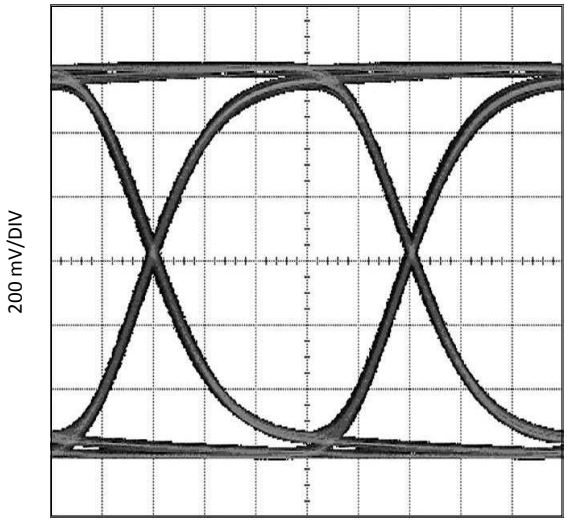

Figure 15. Eye Measured at Point (C), Pre-Emphasis = 0 dB

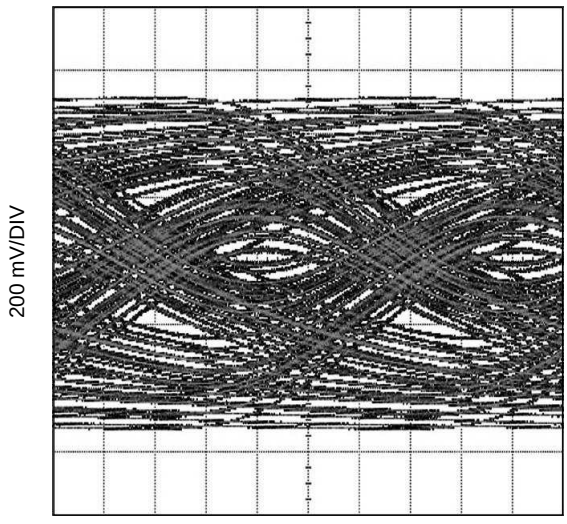

Figure 16. Eye Measured at Point (D), Pre-Emphasis = 0 dB

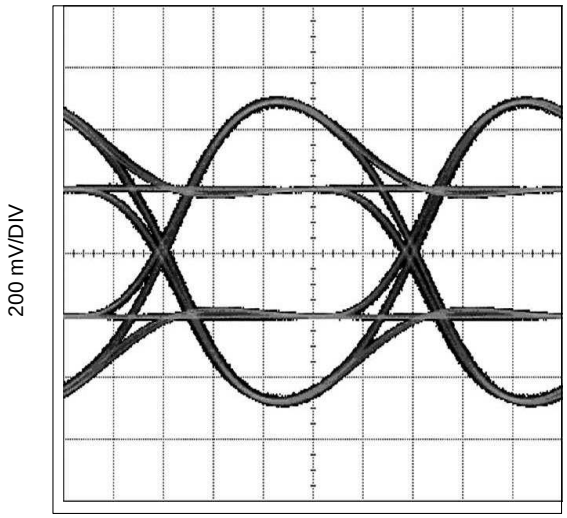

Figure 17. Eye Measured at Point (C), Pre-Emphasis = –9 dB

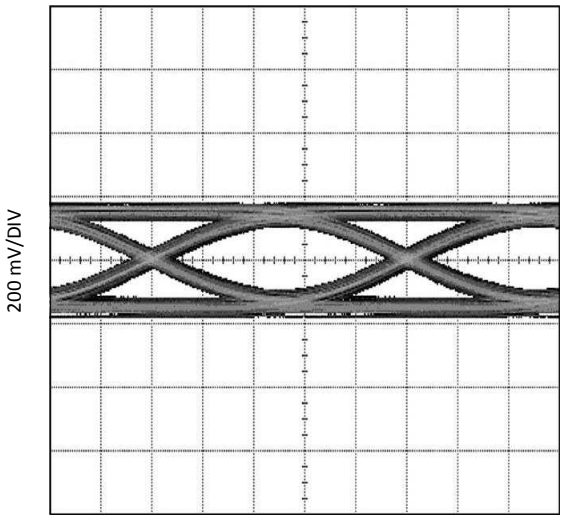

Figure 18. Eye Measured at Point (D), Pre-Emphasis = –9 dB

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10 Power Supply Recommendations

The supply (V_{CC}) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{CC} and GND planes create a low inductance supply with distributed capacitance. Careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01-µF or 0.1-µF bypass capacitor should be connected to each V_{CC} pin such that the capacitor is placed as close as possible to the V_{CC} pins. Smaller body size capacitors, such as 0402 body size, can help facilitate proper component placement. Refer to the V_{CC} pin connections in Figure 11 for further details.

11 Layout

11.1 Layout Guidelines

Use at least a four layer board with a power and ground plane. Closely-coupled differential lines of 100 Ω are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus will be rejected by the receivers. Information on the WQFN style package is provided in *AN-1187 Leadless Leadframe Package (LLP)*, SNOA401.

11.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in Figure 19. A layout example for the DS42MB100 is shown in Figure 20, where 16 stencil openings are used for the DAP alongside nine vias to GND.

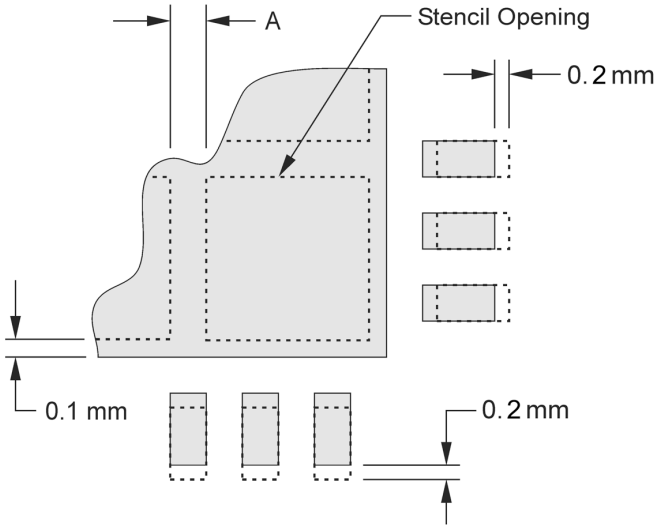

Figure 19. No Pullback WQFN, Single Row Reference Diagram

Table 7. No Pullback WQFN Stencil Aperture Summary for DS42MB100

DEVICE	PIN COUNT	MKT DWG	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS42MB100	36	SQA36A	0.25 × 0.6	0.5	4.6 × 4.6	0.25 × 0.7	1.0 × 1.0	16	0.2

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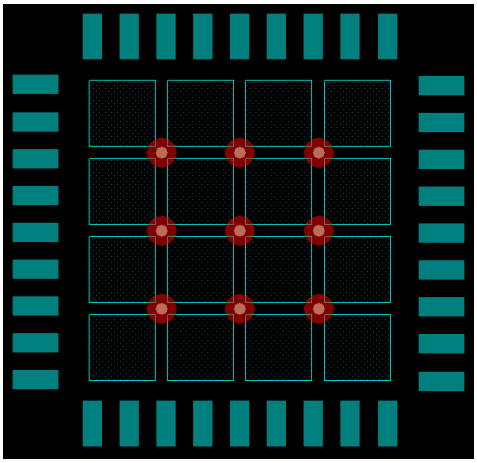

Figure 20. 36-Pin WQFN Stencil Example of Via and Opening Placement

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

AN-1187 Leadless Leadframe Package (LLP), SNOA401

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS42MB100TSQ/NOPB	ACTIVE	WQFN	NJK	36	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	42MB100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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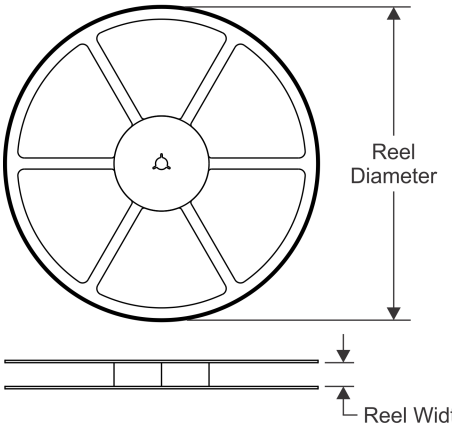
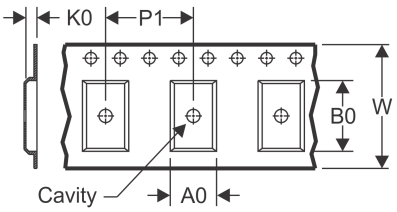
TAPE AND REEL INFORMATION

REEL DIMENSIONS

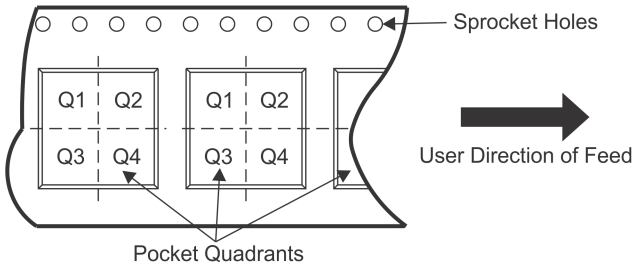


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

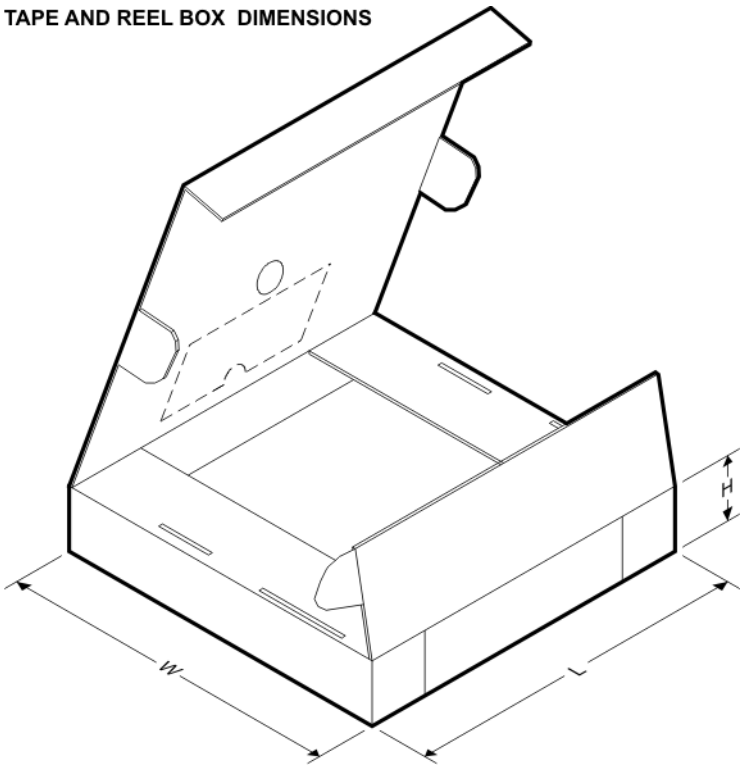
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS42MB100TSQ/NOPB	WQFN	NJK	36	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

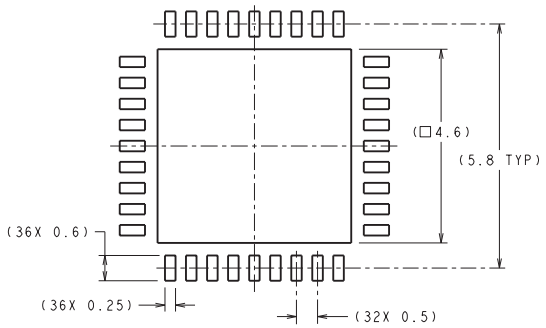
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

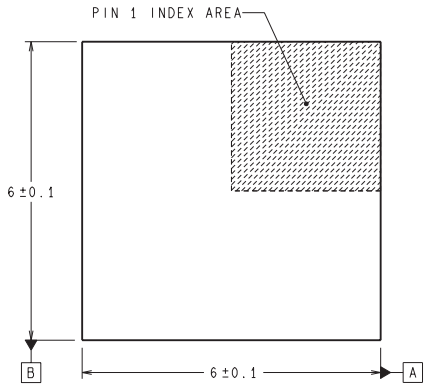
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS42MB100TSQ/NOPB	WQFN	NJK	36	250	210.0	185.0	35.0

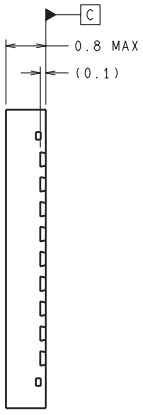
NJK0036A

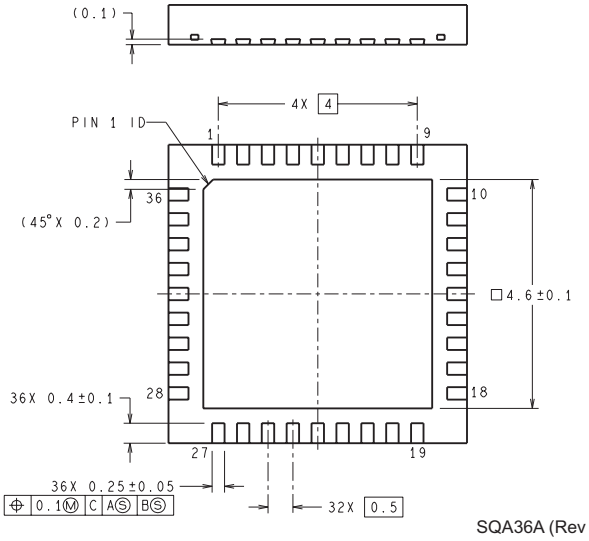


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







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