DS64BR401 Quad Bi-Directional Repeater with Equalization and De-Emphasis

Check for Samples: DS64BR401

FEATURES

- **Quad lane bi-directional repeater up to 6.4 Gbps rate**
- **Signal conditioning on input and output for extended reach**
- **Adjustable receive equalization up to +33 dB gain**
- **Adjustable transmit de-emphasis up to −12 dB**
- **Adjustable transmit VOD (600 mVp-p to 1200 mVp-p)**
- **<0.25 UI of residual DJ at 6.4 Gbps with 40" FR4 trace**
- **Automatic de-emphasis scaling based on rate detect**
- **SATA/SAS: OOB signal pass-through,**
  - **<3 ns (typ) envelope distortion**
- **Adjustable electrical IDLE detect threshold**
- **Low power (100 mW/channel), per-channel power down**
- **Programmable via pin selection or SMBus interface**
- **Single supply operation at 2.5V ±5%**
- **>6 kV HBM ESD Rating**
- **3.3V LVCMOS input tolerant for SMBus interface**
- **High speed signal flow–thru pinout package: 54-pin WQFN (10 mm x 5.5 mm)**

APPLICATIONS

- **SATA (1.5, 3.0 and 6 Gbps)**
- **SAS (1.5, 3.0 and 6 Gbps)**
- **XAUI (3.125 Gbps), RXAUI (6.25 Gbps)**
- **sRIO – Serial Rapid I/O**
- **Fibre Channel (4.25 Gbps)**
- **10GBase-CX4, InfiniBand 4x (SDR & DDR)**
- **QSFP active copper cable modules**
- **High-speed active cable and FR-4 backplane traces**

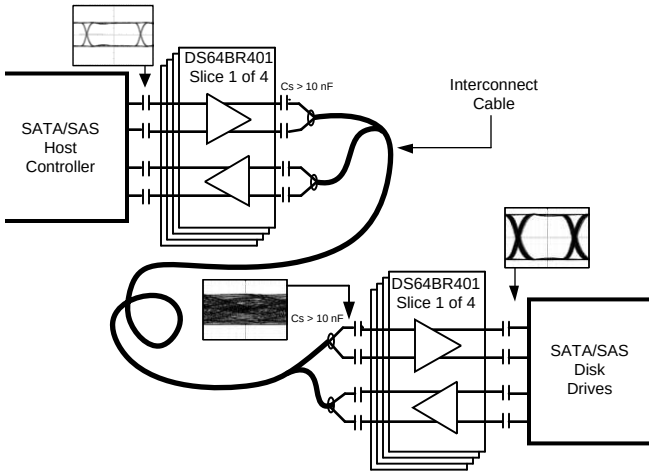
DESCRIPTION

The DS64BR401 is a quad lane bi-directional signal conditioning repeater for 6.0/3.0/1.5 Gbps SATA/SAS and other high-speed bus applications with data rates up to 6.4 Gbps. The device performs both receive equalization and transmit de-emphasis on each of its 8 channels to compensate for channel loss, allowing maximum flexibility of physical placement within a system. The receiver's continuous time linear equalizer (CTLE) provides a boost of up to +33 dB at 3 GHz and is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium. The transmitter features a programmable output de-emphasis driver and allows amplitude voltage levels to be selected from 600 mVp-p to 1200 mVp-p to suit multiple application scenarios. This Low Power Differential Signaling (LPDS) output driver is a power efficient implementation that maintains compatibility with AC coupled CML receiver. The programmable settings can be applied via pin settings or SMBus interface.

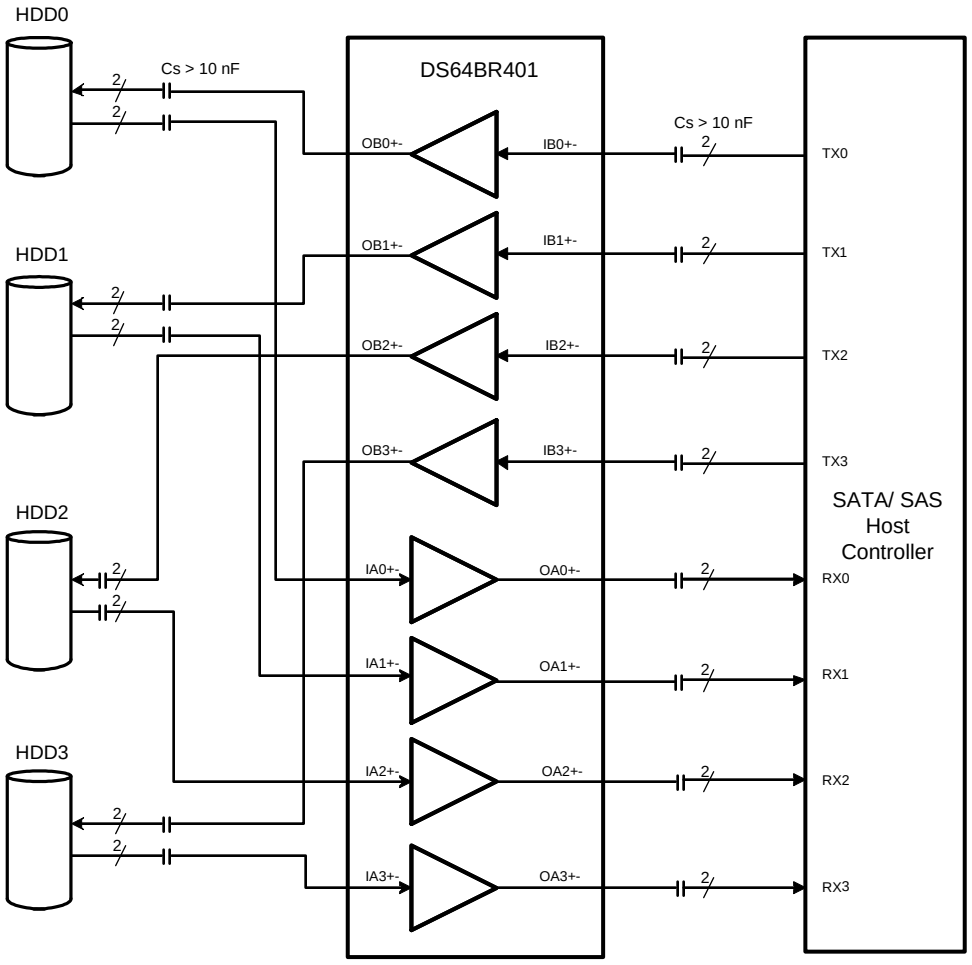
To enable seamless upgrade from SAS/SATA 3.0 Gbps to 6.0 Gbps data rates without compromising physical reach, DS64BR401 automatically detects the incoming data rate and selects the optimal de-emphasis pulse width. The device detects the out-of-band (OOB) idle and active signals of the SAS/SATA specification and passes through with minimum signal distortion.

With a typical power consumption of 200 mW/lane (100 mW/channel) at 6.4 Gbps, and control to turn-off unused channels, the DS64BR401 is part of Texas Instruments' PowerWise family of energy efficient devices.

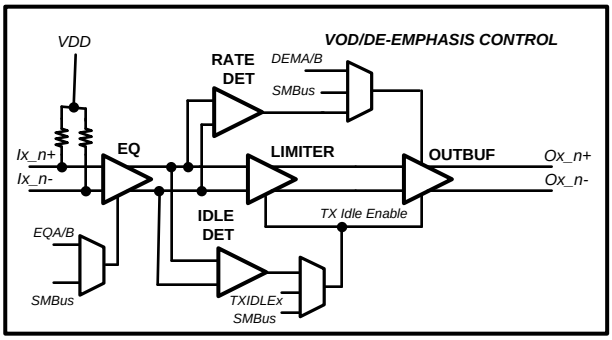
TYPICAL CABLE APPLICATION



TYPICAL APPLICATION CONNECTION DIAGRAM



BLOCK DIAGRAM - DETAIL VIEW OF THE EACH CHANNEL (1 OF 8)



PIN DIAGRAM

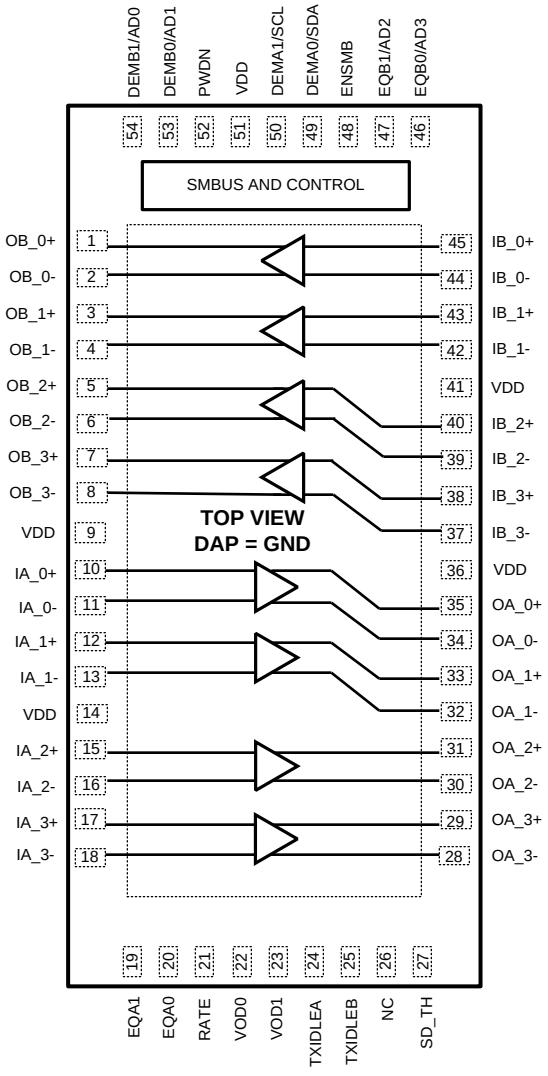


Figure 1. DS64BR401 Pin Diagram 54L WQFN

Table 1. PIN DESCRIPTIONS

Pin Name	Pin Number	I/O, Type	Pin Descriptions
Differential High Speed I/O's			
IA_0+, IA_0- , IA_1+, IA_1-, IA_2+, IA_2-, IA_3+, IA_3-	10, 11 12, 13 15, 16 17, 18	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects INA_n+ to VDD and INA_n- to VDD when enabled.
OA_0+, OA_0-, OA_1+, OA_1-, OA_2+, OA_2-, OA_3+, OA_3-	35, 34 33, 32 31, 30 29, 28	O, LPDS	Inverting and non-inverting low power differential signaling (LPDS) 50Ω outputs with de-emphasis. Compatible with AC coupled CML inputs.
IB_0+, IB_0- , IB_1+, IB_1-, IB_2+, IB_2-, IB_3+, IB_3-	45, 44 43, 42 40, 39 38, 37	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD when enabled.
OB_0+, OB_0-, OB_1+, OB_1-, OB_2+, OB_2-, OB_3+, OB_3-	1, 2 3, 4 5, 6 7, 8	O, LPDS	Inverting and non-inverting low power differential signaling (LPDS) 50Ω outputs with de-emphasis. Compatible with AC coupled CML inputs.
Control Pins — Shared (LVCMOS)			
ENSMB	48	I, LVCMOS w/ internal pull-down	System Management Bus (SMBus) enable pin. When pulled high provide access internal digital registers that are a means of auxiliary control for such functions as equalization, de-emphasis, VOD, rate, and idle detection threshold. When pulled low, access to the SMBus registers are disabled and SMBus function pins are used to control the Equalizer and De-Emphasis. Please refer to SYSTEM MANAGEMENT BUS (SMBUS) AND CONFIGURATION REGISTERS section and ELECTRICAL CHARACTERISTICS — SERIAL MANAGEMENT BUS INTERFACE for detail information.
ENSMB = 1 (SMBUS MODE)			
SCL	50	I, LVCMOS	ENSMB = 1 SMBUS clock input pin is enabled. External pull-up resistor maybe needed. Refer to R_{TERM} in the SMBus specification.
SDA	49	I, LVCMOS O, Open Drain	ENSMB = 1 The SMBus bi-directional SDA pin is enabled. Data input or open drain output. External pull-up resistor is required. Refer to R_{TERM} in the SMBus specification.
AD0–AD3	54, 53, 47, 46	I, LVCMOS w/ internal pull-down	ENSMB = 1 SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs. See section — SYSTEM MANAGEMENT BUS (SMBUS) AND CONFIGURATION REGISTERS for additional information.
ENSMB = 0 (NORMAL PIN MODE)			
EQA0, EQA1 EQB0, EQB1	20, 19 46, 47	I, Float, LVCMOS	EQA/B, 3–level controls the level of equalization of the A/B sides. The EQA/B pins are active only when ENSMB is de-asserted (Low). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes high the SMBus registers provide independent control of each lane. See Table 2,Table 3,Table 4
DEMA0, DEMA1 DEMB0, DEMB1	49, 50 53, 54	I, Float, LVCMOS	DEMA/B, 3–level controls the level of de-emphasis of the A/B sides. The DEMA/B pins are only active when ENSMB is de-asserted (Low). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes High the SMBus registers provide independent control of each lane. See Table 5
Control Pins — Both Modes (LVCMOS)			
RATE	21	I, Float, LVCMOS	RATE, 3–level controls the pulse width of de-emphasis of the output. RATE = 0 forces 3 Gbps, RATE = 1 forces 6 Gbps, RATE = Float enables auto rate detection and the pulse width (pull-back) is set appropriately after each exit from IDLE. This requires the transition from IDLE to ACTIVE state — OOB signal. See Table 5

Table 1. PIN DESCRIPTIONS (continued)

Pin Name	Pin Number	I/O, Type	Pin Descriptions
TXIDLEA,TXIDLEB	24, 25	I, Float, LVCMOS	TXIDLEA/B, 3–level controls the driver output. TXIDLEA/B = 0 disables the signal detect/squelch function for all A/B outputs. TXIDLEA/B = 1 forces the outputs to be muted (electrical idle). TXIDLEA/B = Float enables the signal auto detect/squelch function and the signal detect voltage threshold level can be adjusted using the SD_TH pin. See Table 6
VOD0, VOD1	22, 23	I, LVCMOS w/ internal pull-down	VOD[1:0] adjusts the output differential amplitude voltage level. VOD[1:0] = 00 sets output VOD = 600 mV (Default) VOD[1:0] = 01 sets output VOD = 800 mV VOD[1:0] = 10 sets output VOD = 1000 mV VOD[1:0] = 11 sets output VOD = 1200 mV
PWDN	52	I, LVCMOS	PWDN = 0 enables the device (normal operation). PWDN = 1 disables the device (low power mode). Pin must be driven to a logic low at all times for normal operation
Analog			
SD_TH	27	I, ANALOG	Threshold select pin for electrical idle detect threshold. Float pin for typical default 130 mVp-p (differential), otherwise connect resistor from SD_TH to GND to set threshold voltage. See Table 7, Figure 6
Power			
VDD	9, 14, 36, 41, 51	Power	Power supply pins. 2.5 V +/-5%
GND	DAP	Power	DAP is the large metal contact at the bottom side, located at the center of the 54 pin WQFN package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.
NC	26		No Connect — Leave pin open

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (VDD)	-0.5V to +3.0V
LVCMOS Input/Output Voltage	-0.5V to +4.0V
CML Input Voltage	-0.5V to (VDD+0.5V)
LPDS Output Voltage	-0.5V to (VDD+0.5V)
Analog (SD_TH)	-0.5V to (VDD+0.5V)
Junction Temperature	+125°C
Storage Temperature	-40°C to +125°C
Maximum Package Power Dissipation at 25°C	
NJY Package	4.21 W
Derate NJY Package	52.6mW/°C above +25°C
ESD Rating	
HBM, STD - JESD22-A114C	≥6 kV
MM, STD - JESD22-A115-A	≥250 V
CDM, STD - JESD22-C101-C	≥1250 V
Thermal Resistance	
θ_{JC}	11.5°C/W
θ_{JA}, No Airflow, 4 layer JEDEC	19.1°C/W
For soldering specifications: See SNOA549	

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are specified for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**

RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Units
Supply Voltage				
VDD to GND	2.375	2.5	2.625	V
Ambient Temperature	-10	25	+85	°C
SMBus (SDA, SCL)	0		3.6	V
CML Differential Input Voltage	0		2.0	Vp-p
Supply Noise Tolerance up to 50 MHz, (1)		100		mVp-p

(1) Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges with default register settings unless other specified. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER						
PD	Power Dissipation	PWDN = 0, EQx = 0, DEMx = 0 dB, K28.5 pattern VOD = 1.0 Vp-p		758	950	mW
		PWDN = 1, ENSMB = 0		0.92	1.125	mW
LVCMOS / LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		3.6	V
V_{IL}	Low Level Input Voltage		0		0.8	V
I_{IH}	Input High Current	V_{IN} = 3.3V, Inputs OPEN: SDA, SCL, PWDN	-15		+15	µA
		V_{IN} = 3.3V, Inputs with PULL-DOWN and FLOAT — mid level	-15		+120	uA
I_{IL}	Input Low Current	V_{IN} = 0V, Inputs OPEN: SDA, SCL, PWDN and with PULL-DOWN	-15		+15	µA
		V_{IN} = 0V, Inputs with FLOAT — mid level	-80		+15	uA
CML RECEIVER INPUTS (IN_n+, IN_n-)						
$RL_{RX-DIFF}$	Rx Differential Return Loss (SDD11), (2)	150 MHz – 1.5 GHz		-20		dB
		150 MHz – 3.0 GHz		-13.5		
		150 MHz – 6.0 GHz		-8		
RL_{RX-CM}	Rx Common Mode Input Return Loss (SCC11)	150 MHz – 3.0 GHz, (2)		-10		dB
R_{RX-IB}	Rx Impedance Balance (SDC11)	150 MHz – 3.0 GHz, (2)		-27		dB
I_{IN}	Maximum current allowed at IN+ or IN- input pin.		−30		+30	mA
R_{IN}	Input Resistance	Single ended to V_{DD}, (2)		50		Ω
R_{ITD}	Input Differential Impedance between IN+ and IN-	DC tested, (2)	85	100	115	Ω
R_{ITIB}	Input Differential Impedance Imbalance	DC tested, (2)			5	Ω
R_{ICM}	Input Common Mode Impedance	DC tested, (2)	20	25	35	Ω
$V_{RX-DIFF}$	Differential Rx peak to peak voltage	DC voltage, SD_TH = 20 kΩ to GND	0.1		1.2	V
V_{RX-SD_TH}	Electrical Idle detect threshold (differential)	SD_TH = Float, (3),Figure 6	40		175	mVp-p
LPDS OUTPUTS (OUT_n+, OUT_n-)						
V_{OD}	Output Voltage Swing	R_L = 50 Ω ±1% to GND (AC coupled with 10 nF), 6.4 Gbps, (4) DEMx = 0 dB, VOD[1:0] = 00	500	600	700	mV_{P-P}
		VOD[1:0] = 11	1100	1265	1450	mV_{P-P}

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.
(2) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not verified.
(3) Measured at package pins of receiver. The 130 mVp-p is a typical threshold level and does not include hysteresis, thus less than 40 mVp-p is IDLE, greater than 175 mVp-p is ACTIVE. SD_TH pin connected with resistor to GND overrides this default setting.
(4) Measured with clock-like {11111 00000} pattern.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OCM}	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with 50Ω termination, (2)		V_{DD} – 1.4		V
T_{TX-RF}	Transmitter Rise/ Fall Time	20% to 80% of differential output voltage, measured within 1" from output pins, (2) (4), Figure 2		67	85	ps
$T_{RF-DELTA}$	Tx rise/fall mismatch	20% to 80% of differential output voltage, (2) (4)			0.1	UI
$RL_{TX-DIFF}$	Tx Differential Return Loss (SDD22), (2)	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, 150 MHz – 1.5 GHz		-11		dB
		150 MHz – 3.0 GHz		-10		
		150 MHz – 6.0 GHz		-5		
RL_{TX-CM}	Tx Common Mode Return Loss (SCC22)	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, (2) 50 MHz – 3.0 GHz		-10		dB
R_{TX-IB}	Tx Impedance Balance (SDC22)	Repeating 1100b (D24.3) pattern, VOD = 1.0 Vp-p, (2) 50 MHz – 3.0 GHz		-30		dB
$I_{TX-SHORT}$	Tx Output Short Circuit Current Limit	OA/B_n = GND			90	mA
R_{OTD}	Output Differential Impedance between OUT+ and OUT-	DC tested, (5)	85	100	125	Ω
R_{OTIB}	Output Differential Impedance Imbalance	DC tested, (5)			5	Ω
R_{OCM}	Output Common Mode Impedance	DC tested, (5)	20	25	35	Ω
$V_{TX-CM-DELTA}$	Common Mode Voltage Delta between active burst and electrical Idle of an OOB signal	(6)			±40	mV
T_{DI}	Max time to transition to valid electrical idle after leaving active burst in OOB signaling	VIN = 800 mVp-p, repeating 1100b (D24.3) pattern at 3 Gbps, SD_TH = Float, Figure 4		6.5	9.5	ns
T_{ID}	Max time to transition to valid active burst after leaving idle in OOB signaling	VIN = 800 mVp-p, repeating 1100b (D24.3) pattern at 3 Gbps, SD_TH = Float, Figure 4		5.5	8	ns
T_{PD}	Differential Propagation Delay (Low to High and High to Low Edge)	Propagation delay measured at midpoint crossing between input to output, Figure 3, EQx[1:0] = 11, DEMx[1:0] = −6 dB	150	200	250	ps
		EQx[1:0] = OFF, DEMx[1:0] = 0 dB	120	170	220	ps
T_{LSK}	Lane to Lane Skew in a Single Part	V_{DD} = 2.5 V, T_A = 25°C			27	ps
T_{PPSK}	Part to Part Propagation Delay Skew	V_{DD} = 2.5 V, T_A = 25°C			35	ps
EQUALIZATION						
DJ1	Residual Deterministic Jitter at 6.4 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 40" 4–mil FR4 trace, EQx[1:0] = 0F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, (5)		0.12	0.25	UI_{P-P}

(5) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not verified.

(6) Common-mode voltage (VCM) is expressed mathematically as the average of the two signal voltages with respect to local ground.VCM = (A + B) / 2, A = OUT+, B = OUT-.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DJ2	Residual Deterministic Jitter at 6.4 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 12 meters (30 AWG), EQx[1:0] = 1F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, (5)		0.05	0.15	UI_{P-P}
DJ3	Residual Deterministic Jitter at 3.2 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 40” 4–mil FR4 trace, EQx[1:0] = 0F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, (5)		0.05	0.12	UI_{P-P}
DJ4	Residual Deterministic Jitter at 3.2 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 12 meters (30 AWG), EQx[1:0] = 1F, DEMx[1:0] = 0 dB, VOD = 1.0 Vp-p, K28.5, SD_TH = float, (5)		0.06	0.16	UI_{P-P}
RJ	Random Jitter	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, Repeating 1100b (D24.3) pattern		0.5		psrms
DE-EMPHASIS						
DJ5	Residual Deterministic Jitter at 6.4 Gbps	Tx Launch amplitude = 0.8 to 1.2 Vp–p, 10” 4–mil FR4 trace, EQx[1:0] = OFF, DEMx[1:0] = −6 dB, VOD = 1.0 Vp-p, K28.5, RATE = 1 (5)		0.09	0.20	UI_{P-P}
DJ6	Residual Deterministic Jitter at 3.2 Gbps	Tx Launch amplitude = 0.8 to 1.2 Vp–p, 20” 4–mil FR4 trace, EQx[1:0] = OFF, DEMx[1:0] = −6 dB, VOD = 1.0 Vp-p, K28.5, RATE = 0 (7)		0.07	0.18	UI_{P-P}

(7) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not verified.

ELECTRICAL CHARACTERISTICS — SERIAL MANAGEMENT BUS INTERFACE

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{OL}	Data (SDA) Low Level Output Voltage	I_{OL} = 3mA			0.4	V
V_{IL}	Data (SDA), Clock (SCL) Input Low Voltage				0.8	V
V_{IH}	Data (SDA), Clock (SCL) Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(1)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	(1) (2)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	$V_{DD3.3}$, (1) (2) (3)		2000		Ω
		$V_{DD2.5}$, (1) (2) (3)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS. See Figure 5						
FSMB	Bus Operating Frequency	(4)	10		100	kHz

(1) Recommended value. Parameter not tested in production.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

ELECTRICAL CHARACTERISTICS — SERIAL MANAGEMENT BUS INTERFACE (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TBUF	Bus Free Time Between Stop and Start Condition		4.7			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	4.0			µs
TSU:STA	Repeated Start Condition Setup Time		4.7			µs
TSU:STO	Stop Condition Setup Time		4.0			µs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
$T_{TIMEOUT}$	Detect Clock Low Timeout	(4)	25		35	ms
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period	(4)	4.0		50	µs
T_{LOW}:SEXT	Cumulative Clock Low Extend Time (Slave Device)	(4)			2	ms
t_F	Clock/Data Fall Time	(4)			300	ns
t_R	Clock/Data Rise Time	(4)			1000	ns
t_{POR}	Time in which a device must be operational after power-on reset	(4)			500	ms

TIMING DIAGRAMS

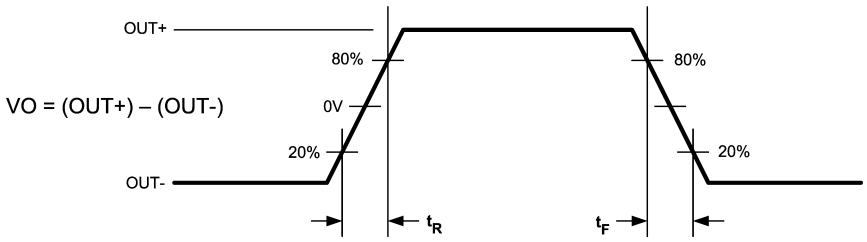


Figure 2. LPDS Output Transition Times

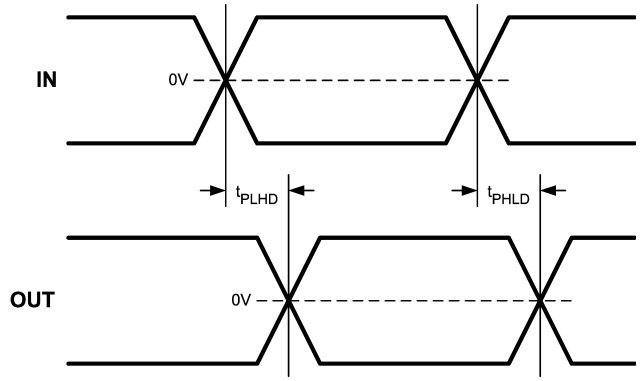


Figure 3. Propagation Delay Timing Diagram

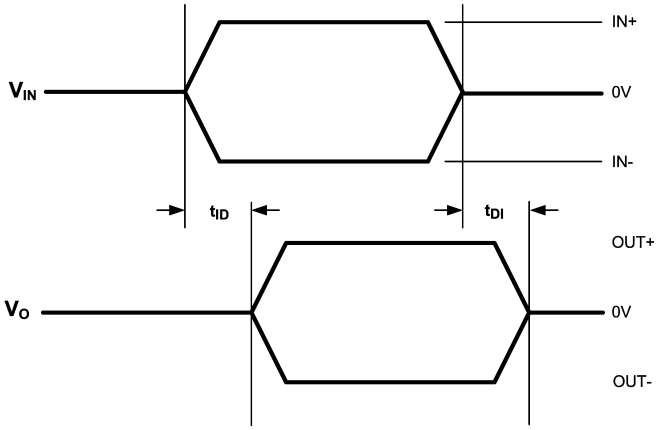


Figure 4. Idle Timing Diagram

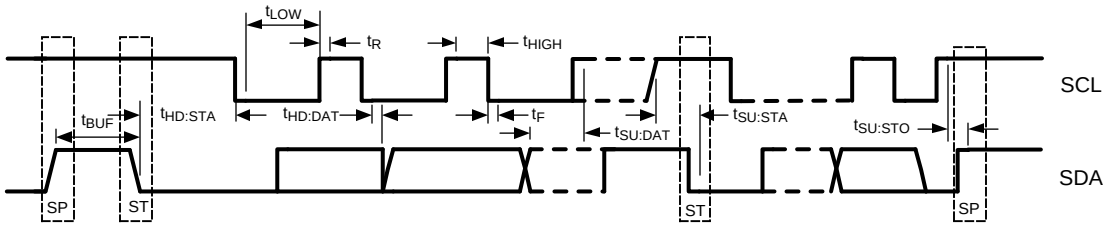


Figure 5. SMBus Timing Parameters

FUNCTIONAL DESCRIPTION

The DS64BR401 is a quad repeater optimized for backplane trace or cable interconnect up to 6.4 Gbps. The DS64BR401 operates in two modes: Pin Control Mode (ENSMB = 0) and SMBus Mode (ENSMB = 1).

Pin Control Mode:

When in pin mode (ENSMB = 0) , the repeater is configurable with external pins. Equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically increased per the De-Emphasis table below for improved performance over lossy media. Rate optimization is also pin controllable, with pin selections for 3 Gbps, 6 Gbps, and auto detect. The receiver electrical idle detect threshold is also programmable via an optional external resistor on the SD_TH pin.

SMBUS MODE

When in SMBus mode the equalization, de-emphasis are all programmable on a individual lane basis, instead of grouped by sides as in the pin mode case. Upon assertion of ENSMB the RATE, EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low. On powerup and when ENSMB is driven low all registers are reset to their default state. If PWDN = 1 is asserted while ENSMB = 1, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 24 possible equalization settings. The tables show a typical gain for each gain stage (GST[4:3]) and boost level (BST[2:0]) combination. When using SMBus mode, the Equalization and De-Emphasis levels are set using registers. See Table 9 (register map) for more information.

Table 2. Equalization Settings with GST=1 for Pins or SMBus Registers

EQ1(1)	EQ0(1)	EQ Setting		EQ Gain (dB)		Suggested Use
		GST[4:3]	BST[2:0]	1.5 GHz	3.0 GHz	
F	F	00	000	0	0	Bypass - Default Setting
		01	000	2.0	3.8	
		01	001	2.6	4.9	
1	1	01	010	3.3	5.8	8 inch FR4 (4-mil trace) or < 0.7m (30 AWG)
		01	011	3.9	6.8	
		01	100	4.9	8.2	
		01	101	5.5	8.9	
		01	110	6.0	9.4	
		01	111	6.5	10.0	

(1) F=Float (don't drive pin, each float pin has an internal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

Table 3. Equalization Settings with GST=2 for Pins or SMBus Registers

EQ1(1)	EQ0(1)	EQ Setting		EQ Gain (dB)		Suggested Use
		GST[4:3]	BST[2:0]	1.5 GHz	3.0 GHz	
0	0	10	000	4.8	9.2	12” FR4 (4-mil trace) or 1m (30 AWG)
F	0	10	001	6.3	11.7	20” FR4 (4-mil trace) or 5m (30 AWG)
		10	010	7.6	13.6	
		10	011	9.1	15.6	
F	1	10	100	11.1	18.4	35” FR4 (4-mil trace) or 9m (30 AWG)
0	1	10	101	12.4	20.0	40” FR4 (4-mil trace) or 10m (30 AWG)
		10	110	13.4	20.9	

(1) F=Float (don't drive pin, each float pin has an internal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

Table 3. Equalization Settings with GST=2 for Pins or SMBus Registers (continued)

EQ1(1)	EQ0(1)	EQ Setting		EQ Gain (dB)		Suggested Use
		GST[4:3]	BST[2:0]	1.5 GHz	3.0 GHz	
		10	111	14.5	22.0	

Table 4. Equalization Settings with GST=3 for Pins or SMBus Registers

EQ1(1)	EQ0(1)	EQ Setting		EQ Gain (dB)		Suggested Use
		GST[4:3]	BST[2:0]	1.5 GHz	3.0 GHz	
1	0	11	000	7.7	14.6	25” FR4 (4-mil trace) or 6m (30 AWG)
		11	001	10.1	18.4	
0	F	11	010	12.2	21.2	10m (30 AWG)
		11	011	14.4	24.4	
1	F	11	100	17.5	28.4	12m (30 AWG)
		11	101	19.4	30.6	
		11	110	20.9	32.1	
		11	111	22.6	33.8	

(1) F=Float (don't drive pin, each float pin has an internal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

Table 5. De-Emphasis Input Select Pins for A and B ports (3–Level Input)

RATE	DEM1 (1)	DEM0 (1)	De-Emphasis Level (typ)	DE Pulse Width (typ)	VOD (typical)	Suggested Use
0/F	0	0	0 dB	0 ps	VOD: 600 to 1200 mVp-p	10 inch FR4 trace or 1 meter (28 AWG)
0/F	0	1	-3.5 dB	330 ps	VOD = 1000 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
			-2 dB	330 ps	VOD = 1200 mVp-p	15 inch FR4 trace or 2 meters (28 AWG)
0/F	1	0	-6 dB	330 ps	VOD = 1000 mVp-p	25 inch FR4 trace or 3 meters (28 AWG)
			-3 dB	330 ps	VOD = 1200 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
0/F	1	1	-9 dB	300 ps enhanced	VOD = 1000 mVp-p	5 meters (28 AWG)
			-11 dB	300 ps enhanced	VOD = 1200 mVp-p	7 meters (28 AWG)
0/F	0	F	-6 dB	300 ps enhanced	VOD = 1000 mVp-p	5 meters (26 AWG)
			-8 dB	300 ps enhanced	VOD = 1200 mVp-p	7 meters (26 AWG)
0/F	1	F	-12 dB	300 ps enhanced	VOD = 1000 mVp-p	8 meters (24 AWG)
			-13 dB	300 ps enhanced	VOD = 1200 mVp-p	9 meters (24 AWG)
0/F	F	0	-9 dB	250 ps enhanced	VOD = 1000 + 200 mVp-p	8 meters (26 AWG)
			-10 dB	250 ps enhanced	VOD = 1200 + 200 mVp-p	9 meters (26 AWG)
0/F	F	1	-12 dB	250 ps enhanced	VOD: (1000 to 1200) + 200 mVp-p	10 meters (24 AWG)
0/F	F	F	Reserved, don't use			
1/F	0	0	0 dB	0 ps	VOD: 600 to 1200 mVp-p	5 inch FR4 trace or 0.5 meter (28 AWG)

(1) F = Float (don't drive pin), 1 = High and 0 = Low. Enhanced DE pulse width provides de-empahsis on second bit.
When RATE = F (auto rate detection active), the DE level and pulse width settings follow detected rate after exiting IDLE. RATE = 0 is 3 Gbps and RATE = 1 is 6 Gbps. De-emphasis should only be used with VOD = 1000 mVp-p or 1200 mVp-p. VOD less then 1000 mVp-p is not recommended with de-emphasis. Please refer to VOD1 and VOD0 pin description to set the output differential voltage level.

Table 5. De-Emphasis Input Select Pins for A and B ports (3–Level Input) (continued)

RATE	DEM1 (1)	DEM0 (1)	De-Emphasis Level (typ)	DE Pulse Width (typ)	VOD (typical)	Suggested Use
1/F	0	1	-3.5 dB	200 ps	VOD = 1000 mVp-p	10 inch FR4 trace or 1 meter (28 AWG)
			-2 dB	200 ps	VOD = 1200 mVp-p	10 inch FR4 trace or 1 meters (28 AWG)
1/F	1	0	-6 dB	200 ps	VOD = 1000 mVp-p	20 inch FR4 trace or 2 meters (28 AWG)
			-3 dB	200 ps	VOD = 1200 mVp-p	15 inch FR4 trace or 1 meters (28 AWG)
1/F	1	1	-9 dB	180 ps enhanced	VOD = 1000 mVp-p	3 meters (28 AWG)
			-11 dB	180 ps enhanced	VOD = 1200 mVp-p	4 meters (28 AWG)
1/F	0	F	-6 dB	180 ps enhanced	VOD = 1000 mVp-p	3 meters (26 AWG)
			-8 dB	180 ps enhanced	VOD = 1200 mVp-p	4 meters (26 AWG)
1/F	1	F	-12 dB	180 ps enhanced	VOD = 1000 mVp-p	5 meters (24 AWG)
			-13 dB	180 ps enhanced	VOD = 1200 mVp-p	6 meters (24 AWG)
1/F	F	0	-9 dB	160 ps enhanced	VOD = 1000 + 200 mVp-p	5 meters (26 AWG)
			-10 dB	160 ps enhanced	VOD = 1200 + 200 mVp-p	6 meters (26 AWG)
1/F	F	1	-12 dB	160 ps enhanced	VOD: (1000 to 1200) + 200 mVp-p	7 meters (24 AWG)
1/F	F	F	Reserved, don't use			

Table 6. Idle Control (3–Level Input)

TXIDLEA/B	Function
0	This state is for lossy media, dedicated Idle threshold detect circuit disabled, output follows input based on EQ settings. Idle state not verified.
Float	Float enables automatic idle detection. Idle on the input is passed to the output. Internal 50KΩ resistors hold TXIDLEA/B pin at a mid level - don't connect this pin if the automatic idle detect function is desired. This is the default state. Output in Idle if differential input signal less than value set by SD_TH pin.
1	Manual override, output in electrical Idle. Differential inputs are ignored.

Table 7. Receiver Electrical Idle Detect Threshold Adjust

SD_TH resistor value (Ω) (1)	Receiver Electrical Idle Detect Threshold (DIFF p-p)
Float (no resistor required)	130 mV (default condition)
0	225 mV
80k	20 mV

(1) SD_TH resistor value can be set from 0 through 80k ohms to achieve desired idle detect threshold, see Figure 6

TYPICAL PERFORMANCE CURVES

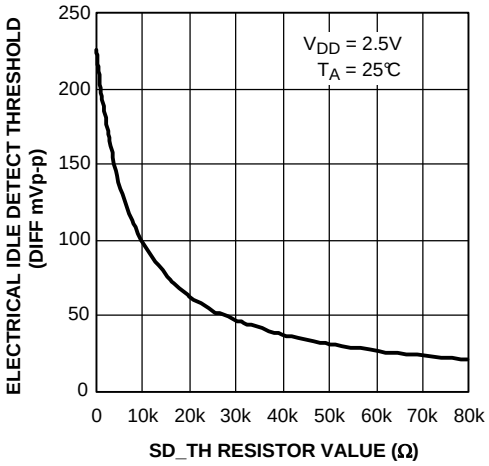


Figure 6. Typical Idle Threshold vs. SD_TH resistor value

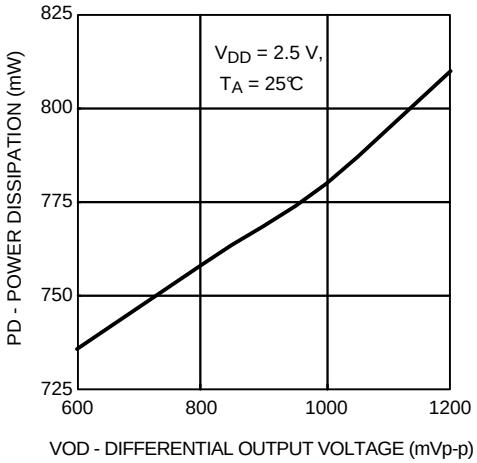


Figure 7. Typical Power Dissipation (PD) vs. Output Differential Voltage (VOD)

SYSTEM MANAGEMENT BUS (SMBUS) AND CONFIGURATION REGISTERS

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB must be pulled high to enable SMBus mode and allow access to the configuration registers.

The DS64BR401 has the AD[3:0] inputs in SMBus mode. These pins set the SMBus slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is A0'h. Based on the SMBus 2.0 specification, the DS64BR401 has a 7-bit slave address of 1010000'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 101**0 000**0'b or A0'h. The bold bits indicate the AD[3:0] pin map to the slave address bits [4:1]. The device address byte can be set with the use of the AD[3:0] inputs. Below are some examples.

AD[3:0] = 0001'b, the device address byte is A2'h

AD[3:0] = 0010'b, the device address byte is A4'h

AD[3:0] = 0100'b, the device address byte is A8'h

AD[3:0] = 1000'b, the device address byte is B0'h

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

TRANSFER OF DATA VIA THE SMBUS

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBUS TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

When SMBus is enabled, the DS64BR401 **must use one of the following De-emphasis settings** (Table 8). The driver de-emphasis value is set on a per channel basis using 8 different registers. Each register (0x11, 0x18, 0x1F, 0x26, 0x2E, 0x35, 0x3C, 0x43) requires one of the following De-emphasis settings when in SMBus mode.

Table 8. De-Emphasis Register Settings (must write one of the following when in SMBus mode)

De-Emphasis Value	Register Setting	3 Gbps Operation	6 Gbps Operation
0.0 dB	0x01	10” trace or 1 meter 28 awg cable	5” trace or 0.5 meter 28 awg cable
-3.5 dB	0x38	20” trace or 2 meters 28 awg cable	10” trace or 1meters 28 awg cable
-6 dB	0x88	25” trace or 3 meters cable	20” trace or 2 meters cable
-9 dB	0x90	5 meters 28 awg cable	3 meters 28 awg cable
-12 dB	0xA0	8 meters 28 awg cable	5 meters 28 awg cable

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

RECOMMENDED SMBUS REGISTER SETTINGS

When SMBus mode is enabled (ENSMB = 1), the default register are not configured to an appropriate settings. Below is the recommended settings to configure the EQ, VOD and DE to a medium level that supports interconnect length of 20 inches FR4 trace or 3 to 5 meters of cable length. Please refer to , Table 2,Table 3,Table 4,Table 5, Table 8,Table 9 for additional information and recommended settings.

1. Reset the SMBus registers to default values:
   - **Write 01'h to address 0x00.**
2. Set de-emphasis to -6 dB enhance for all channels (CH0–CH7):
   - **Write 88'h to address 0x11, 0x18, 0x1F, 0x26, 0x2E, 0x35, 0x3C, 0x43.**
3. Set equalization to external pin level EQ[1:0] = 00 (~9 dB at 3 GHz) for all channels (CH0–CH7):

– **Write 30'h to address 0x0F, 0x16, 0x1D, 0x24, 0x2C, 0x33, 0x3A, 0x41.**

4. Set VOD = 1.0V for all channels (CH0–CH7):
   – **Write 0F'h to address 0x10, 0x17, 0x1E, 0x25, 0x2D, 0x34, 0x3B, 0x42.**

IDLE AND RATE DETECTION TO EXTERNAL PINS

The functions of IDLE and RATE detection to external pins for monitoring can be supported in SMBus mode. The external GPIO pins of 19, 20, 46 and 47 will be changed and they will serve as outputs for IDLE and RATE detect signals.

The following external pins should be set to auto detection:

RATE = F (FLOAT) – auto RATE detect enabled

TXIDLEA/B = F (FLOAT) – auto IDLE detect enabled

There are 4 GPIO pins that can be configured as outputs with reg_4E[0].

To disable the external SMBus address pins, so pin 46 and 47 can be used as outputs:

WRITE 01'H TO ADDRESS 0X4E.

Care must be taken to ensure that only the desired status block is enabled and attached to the external pin as the status blocks can be OR'ed together internally. Register bits reg_47[5:4] and bits reg_4C[7:6] are used to enable each of the status block outputs to the external pins. The channel status blocks can be internally OR'ed together to monitor more than one channel at a time. This allows more information to be presented on the status outputs and later if desired, a diagnosis of the channel identity can be made with additional SMBus writes to register bits reg_47[5:4] and bits reg_4C[7:6].

Below are examples to configure the device and bring the internal IDLE and RATE status to pins 19, 20, 46, 47.

To monitor the IDLE detect with two channels ORed (CH0 with CH2, CH1 with CH3, CH4 with CH6, CH5 with CH7):

WRITE 32'H TO ADDRESS 0X47.

The following IDLE status should be observable on the external pins:

pin 19 – CH0 with CH2,

pin 20 – CH1 with CH3,

pin 46 – CH4 with CH6,

pin 47 – CH5 with CH7.

Pin = HIGH (VDD) means IDLE is detected (no signal present).

Pin = LOW (GND) means ACTIVE (data signal present).

To monitor the RATE detect with two channels ORed (CH0 with CH2, CH1 with CH3, CH4 with CH6, CH5 with CH7):

WRITE C0'H TO ADDRESS 0X4C.

The following RATE status should be observable on the external pins:

pin 19 – CH0 with CH2,

pin 20 – CH1 with CH3,

pin 46 – CH4 with CH6,

pin 47 – CH5 with CH7.

Pin = HIGH (VDD) means high data rate is detected (6 Gbps).

Pin = LOW (GND) means low rate is detected (3 Gbps).

Table 9. SMBus Register Map

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x00	Reset	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Reset			SMBus Reset 1: Reset registers to default value
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel [7]: CHA_3 [6]: CHA_2 [5]: CHA_1 [4]: CHA_0 [3]: CHB_3 [2]: CHB_2 [1]: CHB_1 [0]: CHB_0 00'h = all channels enabled FF'h = all channels disabled
0x02	PWDN Control	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Override PWDN			0: Allow PWDN pin control 1: Block PWDN pin control
0x08	Pin Control Override	7:5	Reserved	R/W	0x00	Set bits to 0.
		4	Override IDLE			0: Allow IDLE pin control 1: Block IDLE pin control
		3	Reserved			Set bit to 0.
		2	Override RATE			0: Allow RATE pin control 1: Block RATE pin control
		1:0	Reserved			Set bits to 0.
0x0E	CH0 - CHB0 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x0F	CH0 - CHB0 EQ Control	7:6	Reserved	R	0x0	Set bits to 0.
		5:0	CH0 IB0 EQ	R/W	0x20	IB0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x10	CH0 - CHB0 VOD Control	7:6	Reserved	R	0x00	Set bit to 0.
		5:0	CH0 OB0 VOD	R/W	0x03	OB0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV

Table 9. SMBus Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x11	CH0 - CHB0 DE Control	7:0	CH0 OB0 DEM	R/W	0x03	OB0 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = −3.5 dB 0F = 10001000 = 88'h = −6.0 dB 01 = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x12	CH0 - CHB0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x15	CH1 - CHB1 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x16	CH1 - CHB1 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH1 IB1 EQ			IB1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x17	CH1 - CHB1 VOD Control	7:6	Reserved	R	0x00	Set bit to 0.
		5:0	CH1 OB1 VOD	R/W	0x03	OB1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV

Table 9. SMBus Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x18	CH1 - CHB1 DE Control	7:0	CH1 OB1 DEM	R/W	0x03	OB1 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = −3.5 dB 0F = 10001000 = 88'h = −6.0 dB 01 = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x19	CH1 - CHB1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x1C	CH2 - CHB2 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x1D	CH2 - CHB2 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH2 IB2 EQ			IB2 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x1E	CH2 - CHB2 VOD Control	7:6	Reserved	R	0x00	Set bit to 0.
		5:0	CH2 OB2 VOD	R/W	0x03	OB2 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV

Table 9. SMBus Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x1F	CH2 - CHB2 DE Control	7:0	CH2 OB2 DEM	R/W	0x03	OB2 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = −3.5 dB 0F = 10001000 = 88'h = −6.0 dB 01 = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x20	CH2 - CHB2 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x23	CH3 - CHB3 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x24	CH3 - CHB3 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH3 IB3 EQ			IB3 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x25	CH3 - CHB3 VOD Control	7:6	Reserved	R	0x00	Set bit to 0.
		5:0	CH3 OB3 VOD	R/W	0x03	OB3 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV

Table 9. SMBus Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x26	CH3 - CHB3 DE Control	7:0	CH3 OB3 DEM	R/W	0x03	OB3 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = −3.5 dB 0F = 10001000 = 88'h = −6.0 dB 01 = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x27	CH3 - CHB3 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x2B	CH4 - CHA0 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x2C	CH4 - CHA0 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH4 IA0 EQ			IA0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x2D	CH4 - CHA0 VOD Control	7:6	Reserved	R	0x00	Set bit to 0.
		5:0	CH4 OA0 VOD	R/W	0x03	OA0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV

Table 9. SMBus Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x2E	CH4 - CHA0 DE Control	7:0	CH4 OA0 DEM	R/W	0x03	OA0 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = −3.5 dB 0F = 10001000 = 88'h = −6.0 dB 01 = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x2F	CH4 - CHA0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x32	CH5 - CHA1 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x33	CH5 - CHA1 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH5 IA1 EQ			IA1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x34	CH5 - CHA1 VOD Control	7:6	Reserved	R	0x00	Set bit to 0.
		5:0	CH5 OA1 VOD	R/W	0x03	OA1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV

Table 9. SMBus Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x35	CH5 - CHA1 DE Control	7:0	CH5 OA1 DEM	R/W	0x03	OA1 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = −3.5 dB 0F = 10001000 = 88'h = −6.0 dB 01 = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x36	CH5 - CHA1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x39	CH6 - CHA2 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x3A	CH6 - CHA2 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH6 IA2 EQ			IA2 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x3B	CH6 - CHA2 VOD Control	7:6	Reserved	R	0x00	Set bit to 0.
		5:0	CH6 OA2 VOD	R/W	0x03	OA2 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV

Table 9. SMBus Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x3C	CH6 - CHA2 DE Control	7:0	CH6 OA2 DEM	R/W	0x03	OA2 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = −3.5 dB 0F = 10001000 = 88'h = −6.0 dB 01 = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x3D	CH6 - CHA2 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x40	CH7 - CHA3 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 to 3.2 Gbps 1: 5.0 to 6.4 Gbps
0x41	CH7 - CHA3 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH7 IA3 EQ			IA3 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h 0F = 110001 = 31'h 01 = 111000 = 38'h 1F = 110100 = 34'h 10 = 110101 = 35'h F0 = 111010 = 3A'h F1 = 111100 = 3C'h
0x42	CH7 - CHA3 VOD Control	7:6	Reserved	R	0x00	Set bit to 0.
		5:0	CH7 OA3 VOD	R/W	0x03	OA3 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV 3F'h = 1400 mV

Table 9. SMBus Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x43	CH7 - CHA3 DE Control	7:0	CH7 OA3 DEM	R/W	0x03	OA3 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 00111000 = 38'h = −3.5 dB 0F = 10001000 = 88'h = −6.0 dB 01 = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x44	CH7 - CHA3 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x47	EN Digital Test Point IDLE Detect	7:6	Reserved	R/W	0x02	Set bits to 0.
		5	CH2, CH3 CH6, CH7			0: Disabled IDLE Test Point for CH2, 3, 6, 7. 1: Enable IDLE Test Point for CH2, 3, 6, 7.
		4	CH0, CH1 CH4, CH5			0: Disabled IDLE Test Point for CH0, 1, 4, 5. 1: Enable IDLE Test Point for CH0, 1, 4, 5.
		3:2	Reserved			Set bits to 0.
	Global VOD Adjust	1:0	VOD Adjust			00 = −25% 01 = −12.5% 10 = 0% (Default) 11 = +12.5%
0x4C	EN Digital Test Point RATE Detect	7	CH2, CH3 CH6, CH7	R/W	0x00	0: Disabled RATE Test Point for CH2, 3, 6, 7. 1: Enable RATE Test Point for CH2, 3, 6, 7.
		6	CH0, CH1 CH4, CH5			0: Disabled RATE Test Point for CH0, 1, 4, 5. 1: Enable RATE Test Point for CH0, 1, 4, 5.
		5:0	Reserved			Set bits to 0.
0x4E	Digital Test	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Block AD[3:0] pins			1: Configure GPIO pin 46, 47, 53, 54 to be outputs.

APPLICATION INFORMATION

GENERAL RECOMMENDATIONS

The DS64BR401 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and LPDS outputs must have a controlled differential impedance of 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187(SNOA401) for additional information on WQFN packages.

The graphic shown below depicts a typical microstrip trace routing design of the top and bottom layers. This should be used as a reference to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each via hole. To further improve the signal quality, a ground via placed close to the signal via for a low inductance return current path is recommended. When the via structure is associated with stripline trace and a thick board, further optimization such as back drilling is often used to reduce the high frequency effects of via stubs on the signal path. To minimize cross-talk coupling, it is recommended to have >3X gap spacing between the differential pairs. For example, if the trace width is 5 mils with 5 mils spacing – 100Ω differential impedance (closely coupled). The gap spacing between the differential pairs should be >15 mils.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS64BR401 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS64BR401. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

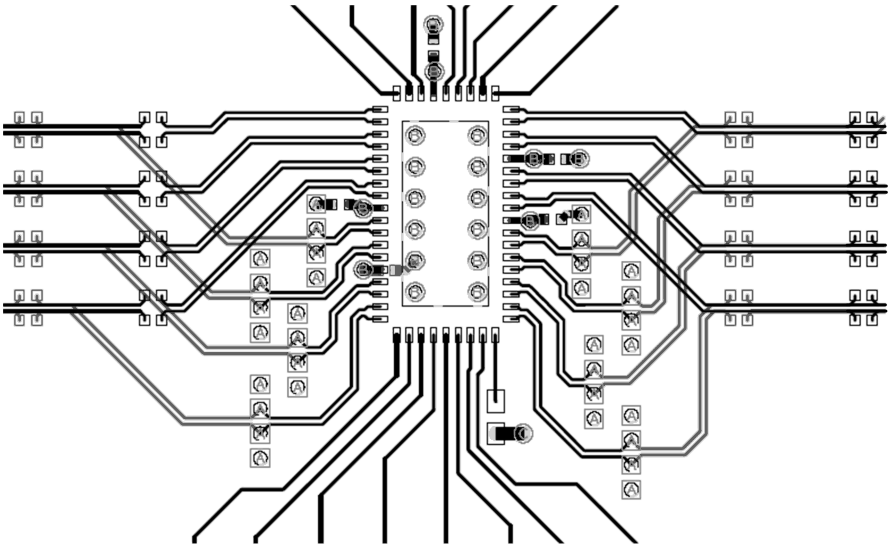


Figure 8. Typical PCB Trace Routing

TYPICAL PERFORMANCE EYE-DIAGRAM CHARACTERISTIC

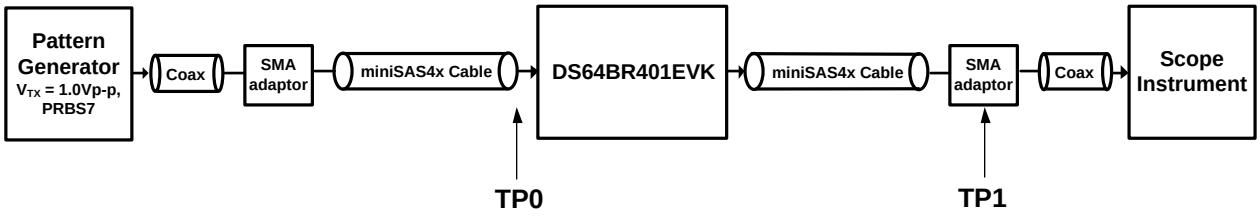


Figure 9. Test Setup Connection Diagram

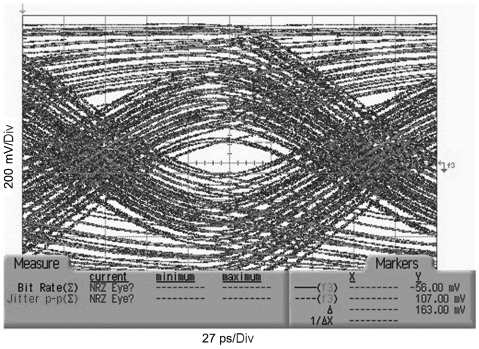


Figure 10. TP0: Input — After 5m 26–AWG Cable at 6 Gbps

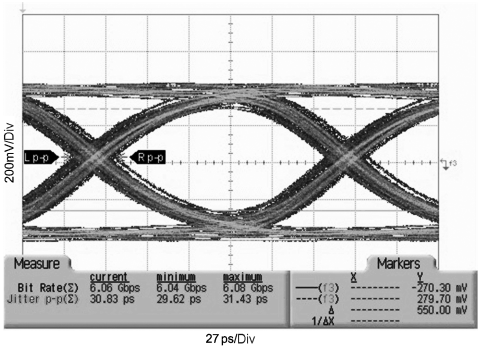


Figure 11. TP1: Output — After 1m 28–AWG Cable at 6 Gbps (EQ[1:0] = F0, DEM[1:0] = 01)

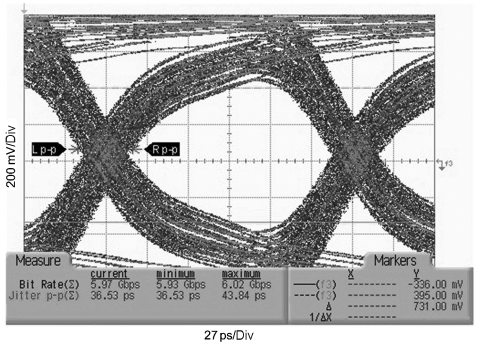


Figure 12. TP0: Input — After 1m 28–AWG cable at 6 Gbps

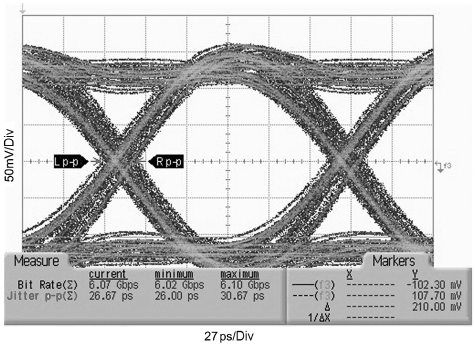


Figure 13. TP1: Output — After 5m 26–AWG Cable at 6 Gbps (EQ[1:0] = 11, DEM[1:0] = F0)

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS64BR401SQ/NOPB	ACTIVE	WQFN	NJY	54	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-10 to 85	DS64BR401 SQ	Samples
DS64BR401SQE/NOPB	ACTIVE	WQFN	NJY	54	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-10 to 85	DS64BR401 SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

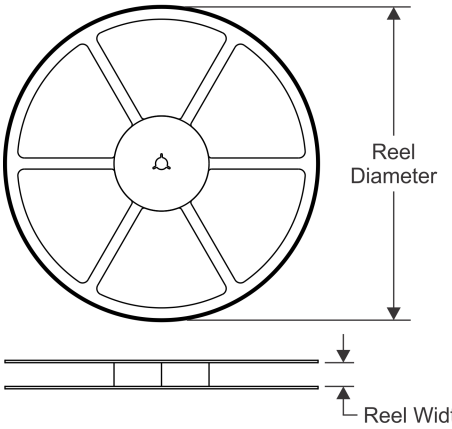
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

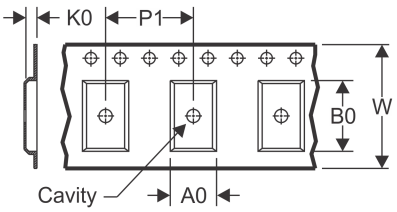
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

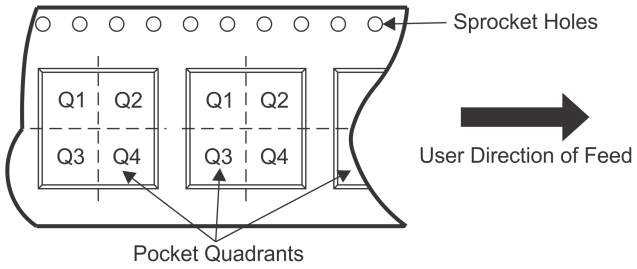


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

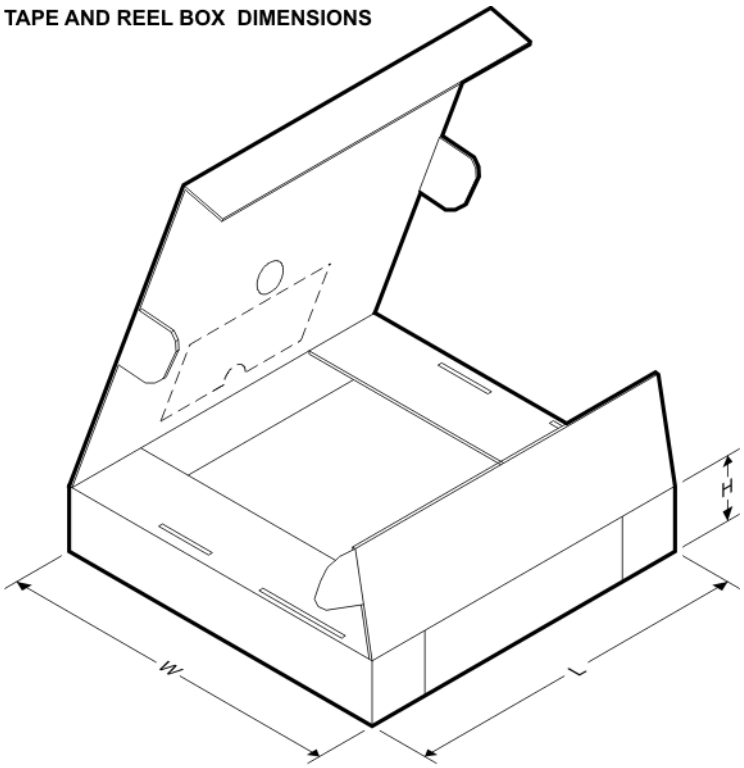
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

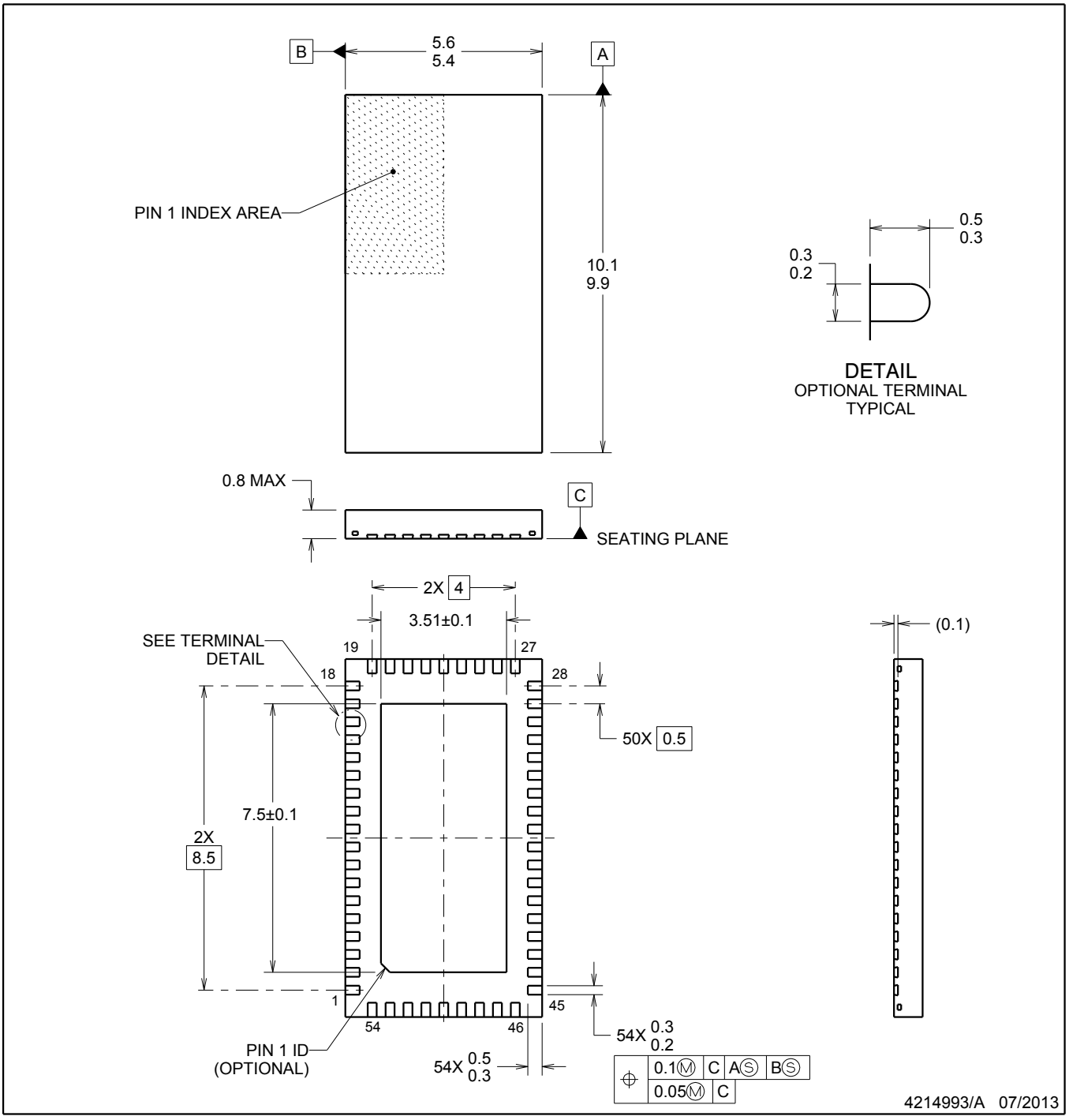
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS64BR401SQ/NOPB	WQFN	NJY	54	2000	330.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1
DS64BR401SQE/NOPB	WQFN	NJY	54	250	178.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



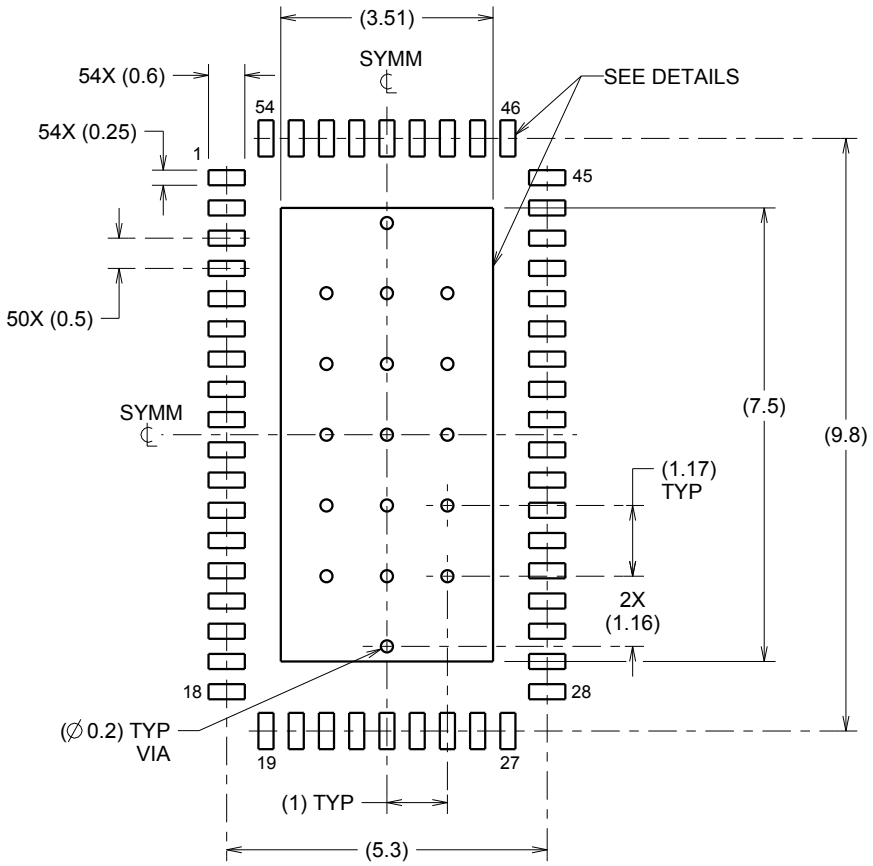
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS64BR401SQ/NOPB	WQFN	NJY	54	2000	367.0	367.0	38.0
DS64BR401SQE/NOPB	WQFN	NJY	54	250	210.0	185.0	35.0

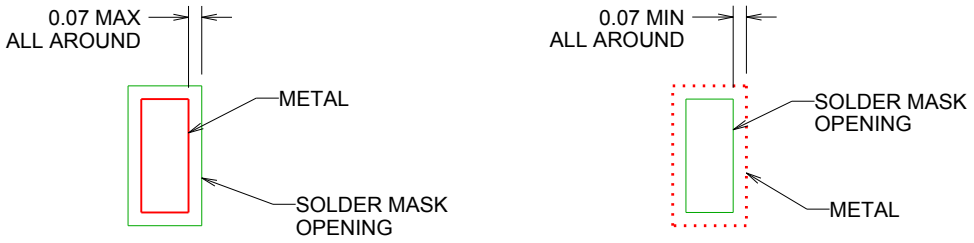


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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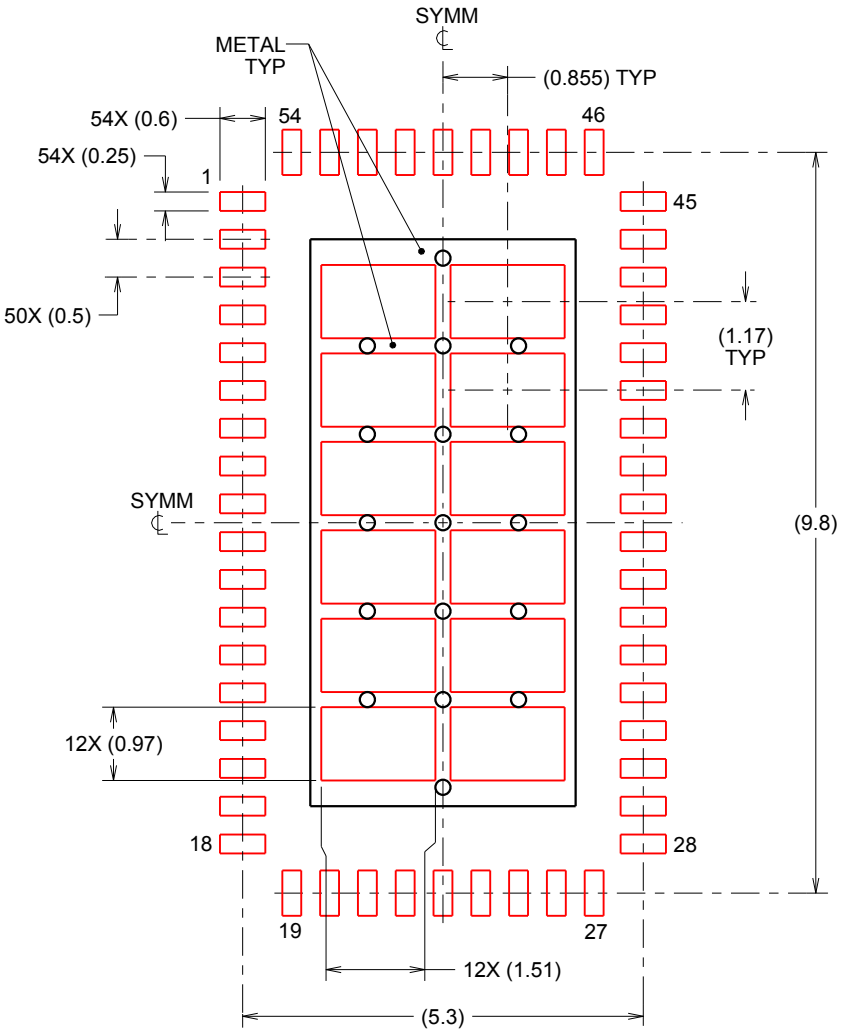
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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