DP83TC812-Q1 TC-10 Compliant 100BASE-T1 Automotive Ethernet PHY

1 Features

- Open Alliance and IEEE 802.3bw 100BASE-T1 compliant
  - Passes Level IV emissions with Integrated LPF
  - TC-10 compliant with < 30µA sleep current
- SAE J2962-3 EMC compliant
- Configurable I/O voltages: 3.3 V, 2.5 V, and 1.8 V
- MAC interfaces: MII, RMII, RGMII and SGMII
- Optional separate voltage rail for MAC interface pins (3.3V, 2.5V, 1.8V)
- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125 °C ambient operating temperature
  - HBM ESD classification Level: 2
  - CDM ESD classification Level: C6
  - IEC61000-4-2 ESD classification level 4 for pins 12 and 13: ±6-kV contact discharge
- IEEE 1588 SFD support
- TSN Compliant with 802.3br frame pre-emption support
- Low active power operation: < 230 mW
- Diagnostic tool kit
  - Signal quality indication (SQI)
  - Time domain reflectometry (TDR)
  - Electrostatic discharge sensor
  - Voltage sensor
  - Temperature sensor
  - PRBS built-in self-test
  - Loopbacks
- VQFN, wettable flank packaging

2 Applications

- ADAS
- Gateway and Body Control
- Telematics

3 Description

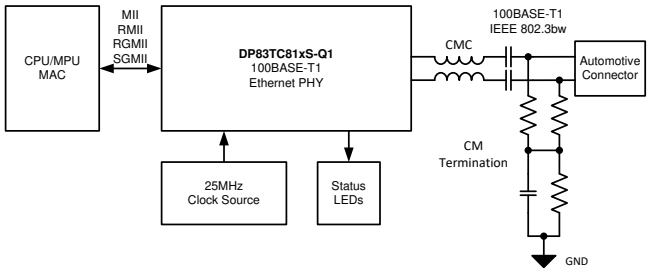
The DP83TC812S-Q1 device is an IEEE 802.3bw-compliant automotive PHYTER™ Ethernet physical layer transceiver which can work with Unshielded Twisted Pair cable. The PHY supports TC10 sleep and wake features. It provides all physical layer functions needed to transmit and receive data over unshielded single twisted-pair cables. The device provides xMII flexibility with support for standard MII, RMII, RGMII, and SGMII MAC interfaces.The PHY also integrates a low pass filter on the MDI side to reduce emissions.

This device includes the Diagnostic Tool Kit, providing an extensive list of real-time monitoring tools, debug tools and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool. It is capable of counting ESD events on both the xMII and MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TC812S-Q1 includes a pseudo random binary sequence (PRBS) frame generation tool, which is fully compatible with internal loopbacks, to transmit and receive data without the use of a MAC. The device is housed in a 6.00-mm × 6.00-mm, 36-pin VQFN wettable flank package. DP83TC812 is pin-2-pin compatible with DP83TG720 (1000BASE-T1). It is also form factor compatible with DP83TC811.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DP83TC812S-Q1	VQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2021	*	Initial Release

5 Pin Configuration and Functions

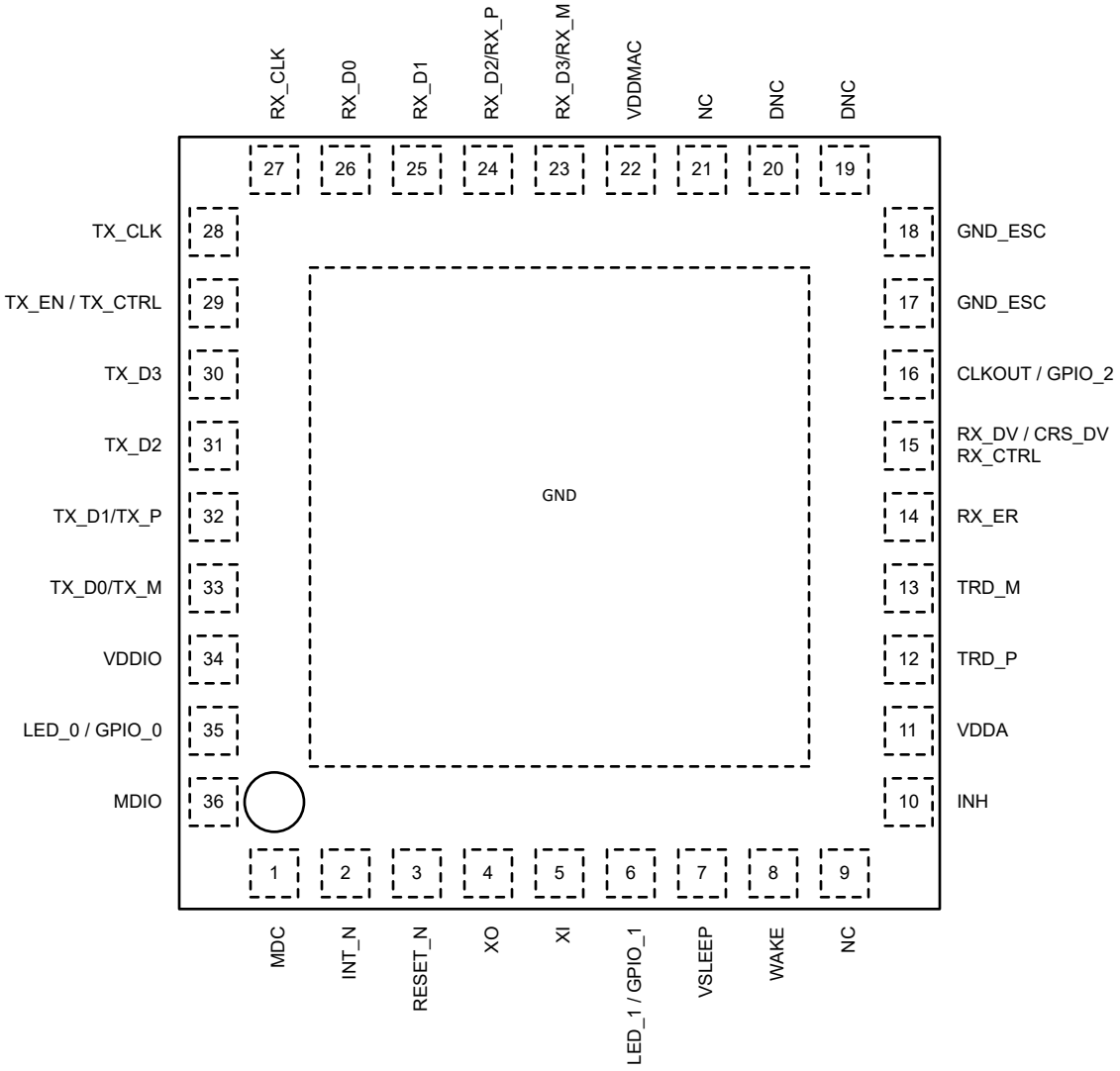

Figure 5-1. RHA Package 36-Pin VQFN Top View

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Table 5-1. Pin Functions

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
MAC INTERFACE			
RX_D3 RX_M	23	S, PD, O	**Receive Data:** Symbols received on the cable are decoded and transmitted out of these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV is asserted. A data nibble, RX_D[3:0], is transmitted in MII and RGMII modes. 2 bits; RX_D[1:0], are transmitted in RMII mode. RX_D[3:2] are not used when in RMII mode. If the PHY is bootstrapped to RMII Master mode, a 50-MHz clock reference is automatically outputted on RX_D3. This clock must be fed to the MAC. **RX_M / RX_P:** Differential SGMII Data Output. These pins transmit data from the PHY to the MAC.
RX_D2 RX_P	24		
RX_D1	25		
RX_D0	26		
RX_CLK	27	S, PD, O	**Receive Clock:** In MII and RGMII modes, the receive clock provides a 25-MHz reference clock. **Unused in RMII and SGMII modes**
RX_ER	14	S, PD, O	**Receive Error:** In MII and RMII modes, this pin indicates a receive error symbol has been detected within a received packet. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is not required to be used by the MAC in MII or RMII because the PHY will automatically corrupt data on a receive error. **Unused in RGMII and SGMII modes**
RX_DV CRS_DV RX_CTRL	15	S, PD, O	**Receive Data Valid:** This pin indicates when valid data is presented on RX_D[3:0] for MII mode. **Carrier Sense Data Valid:** This pin combines carrier sense and data valid into an asynchronous signal. When CRS_DV is asserted, data is presented on RX_D[1:0] in RMII mode. **RGMII Receive Control:** Receive control combines receive data valid indication and receive error indication into a single signal. RX_DV is presented on the rising edge of RX_CLK and RX_ER is presented on the falling edge of RX_CLK. **Unused in SGMII mode**
TX_CLK	28	PD, I, O	**Transmit Clock:** In MII mode, the transmit clock is a 25-MHz output and has constant phase referenced to the reference clock. In RGMII mode, this clock is sourced from the MAC layer to the PHY. A 25-MHz clock must be provided (not required to have constant phase to the reference clock unless synchronous RGMII is enabled) **Unused in RMII and SGMII modes**
TX_EN TX_CTRL	29	PD, I	**Transmit Enable:** In MII mode, transmit enable is presented prior to the rising edge of the transmit clock. TX_EN indicates the presence of valid data inputs on TX_D[3:0]. In RMII mode, transmit enable is presented prior to the rising edge of the reference clock. TX_EN indicates the presence of valid data inputs on TX_D[1:0]. **RGMII Transmit Control:** Transmit control combines transmit enable and transmit error indication into a single signal. TX_EN is presented prior to the rising edge of TX_CLK; TX_ER is presented prior to the falling edge of TX_CLK. **Unused in SGMII mode**
TX_D3	30	PD, I	**Transmit Data:** In MII and RGMII modes, the transmit data nibble, TX_D[3:0], is received from the MAC prior to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] is received from the MAC prior to the rising edge of the reference clock. TX_D[3:2] are not used in RMII mode. **TX_M / TX_P:** Differential SGMII Data Input. These pins receive data that is transmitted from the MAC to the PHY.
TX_D2	31		
TX_D1 TX_P	32		
TX_D0 TX_M	33		
SERIAL MANAGEMENT INTERFACE			
MDC	1	I	**Management Data Clock:** Synchronous clock to the MDIO serial management input and output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25 MHz. There is no minimum clock rate.
MDIO	36	OD, IO	**Management Data Input/Output:** Bidirectional management data signal that may be sourced by the management station or the PHY. This pin requires a pullup resistor. Recommended to use a resistor between 2.2 kΩ and 9 kΩ.

Table 5-1. Pin Functions (continued)

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
CONTROL INTERFACE			
$\overline{\text{INT}}$	2	PU, OD, O	**Interrupt:** Active-LOW output, which will be asserted LOW when an interrupt condition occurs. This pin has a weak internal pullup. Register access is necessary to enable various interrupt triggers. Once an interrupt event flag is set, register access is required to clear the interrupt event. **Note:** Power-on-RESET (POR) Done interrupt is enabled by default. POR Done interrupt can be cleared by reading register *0x0018*. This pin can be configured as an Active-HIGH output using register *0x0011*.
$\overline{\text{RESET}}$	3	PU, I	**Reset:** Active-LOW input, which initializes or reinitializes the PHY. Asserting this pin LOW for at least 1 µs will force a reset process to occur. All internal registers will reinitialize to their default states as specified for each bit in the Register Maps section. All bootstrap pins are resampled upon deassertion of reset.
WAKE	8	PD, I/O	**WAKE:** Active-HIGH input, which wakes the PHY from TC-10 SLEEP. Asserting this pin HIGH at power-up will prevent the PHY from going to SLEEP. External 2.49kΩ pull down resistor can be used when implementing TC-10 circuit to prevent accidental wake-up. This pin can be directly tied to VSLEEP to wake the device.
INH	10	O, OD	**INH:** Active-HIGH output. This pin will be Hi-Z when the PHY is in TC-10 SLEEP. This pin is HIGH for all other PHY states. External 2.49kΩ pull down resistor must be used when implementing TC-10 circuit. If multiple devices are sharing INH pin, then a single pull down resistor must be used.
CLOCK INTERFACE			
XI	5	I	**Reference Clock Input (RMII):** Reference clock 50-MHz CMOS-level oscillator in RMII Slave mode. Reference clock 25-MHz crystal or oscillator in RMII Master mode. **Reference Clock Input (Other MAC Interfaces):** Reference clock 25-MHz crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only and XO left floating.
XO	4	O	**Reference Clock Output:** XO pin is used for crystal only. This pin must be left floating when a CMOS-level oscillator is connected to XI.
LED/GPIO INTERFACE			
LED_0 / GPIO_0	35	S, PD, IO	**LED_0:** Link Status
LED_1 / GPIO_1	6	S, PD, IO	**LED_1:** Link Status and BLINK for TX/RX Activity
CLKOUT / GPIO_2	16	IO	**Clock Output:** 25-MHz reference clock
MEDIUM DEPENDENT INTERFACE			
TRD_M	13	IO	**Differential Transmit and Receive:** Bidirectional differential signaling configured for 100BASE-T1 operation, IEEE 802.3bw compliant.
TRD_P	12		
GROUND ESCAPE			
GND_ESC	17		**Ground Escape:** Optional ground escape pins. These pins can be connected to ground to optimize PCB layout. These pins are not substitute for power ground connection to DAP. DAP must always be connected to power ground. This pin can be left unconnected if not used.
GND_ESC	18		**Ground Escape:** Optional ground escape pins. These pins can be connected to ground to optimize PCB layout. These pins are not substitute for power ground connection to DAP. DAP must always be connected to power ground. This pin can be left unconnected if not used.
POWER CONNECTIONS			
VDDA	11	SUPPLY	**Core Supply:** 3.3 V Recommend using a ferrite bead, 0.47-µF and 0.01-µF ceramic decoupling capacitors; optional ferrite bead.
VDDIO	34	SUPPLY	**IO Supply:** 1.8 V, 2.5 V, or 3.3 V Recommend using ferrite bead 0.47-µF and 0.01-µF ceramic decoupling capacitors; optional ferrite bead.

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Table 5-1. Pin Functions (continued)

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
VDDMAC	22	SUPPLY	**Optional MAC Interface Supply:** 1.8 V, 2.5 V, or 3.3 V Optional separate supply for MAC interface pins. This pin supplies power to the MAC interface pins and can be kept at a different voltage level as compared to other IO pins. Recommend using 0.47-µF, and 0.01-µF ceramic decoupling capacitors; optional ferrite bead. When separate VDDMAC is not required in the system then it must be connected to VDDIO. When connecting to VDDIO, 0.47-µF on the VDDIO can be removed. 0.47-µF must still be connected close to VDDMAC.
VSLEEP	7	SUPPLY	**VSLEEP Supply:** 3.3 V Recommend using 0.1-µF ceramic decoupling capacitors.
GROUND	DAP	GROUND	**Ground:** This must always be connected to power ground.
DO NOT CONNECT			
DNC	19		**DNC:** Do not connect (leave floating)
DNC	20		**DNC:** Do not connect (leave floating)
NO CONNECT			
NC	9		**NC:** No connection. Can be left floating. Connecting to any signal will have no effect on PHY performance.
NC	21		**NC:** No connection. Can be left floating. Connecting to any signal will have no effect on PHY performance.

1. Pin Type:
   I = Input
   O = Output
   IO = Input/Output
   OD = Open Drain
   PD = Internal pulldown
   PU = Internal pullup
   S = Bootstrap configuration pin (all configuration pins have weak internal pullups or pulldowns)
2. When pins are unused, follow the recommended connection requirements provided in the table above. If pins do not have required termination, they may be left floating.

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Table 5-2. Pin States[1]

PIN NAME	POWER-UP / RESET		
	PIN STATE	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	none
$\overline{\text{INT}}$	I	PU	9
$\overline{\text{RESET}}$	I	PU	9
XO	O	none	none
XI	I	none	none
LED_1	I	PD	9
VSLEEP	SUPPLY	none	none
WAKE	I	PD	500
DNC	FLOAT	none	none
INH	OD, O	none	none
VDDA	SUPPLY	none	none
TRD_P	IO	none	none
TRD_M	IO	none	none
RX_ER	I	PD	6
RX_DV	I	PD	6
CLKOUT	O	none	none
GND_ESC	FLOAT	none	none
GND_ESC	FLOAT	none	none
DNC	FLOAT	none	none
DNC	FLOAT	none	none
DNC	FLOAT	none	none
VDDMAC	SUPPLY	none	none
RX_D3	I	PD	9
RX_D2	I	PD	9
RX_D1	I	PD	9
RX_D0	I	PD	9
RX_CLK	I	PD	9
TX_CLK	I	none	none
TX_EN	I	none	none
TX_D3	I	none	none
TX_D2	I	none	none
TX_D1	I	none	none
TX_D0	I	none	none
VDDIO	SUPPLY	none	none
LED_0	I	PD	9
MDIO	OD, IO	none	none

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Table 5-3. Pin States[1]

PIN NAME	MII			RGMII		
	PIN STATE	PULL TYPE	PULL VALUE (kΩ)	PIN STATE	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	none	I	none	none
$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
$\overline{\text{RESET}}$	I	PU	9	I	PU	9
XO	O	none	none	O	none	none
XI	I	none	none	I	none	none
LED_1	O	none	none	O	none	none
VSLEEP	SUPPLY	none	none	SUPPLY	none	none
WAKE	I	PD	500	I	PD	500
DNC	FLOAT	none	none	FLOAT	none	none
INH	OD, O	none	none	OD, O	none	none
VDDA	SUPPLY	none	none	SUPPLY	none	none
TRD_P	IO	none	none	IO	none	none
TRD_M	IO	none	none	IO	none	none
RX_ER	O	none	none	I	PD	6
RX_DV	O	none	none	O	none	none
CLKOUT	O	none	none	O	none	none
GND_ESC	FLOAT	none	none	FLOAT	none	none
GND_ESC	FLOAT	none	none	FLOAT	none	none
DNC	FLOAT	none	none	FLOAT	none	none
DNC	FLOAT	none	none	FLOAT	none	none
DNC	FLOAT	none	none	FLOAT	none	none
VDDMAC	SUPPLY	none	none	SUPPLY	none	none
RX_D3	O	none	none	O	none	none
RX_D2	O	none	none	O	none	none
RX_D1	O	none	none	O	none	none
RX_D0	O	none	none	O	none	none
RX_CLK	O	none	none	O	none	none
TX_CLK	O	none	none	I	none	none
TX_EN	I	none	none	I	none	none
TX_D3	I	none	none	I	none	none
TX_D2	I	none	none	I	none	none
TX_D1	I	none	none	I	none	none
TX_D0	I	none	none	I	none	none
VDDIO	SUPPLY	non	none	SUPPLY	non	none
LED_0	O	none	none	O	none	none
MDIO	OD, IO	none	none	OD, IO	none	none

Table 5-4. Pin States[1]

PIN NAME	RMII Master			RMII Slave		
	PIN STATE	PULL TYPE	PULL VALUE (kΩ)	PIN STATE	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	none	I	none	none
$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
$\overline{\text{RESET}}$	I	PU	9	I	PU	9
XO	O	none	none	O	none	none
XI	I	none	none	I	none	none
LED_1	O	none	none	O	none	none
VSLEEP	SUPPLY	none	none	SUPPLY	none	none
WAKE	I	PD	500	I	PD	500
DNC	FLOAT	none	none	FLOAT	none	none
INH	OD, O	none	none	OD, O	none	none
VDDA	SUPPLY	none	none	SUPPLY	none	none
TRD_P	IO	none	none	IO	none	none
TRD_M	IO	none	none	IO	none	none
RX_ER	O	none	none	O	none	none
RX_DV	O	none	none	O	none	none
CLKOUT	O	none	none	O	none	none
GND_ESC	FLOAT	none	none	FLOAT	none	none
GND_ESC	FLOAT	none	none	FLOAT	none	none
DNC	FLOAT	none	none	FLOAT	none	none
DNC	FLOAT	none	none	FLOAT	none	none
DNC	FLOAT	none	none	FLOAT	none	none
VDDMAC	SUPPLY	none	none	SUPPLY	none	none
RX_D3	O, 50MHz	none	none	I	PD	9
RX_D2	I	PD	9	I	PD	9
RX_D1	O	none	none	O	none	none
RX_D0	O	none	none	O	none	none
RX_CLK	I	PD	9	I	PD	9
TX_CLK	I	none	none	I	none	none
TX_EN	I	none	none	I	none	none
TX_D3	I	none	none	I	none	none
TX_D2	I	none	none	I	none	none
TX_D1	I	none	none	I	none	none
TX_D0	I	none	none	I	none	none
VDDIO	SUPPLY	non	none	SUPPLY	non	none
LED_0	O	none	none	O	none	none
MDIO	OD, IO	none	none	OD, IO	none	none

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Table 5-5. Pin States(1)

PIN NAME	SGMII		
	PIN STATE	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	none
$\overline{\text{INT}}$	OD, O	PU	9
$\overline{\text{RESET}}$	I	PU	9
XO	O	none	none
XI	I	none	none
LED_1	O	none	none
VSLEEP	SUPPLY	none	none
WAKE	I	PD	500
DNC	FLOAT	none	none
INH	OD, O	none	none
VDDA	SUPPLY	none	none
TRD_P	IO	none	none
TRD_M	IO	none	none
RX_ER	I	PD	6
RX_DV	I	PD	6
CLKOUT	O	none	none
GND_ESC	FLOAT	none	none
GND_ESC	FLOAT	none	none
DNC	FLOAT	none	none
DNC	FLOAT	none	none
DNC	FLOAT	none	none
VDDMAC	SUPPLY	none	none
RX_D3	O	none	none
RX_D2	O	none	none
RX_D1	I	PD	9
RX_D0	I	PD	9
RX_CLK	I	PD	9
TX_CLK	I	none	none
TX_EN	I	none	none
TX_D3	I	none	none
TX_D2	I	none	none
TX_D1	I	none	none
TX_D0	I	none	none
VDDIO	SUPPLY	non	none
LED_0	O	none	none
MDIO	OD, IO	none	none

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
Input Voltage	VDDA	–0.3		4	V
Input Voltage	VDDIO/VDDMAC (3.3V)	–0.3		4	V
Input Voltage	VDDIO/VDDMAC (2.5V)	–0.3		2.9	V
Input Voltage	VDDIO/VDDMAC (1.8V)	–0.3		2.2	V
Input Voltage	VSLEEP	-0.3		4	V
Pins	MDI	–0.3		4	V
Pins	MAC interface	–0.3		VDDMAC + 0.3	V
Pins	MDIO, MDC, GPIO, XI, XO, INT, RESET, CLKOUT	–0.3		VDDIO + 0.3	V
Pins	WAKE, INH	–0.3		VSLEEP + 0.3	V
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
			TRD_N, TRD_P pins	±6000	
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±750	
		IEC 61000-4-2 contact discharge	TRD_N, TRD_P pins	±6000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIO / VDDMAC	IO Supply Voltage, 1.8V operation	1.62	1.8	1.98	V
	IO Supply Voltage, 2.5V operation	2.25	2.5	2.75	
	IO Supply Voltage, 3.3V operation	2.97	3.3	3.63	
VDDA	Core Supply Voltage, 3.3V	2.97	3.3	3.63	V
VSLEEP	Sleep Supply Voltage, 3.3V	2.97	3.3	3.63	V
T_A	Ambient temperature	–40		125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		DP83TC812 RHA (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
100BASE-T1 PMA CONFORMANCE						
V_{OD-MDI}	Output Differential Voltage	$R_{L(diff)}$ = 100Ω			2.2	V
$R_{MDI-Diff}$	Integrated Differential Output Termination	TRD_P and TRD_M		100		Ω
BOOTSTRAP DC CHARACTERISTICS (2 Level)						
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 3.3V ±10%, 2-level strap	0		0.8	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 3.3V ±10%, 2-level strap	2		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 2.5V ±10%, 2-level strap	0		0.7	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 2.5V ±10%, 2-level strap	1.5		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 1.8V ±10%, 2-level strap	0		0.35 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 1.8V ±10%, 2-level strap	0.65 x VDDIO		VDDIO	V
BOOTSTRAP DC CHARACTERISTICS (3 Level)						
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0		0.18 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0.22 x VDDIO		0.42 x VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0.46 x VDDIO		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0		0.19 x VDDIO	
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0.27 x VDDIO		0.41 x VDDIO	
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0.58 x VDDIO		VDDIO	
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0		0.35 x VDDIO	
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0.40 x VDDIO		0.75 x VDDIO	

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0.84 x VDDIO		VDDIO	
IO CHARACTERISTICS						
V_{IH}	High Level Input Voltage	VDDIO = 3.3V ±10%	2			V
V_{IL}	Low Level Input Voltage	VDDIO = 3.3V ±10%			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ±10%	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 3.3V ±10%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 2.5V ±10%	1.7			V
V_{IL}	Low Level Input Voltage	VDDIO = 2.5V ±10%			0.7	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ±10%	2			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 2.5V ±10%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 1.8V ±10%	0.65*VDDIO			V
V_{IL}	Low Level Input Voltage	VDDIO = 1.8V ±10%			0.35*VDDIO	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ±10%	VDDIO-0.45			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 1.8V ±10%			0.45	V
I_{IH} (105C)	Input High Current(1)	T_A = -40°C to 105°C, VIN=VDDIO, All pins	-10		10	µA
I_{IH}	Input High Current(1)	T_A = -40°C to 125°C, VIN=VDDIO	-10		10	µA
I_{IL} (125C)	Input Low Current(1)	T_A = 105°C to 125°C, VIN=GND	-25		25	µA
Iozh	Tri-state Output High Current(2)	T_A = -40°C to 125°C, VIN=VDDIO, All pins except RX_CTRL and RX_ER	-10		10	µA
Iozh	Tri-state Output High Current(2)	T_A = -40°C to 125°C, VIN=VDDIO, RX_CTRL and RX_ER	-50		50	µA
Iozl	Tri-state Output Low Current(2)	T_A = -40°C to 125°C, VOUT=GND	-10		10	µA
R_{pulldn}	Internal Pull Down Resistor	RX_D[3:0], RX_CLK, LED_0, LED_1	6.75	9	11.25	kΩ
R_{pulldn}	Internal Pull Down Resistor	RX_CTRL, RX_ER	4.725	6.5	7.875	kΩ
R_{pulldn}	Internal Pull Down Resistor	WAKE		425		kΩ
R_{pullup}	Internal Pull Up Resistor	INT, RESET	6.75	9	11.25	kΩ
XI V_{IH}	High Level Input Voltage		1.3		VDDIO	V
XI V_{IL}	Low Level Input Voltage				0.5	V
C_{IN}	Input Capacitance XI			1		pF
C_{IN}	Input Capacitance INPUT PINS			5		pF
C_{OUT}	Output Capacitance XO			1		pF
C_{OUT}	Output Capacitance OUTPUT PINS			5		pF

ADVANCE INFORMATION

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{series}	Integrated MAC Series Termination Resistor	RX_D[3:0], RX_ER, RX_DV, RX_CLK		50		Ω
POWER CONSUMPTION						
I(3V3)	MII	-40°C to 125°C		57		mA
I(3V3)	RMII	-40°C to 125°C		57		mA
I(3V3)	RGMII	-40°C to 125°C		57		mA
I(3V3)	SGMII	-40°C to 125°C		81		mA
I(VDDIO=3.3V)	MII	-40°C to 125°C, VDDIO = VDDMAC		19		mA
I(VDDIO=3.3V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		18		mA
I(VDDIO=3.3V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		13		mA
I(VDDIO=3.3V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		7		mA
I(VDDIO=2.5V)	MII	-40°C to 125°C, VDDIO = VDDMAC		12		mA
I(VDDIO=2.5V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		12		mA
I(VDDIO=2.5V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		12		mA
I(VDDIO=2.5V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		6		mA
I(VDDIO=1.8V)	MII	-40°C to 125°C, VDDIO = VDDMAC		9		mA
I(VDDIO=1.8V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		9		mA
I(VDDIO=1.8V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		9		mA
I(VDDIO=1.8V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		4		mA
POWER CONSUMPTION (LOW POWER MODE)						
I(VDDA3V3)	IEEE Power Down	-40°C to 125°C, All interfaces		8		mA
I(VDDA3V3)	TC-10 Sleep	-40°C to 125°C, All interfaces		30		mA
I(VDDA3V3)	RESET	-40°C to 125°C, All interfaces		9		mA
I(VDDA3V3)	Standby	-40°C to 125°C, MII		15		mA
I(VDDA3V3)	Standby	-40°C to 125°C, RMII		15		mA
I(VDDA3V3)	Standby	-40°C to 125°C, RGMII		15		mA
I(VDDA3V3)	Standby	-40°C to 125°C, SGMII		15		mA
I(VDDIO=3.3V)	IEEE Power Down	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		15		mA
I(VDDIO=3.3V)	TC-10 Sleep	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		15		mA

ADVANCE INFORMATION

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I(VDDIO=3.3V)	RESET	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		15		mA
I(VDDIO=3.3V)	Standby	-40℃ to 125℃, MII, VDDIO=VDDMAC		19		mA
I(VDDIO=3.3V)	Standby	-40℃ to 125℃, RMII, VDDIO=VDDMAC		16		mA
I(VDDIO=3.3V)	Standby	-40℃ to 125℃, RGMII, VDDIO=VDDMAC		14		mA
I(VDDIO=3.3V)	Standby	-40℃ to 125℃, SGMII, VDDIO=VDDMAC		14		mA
I(VDDIO=2.5V)	IEEE Power Down	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		10		mA
I(VDDIO=2.5V)	TC-10 Sleep	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		10		mA
I(VDDIO=2.5V)	RESET	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		10		mA
I(VDDIO=2.5V)	Standby	-40℃ to 125℃, MII, VDDIO=VDDMAC		14		mA
I(VDDIO=2.5V)	Standby	-40℃ to 125℃, RMII, VDDIO=VDDMAC		11		mA
I(VDDIO=2.5V)	Standby	-40℃ to 125℃, RGMII, VDDIO=VDDMAC		9		mA
I(VDDIO=2.5V)	Standby	-40℃ to 125℃, SGMII, VDDIO=VDDMAC		9		mA
I(VDDIO=1.8V)	IEEE Power Down	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		7		mA
I(VDDIO=1.8V)	TC-10 Sleep	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		7		mA
I(VDDIO=1.8V)	RESET	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		7		mA
I(VDDIO=1.8V)	Standby	-40℃ to 125℃, MII, VDDIO=VDDMAC		10		mA
I(VDDIO=1.8V)	Standby	-40℃ to 125℃, RMII, VDDIO=VDDMAC		7		mA
I(VDDIO=1.8V)	Standby	-40℃ to 125℃, RGMII, VDDIO=VDDMAC		6		mA
I(VDDIO=1.8V)	Standby	-40℃ to 125℃, SGMII, VDDIO=VDDMAC		6		mA
I(VSLEEP)	TC-10 Sleep	-40℃ to 125℃, All interfaces		7		µA
SGMII Input						
$R_{IN-DIFF}$	Receiver differential input impedance (DC)		80		120	ohm
SGMII Output						
	Clock signal duty cycle	SO_P and SO_N, AC coupled, 0101010101 pattern	48		52	%
	Vod fall time (20%-80%)	SO_P and SO_N, AC coupled, 0101010101 pattern	100		200	ps
	Vod rise time (20%-80%)	SO_P and SO_N, AC coupled, 0101010101 pattern	100		200	ps
	Output Jitter	SO_P and SO_N, AC coupled			300	ps

ADVANCE INFORMATION

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output Differential Voltage	SO_P and SO_N, AC coupled	150		400	mV

(1) For pins: MDC, TX_CLK, TX_CTRL, TX_D[3:0], and RESET_N

(2) For pins: RX_D[3:0], RX_CLK, RX_CTRL, MDIO, INT_N, and XO.

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
MII TIMING						
T1.1	TX_CLK High / Low Time		16	20	24	ns
T1.2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK		10			ns
T1.3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK		0			ns
T2.1	RX_CLK High / Low Time		16	20	24	ns
T2.2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising		10		30	ns
RMII MASTER TIMING						
T3.1	RMII Master Clock Period			20		ns
	RMII Master Clock Duty Cycle		35		65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to RMII Master Clock		4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from RMII Master Clock		2			ns
T3.4	RX_D[1:0], RX_ER, CRS_DV Delay from RMII Master Clock rising edge		4	10	14	ns
RMII SLAVE TIMING						
T3.1	Input Reference Clock Period			20		ns
	Reference Clock Duty Cycle		35		65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to XI Clock rising		4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from XI Clock rising		2			ns
T3.4	RX_D[1:0], RX_ER, CRS_DV Delay from XI Clock rising		4		14	ns
RGMII INPUT TIMING						
T_{cyc}	Clock Cycle Duration	TX_CLK	36	40	44	
$T_{setup(align)}$	TX_D[3:0], TX_CTRL Setup to TX_CLK (Align Mode)		1	2		ns
$T_{hold(align)}$	TX_D[3:0], TX_CTRL Hold from TX_CLK (Align Mode)		1	2		ns
RGMII OUTPUT TIMING						
$T_{skew(align)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Align Mode Enabled)	On PHY Pins	-750		750	ps
$T_{setup(shift)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Shift Mode Enabled, default)	On PHY Pins	1	2		ns
$T_{hold(shift)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Shift Mode Enabled, default)	On PHY Pins	1	2		ns
T_{cyc}	Clock Cycle Duration	RX_CLK	36	40	44	ns
Duty_G	Duty Cycle	RX_CLK	45	50	55	%
Tr/Tf	Rise / Fall Time (20% to 80%)	C_{LOAD} = 5pF			1	ns
SMI TIMING						
T4.1	MDC to MDIO (Output) Delay Time		0		10	ns
T4.2	MDIO (Input) to MDC Setup Time		10			ns
T4.3	MDIO (Input) to MDC Hold Time		10			ns

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6.6 Timing Requirements (continued)

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
	MDC Frequency			2.5	25	MHz
POWER-UP TIMING						
T5.1	Supply ramp time: For all supplies		0.6		39	ms
T5.2	Supply ramp delay offset: For all supplies				50	ms
T5.3	XTAL Startup / Settling: Powerup to XI good/stabilized			0.35		ms
T5.4	Oscillator stabilization time from power up				50	ms
	Last Supply power up To Reset Release				50	ms
T5.5	Post power-up to SMI ready: stabilization time prior to MDC preamble for register access after power up				50	ms
T5.6	Power-up to Strap latch-in				50	ms
T5.7	CLKOUT Startup/Settling: Powerup to CLKOUT good/stabilized				50	ms
T5.8	Power-up to idle stream				50	ms
RESET TIMING (RESET_N)						
T6.1	Reset Pulse Width: Miminum Reset pulse width to be able to reset		720			ns
T6.2	Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access		30			us
T6.3	Reset to Strap latch-in: Hardware configuration pins transition to output drivers			720		ns
T6.5	Reset to idle stream				1700	µs
TRANSMIT LATENCY TIMING						
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI				8	µs
RECEIVE LATENCY TIMING						
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL				8	µs
25 MHz OSCILLATOR REQUIREMENTS						
	Frequency Tolerance		-100		+100	ppm
	Rise / Fall Time (10%-90%)				8	ns
	Jitter Tolerance (RMS)				25	ps
	XI Duty Cycle in external clock mode		40		60	%
50 MHz OSCILLATOR REQUIREMENTS						
	Frequency			50		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Rise / Fall Time (10% - 90%)				4	ns
	Duty Cycle		35		65	%
25 MHz CRYSTAL REQUIREMENTS						
	Frequency			25		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Equivalent Series Resistance				50	Ω
OUTPUT CLOCK TIMING (25 MHz)						
	Frequency (PPM)		-100		100	-
	Duty Cycle		40		60	%
	Rise Time				5000	ps
	Fall Time				5000	ps
	Jitter (Short Term)				1000	ps

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6.6 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Frequency			25		MHz

6.7 Timing Diagrams

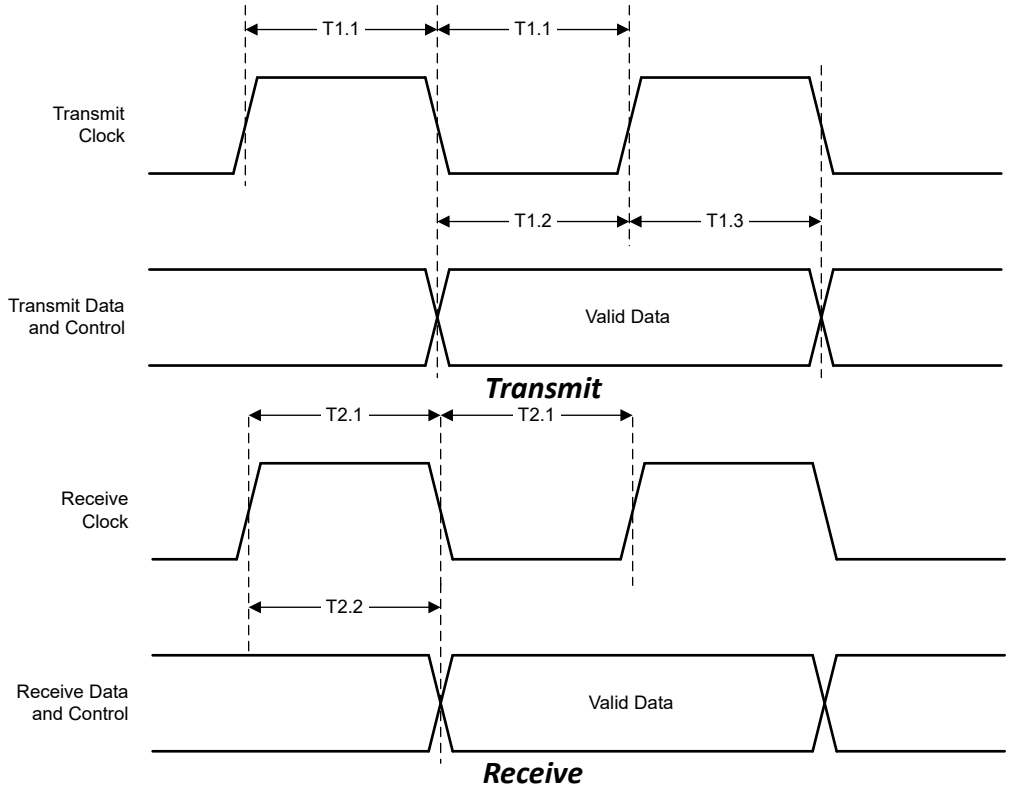

Figure 6-1. MII Timing

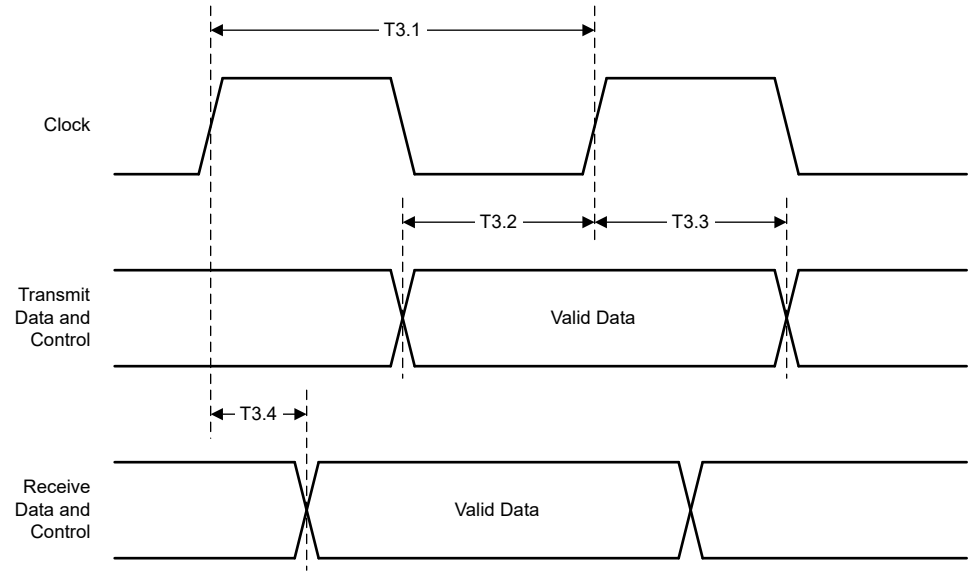

Figure 6-2. RMII Transmit and Receive Timing

ADVANCE INFORMATION

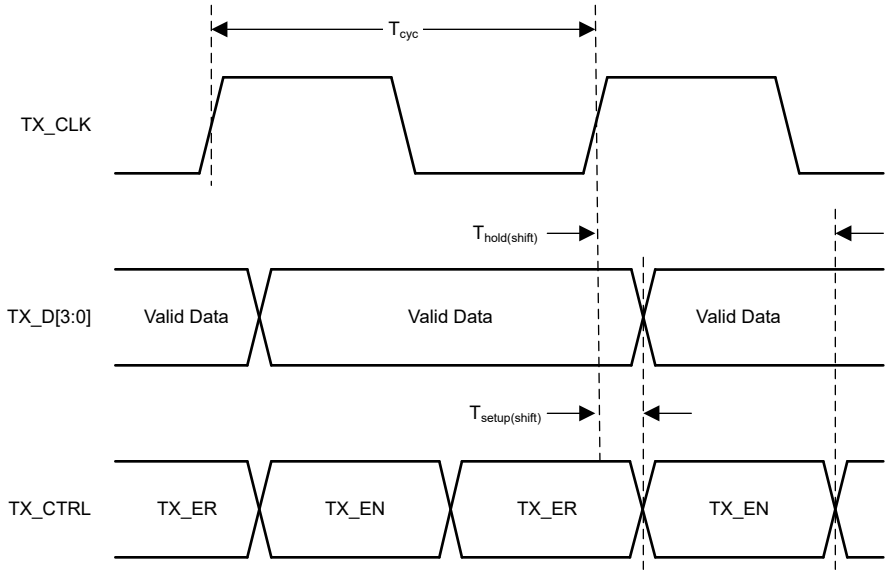

Figure 6-3. RGMII Transmit Timing (Internal Delay Enabled)

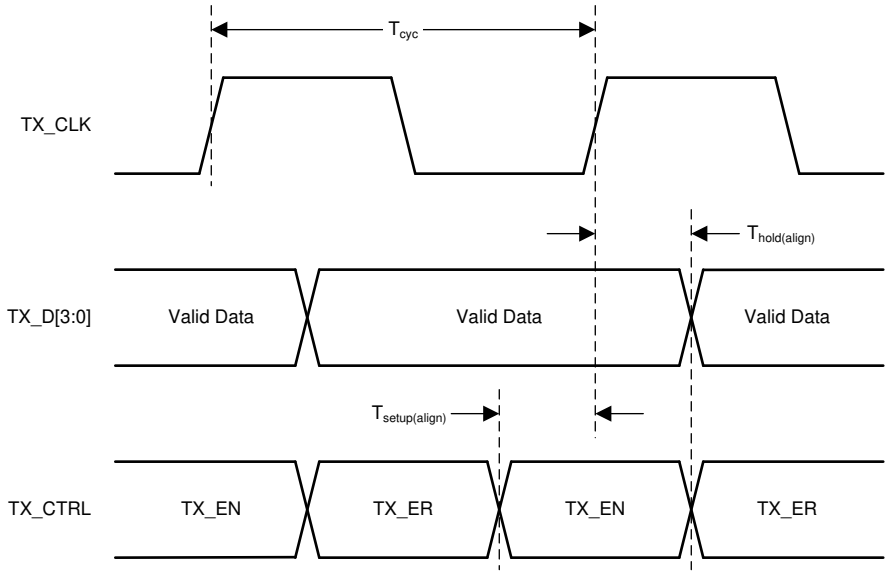

Figure 6-4. RGMII Transmit Timing (Internal Delay Disabled)

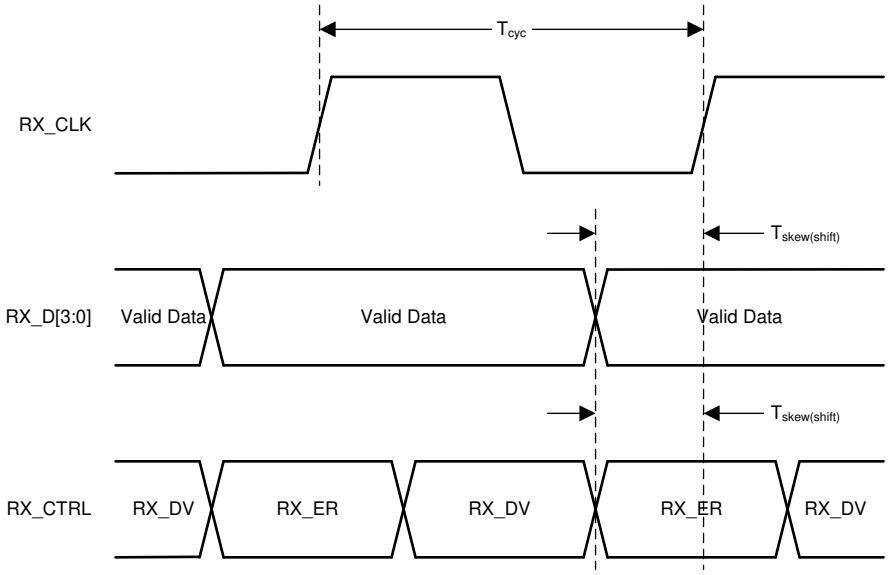

Figure 6-5. RGMII Receive Timing (Internal Delay Enabled)

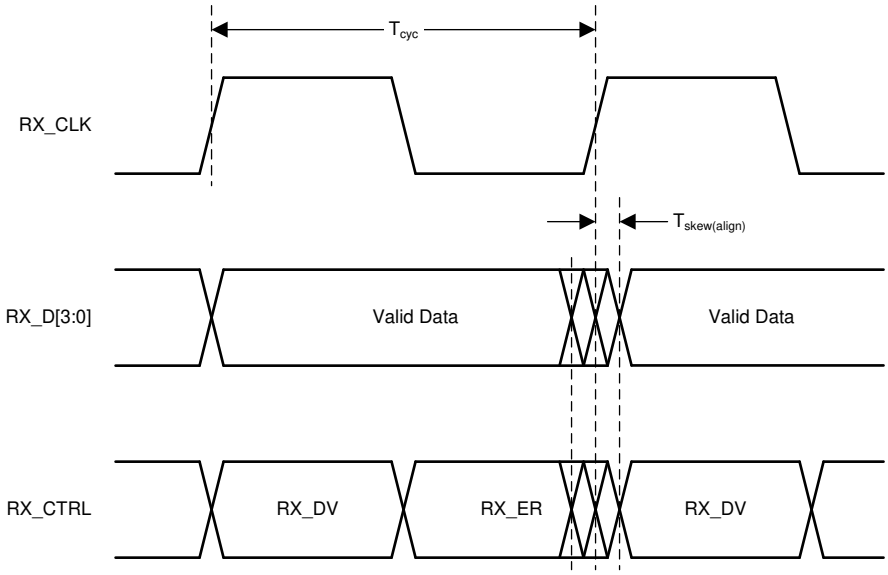

Figure 6-6. RGMII Receive Timing (Internal Delay Disabled)

ADVANCE INFORMATION

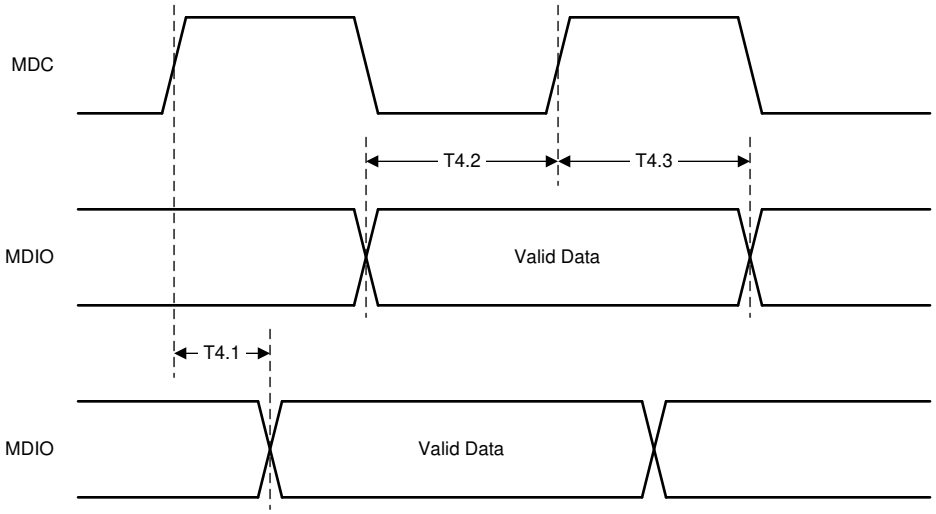

Figure 6-7. Serial Management Timing

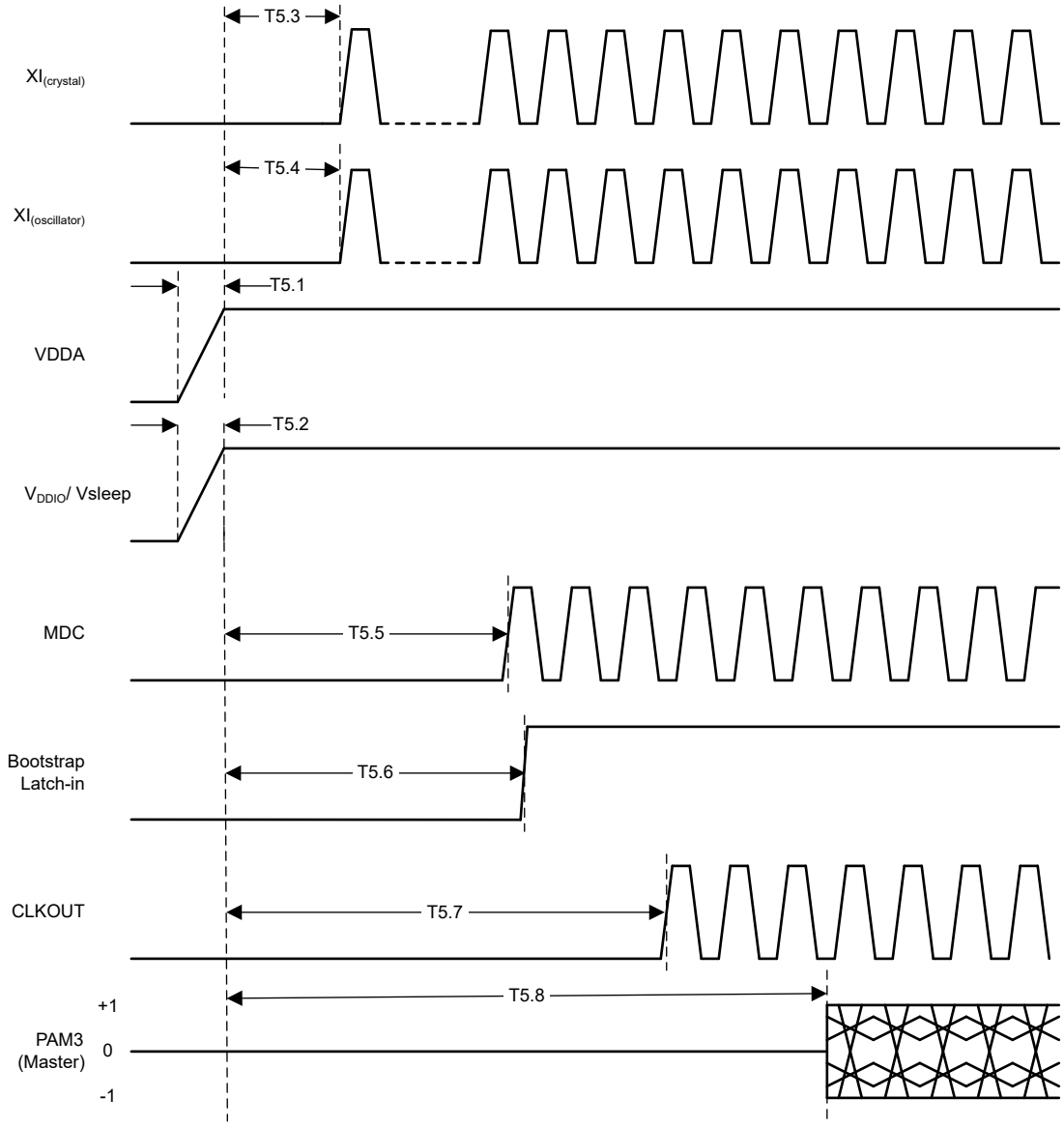

Figure 6-8. Power-Up Timing

ADVANCE INFORMATION

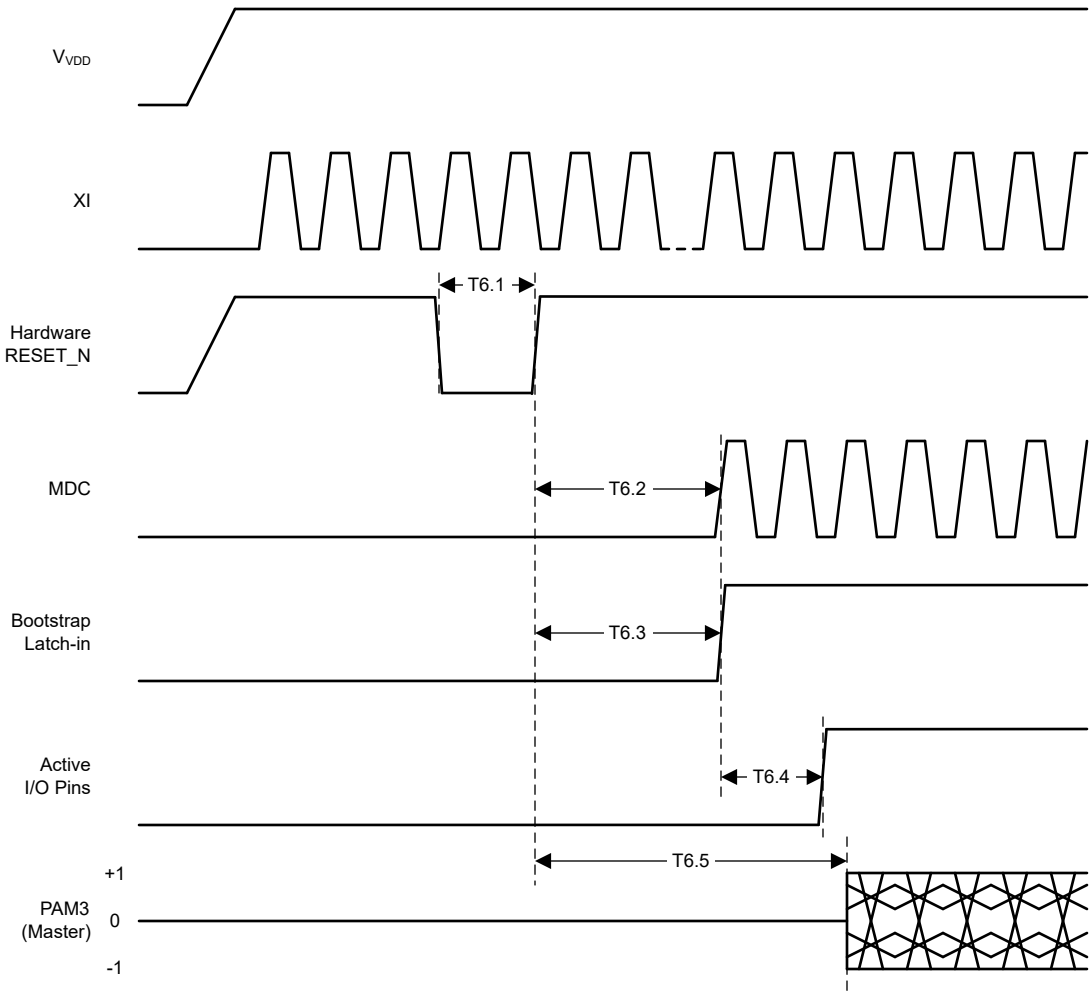

Figure 6-9. Reset Timing

7 Detailed Description

7.1 Overview

The DP83TC812S-Q1 is a 100BASE-T1 automotive Ethernet Physical Layer transceiver. It is IEEE 802.3bw compliant and AEC-Q100 qualified for automotive applications. The DP83TC812S-Q1 is interoperable with both BroadR-Reach PHYs and 100BASE-T1 PHYs.

The DP83TC812S-Q1 also supports Open Alliance TC-10 low power mode for additional power savings. The PHY supports WAKE and INH pins for implementing TC-10 functionality in the system.

This device is specifically designed to operate at 100-Mbps speed while meeting stringent automotive EMC limits. TheDP83TC812S-Q1 transmits PAM3 ternary symbols at 66.667 MHz over unshielded single twisted-pair cable. It is application flexible; supporting MII, RMII, RGMII, and SGMII in a single 36-pin VQFN wettable flank package.

There is an extensive Diagnostic Tool Kit within the DP83TC812S-Q1 for both in-system use as well as debug, compliance and system prototyping for bring-up. The DP83TC812S-Q1 can meet IEC61000-4-2 Level 4 electrostatic discharge limits and it also includes an on-chip ESD sensor for detecting ESD events in real-time.

7.2 Functional Block Diagram

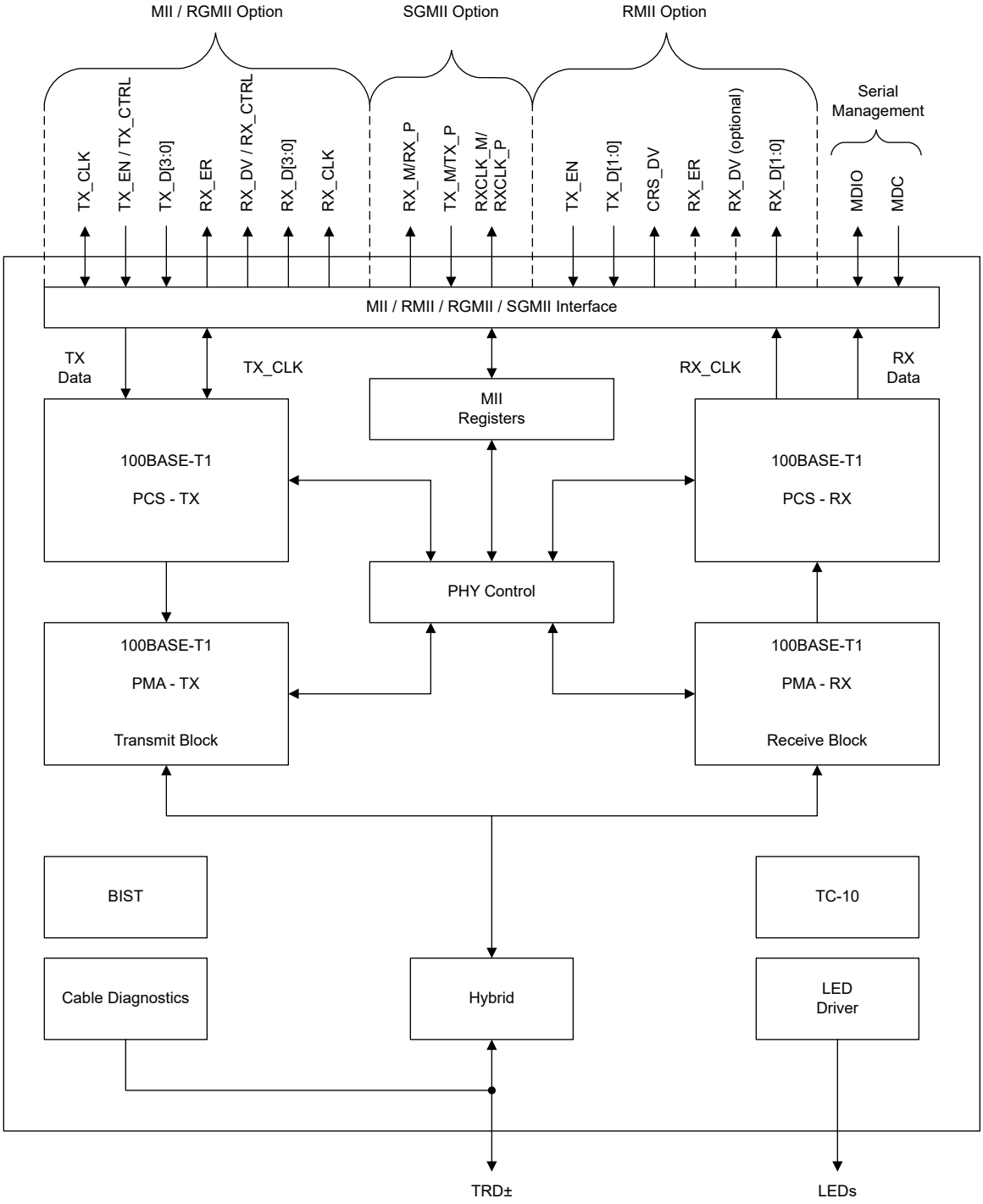

Figure 7-1. DP83TC812S-Q1

7.3 Feature Description

7.3.1 Compliance Test Modes

There are four PMA compliance test modes required in IEEE 802.3bw, sub-clause 96.5.2, which are all supported by the DP83TC812-Q1 . These compliance test modes include: transmitter waveform Power Spectral Density (PSD) mask, amplitude, distortion, 100BASE-T1 Master jitter, 100BASE-T1 Slave jitter, droop, transmitter frequency, frequency tolerance, return loss, and mode conversion. Any of the three GPIOs can be used to output TX_TCLK for the 100BASE-T1 Slave jitter measurement.

7.3.1.1 Test Mode 1

Test mode 1 evaluates transmitter droop. In test mode 1, the DP83TC812-Q1 transmits '+1' symbols for a minimum of 600 ns followed by '–1' symbols for a minimum of 600 ns. This pattern is repeated continuously until the test mode is disabled.

Test mode 1 is enabled by setting bits[15:13] = 0b001 in the MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.1.2 Test Mode 2

Test mode 2 evaluates the transmitter 100BASE-T1 Master mode jitter. In test mode 2, the DP83TC812-Q1 transmits a {+1,-1} data symbol sequence. The transmitter synchronizes the transmitted symbols from the local reference clock.

Test mode 2 is enabled by setting bits[15:13] = 0b010 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.1.3 Test Mode 4

Test mode 4 evaluates the transmitter distortion. In test mode 4, the DP83TC812-Q1 transmits the sequence of symbols generated by Equation 1:

$$g(x) = 1 + x^9 + x^{11} \quad (1)$$

The bit sequences, x0n and x1n, are generated from combinations of the scrambler in accordance to Equation 2 and Equation 3:

$$'x0_n = Scr_n[0] \quad (2)$$

$$x1_n = Scr_n[1] \text{ ^ } Scr_n[4] \quad (3)$$

Example streams of the 3-bit nibbles are shown in Table 7-1.

Table 7-1. Transmitter Test Mode 4 Symbol Mapping

x1n	x0n	PAM3 SYMBOL
0	0	0
0	1	+1
1	0	0
1	1	–1

Test mode 4 is enabled by setting bits[15:13] = 0b100 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.1.4 Test Mode 5

Test mode 5 evaluates the transmitter PSD mask. In test mode 5, the DP83TC812-Q1 transmits a pseudo-random sequence of PAM3 symbols.

Test mode 5 is enabled by setting bits[15:13] = 0b101 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

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7.4 Device Functional Modes

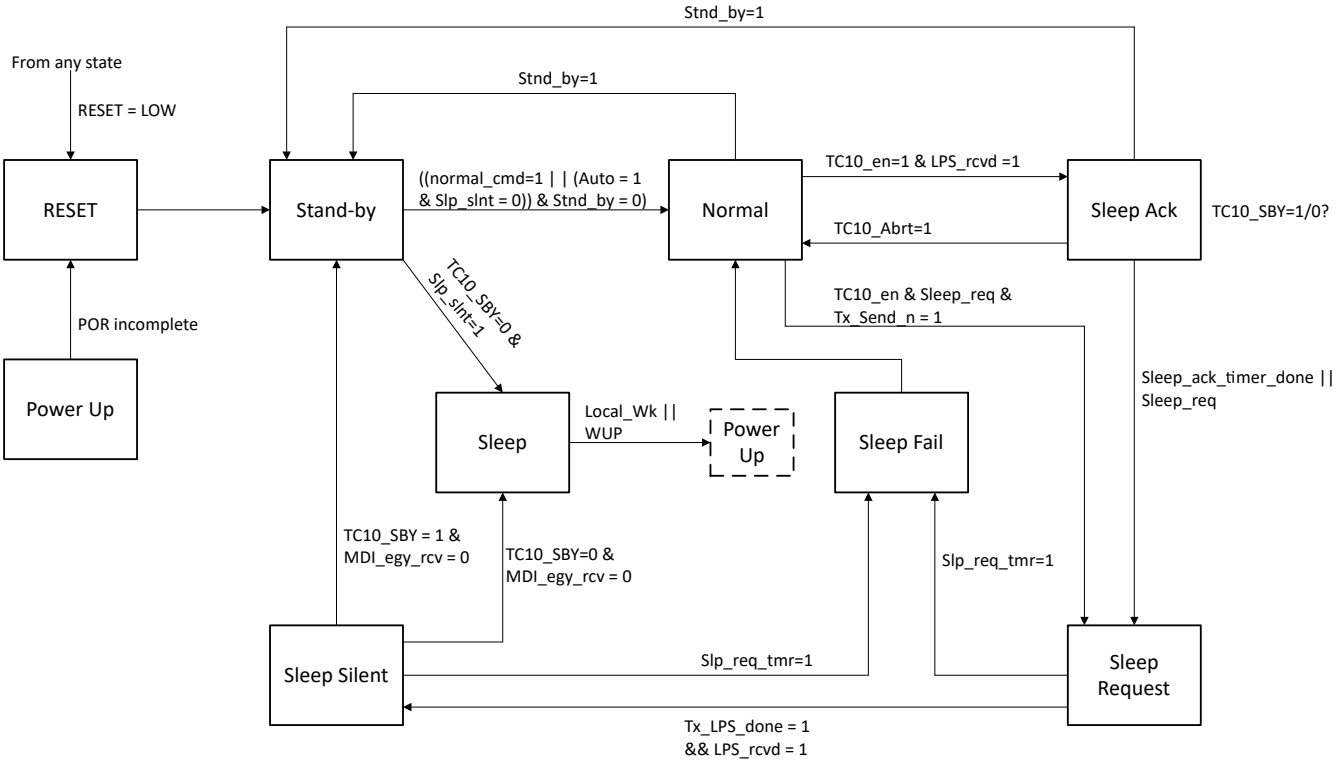

Figure 7-2. PHY Operation State Diagram

ADVANCE INFORMATION

7.4.1 Power Down

When any of the supply rails are below the POR threshold (~0.6V), the PHY is in a power-down state. All digital IOs will remain in high impedance states and analog blocks are disabled. PMA termination is not present when powered down.

7.4.2 Reset

Reset is activated upon power-up, when $\overline{\text{RESET}}$ is pulled LOW (for the minimum reset pulse time) or if hardware reset is initiated by setting bit[15] in register 0x1F. All digital circuitry is cleared along with register settings during reset. Once reset completes, device bootstraps are re-sampled and associated bootstrap registers are set accordingly. PMA termination is not present in reset.

7.4.3 Standby

The device (100BASE-T1 Master mode only) automatically enters into standby post power-up and reset so long that all supplies including VSLEEP are available and the device is bootstrapped for managed operation.

In standby, all PHY functions are operational except for PCS and PMA blocks. The PMA termination is also not present. Link establishment is not possible in standby and data cannot be transmitted or received. SMI functions are operational and register configurations are maintained.

If the device is configured for autonomous operation through bootstrap setting, the PHY automatically switches to normal operation once POR is complete.

7.4.4 Normal

Normal mode can be entered from either autonomous or managed operation. When in autonomous operation, the PHY will automatically try to establish a link with a valid Link Partner once POR is complete.

In managed operation, SMI access is required to allow the device to exit standby (100BASE-T1 Master mode only); commands issued through the SMI allow the device to exit standby and enables both the PCS and PMA blocks. All device features are operational in normal mode.

Autonomous operation can be enabled through SMI access by setting bit[6] in the register 0x18B.

7.4.5 Sleep Request

Sleep request is entered when switching from normal mode to sleep mode. This is an intermediate state and is used to for a smooth transition into sleep mode. In sleep request mode, the PHY transmits LPS code-groups, informing the Link Partner that sleep is requested.

PHY sleep_rqst_timer (default = 16ms) begins once the PHY enters into sleep request mode. LPS decoding at the Link Partner will trigger the LPS RECEIVED interrupt. In sleep request state device waits for Link Partner to send LPS symbols. Once LPS symbols are received by the device, it transitions to SLEEP_SILENT state. If the sleep_rqst_timer expires before device receives LPS codes, the device enters SLEEP FAIL state. .

7.4.6 Sleep Fail

The PHY enters sleep fail mode if the Sleep_rqst_timer expires when in sleep_request state or sleep_silent state.. This indicates that the link partner has not entered sleep mode. After entering sleep fail mode, the PHY transitions to Normal mode.

7.4.7 Sleep

If sleep enable is set, the PHY transitions to sleep mode after the MDI line goes silent when in sleep_silent state; however, if sleep enable is not set, the device transitions to standby after the MDI line goes silent. By default, sleep enable is set. Once in sleep mode, all PHY blocks are disabled except for energy detection on the MDI. All register configurations are lost in sleep mode. No link can be established, data cannot be transmitted or received and SMI access is not available when in sleep mode.

7.4.8 Sleep Ack

When the PHY receives low power sleep requests from the link partner, it enter Sleep Ack mode. In this mode, the PHY allows 8ms for the MAC to decide if TC-10 sleep mode must be enabled or not. If the MAC decides to allow TC-10, the PHY proceeds to the next step in TC-10 state machine. However, the MAC can decide to abort TC-10 and the PHY returns to Normal mode.

7.4.9 Wake-Up

The user can wake up the DP83TC812S-Q1 remotely through energy detection on the MDI or locally using the WAKE pin. For local wake, the WAKE pin must be pulled HIGH. If the WAKE pin is tied LOW, the PHY will only exit sleep if energy is detected on the MDI.

7.4.10 TC10 System Example

The following block diagram explains how TC10 sleep and wake function works in a system.

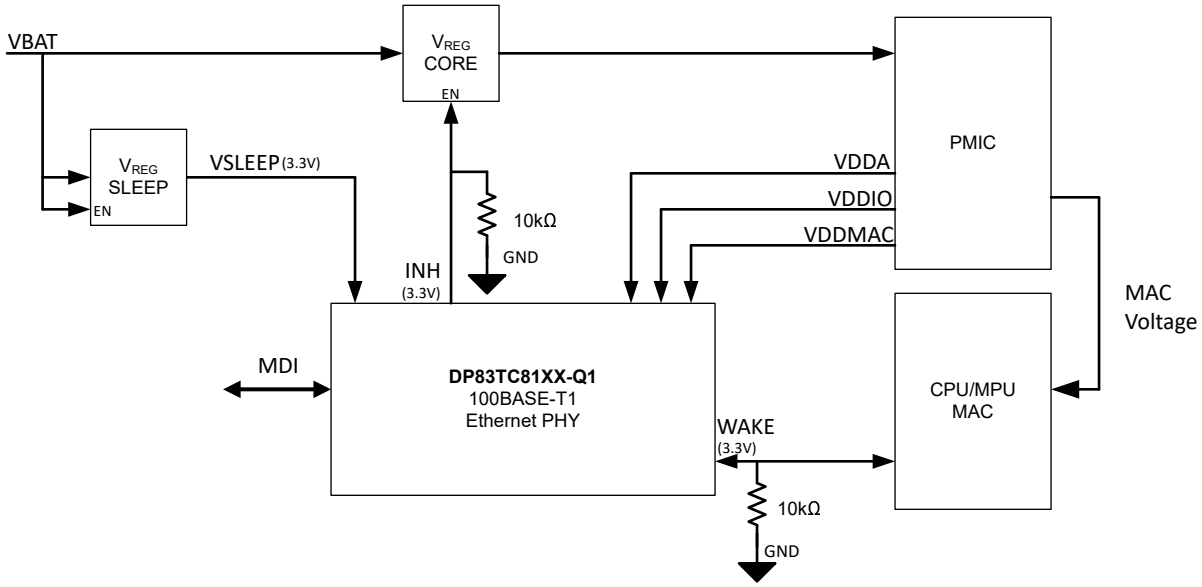

Figure 7-3. TC10 System Example

Remote Wake Up

For remote wake up, the initial state of the system is TC10 sleep. Core voltages to the PHY and MAC are turned off but the VSLEEP of the PHY is present. At some time, wake-up pulses (WUP) are received on the MDI lines. The PHY recevies the message and if its a valid sequence then the PHY wakes up and drives INH pin HIGH. INH pin is used as enable input to voltage regulator (e.g. LDO). Voltage regulators turns on and supplies power to a power management device. The power management device then supplies power to the PHY, MAC, and any other devices on the system. The whole system powers up and becomes operational.

Local Wake Up

For local wake, it is assumed that the MAC is already ON and the PHY is in TC10 sleep. When the MAC wants to wake up the PHY from TC10 sleep, it raises the WAKE pin to 3.3V to send a wake pulse (min. 40µs). The PHY wakes up and drives INH pin HIGH. INH pin is used as enable input to voltage regulator (e.g. LDO). Voltage regulators turns on and supplies power to a power management device. The power management device then supplies power to the PHY. Any other device on the system that depends on the PHY wake up can now be powered up and the system becomes operational.

Local Sleep

When the PHY is in normal operational mode and the MAC needs to put it in TC10 sleep, it initiates the TC10 sleep process via SMI on the PHY. DP83TC812S-Q1 then sends LPS signals on MDI to the link partner. If the link partner also agrees to enter TC10 sleep, the host PHY enters TC10 sleep. It then releases the INH pin and it gets pulled low through the external pull down resistor. Voltage regulator that uses INH pin as enable input will be turned off. PHY, MAC, and any other devices that are dependent on the voltage regulator will be turned off. The PHY will still have VSLEEP voltage present and continue to stay in TC10 sleep.

7.4.11 Serial Management Interface

The Serial Management Interface (SMI) provides access to the DP83TC812S-Q1 internal register space for status information and configuration. The SMI frames and base registers are compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83TC812S-Q1 . Additionally, the DP83TC812S-Q1 includes control and status registers added to clause 45 as defined by IEEE 802.3bw. Access to clause 45 register field is achieved using clause 22 access.

The SMI includes the management clock (MDC) and the management input and output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 24 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 9 DP83TC812S-Q1 PHYs can share a common SMI bus. To distinguish between the PHYs, a 4-bit address is used. During power-up-reset, the DP83TC812S-Q1 latches the PHYAD[3:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up-reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83TC812S-Q1 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83TC812S-Q1 , thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 7-2. SMI Protocol Structure

SMI PROTOCOL	<idle> <start> <op code> <device address> <reg address> <turnaround> <data> <idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

7.4.12 Direct Register Access

Direct register access can be used for the first 31 registers (0x0 through 0x1F).

7.4.13 Extended Register Space Access

The DP83TC812S-Q1 SMI function supports read and write access to the extended register set using registers REGCR (0xD) and ADDAR (0xE) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for Clause 22 for accessing the Clause 45 extended register set.

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REGCR (0xD) is the MDIO Manageable MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of ADDAR (0xE) register to the appropriate MMD.

The DP83TC812S-Q1 supports 3 MMD device addresses:

1. DEVAD[4:0] = 11111 is used for general MMD register accesses for IEEE defined registers as well as vendor defined registers.
2. DEVAD[4:0] = 00001 is used for 100BASE-T1 PMA MMD register accesses. Register names for registers accessible at this device address are preceded by MMD1.
3. DEVAD[4:0] = 00011 is used for vendor specific registers. This registers space is called MMD3.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVADs are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address and data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to (10), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to (11), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write access only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR.

7.4.14 Write Address Operation

To set the address register:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

7.4.14.1 MMD1 - Write Address Operation

For writing register addresses within MMD1 field:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the register address to register ADDAR.

7.4.15 Read Address Operation

To read the address register:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

7.4.15.1 MMD1 - Read Address Operation

For reading register addresses within MMD1 field:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Read the register address from register ADDAR.

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7.4.16 Write Operation (No Post Increment)

To write a register in the extended register set:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.16.1 MMD1 - Write Operation (No Post Increment)

To write a register in the MMD1 extended register set:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

7.4.17 Read Operation (No Post Increment)

To read a register in the extended register set:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) continue to reading the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.17.1 MMD1 - Read Operation (No Post Increment)

To read a register in the MMD1 extended register set:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

7.4.18 Write Operation (Post Increment)

To write a register in the extended register set with post increment:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') or the value 0xC01F (data, post increment on writes function field = 11, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.4.18.1 MMD1 - Write Operation (Post Increment)

To write a register in the MMD1 extended register set with post increment:

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1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') or the value 0xC001 (data, post increment on writes function field = 11, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

7.4.19 Read Operation (Post Increment)

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.4.19.1 MMD1 - Read Operation (Post Increment)

To read a register in the MMD1 extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

7.5 Programming

7.5.1 Strap Configuration

The DP83TC812S-Q1 uses functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up and hardware reset (through either the $\overline{\text{RESET}}$ pin or register access). Some strap pins support 3 levels and some strap pins support 2 levels, which are described in greater detail below. Configuration of the device may be done through strapping or through serial management interface.

Note

Because strap pins are functional pins after reset is deasserted, they must not be connected directly to VDDIO or GND. Either pullup resistors, pulldown resistors, or both are required for proper operation.

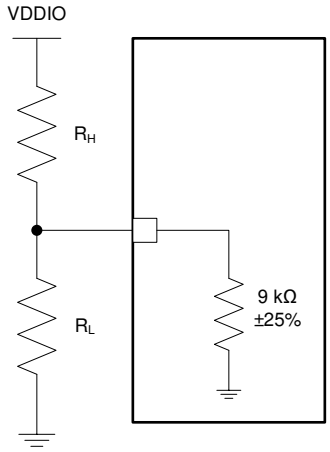

Figure 7-4. Strap Circuit

Table 7-3. Recommended 3-Level Strap Resistor Ratios

MODE	IDEAL RH (kΩ) (VDDIO = 3.3V)[1]	IDEAL RH (kΩ) (VDDIO = 2.5V)[2]	IDEAL RH (kΩ) (VDDIO = 1.8V)[1]
1	OPEN	OPEN	OPEN
2	13	12	4
3	4.5	2	0.8

1. Strap resistors with 10% tolerance.
2. Strap resistors with 1% tolerance.

Table 7-4. Recommended 2-Level Strap Resistors

MODE	IDEAL RH (kΩ) [1, 2]
1	OPEN
2	2.49

1. Strap resistors with upto 10% tolerance can be used.
2. To gain more margin in customer application for 1.8V VDDIO, either 2.1kΩ +/-10% pull-up can be used or resistor accuracy of 2.49kΩ resistor can be limited to 1%.

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The following table describes the PHY configuration bootstraps:

Table 7-5. Bootstraps

PIN NAME	PIN NO.	DEFAULT MODE	STRAP FUNCTION			DESCRIPTION
RX_DV/ RX_CTRL	15	1	**MODE**	**PHY_AD[0]**	**PHY_AD[2]**	PHY_AD: PHY Address ID
			1	0	0	
			2	0	1	
			3	1	1	
RX_ER	14	1	**MODE**	**PHY_AD[1]**	**PHY_AD[3]**	PHY_AD: PHY Address ID
			1	0	0	
			2	0	1	
			3	1	1	
CLKOUT	16	1	**MODE**	**$\overline{\text{AUTO}}$**		$\overline{\text{AUTO}}$: Autonomous Disable. This is a duplicate strap for LED_1. If CLKOUT pin is configured as LED_1 pin then the $\overline{\text{AUTO}}$strap functionality also moves to the CLKOUT pin.
			1	0		
			2	1		
RX_D0	26	1	**MODE**	**MAC[0]**		MAC: MAC Interface Selection
			1	0		
			2	1		
RX_D1	25	1	**MODE**	**MAC[1]**		MAC: MAC Interface Selection
			1	0		
			2	1		
RX_D2	24	1	**MODE**	**MAC[2]**		MAC: MAC Interface Selection
			1	0		
			2	1		
RX_D3	23	1	**MODE**	**CLKOUT_PIN**		CLKOUT_PIN: This strap determines which pin will be used for output clock.
			1	0		
			2	1		
LED_0	35	1	**MODE**	**MS**		MS: 100BASE-T1 Master & 100BASE-T1 Slave Selection **Note:** LED_0 must only be set for bootstrap MODE 1 or MODE 2.
			1	0		
			2	1		
LED_1	6	1	**MODE**	**$\overline{\text{AUTO}}$**		$\overline{\text{AUTO}}$: Autonomous Disable **Note 1:** LED_1 must only be set for bootstrap MODE 1 or MODE 2. **Note 2:** Autonomous bootstrap is only active for 100BASE-T1 Master mode PHYs. This bootstrap is ignored when the PHY is bootstrapped for 100BASE-T1 Slave mode operation.
			1	0		
			2	1		

Table 7-6. 100BASE-T1 Master and 100BASE-T1 Slave Selection Bootstrap

MS	DESCRIPTION
0	100BASE-T1 Slave Configuration
1	100BASE-T1 Master Configuration

Table 7-7. Autonomous Mode Bootstrap

$\overline{\text{AUTO}}$	DESCRIPTION
0	Autonomous Mode, PHY able to establish link after power-up
1	Managed Mode, PHY must be allowed to establish link after power-up based on register write

Table 7-8. MAC Interface Selection Bootstraps

MAC[2]	MAC[1]	MAC[0]	DESCRIPTION
0	0	0	SGMII (4-wire)
0	0	1	MII
0	1	0	RMII Slave
0	1	1	RMII Master
1	0	0	RGMII (Align Mode)
1	0	1	RGMII (TX Internal Delay Mode)
1	1	0	RGMII (TX and RX Internal Delay Mode)
1	1	1	RGMII (RX Internal Delay Mode)

Table 7-9. PHY Address Bootstraps

PHY_AD[3:0]	RX_CTRL STRAP MODE	RX_ER STRAP MODE	DESCRIPTIONSection 7.5.1
0000	1	1	PHY Address: 0b00000 (0x0)
0001	-	-	NA
0010	-	-	NA
0011	-	-	NA
0100	2	1	PHY Address: 0b00001 (0x1)
0101	3	1	PHY Address: 0b00101 (0x5)
0110	-	-	NA
0111	-	-	NA
1000	1	2	PHY Address: 0b00010 (0x2)
1001	-	-	NA
1010	1	3	PHY Address: 0b01010 (0xA)
1011	-	-	NA
1100	2	2	PHY Address: 0b00011 (0x3)
1101	3	2	PHY Address: 0b00111 (0x7)
1110	2	3	PHY Address: 0b01011 (0xB)
1111	3	3	PHY Address: 0b01111 (0xF)

7.5.2 LED Configuration

The DP83TC812S-Q1 supports up to three configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2 (CLKOUT). Several functions can be multiplexed onto the LEDs for different modes of operation. LED operations are selected using registers 0x0450.

Because the LED output pins are also used as strap pins, external components required for strapping and the user must consider the LED usage to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding input upon power up or hardware reset.

Figure 7-5 shows the two proper ways of connecting LEDs directly to the DP83TC812S-Q1 .

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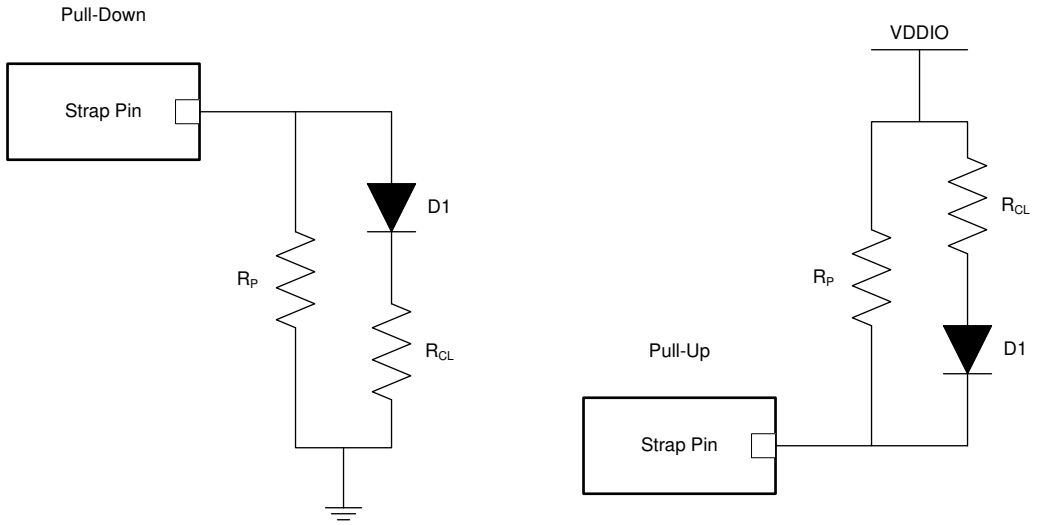

Figure 7-5. Example Strap Connections

7.5.3 PHY Address Configuration

The DP83TC812S-Q1 can be set to respond to any of 9 possible PHY addresses through bootstrap pins. The PHY address is latched into the device upon power-up or hardware reset. Each PHY on the serial management bus in the system must have a unique PHY address.

By default, DP83TC812S-Q1 will latch to a PHY address of 0 (<0b00000>). This address can be changed by adding pullup resistors to bootstrap pins found in Section 7.5.3.

7.6 Register Maps

7.6.1 Register Access Summary

There are two different methods for accessing registers within the field. Direct register access method is only allowed for the first 31 registers (0x0 through 0x1F). Registers beyond 0x1F must be accessed by use of the Indirect Method (Extended Register Space) described in *Section 7.4.13*.

Table 7-10. MMD Register Space Division

MMD REGISTER SPACE	REGISTER ADDRESS RANGE
MMD1F	0x0000 - 0x0EFD
MMD1	0x1000 - 0x1836
MMD3	0x3000 - 0x3001

Note

For MMD1 and MMD3, the most significant nibble of the register address is used to denote the respective MMD space. This nibble must be ignored during actual register access operation. For example, to access register 0x1836, use 0x1 as the MMD indicator and 0x0836 as the register address.

Table 7-11. Register Access Summary

REGISTER FIELD	REGISTER ACCESS METHODS
0x0 through 0x1F	Direct Access
	Indirect Access, MMD1F = '11111' **Example:** to read register 0x17 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x17 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1F Field 0x20 - 0xFFF	Indirect Access, MMD1F = '11111' **Example:** to read register 0x462 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x462 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1 Field 0x0 - 0xFFF	Indirect Access, MMD1 = '00001' **Example:** to read register 0x7 in MMD1 field (register 0x1007) with no post increment Step 1) write 0x1 to register 0xD Step 2) write 0x7 to register 0xE Step 3) write 0x4001 to register 0xD Step 4) read register 0xE

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7.6.2 DP83TC81X Registers

DP83TC81X Registers lists the memory-mapped registers for the DP83TC81X registers. All register offset addresses not listed in DP83TC81X Registers should be considered as reserved locations and the register contents should not be modified.

DP83TC81X

Table 7-12. DP83TC81X Registers

Address	Acronym	Register Name	Section
0x0	BMCR		Go
0x1	BMSR		Go
0x2	PHYIDR1		Go
0x3	PHYIDR2		Go
0xD	REGCR		Go
0xE	ADDAR		Go
0x10	PHYSTS		Go
0x11	PHYSCR		Go
0x12	MISR1		Go
0x13	MISR2		Go
0x15	RECR		Go
0x16	BISCR		Go
0x18	MISR3		Go
0x19	REG_19		Go
0x1E	CDCR		Go
0x1F	PHYRCR		Go
0x18B	LPS_CFG2		Go
0x18C	LPS_CFG3		Go
0x18E	LPS_STATUS		Go
0x198	SQI		Go
0x300	TDR_TX_CFG		Go
0x301	TAP_PROCESS_CFG		Go
0x302	TDR_CFG1		Go
0x303	TDR_CFG2		Go
0x304	TDR_CFG3		Go
0x305	TDR_CFG4		Go
0x306	TDR_CFG5		Go
0x309	TDR_STATUS0		Go
0x30A	TDR_STATUS1		Go
0x30B	TDR_STATUS2		Go
0x30C	TDR_STATUS3		Go
0x30D	TDR_STATUS4		Go
0x30E	TDR_STATUS5		Go
0x310	TDR_TC1		Go
0x450	LEDS_CFG_1		Go
0x451	LEDS_CFG_2		Go
0x452	IO_MUX_CFG_1		Go
0x453	IO_MUX_CFG_2		Go
0x45D	CHIP_SOR_1		Go
0x45E	CHIP_SOR_2		Go

Table 7-12. DP83TC81X Registers (continued)

Address	Acronym	Register Name	Section
0x45F	LED1_CLKOUT_ANA_CTRL		Go
0x466	REV_ID		Go
0x497	TEST_MODE_CTRL		Go
0x560	TC1_CFG_RW		Go
0x561	TC1_LINK_FAIL_LOSS		Go
0x562	TC1_LINK_TRAINING_TIME		Go
0x600	RGMII_CTRL		Go
0x601	RGMII_FIFO_STATUS		Go
0x602	RGMII_CLK_SHIFT_CTRL		Go
0x608	SGMII_CTRL_1		Go
0x60A	SGMII_STATUS		Go
0x60C	SGMII_CTRL_2		Go
0x60D	SGMII_FIFO_STATUS		Go
0x618	PRBS_STATUS_1		Go
0x619	PRBS_CTRL_1		Go
0x61A	PRBS_CTRL_2		Go
0x61B	PRBS_CTRL_3		Go
0x61C	PRBS_STATUS_2		Go
0x61D	PRBS_STATUS_3		Go
0x61E	PRBS_STATUS_4		Go
0x620	PRBS_STATUS_5		Go
0x622	PRBS_STATUS_6		Go
0x623	PRBS_STATUS_7		Go
0x624	PRBS_CTRL_4		Go
0x625	PATTERN_CTRL_1		Go
0x626	PATTERN_CTRL_2		Go
0x627	PATTERN_CTRL_3		Go
0x628	PMATCH_CTRL_1		Go
0x629	PMATCH_CTRL_2		Go
0x62A	PMATCH_CTRL_3		Go
0x638	PKT_CRC_STAT		Go
0x639	TX_PKT_CNT_1		Go
0x63A	TX_PKT_CNT_2		Go
0x63B	TX_PKT_CNT_3		Go
0x63C	RX_PKT_CNT_1		Go
0x63D	RX_PKT_CNT_2		Go
0x63E	RX_PKT_CNT_3		Go
0x648	RMII_CTRL_1		Go
0x649	RMII_STATUS_1		Go
0x64A	RMII_OVERRIDE_CTRL		Go
0x1000	MMD1_PMA_CTRL_1		Go
0x1001	MMD1_PMA_STATUS_1		Go
0x1007	MMD1_PMA_STATUS_2		Go
0x100B	MMD1_PMA_EXT_ABILITY_1		Go
0x1012	MMD1_PMA_EXT_ABILITY_2		Go

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Table 7-12. DP83TC81X Registers (continued)

Address	Acronym	Register Name	Section
0x1834	MMD1_PMA_CTRL_2		Go
0x1836	MMD1_PMA_TEST_MODE_CTRL		Go
0x3000	MMD3_PCS_CTRL_1		Go
0x3001	MMD3_PCS_Status_1		Go

Complex bit access types are encoded to fit into small table cells. DP83TC81X Access Type Codes shows the codes that are used for access types in this section.

Table 7-13. DP83TC81X Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W0S	W 0S	Write 0 to set
W1S	W 1S	Write 1 to set
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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7.6.2.1 BMCR Register (Address = 0x0) [Reset = 0x2100]

BMCR is shown in BMCR Register Field Descriptions.

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Table 7-14. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MII_reset	RH/W1S	0b	MII Reset. Write 1 to put Digital in reset and all to reset MII regs (0x0 - 0xF) to default 0b = No reset 1b = Digital in reset and all MII regs (0x0 - 0xF) reset to default
14	xMII Loopback	R/W	0b	xMII Loopback: 1 = xMII Loopback enabled 0 = Normal Operation When xMII loopback mode is activated, the transmitted data presented on xMII TXD is looped back to xMII RXD internally. There is no LINK indication generated when xMII loopback is enabled. 1b = Enable Loopback from G/MII input to G/MII output
13	Manual_speed_MII	R	1b	Speed Selection: Always 100-Mbps Speed
12	Auto-Negotiation Enable	R	0b	Auto-Negotiation: Not supported 0b = Disable Auto-Negotiation
11	Power Down	R/W	0b	Power Down: 1 = IEEE Power Down 0 = Normal Operation The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is ORed with the input from the INT/PWDN_N pin. When the active low INT/PWDN_N is asserted, this bit is set. 1b = IEEE Power Down (see register 0x10)
10	Isolate	R/W	0b	Isolate: 1 = Isolates the port from the xMII with the exception of the serial management interface 0 = Normal Operation 1b = Isolate
9	RESERVED	R	0b	Reserved
8	Duplex Mode	R	1b	1 = Full Duplex 0 = Half duplex 0b = Half duplex 1b = Full Duplex
7	RESERVED	R/W	0b	Reserved
6-0	RESERVED	R	0b	Reserved

7.6.2.2 BMSR Register (Address = 0x1) [Reset = 0x0061]

BMSR is shown in BMSR Register Field Descriptions.

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Table 7-15. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4	R	0b	Always 0 - PHY not able to perform 100Base-T4
14	100Base-X Full Duplex	R	0b	1 = PHY able to perform full duplex 100Base-X 0 = PHY not able to perform full duplex 100Base-X 0b = PHY not able to perform full duplex 100Base-X 1b = PHY able to perform full duplex 100Base-X
13	100Base-X Half Duplex	R	0b	1 = PHY able to perform half duplex 100Base-X 0 = PHY not able to perform half duplex 100Base-X 0b = PHY not able to perform half duplex 100Base-X 1b = PHY able to perform half duplex 100Base-X
12	10 Mbps Full Duplex	R	0b	1 = PHY able to operate at 10Mbps in full duplex 0 = PHY not able to operate at 10Mbps in full duplex 0b = PHY not able to operate at 10Mbps in full duplex 1b = PHY able to operate at 10Mbps in full duplex
11	10 Mbps Half Duplex	R	0b	1 = PHY able to operate at 10Mbps in half duplex 0 = PHY not able to operate at 10Mbps in half duplex 0b = PHY not able to operate at 10Mbps in half duplex 1b = PHY able to operate at 10Mbps in half duplex
10-7	RESERVED	R	0b	Reserved
6	MF Preamble Suppression	R	1b	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed 0b = PHY will not accept management frames with preamble suppressed 1b = PHY will accept management frames with preamble suppressed
5	Auto-Negotiation Complete	R	1b	1 = Auto-Negotiation process completed 0 = Auto Negotiation process not completed (either still in process, disabled or reset) 0b = Auto Negotiation process not completed (either still in process, disabled or reset) 1b = Auto-Negotiation process completed
4	Remote fault	H	0b	1 = Remote fault condition detected 0 = No remote fault condition detected 0b = No remote fault condition detected 1b = Remote fault condition detected
3	Auto-Negotiation Ability	R	0b	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation 0b = PHY is not able to perform Auto-Negotiation 1b = PHY is able to perform Auto-Negotiation
2	Link status		0b	1 = Link is up 0 = Link is down 0b = Link is down 1b = Link is up
1	jabber detect	H	0b	1= jabber condition detected 0 = No jabber condition detected 0b = No jabber condition detected 1b = jabber condition detected
0	Extended Capability	R	1b	1 = Extended register capabilities 0 = Basic register set capabilities only 0b = Basic register set capabilities only 1b = Extended register capabilities

7.6.2.3 PHYIDR1 Register (Address = 0x2) [Reset = 0x2000]

PHYIDR1 is shown in PHYIDR1 Register Field Descriptions.

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Table 7-16. PHYIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally Unique Identifier Bits 21:6	R	1000000000 0000b	organizationally unique identification number

7.6.2.4 PHYIDR2 Register (Address = 0x3) [Reset = 0xA270]

PHYIDR2 is shown in PHYIDR2 Register Field Descriptions.

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Table 7-17. PHYIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Organizationally Unique Identifier Bits 5:0	R	101000b	organizationally unique identification number
9-4	Model Number	R	100111b	Vendor Model Number: The six bits of vendor model number are mapped from bits 9 to 4
3-0	RESERVED	R	0b	

7.6.2.5 REGCR Register (Address = 0xD) [Reset = 0x0000]

REGCR is shown in REGCR Register Field Descriptions.

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Table 7-18. REGCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Extended Register Command	R/W	0b	Extended Register Command: 00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13-5	RESERVED	R/W	0b	Reserved
4-0	DEVAD	R/W	0b	Device Address: Bits[4:0] are the device address, DEVAD, that directs any accesses of ADDAR Register 0x000E – Address/Data Register to the appropriate MMD. Specifically, the DP83TC811S-Q1 uses the vendor specific DEVAD [4:0] = "11111" for accesses to registers 0x04D1 and lower. For MMD1 access, the DEVAD[4:0] = '00001'. All accesses through registers REGCR and ADDAR must use the DEVAD for either MMD or MMD1. Transactions with other DEVAD are ignored.

7.6.2.6 ADDAR Register (Address = 0xE) [Reset = 0x0000]

ADDAR is shown in ADDAR Register Field Descriptions.

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Table 7-19. ADDAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Address/Data	R/W	0b	If REGCR register 15:14 = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

7.6.2.7 PHYSTS Register (Address = 0x10) [Reset = 0x0004]

PHYSTS is shown in PHYSTS Register Field Descriptions.

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Table 7-20. PHYSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved
14	RESERVED	R	0b	Reserved
13	receive_error_latch	H	0b	RxerrCnt>0 since last read.clear on read
12	RESERVED	H	0b	Reserved
11	RESERVED	H	0b	Reserved
10	signal_detect	R/W0S	0b	Channel ok latch low 0b = Channel ok had been reset 1b = Channel ok is set
9	descrambler_lock	R/W0S	0b	Descrambler lock latch low 0b = Descrmabler had been locked 1b = Descrambler is locked
8	RESERVED	R	0b	Reserved
7	mii_interrupt	H	0b	Interrupts pin status, cleared on reading 0x12 0b = Interrupts pin not set 1b = Interrupt pin had been set
6	RESERVED	R	0b	Reserved
5	jabber_dtct	R	0b	duplicate from reg.0x1.1
4	RESERVED	H	0b	Reserved
3	loopback_status	R	0b	MII loopback status 0b = No MII loopback 1b = MII loopback
2	duplex_status	R	1b	Duplex mode status 0b = Half duplex 1b = Full duplex
1	speed_10_status	R	0b	speed status
0	link_status	R	0b	duplication of reg.0x1.2 - link_status_bit

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7.6.2.8 PHYSCR Register (Address = 0x11) [Reset = 0x010B]

PHYSCR is shown in PHYSCR Register Field Descriptions.

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Table 7-21. PHYSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	dis_clk_125	R/W	0b	0b = Enable CLK125 (Sourced by the CLK125 port) 1b = Disable CLK125 (Sourced by the CLK125 port)
14	pwr_save_mode_en	R/W	0b	Enable power save mode config from reg 0b = Normal mode 1b = Power save mode
13-12	pwr_save_mode	R/W	0b	power save mode status 0b = Normal mode 1b = IEEE mode: power down all digital and analog blocks, if bit [4] set to zero, PLL is also powered down 10b = Reserved 11b = Reserved
11	sgmii_soft_reset	R/WSC	0b	Reset SGMII
10	use_PHYAD0_as_Isolate	R/W	0b	enables using PHYAD = 0 as isolate 0b = do not Isolate for PHYAD == 0. 1b = when phy_addr == 0, isolate MAC Interface
9-8	tx_fifo_depth	R/W	1b	RMII TX fifo depth 0b = 4 nibbles 1b = 5 nibbles 1010b = 6 nibbles 1011b = 8 nibbles
7	RESERVED	R/W	0b	Reserved
6-4	RESERVED	R	0b	Reserved
3	int_pol	R/W	1b	Interrupt Polarity 0b = Active High output. Interrupt pin will be driven high when interrupt occurs. 1b = Active Low output. Interrupt will be driven low when interrupt occurs.
2	force_interrupt	R/W	0b	Force interrupt pin 0b = Do not force interrupt pin 1b = Force interrupt pin
1	INTEN	R/W	1b	Enable interrupts 0b = Disable interrupts 1b = Enable interrupts
0	INT_OE	R/W	1b	Interrupt/Power down pin configuration 0b = PIN is a power down PIN (input) 1b = PIN is an interrupt pin (output)

7.6.2.9 MISR1 Register (Address = 0x12) [Reset = 0x0000]

MISR1 is shown in MISR1 Register Field Descriptions.

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Table 7-22. MISR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	link_qual_int	R	0b	Link quality(Not good) interrupt 0b = Link qual is Good 1b = Link qual is Not Good when link is ON.
14	energy_det_int	R	0b	This INT can be asserted upon Rising edge only of energy_det signal using reg0x101 bit [0] : cfg_energy_det_int_le_only. status output of energy_det_hist signal on reg0x19 bit[10]. 0b = No Change of energy detected 1b = Change of energy_detected (both rising and falling edges)
13	link_int	R	0b	Link status change interrupt 0b = No change of link status interrupt pending. 1b = Change of link status interrupt is pending and is cleared by the current read.
12	wol_int	R	0b	Interrupt bit indicating that WOL packet is received 0b = No WoL interrupt pending. 1b = WoL packet received interrupt is pending and is cleared by the current read.
11	esd_int	R	0b	1 = ESD detected interrupt is pending and is cleared by the current read. 0 = No ESD interrupt pending.
10	ms_train_done_int	R	0b	1 = M/S Link Training Completed interrupt is pending and is cleared by the current read. 0 = No M/S Link Training Completed interrupt pending.
9	fhf_int	R	0b	1 = False carrier counter half-full interrupt is pending and is cleared by the current read. 0 = No false carrier counter half-full interrupt pending.
8	rhf_int	R	0b	1 = Receive error counter half-full interrupt is pending and is cleared by the current read. 0 = No receive error carrier counter half-full interrupt pending.
7	link_qual_int_en	R/W	0b	Enable Interrupt on Link Quality status.
6	energy_det_int_en	R/W	0b	Enable Interrupt on change of Energy Detect histr. Status
5	link_int_en	R/W	0b	Enable Interrupt on change of link status
4	wol_int_en	R/W	0b	Enable Interrupt on WoL detection
3	esd_int_en	R/W	0b	Enable Interrupt on ESD detect event
2	ms_train_done_int_en	R/W	0b	Enable Interrupt on M/S Link Training Completed event
1	fhf_int_en	R/W	0b	Enable Interrupt on False Carrier Counter Register half-full event
0	rhf_int_en	R/W	0b	Enable Interrupt on Receive Error Counter Register half-full event

7.6.2.10 MISR2 Register (Address = 0x13) [Reset = 0x0000]

MISR2 is shown in MISR2 Register Field Descriptions.

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Table 7-23. MISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	under_volt_int	H	0b	1 = Under Voltage has been detected 0 =Under Voltage has not been detected 0b = Under Voltage has not been detected 1b = Under Voltage has been detected
14	over_volt_int	H	0b	1 = Over Voltage has been detected 0 = Over Voltage has not been detected 0b = Over Voltage has not been detected 1b = Over Voltage has been detected
13	RESERVED	H	0b	Reserved
12	RESERVED	H	0b	Reserved
11	over_temp_int	H	0b	1 = Over Temperature has been detected 0 = Over Temperature has not been detected 0b = Over Temperature has not been detected 1b = Over Temperature has been detected
10	sleep_int	H	0b	1 = Sleep mode has changed 0 = Sleep mode has not changed 0b = Sleep mode has not changed 1b = Sleep mode has changed
9	pol_int	H	0b	1 = Data polarity has changed 0 = Data polarity has not changed 0b = Data polarity has not changed 1b = Data polarity has changed
8	jabber_int	H	0b	1 = Jabber detected 0 = Jabber not detected 0b = Jabber not detected 1b = Jabber detected
7	under_volt_int_en	R/W	0b	0 = Disable interrupt 0b = Disable interrupt
6	over_volt_int_en	R/W	0b	0 = Disable interrupt 0b = Disable interrupt
5	page_rcvd_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
4	Fifo_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
3	over_temp_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
2	sleep_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
1	pol_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt
0	jabber_int_en	R/W	0b	1 = Enable interrupt 1b = Enable interrupt

7.6.2.11 RECR Register (Address = 0x15) [Reset = 0x0000]

RECR is shown in RECR Register Field Descriptions.

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Table 7-24. RECR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_err_cnt		0b	RX_ER Counter: When a valid carrier is presented (only while RX_DV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in xMII loopback mode. The counter stops when it reaches its maximum count (0xFFFF). When the counter exceeds half-full (0x7FFF), an interrupt is generated. This register is cleared on read.

7.6.2.12 BISCR Register (Address = 0x16) [Reset = 0x0100]

BISCR is shown in BISCR Register Field Descriptions.

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Table 7-25. BISCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0b	Reserved
10	prbs_sync_loss	H	0b	Prbs lock lost latch status 0b = Prbs lock never lost 1b = Prbs lock had been lost
9	RESERVED	R	0b	Reserved
8	core_pwr_mode	R	1b	1b0 = Core is in power down or sleep mode 1b1 = Core is is normal power mode 0b = Core is in power down or sleep mode 1b = Core is is normal power mode
7	RESERVED	R	0b	Reserved
6-0	loopback_mode	R/W	0b	Bit[0]: Unused Bit[1]: PCS loopback after PAM3 Bits[5:2] (Bits [1:0] must be off): 0001: Digital loop 0010: Analog loop 0100: Reverse loop 1000: Ext Reverse loop Bit[6] (may be set only in MII loop) 1 = Transmit data to MDI in MII loop 0 = Suppress data to MDI in MII loop

7.6.2.13 MISR3 Register (Address = 0x18) [Reset = 0x0025]

MISR3 is shown in MISR3 Register Field Descriptions.

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Table 7-26. MISR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	sleep_fail_int	H	0b	0b = Sleep negotiation not failed yet 1b = Sleep negotiation failed
12	POR_done_int	H	0b	0b = POR not completed yet 1b = POR completed (required for re-initialization of registers when we come out of sleep)
11	no_frame_int	H	0b	0b = Frame was detected 1b = No Frame detected for transmission or reception in given time
10	wake_req_int	H	0b	0b = Wake-up request not received 1b = Wake-up request command was received from remote PHY
9	WUP_int	H	0b	0b = WUP not received 1b = WUP received from remote PHY
8	LPS_int	H	0b	0b = LPS symbols not detected 1b = LPS symbols detetced
7-6	RESERVED	R	0b	Reserved
5	sleep_fail_int_en	R/W	1b	0b = Disable interrupt 1b = Enable interrupt
4	POR_done_int_en	R/W	0b	0b = Disable interrupt 1b = Enable interrupt
3	no_frame_int_en	R/W	0b	0b = Disable interrupt 1b = Enable interrupt
2	wake_req_int_en	R/W	1b	0b = Disable interrupt 1b = Enable interrupt
1	WUP_int_en	R/W	0b	0b = Disable interrupt 1b = Enable interrupt
0	LPS_int_en	R/W	1b	0b = Disable interrupt 1b = Enable interrupt

7.6.2.14 REG_19 Register (Address = 0x19) [Reset = 0x0800]

REG_19 is shown in REG_19 Register Field Descriptions.

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Table 7-27. REG_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	RESERVED	R	0b	Reserved
12	RESERVED	R	0b	Reserved
11	RESERVED	R	1b	Reserved
10	dsp_energy_detect	R	0b	DSP energy detected status
9-5	RESERVED	R	0b	Reserved
4-0	PHY_ADDR	R	0b	PHY address decode from straps

7.6.2.15 CDCR Register (Address = 0x1E) [Reset = 0x0000]

CDCR is shown in CDCR Register Field Descriptions.

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Table 7-28. CDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	tdr_start	RH/W1S	0b	clr by tdr done Start TDR manually 0b = No TDR 1b = TDR start
14	cfg_tdr_auto_run	R/W	0b	Enable TDR auto run on link down 0b = TDR start manually 1b = TDR start automatically on link down
13-2	RESERVED	R	0b	Reserved
1	tdr_done	R	0b	TDR done status 0b = TDR still not done 1b = TDR done
0	tdr_fail	R	0b	TDR fail status

7.6.2.16 PHYRCR Register (Address = 0x1F) [Reset = 0x0000]

PHYRCR is shown in PHYRCR Register Field Descriptions.

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Table 7-29. PHYRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Software Global Reset	RH/W1S	0b	Hardware Reset(Reset digital + register file) 0b = Normal Operation 1b = Reset PHY. This bit is self cleared and has the same effect as the RESET pin.
14	Digital reset	RH/W1S	0b	Software Restart 0b = Normal Operation 1b = Restart PHY. This bit is self cleared and resets all PHY circuitry except registers.
13	RESERVED	R/W	0b	Reserved
12-8	RESERVED	R/W	0b	Reserved
7	Standby_mode	R/W	0b	Standby Mode 0b = Normal operation 1b = Standby mode enabled
6	RESERVED	R/W	0b	Reserved
5	RESERVED	R	0b	Reserved
4-0	RESERVED	R/W	0b	Reserved

7.6.2.17 LPS_CFG2 Register (Address = 0x18B) [Reset = 0x0443]

LPS_CFG2 is shown in LPS_CFG2 Register Field Descriptions.

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Table 7-30. LPS_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0b	Reserved
10	cfg_sleep_fail_fix_tc10_sm	R/W	1b	comes out of sleep_request state when no activity is detected if sleep is inititated by LP
9	cfg_sleep_fail_fix_pcs	R/W	0b	bypasses loc_rcvr_status till tx_lps_done and sleep initiated by LP
8	cfg_tc10_dis_bond_pad_bypass	R/W	0b	Provides control to disable TC10 in a TC10 enabled device. If TC10 feature is enabled by bondpad 0b = Enables TC10 1b = Disables TC10
7	cfg_sleep_abort	R/W	0b	LPS abort command
6	cfg_auto_mode_en	R/W	1b	LPS autonomous mode enable if(RX_D3_strap ==1) reset_val = ~CLKOUT_strap else reset_val = ~LED_1_strap 0b = AUTO mode disabled 1b = AUTO mode enable
5	cfg_lps_mon_en	R/W	0b	controls transition from normal to standby transition based on monitors output 0b = Disable normal to standby transition on over temp/under volt 1b = Enable normal to standby transition on over temp/under volt
4-2	RESERVED	R	0b	Reserved
1	cfg_lps_sleep_en	R/W	1b	Controls state change after TC10 sleep negotiation 0b = Enter standby after negotiated LPS 1b = Enter sleep after negotiated LPS
0	cfg_lps_sm_en	R/W	1b	Enable TC10 mode of power management. Refers to en_sleep_cap variable in TC10 standard.

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7.6.2.18 LPS_CFG3 Register (Address = 0x18C) [Reset = 0x0000]

LPS_CFG3 is shown in LPS_CFG3 Register Field Descriptions.

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Table 7-31. LPS_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-0	cfg_lps_pwr_mode	RH/W1S	0b	bit 0 : normal command bit4 : standby command bit 0 : normal command bit 1 : sleep requrest bit4 : standby command bit 7 : wur command

7.6.2.19 LPS_STATUS Register (Address = 0x18E) [Reset = 0x0000]

LPS_STATUS is shown in LPS_STATUS Register Field Descriptions.

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Table 7-32. LPS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0b	Reserved
6-0	status_lps_st	R	0b	LPS SM state 0b = SLEEP 10b = STANDBY 100b = NORMAL 1000b = SLEEP_ACK 10000b = SLEEP_REQ 100000b = SLEEP_FAIL 1000000b = SLEEP_SILENT

7.6.2.20 SQI Register (Address = 0x198) [Reset = 0x0000]

SQI is shown in SQI Register Field Descriptions.

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Table 7-33. SQI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-0	sqi	R	0b	3-bit SQI as per TC1

7.6.2.21 TDR_TX_CFG Register (Address = 0x300) [Reset = 0x2710]

TDR_TX_CFG is shown in TDR_TX_CFG Register Field Descriptions.

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Table 7-34. TDR_TX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_tdr_tx_duration	R/W	1001110001 0000b	TDR transmit duration in usec

7.6.2.22 TAP_PROCESS_CFG Register (Address = 0x301) [Reset = 0x1703]

TAP_PROCESS_CFG is shown in TAP_PROCESS_CFG Register Field Descriptions.

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Table 7-35. TAP_PROCESS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12-8	cfg_end_tap_index	R/W	10111b	End tap index for echo coeff sweep
7-5	RESERVED	R	0b	Reserved
4-0	cfg_start_tap_index	R/W	11b	Start tap index for echo coeff sweep

7.6.2.23 TDR_CFG1 Register (Address = 0x302) [Reset = 0x0045]

TDR_CFG1 is shown in TDR_CFG1 Register Field Descriptions.

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Table 7-36. TDR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-4	cfg_forward_shadow	R/W	100b	Forward shadow
3-2	cfg_post_silence_time	R/W	1b	Post-Silence time
1-0	cfg_pre_silence_time	R/W	1b	Pre-Silence time

7.6.2.24 TDR_CFG2 Register (Address = 0x303) [Reset = 0x0419]

TDR_CFG2 is shown in TDR_CFG2 Register Field Descriptions.

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Table 7-37. TDR_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12-8	cfg_tdr_filt_loc_offset	R/W	100b	tap index offset of dyamic peak equation
7-0	cfg_tdr_filt_init	R/W	11001b	Offset of dynamic peak equation

7.6.2.25 TDR_CFG3 Register (Address = 0x304) [Reset = 0x0030]

TDR_CFG3 is shown in TDR_CFG3 Register Field Descriptions.

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Table 7-38. TDR_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-0	cfg_tdr_filt_slope	R/W	110000b	Slope of dynamic peak equation (0.4)

7.6.2.26 TDR_CFG4 Register (Address = 0x305) [Reset = 0x0004]

TDR_CFG4 is shown in TDR_CFG4 Register Field Descriptions.

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Table 7-39. TDR_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9	mas_mode_tdr	R/W	0b	Master slave config during TDR
8-7	pi_pud_ctrl_tdr	R/W	0b	PUD control during TDR
6	pi_pud_clk_tdr	R/W	0b	PUD clock during TDR
5-4	hpf_gain_tdr	R/W	0b	HPF gain during TDR
3-0	pga_gain_tdr	R/W	100b	PGA gain during TDR

7.6.2.27 TDR_CFG5 Register (Address = 0x306) [Reset = 0x000A]

TDR_CFG5 is shown in TDR_CFG5 Register Field Descriptions.

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Table 7-40. TDR_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0b	Reserved
4	cfg_half_open_det_en	R/W	0b	enables detection of half cable 0b = Disabled half open detection 1b = Enbales half open detection
3-0	cfg_cable_delay_num	R/W	1010b	To be configured according to the prop delay of the cable used Valid values : 4d0 to 4d11 - [4.5:0.1:5.6]ns Default : 4d10 (5.5 ns)

7.6.2.28 TDR_STATUS0 Register (Address = 0x309) [Reset = 0x0000]

TDR_STATUS0 is shown in TDR_STATUS0 Register Field Descriptions.

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Table 7-41. TDR_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12-8	peak1_loc	R	0b	Peak 1 location in tap index
7-5	RESERVED	R	0b	Reserved
4-0	peak0_loc	R	0b	Peak 0 location in tap index

7.6.2.29 TDR_STATUS1 Register (Address = 0x30A) [Reset = 0x0000]

TDR_STATUS1 is shown in TDR_STATUS1 Register Field Descriptions.

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Table 7-42. TDR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12-8	peak3_loc	R	0b	Peak 3 location in tap index
7-5	RESERVED	R	0b	Reserved
4-0	peak2_loc	R	0b	Peak 2 location in tap index

7.6.2.30 TDR_STATUS2 Register (Address = 0x30B) [Reset = 0x0000]

TDR_STATUS2 is shown in TDR_STATUS2 Register Field Descriptions.

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Table 7-43. TDR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak0_amp	R	0b	Peak 0 amplitude in echo coeff
7-5	RESERVED	R	0b	Reserved
4-0	peak4_loc	R	0b	Peak 4 location in tap index

7.6.2.31 TDR_STATUS3 Register (Address = 0x30C) [Reset = 0x0000]

TDR_STATUS3 is shown in TDR_STATUS3 Register Field Descriptions.

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Table 7-44. TDR_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak2_amp	R	0b	Peak 2 amplitude in echo coeff
7-0	peak1_amp	R	0b	Peak 1 plitude in echo coeff

7.6.2.32 TDR_STATUS4 Register (Address = 0x30D) [Reset = 0x0000]

TDR_STATUS4 is shown in TDR_STATUS4 Register Field Descriptions.

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Table 7-45. TDR_STATUS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak4_amp	R	0b	Peak 4 amplitude in echo coeff
7-0	peak3_amp	R	0b	Peak 3 amplitude in echo coeff

7.6.2.33 TDR_STATUS5 Register (Address = 0x30E) [Reset = 0x0000]

TDR_STATUS5 is shown in TDR_STATUS5 Register Field Descriptions.

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Table 7-46. TDR_STATUS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0b	Reserved
4	peak_4_sign	R	0b	Peak 4 sign
3	peak_3_sign	R	0b	Peak 3 sign
2	peak_2_sign	R	0b	Peak 2 sign
1	peak_1_sign	R	0b	Peak 1 sign
0	peak_0_sign	R	0b	Peak 0 sign

7.6.2.34 TDR_TC1 Register (Address = 0x310) [Reset = 0x0000]

TDR_TC1 is shown in TDR_TC1 Register Field Descriptions.

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Table 7-47. TDR_TC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0b	Reserved
8	half_open_detect	R	0b	Half wire open detect value 0b = Half wire open not detected 1b = Half wire open detected
7	peak_detect	R	0b	Set if fault is detected in cable 0b = Fault not detected in cable 1b = Fault detected in cable
6	peak_sign	R	0b	Valid only is peak_detect is set 0b = Open 1b = Short
5-0	peak_loc_in_meters	R	0b	Fault location in meters (Valid only is peak_detect is set)

7.6.2.35 LEDS_CFG_1 Register (Address = 0x450) [Reset = 0x2600]

LEDS_CFG_1 is shown in LEDS_CFG_1 Register Field Descriptions.

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Table 7-48. LEDS_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved
14	leds_bypass_stretching	R/W	0b	Bypass leds stretching option 0b = Noraml Operation 1b = Bypass LEDs stretching
13-12	leds_blink_rate	R/W	10b	Controls blink rate of LEDs 0b = 20Hz (50mSec) 1b = 10Hz (100mSec) 10b = 5Hz (200mSec) 11b = 2Hz (500mSec)
11-8	led_2_option	R/W	110b	Controls LED_2 sources (same as bits 3:0)
7-4	led_1_option	R/W	0b	Controls LED_1 sources
3-0	led_0_option	R/W	0b	Controls LED_0 source: 0b = link OK 1b = link OK + blink on TX/RX activity 10b = link OK + blink on TX activity 11b = link OK + blink on RX activity 100b = link OK + 100Base-T1 Master 101b = link OK + 100Base-T1 Slave 110b = TX/RX activity with stretch option 111b = Reserved 1000b = Reserved 1001b = Link lost (remains on until register 0x1 is read) 1010b = PRBS error (toggles on error) 1011b = XMII TX/RX Error with stretch option

7.6.2.36 LEDS_CFG_2 Register (Address = 0x451) [Reset = 0x0041]

LEDS_CFG_2 is shown in LEDS_CFG_2 Register Field Descriptions.

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Table 7-49. LEDS_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0b	Reserved
8	led_2_drv_en	R/W	0b	0b = LED_2 is in normal operation mode 1b = Drive the value of LED_2 (driven value is bit 9)
7	led_2_drv_val	R/W	0b	If bit #8 is set, this bit will set the value of LED_2 0b = Drive low on LED 1b = Drive High on LED
6	led_2_polarity	R/W	1b	LED_2 polarity 0b = Active low 1b = Active high
5	led_1_drv_en	R/W	0b	0b = LED_1 is in normal operation mode 1b = Drive the value of LED_1 (driven value is bit #5)
4	led_1_drv_val	R/W	0b	If bit #5 is set, this is the value of LED_1 0b = Drive low on LED 1b = Drive High on LED
3	led_1_polarity	R/W	0b	LED_1 polarity: if(RX_D3_strap == 1) reset_val = ~CLKOUT_strap else reset_val = ~LED_1_strap LED_1 polarity 0b = Active low 1b = Active high
2	led_0_drv_en	R/W	0b	0b = LED_0 is in normal operation mode 1b = Drive the value of LED_0 (driven value is bit #1)
1	led_0_drv_val	R/W	0b	If bit #2 is set, this is the value of LED_1 0b = Drive low on LED 1b = Drive High on LED
0	led_0_polarity	R/W	1b	LED_0 polarity: reset_val = ~LED_0_strap 0b = Active low 1b = Active high

7.6.2.37 IO_MUX_CFG_1 Register (Address = 0x452) [Reset = 0x0100]

IO_MUX_CFG_1 is shown in IO_MUX_CFG_1 Register Field Descriptions.

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Table 7-50. IO_MUX_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	led_1_clk_div_2_en	R/W	0b	If led_1_gpio is configured to led_1_clk_source, Selects divide by 2 of clock at led_1_clk_source
14-12	led_1_clk_source	R/W	0b	In case clk_out is MUXed to LED_1 IO, this field controls clk_out source:_x000D_ 0 - XI clock_x000D_ 1 - 200M pll clock_x000D_ 2 - 67 MHz ADC clock (recovered)_x000D_ 3 - Free 200MHz clock_x000D_ 4 - 25M MII clock derived from 200M LD clock_x000D_ 5 - 25MHz clock to PLL (XI or XI/2) or POR clock_x000D_ 6 - Core 100 MHz clock_x000D_ 7 - 67 MHz DSP clock (recovered, 1/3 duty cycle)
11	led_1_clk_inv_en	R/W	0b	If led_1_gpio is configured to led_1_clk_source, Selects inversion of clock at led_1_clk_source
10-8	led_1_gpio_ctrl	R/W	1b	controls the output of LED_1 IO:_x000D_ 0 - LED_1 (default: LINK + ACT)_x000D_ 1 - LED_1 Clock mux out_x000D_ 2 - WoL_x000D_ 3 - Under-Voltage indication_x000D_ 4 - 1588 TX_x000D_ 5 - 1588 RX_x000D_ 6 - ESD_x000D_ 7 - interrupt if(RX_D3_strap ==1) reset_val = 3b001 else reset_val = 3b000 controls the output of LED_1 IO:_x000D_ 0 - LED_1 (default: LINK + ACT)_x000D_ 1 - LED_1 Clock mux out_x000D_ 2 - WoL_x000D_ 3 - Under-Voltage indication_x000D_ 4 - 1588 TX_x000D_ 5 - 1588 RX_x000D_ 6 - ESD_x000D_ 7 - interrupt reset_val = 3b001
7	led_0_clk_div_2_en	R/W	0b	If led_0_gpio is configured to led_0_clk_source, Selects divide by 2 of clock at led_0_clk_source
6-4	led_0_clk_source	R/W	0b	In case clk_out is MUXed to LED_0 IO, this field controls clk_out source:_x000D_ 0 - XI clock_x000D_ 1 - 200M pll clock_x000D_ 2 - 67 MHz ADC clock (recovered)_x000D_ 3 - Free 200MHz clock_x000D_ 4 - 25M MII clock derived from 200M LD clock_x000D_ 5 - 25MHz clock to PLL (XI or XI/2) or POR clock_x000D_ 6 - Core 100 MHz clock_x000D_ 7 - 67 MHz DSP clock (recovered, 1/3 duty cycle)
3	led_0_clk_inv_en	R/W	0b	If led_0_gpio is configured to led_0_clk_source, Selects inversion of clock at led_0_clk_source
2-0	led_0_gpio_ctrl	R/W	0b	controls the output of LED_0 IO 0b = LED_0 (default: LINK) 001b =LED_0 Clock mux out 010b = WoL 011b = Under-Voltage indication 100b = 1588 TX 101b = 1588 RX 110b = ESD 111b = interrupt

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7.6.2.38 IO_MUX_CFG_2 Register (Address = 0x453) [Reset = 0x0001]

IO_MUX_CFG_2 is shown in IO_MUX_CFG_2 Register Field Descriptions.

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Table 7-51. IO_MUX_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_tx_er_on_led1	R/W	0b	configures led_1 pin to tx_er pin and LED_1 pin is made input
14-9	RESERVED	R	0b	Reserved
8	clk_o_clk_div_2_en	R/W	0b	If clk_out is configured to output clk_o_clk_source, Selects divide by 2 of clock at clk_o_clk_source
7-4	clk_o_clk_source	R/W	0b	In case clk_out is MUXed to CLK_O IO, this field controls clk_out source:_x000D_ 0 - XI clock_x000D_ 1 - 200M pll clock_x000D_ 2 - 67 MHz ADC clock (recovered)_x000D_ 3 - Free 200MHz clock_x000D_ 4 - 25M MII clock derived from 200M LD clock_x000D_ 5 - 25MHz clock to PLL (XI or XI/2) or POR clock_x000D_ 6 - Core 100 MHz clock_x000D_ 7 - 67 MHz DSP clock (recovered, 1/3 duty cycle)_x000D_ 8 - CLK25_50 (50 MHz in RMII, 25 MHz in others)_x000D_ 9 - 50M RMII RX clk_x000D_ 10 - SGMII serlz clk_x000D_ 11- SGMII deserlz clk_x000D_ 12 - 30ns tick_x000D_ 13 - 40ns tick_x000D_ 14 - DLL TX CLK_x000D_ 15 - DLL RX CLK
3	clk_o_clk_inv_en	R/W	0b	If clk_out is configured to output clk_o_clk_source, Selects inversion of clock at clk_o_clk_source
2-0	clk_o_gpio_ctrl	R/W	1b	controls the output of CLK_O IO:_x000D_ 0 - LED_1 _x000D_ 1 - CLKOUT Clock mux out_x000D_ 2 - WoL_x000D_ 3 - Under-Voltage indication_x000D_ 4 - 1588 TX_x000D_ 5 - 1588 RX_x000D_ 6 - ESD_x000D_ 7 - interrupt Automatically gets configured to 3 'h0 if pin6(LED_1) is strapped As daisy chain CLKOUT if(RX_D3_strap ==1) reset_val = 3b000 else reset_val = 3b001

7.6.2.39 CHIP_SOR_1 Register (Address = 0x45D) [Reset = 0x0000]

CHIP_SOR_1 is shown in CHIP_SOR_1 Register Field Descriptions.

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Table 7-52. CHIP_SOR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved
14	CLKOUT_POR	R	0b	Strap sampled at CLKOUT pin during power up
13	LED1_POR	R	0b	Strap sampled at LED1 pin during power up
12	RXD3_POR	R	0b	Strap sampled at RX_D3 pin during power up
11	RESERVED	R	0b	Reserved
10	RESERVED	R	0b	Reserved
9	LED0_STRAP	R	0b	LED0 strap status
8	RXD3_STRAP	R	0b	RX_D3 strap status
7	RXD2_STRAP	R	0b	RX_D2 strap status
6	RXD1_STRAP	R	0b	RX_D1 strap status
5	RXD0_STRAP	R	0b	RX_D0 strap status
4	RXCLK_STRAP	R	0b	RX_CLK strap status
3-2	RXER_STRAP	R	0b	RX_ER strap status
1-0	RXDV_STRAP	R	0b	RX_DV strap status

7.6.2.40 CHIP_SOR_2 Register (Address = 0x45E) [Reset = 0x0000]

CHIP_SOR_2 is shown in CHIP_SOR_2 Register Field Descriptions.

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Table 7-53. CHIP_SOR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0b	Reserved
3-0	sor_vector_2	R	0b	SOR vector, bits [19:16] : SOR[17:16] - b00 SOR[19:18] - reserved

7.6.2.41 LED1_CLKOUT_ANA_CTRL Register (Address = 0x45F) [Reset = 0x000C]

LED1_CLKOUT_ANA_CTRL is shown in LED1_CLKOUT_ANA_CTRL Register Field Descriptions.

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Table 7-54. LED1_CLKOUT_ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved
14	RESERVED	R/W	0b	Reserved
13-5	RESERVED	R	0b	Reserved
4	RESERVED	R/W	0b	Reserved
3-2	led_1_ana_mux_ctrl	R/W	11b	Selects the signal to be sent out on LED_1 pin Automatically selects output from digital if Pin6(LED_1) is strapped As daisy chain CLKOUT if(RX_D3_strap == 1) reset_val = 2b00 else reset_val = 2b11 0b = Daisy chain clock 1b = TX_TCLK for test modes 10b = ANA Test clock 11b = clkout_out_1p0v_sl from digital
1-0	clkout_ana_mux_ctrl	R/W	0b	Selects the signal to be sent out on CLKOUT pin Automatically selects output from digital if Pin6(LED_1) is strapped As daisy chain CLKOUT if(RX_D3_strap == 1) reset_val = 2b11 else reset_val = 2b00 0b = Daisy chain clock 1b = TX_TCLK for test modes 10b = ANA Test clock 11b = clkout_out_1p0v_sl from digital

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7.6.2.42 REV_ID Register (Address = 0x466) [Reset = 0x0000]

REV_ID is shown in REV_ID Register Field Descriptions.

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Table 7-55. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0b	Reserved
3-0	si_rev_id	R	0b	internal revision ID

7.6.2.43 TEST_MODE_CTRL Register (Address = 0x497) [Reset = 0x01C0]

TEST_MODE_CTRL is shown in TEST_MODE_CTRL Register Field Descriptions.

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Table 7-56. TEST_MODE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0b	Reserved
9-4	cfg_test_mode1_symbol_cnt	R/W	11100b	number of +1/-1 symbols to send in test_mode_1 N= 2 + 2* CFG_TEST_MODE1_SYMBOL_CNT
3-0	RESERVED	R	0b	Reserved

7.6.2.44 TC1_CFG_RW Register (Address = 0x560) [Reset = 0x07E4]

TC1_CFG_RW is shown in TC1_CFG_RW Register Field Descriptions.

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Table 7-57. TC1_CFG_RW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	cfg_bad_sqi_count_twice	R/W	0b	
12-11	cfg_link_status_metric	R/W	0b	selects following link up signals 0b = link_up_c_and_s 1b = link_montor_status 10b = (phy_control = SEND_DATA) 11b = comm_ready from TC1 spec
10-5	cfg_link_failure_multihot	R/W	111111b	each bit enables logging of lini failure in te given scenario: 0 - SQI greater than configured thershold in register cfg_bad_sqi_thrs 5 - BAD_SSD 4 - BAD_END 3 - RX_ERROR 2 - LINK_FAILED 1 - RCV_JABBER_DET
4-3	cfg_comm_timer_thrs	R/W	0b	selects the hysteresis timer value for TC1 comm ready 0b = 2ms 1b = 500us 10b = 1ms 11b = 4ms
2-0	cfg_bad_sqi_thrs	R/W	100b	

7.6.2.45 TC1_LINK_FAIL_LOSS Register (Address = 0x561) [Reset = 0x0000]

TC1_LINK_FAIL_LOSS is shown in TC1_LINK_FAIL_LOSS Register Field Descriptions.

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Table 7-58. TC1_LINK_FAIL_LOSS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	link_failure_losses	R	0b	9:0 - link failures 15-10 - link losses

7.6.2.46 TC1_LINK_TRAINING_TIME Register (Address = 0x562) [Reset = 0x0000]

TC1_LINK_TRAINING_TIME is shown in TC1_LINK_TRAINING_TIME Register Field Descriptions.

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Table 7-59. TC1_LINK_TRAINING_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
15	comm_ready	R	0b	TC1 comm ready signal
14-8	RESERVED	R	0b	Reserved
7-0	lq_ltt	R	0b	logs the link training time as per TC1 standard

7.6.2.47 RGMII_CTRL Register (Address = 0x600) [Reset = 0x0030]

RGMII_CTRL is shown in RGMII_CTRL Register Field Descriptions.

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Table 7-60. RGMII_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0b	Reserved
6-4	rgmii_tx_half_full_th	R/W	11b	RGMII TX sync FIFO half full threshold
3	cfg_rgmii_en	R/W	0b	RGMII enable bit Default from strap if(RX_D2_strap == 1) reset_val = 1 else reset_val = 0 0b = RGMII disable 1b = RGMII enable
2	inv_rgmii_txd	R/W	0b	Invert RGMII Tx wire order - full swap [3:0] to [0:3]
1	inv_rgmii_rxd	R/W	0b	Invert RGMII Rx wire order - full swap [3:0] to [0:3]
0	sup_tx_err_fd_rgmii	R/W	0b	this bit can disable the TX_ERR indication input

7.6.2.48 RGMII_FIFO_STATUS Register (Address = 0x601) [Reset = 0x0000]

RGMII_FIFO_STATUS is shown in RGMII_FIFO_STATUS Register Field Descriptions.

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Table 7-61. RGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1	rgmii_tx_af_full_err	R	0b	RGMII Tx fifo full error
0	rgmii_tx_af_empty_err	R	0b	RGMII Tx fifo empty error

7.6.2.49 RGMII_CLK_SHIFT_CTRL Register (Address = 0x602) [Reset = 0x0000]

RGMII_CLK_SHIFT_CTRL is shown in RGMII_CLK_SHIFT_CTRL Register Field Descriptions.

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Table 7-62. RGMII_CLK_SHIFT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1	cfg_rgmii_rx_clk_shift_sel	R/W	0b	0: clock and data are aligned 1: clock on PIN is delayed by 90 degrees relative to RGMII_RX data if({RX_D2_strap, RX_D1_strap} == 2b11) reset_val = 1 else resett_val = 0 0b = clock and data are aligned 1b = clock on PIN is delayed by 90 degrees relative to RGMII_RX data
0	cfg_rgmii_tx_clk_shift_sel	R/W	0b	use this mode when RGMII_TX_CLK (and) RGMII_TXD are aligned if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3b101) reset_val = 1 else if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3b110) reset_val = 1 else reset_val = 0

7.6.2.50 SGMII_CTRL_1 Register (Address = 0x608) [Reset = 0x007B]

SGMII_CTRL_1 is shown in SGMII_CTRL_1 Register Field Descriptions.

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Table 7-63. SGMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	sgmii_tx_err_dis	R/W	0b	SGMII TX err disable bit
14	cfg_align_idx_force_en	R/W	0b	Force word boundray index selection
13-10	cfg_align_idx_value	R/W	0b	when cfg_align_idx_force is set,This value set the iword boundray index
9	cfg_sgmii_en	R/W	0b	SGMII enable bit Default from strap if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3b000) reset_val = 1 else reset_val = 0 0b = SGMII MAC i/f disabled 1b = SGMII MAC i/f enabled
8	cfg_sgmii_rx_pol_invert	R/W	0b	SGMII RX bus invert polarity
7	cfg_sgmii_tx_pol_invert	R/W	0b	SGMII TX bus invert polarity
6-5	serdes_tx_bits_order	R/W	11b	SERDES TX bits order (input to digital core)
4	serdes_rx_bits_order	R/W	1b	SERDES RX bits order (output of digital core) 0b = MSB-first (default) 1b = LSB-first (reversed order)
3	cfg_sgmii_align_pkt_en	R/W	1b	For aligning the start of read out TX packet (towards serializer) w/ tx_even pulse. To sync with the Code_Group/OSET FSM code slots. Default is 1, when using 0 we go back to Gemini code
2-1	sgmii_autoneg_timer	R/W	1b	Selects duration of SGMII Auto-Negotiation timer
0	sgmii_autoneg_en	R/W	1b	sgmii auto negotiation enable 0b = SGMII autoneg disabled 1b = SGMII autoneg enabled

7.6.2.51 SGMII_STATUS Register (Address = 0x60A) [Reset = 0x0000]

SGMII_STATUS is shown in SGMII_STATUS Register Field Descriptions.

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Table 7-64. SGMII_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12	sgmii_page_received	R	0b	Clear on read bit. Indicates that a new auto neg page was received
11	link_status_1000bx	R	0b	sgmii link status 0b = SGMII link is down 1b = SGMII link is up
10	sgmii_autoneg_complete	R	0b	sgmii autoneg complete indication 0b = SGMII autoneg incomplete 1b = SGMII autoneg completed
9	cfg_align_en	R	0b	word boundary FSM - align indication
8	cfg_sync_status	R	0b	word boundary FSM - sync status indication
7-4	cfg_align_idx	R	0b	word boundary index selection
3-0	cfg_state	R	0b	word boundary FSM state

7.6.2.52 SGMII_CTRL_2 Register (Address = 0x60C) [Reset = 0x0024]

SGMII_CTRL_2 is shown in SGMII_CTRL_2 Register Field Descriptions.

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Table 7-65. SGMII_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0b	Reserved
8	sgmii_cdr_lock_force_val	R/W	0b	SGMII cdr lock force value
7	sgmii_cdr_lock_force_ctrl	R/W	0b	SGMII cdr lock force enable
6	sgmii_mr_restart_an	RH/W1S	0b	Restart sgmii autonegotiation
5-3	tx_half_full_th	R/W	100b	SGMII TX sync FIFO half full threshold
2-0	rx_half_full_th	R/W	100b	SGMII RX sync FIFO half full threshold

7.6.2.53 SGMII_FIFO_STATUS Register (Address = 0x60D) [Reset = 0x0000]

SGMII_FIFO_STATUS is shown in SGMII_FIFO_STATUS Register Field Descriptions.

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Table 7-66. SGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0b	Reserved
3	sgmii_rx_af_full_err	H	0b	SGMII RX fifo full error. Cleared on read 0b = No error indication 1b = SGMII RX fifo full error has been indicated
2	sgmii_rx_af_empty_err	H	0b	SGMII RX fifo empty error. Cleared on read 0b = No error indication 1b = SGMII RX fifo empty error has been indicated
1	sgmii_tx_af_full_err	H	0b	SGMII TX fifo full error. Cleared on read 0b = No error indication 1b = SGMII TX fifo full error has been indicated
0	sgmii_tx_af_empty_err	H	0b	SGMII TX fifo empty error. Cleared on read 0b = No error indication 1b = SGMII TX fifo empty error has been indicated

7.6.2.54 PRBS_STATUS_1 Register (Address = 0x618) [Reset = 0x0000]

PRBS_STATUS_1 is shown in PRBS_STATUS_1 Register Field Descriptions.

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Table 7-67. PRBS_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-0	prbs_err_ov_cnt	R	0b	Holds number of error counter overflow that received by the PRBS checker. Value in this register is locked when write is done to register 0x001B bit[0] or bit[1]. Counter stops on 0xFF. Note: when PRBS counters work in single mode, overflow counter is not active

7.6.2.55 PRBS_CTRL_1 Register (Address = 0x619) [Reset = 0x0574]

PRBS_CTRL_1 is shown in PRBS_CTRL_1 Register Field Descriptions.

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Table 7-68. PRBS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0b	Reserved
13	cfg_pkt_gen_64	R/W	0b	1 = Transmit 64 byte packets in packet generation mode 0 = Transmit 1518 byte packets in packet generation mode 0b = Transmit 1518 byte packets in packet generation mode 1b = Transmit 64 byte packets in packet generation mode
12	send_pkt	RH/W1S	0b	Enables generating MAC packet with fix/incremental data w CRC (pkt_gen_en has to be set and cfg_pkt_gen_prbs has to be clear) Cleared automatically when pkt_done is set
11	RESERVED	R	0b	Reserved
10-8	cfg_prbs_chk_sel	R/W	101b	000 : Checker receives from RGMII TX 001 : Checker receives from SGMII TX 010 : Checker receives from RMII RX 011 : Checker receives from MII 101 : Checker receives from Cu RX 0b = Checker receives from RGMII TX 1b = Checker receives from SGMII TX 10b = Checker receives from RMII RX 11b = Checker receives from MII 101b = Checker receives from Cu RX
7	RESERVED	R	0b	Reserved
6-4	cfg_prbs_gen_sel	R/W	111b	000 : PRBS transmits to RGMII RX 001 : PRBS transmits to SGMII RX 010 : PRBS transmits to RMII RX 011 : PRBS transmits to MII RX 101 : PRBS transmits to Cu TX 0b = PRBS transmits to RGMII RX 1b = PRBS transmits to SGMII RX 10b = PRBS transmits to RMII RX 11b = PRBS transmits to MII RX 101b = PRBS transmits to Cu TX
3	cfg_prbs_cnt_mode	R/W	0b	1 = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again 0 = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting. 0b = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting. 1b = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again
2	cfg_prbs_chk_enable	R/W	1b	Enable PRBS checker
1	cfg_pkt_gen_prbs	R/W	0b	If set: (1) When pkt_gen_en is set, PRBS packets are generated continuously (3) When pkt_gen_en is cleared, PRBS RX checker is still enabled If cleared: (1) When pkt_gen_en is set, non - PRBS packet is generated (3) When pkt_gen_en is cleared, PRBS RX checker is disabled as well
0	pkt_gen_en	R/W	0b	Enable/disable for prbs/packet generator 0b = Disable for prbs/packet generator 1b = Enable for prbs/packet generator

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7.6.2.56 PRBS_CTRL_2 Register (Address = 0x61A) [Reset = 0x05DC]

PRBS_CTRL_2 is shown in PRBS_CTRL_2 Register Field Descriptions.

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Table 7-69. PRBS_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_pkt_len_prbs	R/W	1011101110 0b	Length (in bytes) of PRBS packets and MAC packets w CRC

7.6.2.57 PRBS_CTRL_3 Register (Address = 0x61B) [Reset = 0x007D]

PRBS_CTRL_3 is shown in PRBS_CTRL_3 Register Field Descriptions.

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Table 7-70. PRBS_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0b	Reserved
7-0	cfg_ipg_len	R/W	1111101b	Inter-packet gap (in bytes) between packets

7.6.2.58 PRBS_STATUS_2 Register (Address = 0x61C) [Reset = 0x0000]

PRBS_STATUS_2 is shown in PRBS_STATUS_2 Register Field Descriptions.

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Table 7-71. PRBS_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_byte_cnt	R	0b	Holds number of total bytes that received by the PRBS checker. Value in this register is locked when write is done to register 0x001B bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFF

7.6.2.59 PRBS_STATUS_3 Register (Address = 0x61D) [Reset = 0x0000]

PRBS_STATUS_3 is shown in PRBS_STATUS_3 Register Field Descriptions.

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Table 7-72. PRBS_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_pkt_cnt_15_0	R	0b	Bits [15:0] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register 0x001B bit[15] or bit[14]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.60 PRBS_STATUS_4 Register (Address = 0x61E) [Reset = 0x0000]

PRBS_STATUS_4 is shown in PRBS_STATUS_4 Register Field Descriptions.

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Table 7-73. PRBS_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_pkt_cnt_31_16	R	0b	Bits [31:16] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register 0x001B bit[15] or bit[14]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.61 PRBS_STATUS_5 Register (Address = 0x620) [Reset = 0x0000]

PRBS_STATUS_5 is shown in PRBS_STATUS_5 Register Field Descriptions.

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Table 7-74. PRBS_STATUS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0b	Reserved
12	pkt_done	R	0b	Set when all MAC packets w CRC are transmitted
11	pkt_gen_busy	R	0b	status of packet generator
10	prbs_pkt_ov	R	0b	If set, packet counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit[15] of 0x001B
9	prbs_byte_ov	R	0b	If set, bytes counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit[15] of 0x001B
8	prbs_lock	R	0b	prbs lock status
7-0	prbs_err_cnt	R	0b	Holds number of errored bytes that received by the PRBS checker Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters

7.6.2.62 PRBS_STATUS_6 Register (Address = 0x622) [Reset = 0x0000]

PRBS_STATUS_6 is shown in PRBS_STATUS_6 Register Field Descriptions.

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Table 7-75. PRBS_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pkt_err_cnt_15_0	R	0b	bits [15:0] of counter which records number or PRBS erroneous bytes received. This field gets cleared when bit[15] or bit[14] is written as 1 to register 0x001B

7.6.2.63 PRBS_STATUS_7 Register (Address = 0x623) [Reset = 0x0000]

PRBS_STATUS_7 is shown in PRBS_STATUS_7 Register Field Descriptions.

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Table 7-76. PRBS_STATUS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pkt_err_cnt_31_16	R	0b	bits [31:16] of counter which records number or PRBS erroneous bytes received. This field gets cleared when bit[15] or bit[14] is written as 1 to register 0x001B

7.6.2.64 PRBS_CTRL_4 Register (Address = 0x624) [Reset = 0x5511]

PRBS_CTRL_4 is shown in PRBS_CTRL_4 Register Field Descriptions.

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Table 7-77. PRBS_CTRL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_pkt_data	R/W	1010101b	Fixed data to be sent in Fix data mode
7-6	cfg_pkt_mode	R/W	0b	
5-3	cfg_pattern_vld_bytes	R/W	10b	Number of bytes of valid pattern in packet (Max - 6)
2-0	cfg_pkt_cnt	R/W	1b	Configures the number of MAC packets to be transmitted by packet generator 0b = 1 packet 1b = 10 packets 10b = 100 packets 11b = 1000 packets 100b = 10000 packets 101b = 100000 packets 110b = 1000000 packets 111b = Continuous packets

7.6.2.65 PATTERN_CTRL_1 Register (Address = 0x625) [Reset = 0x0000]

PATTERN_CTRL_1 is shown in PATTERN_CTRL_1 Register Field Descriptions.

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Table 7-78. PATTERN_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_15_0	R/W	0b	Bits 15:0 of pattern

7.6.2.66 PATTERN_CTRL_2 Register (Address = 0x626) [Reset = 0x0000]

PATTERN_CTRL_2 is shown in PATTERN_CTRL_2 Register Field Descriptions.

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Table 7-79. PATTERN_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_31_16	R/W	0b	Bits 31:16 of pattern

7.6.2.67 PATTERN_CTRL_3 Register (Address = 0x627) [Reset = 0x0000]

PATTERN_CTRL_3 is shown in PATTERN_CTRL_3 Register Field Descriptions.

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Table 7-80. PATTERN_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_47_32	R/W	0b	Bits 47:32 of pattern

7.6.2.68 PMATCH_CTRL_1 Register (Address = 0x628) [Reset = 0x0000]

PMATCH_CTRL_1 is shown in PMATCH_CTRL_1 Register Field Descriptions.

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Table 7-81. PMATCH_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_15_0	R/W	0b	Bits 15:0 of Matched Data - used for DA (destination address) match

7.6.2.69 PMATCH_CTRL_2 Register (Address = 0x629) [Reset = 0x0000]

PMATCH_CTRL_2 is shown in PMATCH_CTRL_2 Register Field Descriptions.

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Table 7-82. PMATCH_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_31_16	R/W	0b	Bits 31:16 of Matched Data - used for DA (destination address) match

7.6.2.70 PMATCH_CTRL_3 Register (Address = 0x62A) [Reset = 0x0000]

PMATCH_CTRL_3 is shown in PMATCH_CTRL_3 Register Field Descriptions.

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Table 7-83. PMATCH_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_47_32	R/W	0b	Bits 47:32 of Matched Data - used for DA (destination address) match

7.6.2.71 PKT_CRC_STAT Register (Address = 0x638) [Reset = 0x0000]

PKT_CRC_STAT is shown in PKT_CRC_STAT Register Field Descriptions.

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Table 7-84. PKT_CRC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1	rx_bad_crc	R	0b	
0	tx_bad_crc	R	0b	

7.6.2.72 TX_PKT_CNT_1 Register (Address = 0x639) [Reset = 0x0000]

TX_PKT_CNT_1 is shown in TX_PKT_CNT_1 Register Field Descriptions.

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Table 7-85. TX_PKT_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_pkt_cnt_15_0		0b	Lower 16 bits of Tx packet counter Note : Register is cleared when 0x60F, 0x610, 0x611 are read in sequence

7.6.2.73 TX_PKT_CNT_2 Register (Address = 0x63A) [Reset = 0x0000]

TX_PKT_CNT_2 is shown in TX_PKT_CNT_2 Register Field Descriptions.

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Table 7-86. TX_PKT_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_pkt_cnt_31_16		0b	Upper 16 bits of Tx packet counter Note : Register is cleared when 0x60F, 0x610, 0x611 are read in sequence

7.6.2.74 TX_PKT_CNT_3 Register (Address = 0x63B) [Reset = 0x0000]

TX_PKT_CNT_3 is shown in TX_PKT_CNT_3 Register Field Descriptions.

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Table 7-87. TX_PKT_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_err_pkt_cnt		0b	Tx packet w error (CRC error) counter Note : Register is cleared when 0x60F, 0x610, 0x611 are read in sequence

7.6.2.75 RX_PKT_CNT_1 Register (Address = 0x63C) [Reset = 0x0000]

RX_PKT_CNT_1 is shown in RX_PKT_CNT_1 Register Field Descriptions.

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Table 7-88. RX_PKT_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_pkt_cnt_15_0		0b	Lower 16 bits of Rx packet counter Note : Register is cleared when 0x612, 0x613, 0x614 are read in sequence

7.6.2.76 RX_PKT_CNT_2 Register (Address = 0x63D) [Reset = 0x0000]

RX_PKT_CNT_2 is shown in RX_PKT_CNT_2 Register Field Descriptions.

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Table 7-89. RX_PKT_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_pkt_cnt_31_16		0b	Upper 16 bits of Rx packet counter Note : Register is cleared when 0x612, 0x613, 0x614 are read in sequence

7.6.2.77 RX_PKT_CNT_3 Register (Address = 0x63E) [Reset = 0x0000]

RX_PKT_CNT_3 is shown in RX_PKT_CNT_3 Register Field Descriptions.

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Table 7-90. RX_PKT_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_err_pkt_cnt		0b	Rx packet w error (CRC error) counter Note : Register is cleared when 0x612, 0x613, 0x614 are read in sequence

7.6.2.78 RMII_CTRL_1 Register (Address = 0x648) [Reset = 0x0120]

RMII_CTRL_1 is shown in RMII_CTRL_1 Register Field Descriptions.

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Table 7-91. RMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0b	Reserved
10	cfg_rmii_dis_delayed_txd_en	R/W	0b	If set, disables delay of TXD in RMII mode
9-7	cfg_rmii_half_full_th	R/W	10b	
6	cfg_rmii_mode	R/W	0b	1 = RMII enabled 0 = RMII disabled if({RX_D2_strap, RX_D1_strap} == 2b01) reset_val = 1 else reset_val = 0 0b = RMII disabled 1b = RMII enabled
5	cfg_rmii_bypass_afifo_en	R/W	1b	1= RMII async fifo bypass enable 0= RMII async fifo not bypassed 0b = RMII async fifo not bypassed 1b = RMII async fifo bypass enable
4	cfg_xi_50	R/W	0b	XI sel for RMII mode if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3b010) reset_val = 1 else reset_val = 0
3	cfg_rmii_clk_shift_en	R/W	0b	
2	cfg_rmii_rcvrd_rx_clk_en	R/W	0b	
1	cfg_rmii_rev1_0	R/W	0b	RMII Rev1.0 enable bit
0	cfg_rmii_enh	R/W	0b	RMII enahnced mode enable bit

7.6.2.79 RMII_STATUS_1 Register (Address = 0x649) [Reset = 0x0000]

RMII_STATUS_1 is shown in RMII_STATUS_1 Register Field Descriptions.

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Table 7-92. RMII_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0b	Reserved
1	rmii_af_unf_err	R	0b	Clear on read bit RMII fifo undeflow error status
0	rmii_af_ovf_err	R	0b	Clear on Read bit RMII fifo overflow status

7.6.2.80 RMII_OVERRIDE_CTRL Register (Address = 0x64A) [Reset = 0x0010]

RMII_OVERRIDE_CTRL is shown in RMII_OVERRIDE_CTRL Register Field Descriptions.

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Table 7-93. RMII_OVERRIDE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0b	Reserved
10	cfg_clk50_tx_dll	R/W	0b	1 = use 50M DLL clock in RMII master for TX 0 = legacy mode if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3b011) reset_val = 1 else reset_val = 0 0b = legacy mode 1b = use 50M DLL clock in RMII master for TX
9	cfg_clk50_dll	R/W	0b	1 = use 50M DLL clock in RMII slave for RX 0 = use legacy mode if({RX_D2_strap, RX_D1_strap, RX_D0_strap} == 3b010) reset_val = 1 else reset_val = 0 0b = use legacy mode 1b = use 50M DLL clock in RMII slave for RX
8	cfg_rmii_sync_crs_dv	R/W	0b	
7	cfg_ovride_mux_rmii_tx_data_val	R/W	0b	
6	cfg_ovride_mux_rmii_tx_data_en	R/W	0b	
5	cfg_ovride_mux_rmii_rxd_val	R/W	0b	
4	cfg_ovride_mux_rmii_rxd_en	R/W	1b	
3	cfg_ovride_mux_rmii_rx_clk_val	R/W	0b	
2	cfg_ovride_mux_rmii_rx_clk_en	R/W	0b	
1	cfg_ovride_mux_rmii_tx_clk_val	R/W	0b	
0	cfg_ovride_mux_rmii_tx_clk_en	R/W	0b	

7.6.2.81 MMD1_PMA_CTRL_1 Register (Address = 0x1000) [Reset = 0x0000]

MMD1_PMA_CTRL_1 is shown in MMD1_PMA_CTRL_1 Register Field Descriptions.

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Table 7-94. MMD1_PMA_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PMA_reset	R/W	0b	0 = PMA not reset 1= PMA reset 0b = PMA not reset 1b = PMA reset
14-2	RESERVED	R	0b	Reserved
1-0	PMA_loopback	R/W	0b	0 = PMA loopback not set 1= PMA loopback set 0b = PMA loopback not set 1b = PMA loopback set

7.6.2.82 MMD1_PMA_STATUS_1 Register (Address = 0x1001) [Reset = 0x0000]

MMD1_PMA_STATUS_1 is shown in MMD1_PMA_STATUS_1 Register Field Descriptions.

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Table 7-95. MMD1_PMA_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0b	Reserved
2	link_status	R	0b	link status from link monitor state machine 0b = link status is down 1b = link status is up
1-0	RESERVED	R	0b	Reserved

7.6.2.83 MMD1_PMA_STATUS_2 Register (Address = 0x1007) [Reset = 0x003D]

MMD1_PMA_STATUS_2 is shown in MMD1_PMA_STATUS_2 Register Field Descriptions.

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Table 7-96. MMD1_PMA_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0b	Reserved
5-0	PMA or PMD type selection	R	111101b	PMA or PMD type selection field 11111xb = reserved for future use 111100b = reserved for future use 1110xxb = reserved for future use 110xxxb = reserved for future use 111101b = 100BASE-T1 PMA or PMD

7.6.2.84 MMD1_PMA_EXT_ABILITY_1 Register (Address = 0x100B) [Reset = 0x0800]

MMD1_PMA_EXT_ABILITY_1 is shown in MMD1_PMA_EXT_ABILITY_1 Register Field Descriptions.

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Table 7-97. MMD1_PMA_EXT_ABILITY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0b	Reserved
11	BASE-T1 extended abilities	R	1b	Base-T1 extended abilities field 0b = PMA or PMD does not have BASE-T1 extended abilities 1b = PMA or PMD has BASE-T1 extended abilities listed in register 1.18
10-0	RESERVED	R	0b	Reserved

7.6.2.85 MMD1_PMA_EXT_ABILITY_2 Register (Address = 0x1012) [Reset = 0x0001]

MMD1_PMA_EXT_ABILITY_2 is shown in MMD1_PMA_EXT_ABILITY_2 Register Field Descriptions.

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Table 7-98. MMD1_PMA_EXT_ABILITY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0b	Reserved
0	100BASE-T1 ability	R	1b	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1 0b = PMA/PMD is not able to perform 100BASE-T1 1b = PMA/PMD is able to perform 100BASE-T1

7.6.2.86 MMD1_PMA_CTRL_2 Register (Address = 0x1834) [Reset = 0x8000]

MMD1_PMA_CTRL_2 is shown in MMD1_PMA_CTRL_2 Register Field Descriptions.

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Table 7-99. MMD1_PMA_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	master_slave_man_cfg_en	R	1b	Value always 1
14	brk_ms_cfg	R/W	0b	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE pkg_36: reset_val = LED_0_strap pkg_28: reset_val = RX_D3_strap 0b = Configure PHY as SLAVE 1b = Configure PHY as MASTER
13-4	RESERVED	R	0b	Reserved
3-0	type selection	R	0b	type selection field 1xxxb = Reserved for future use 01xxb = Reserved for future use 001xb = Reserved for future use 0001b = Reserved for future use 0b = 100BASE-T1

7.6.2.87 MMD1_PMA_TEST_MODE_CTRL Register (Address = 0x1836) [Reset = 0x0000]

MMD1_PMA_TEST_MODE_CTRL is shown in MMD1_PMA_TEST_MODE_CTRL Register Field Descriptions.

Return to the Summary Table.

Table 7-100. MMD1_PMA_TEST_MODE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	brk_test_mode	R/W	0b	100BASE-T1 test mode control 0b = Normal mode operation 1b = Test mode 1 110b = Reserved 111b = Reserved 1010b = Test mode 2 1011b = Reserved 1100100b = Test mode 4 1100101b = Test mode 5
12-0	RESERVED	R	0b	Reserved

7.6.2.88 MMD3_PCS_CTRL_1 Register (Address = 0x3000) [Reset = 0x0000]

MMD3_PCS_CTRL_1 is shown in MMD3_PCS_CTRL_1 Register Field Descriptions.

Return to the Summary Table.

Table 7-101. MMD3_PCS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCS_Reset	R/W	0b	Reset bit, Self Clear. When write to this bit 1: 1. reset the registers (not vendor specific) at MMD3/MMD7. 2. Reset brk_top Please notice: This register is WSC (write-self-clear) and not read-only!
14	PCS_loopback	R/W	0b	This bit is cleared by PCS_Reset
13-11	RESERVED	R	0b	Reserved
10	rx_clock_stoppable	R/W	0b	RW, reset value = 1. 1= PHY may stop receive clock during LPI 0= Clock not stoppable Note: this flop implemented at glue logic
9-0	RESERVED	R	0b	Reserved

7.6.2.89 MMD3_PCS_Status_1 Register (Address = 0x3001) [Reset = 0x0000]

MMD3_PCS_Status_1 is shown in MMD3_PCS_Status_1 Register Field Descriptions.

Return to the Summary Table.

Table 7-102. MMD3_PCS_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0b	Reserved
11	TX_LPI_received	R	0b	RO/LH 1= Tx PCS hs received LPI 0= LPI not received
10	RX_LPI_received	R	0b	RO/LH 1= Rx PCS hs received LPI 0= LPI not received
9	Tx_LPI_indication	R	0b	1= TX PCS is currently receiving LPI 0= PCS is not currently receiving LPI 0b = PCS is not currently receiving LPI 1b = TX PCS is currently receiving LPI
8	Rx_LPI_indication	R	0b	1= RX PCS is currently receiving LPI 0= PCS is not currently receiving LPI 0b = PCS is not currently receiving LPI 1b = RX PCS is currently receiving LPI
7	RESERVED	R	0b	Reserved
6	tx_clock_stoppable	R	0b	1= the MAC may stop the clock during LPI 0= Clock not stoppable 0b = Clock not stoppable 1b = the MAC may stop the clock during LPI
5-0	RESERVED	R	0b	Reserved

8 Application and Implementation

Application Information Disclaimer

8.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.2 Application Information

The DP83TC812S-Q1 is a single-port 100-Mbps Automotive Ethernet PHY. It supports IEEE 802.3bw and allows for connections to an Ethernet MAC through MII, RMII, RGMII, or SGMII. When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required connections.

8.3 Typical Applications

Figure 8-1 through Figure 8-5 show some the typical applications for the DP83TC812S-Q1.

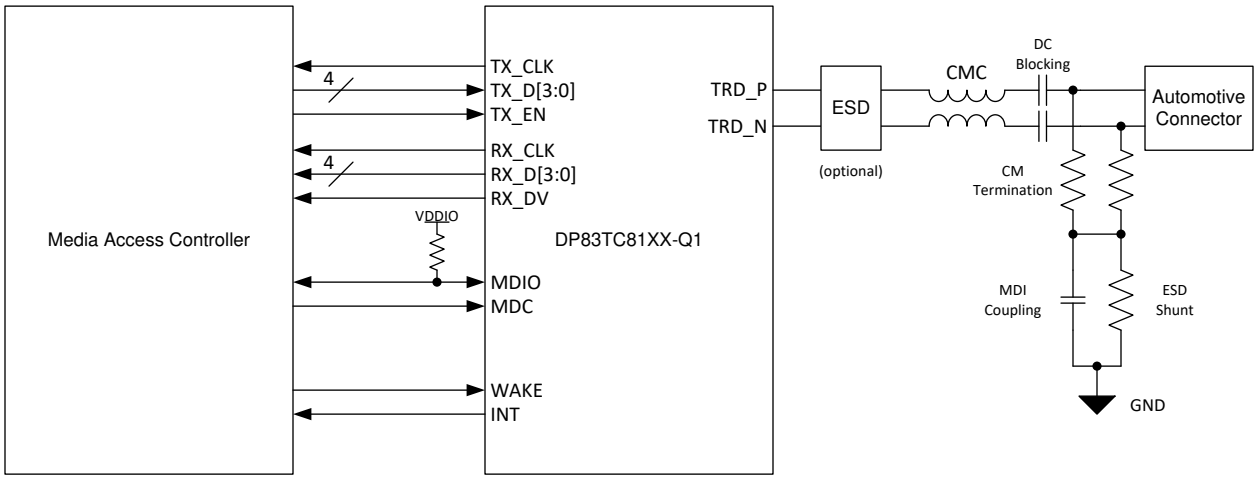


Figure 8-1. Typical Application (MII)

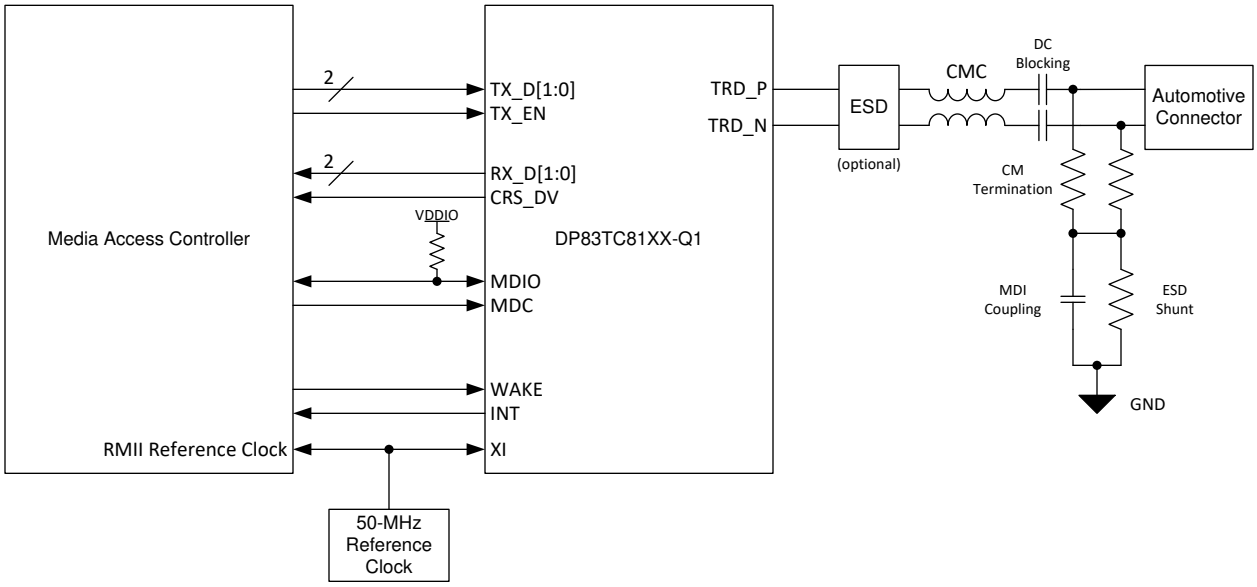


Figure 8-2. Typical Application (RMII Slave)

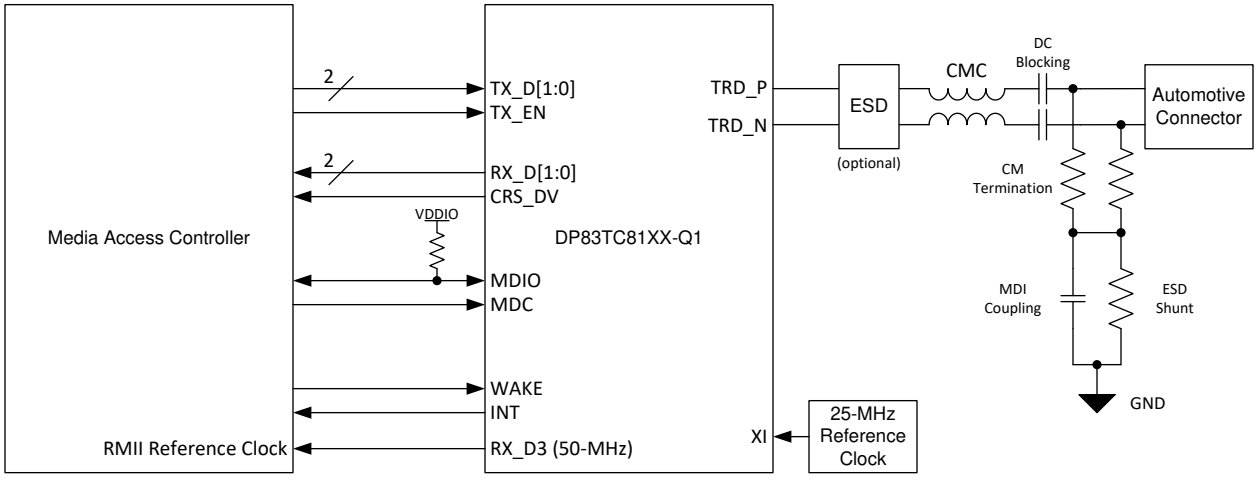


Figure 8-3. Typical Application (RMII Master)

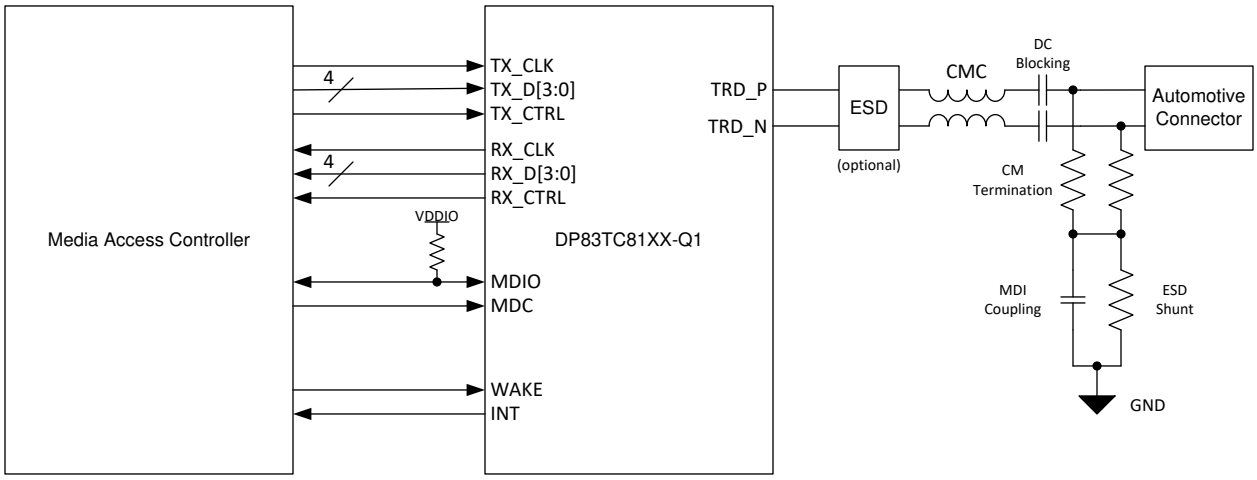


Figure 8-4. Typical Application (RGMII)

ADVANCE INFORMATION

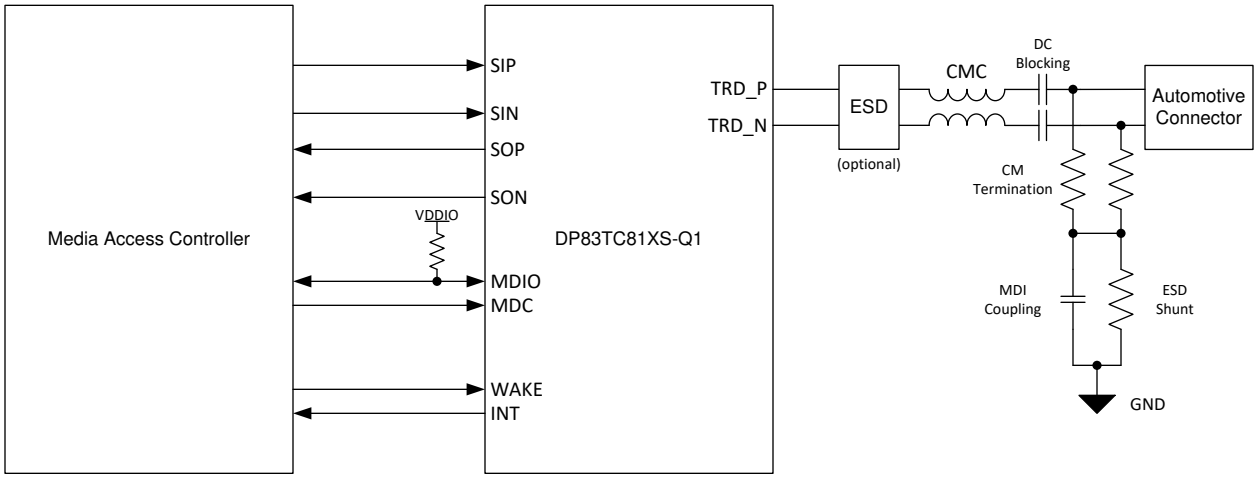


Figure 8-5. Typical Application (SGMII)

8.3.1 Design Requirements

For these typical applications, use the following as design parameters:

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8 V, 2.5 V, or 3.3 V
V_{DDMAC}	1.8 V, 2.5 V, or 3.3 V
V_{DDA}	3.3 V
V_{SLEEP}	3.3 V
Decoupling capacitors V_{DDIO} (2)	0.01 µF
(Optional) ferrite bead for V_{DDIO}	1 kΩ at 100 MHz (BLM18AG102SH)
Decoupling capacitors V_{DDMAC} (2)	0.01 µF, 0.47 µF
Ferrite bead for V_{DDMAC}	1 kΩ at 100 MHz (BLM18AG102SH)
Decoupling capacitors V_{DDA} (2)	0.01 µF, 0.1 µF, 0.47 µF
(Optional) ferrite bead for V_{DDA}	1 kΩ at 100 MHz (BLM18AG102SH)
Decoupling capacitors V_{SLEEP}	0.1 µF
DC Blocking Capacitors (2)	0.1 µF
Common-Mode Choke	200 µH
Common Mode Termination Resistors(1)	1 kΩ
MDI Coupling Capacitor (2)	4.7 nF
ESD Shunt(2)	100 kΩ
Reference Clock	25 MHz

(1) 1% tolerance components are recommended.
(2) 10% tolerance components are recommended.

8.3.1.1 Physical Medium Attachment

There must be no metal running beneath the common-mode choke. CMCs can inject noise into metal beneath them, which can affect the emissions and immunity performance of the system. Because the DP83TC812S-Q1 is a voltage mode line driver, no external termination resistors are required. The ESD shunt and MDI coupling capacitor must be connected to ground. Ensure that the common mode termination resistors are 1% tolerance or better to improve differential coupling.

ADVANCE INFORMATION

8.3.1.1.1 Common-Mode Choke Recommendations

The following CMCs are recommended for use with the DP83TC812S-Q1 :

Table 8-2. Recommended CMCs

MANUFACTURER	PART NUMBER
Pulse Electronics	AE2002
Murata	DLW43MH201XK2L
Murata	DLW32MH201XK2
TDK	ACT1210L-201

Table 8-3. CMC Electrical Specifications

PARAMETER	TYP	UNITS	CONDITIONS
Insertion Loss	–0.5	dB	1 – 30 MHz
	–1.0	dB	30 – 60 MHz
Return Loss	–26	dB	1 – 30 MHz
	–20	dB	30 – 60 MHz
Common-Mode Rejection	–24	dB	1 MHz
	–42	dB	10 – 100 MHz
	–25	dB	400 MHz
Differential Common-Mode Rejection	–70	dB	1 – 10 MHz
	–50	dB	100 MHz
	–24	dB	1000 MHz

ADVANCE INFORMATION

8.3.2 Detailed Design Procedure

When creating a new system design with an Ethernet PHY, follow this schematic capture procedure:

1. Select desired PHY hardware configurations in table Table 7-5.
2. Use the Section 6.5 table, the Table 7-3 table and the Table 7-4 table to select the correct external bootstrap resistors.
3. If using LEDs, ensure the correct external circuit is applied as shown in Figure 7-5.
4. Select an appropriate clock source that adheres to either the CMOS-level oscillator or crystal resonator requirements within the Section 6.5 table.
5. Select a CMC, a list of recommended CMCs are located in Table 8-2.
6. Add common-mode termination, DC-blocking capacitors, an MDI-coupling capacitor, and an ESD shunt found in Table 8-1.
7. Ensure that there is sufficient supply decoupling on VDDIO and VDDA supply pins.
8. Add an external pullup resistor (tie to VDDIO) on MDIO line.
9. If operating with SGMII, place 0.1-µF, DC-blocking capacitors between the MAC and PHY SGMII pins.
10. If sleep modes are not desired, WAKE and EN pins must be tied to VDDIO directly or through an external pullup resistor.

The following layout procedure must be followed:

1. Locate the PHY near the edge of the board so that short MDI traces can be routed to the desired connector.
2. Place the MDI external components: CMC, DC-blocking capacitors, CM termination, MDI-coupling capacitor, and ESD shunt.
3. Create a top-layer metal pour keepout under the CMC.
4. Ensure that the MDI TRD_M and TRD_P traces are routed such that they are 100-Ω differential.
5. Place the clock source near the XI and XO pins.
6. Ensure that when configured for MII, RMII, or RGMII operation, the xMII pins are routed 50-Ω and are single-ended with reference to ground.
7. Ensure that transmit path xMII pins are routed such that setup and hold timing does not violate the PHY requirements.
8. Ensure that receive path xMII pins are routed such that setup and hold timing does not violate the MAC requirements.
9. Ensure that when configured for SGMII operation, the xMII RX_P, RX_M, TX_P, and TX_M pins are routed 100-Ω differential.
10. Place the MDIO pullup close to the PHY.

9 Power Supply Recommendations

The DP83TC812S-Q1 is capable of operating with a wide range of IO supply voltages (3.3 V, 2.5 V, or 1.8 V). No power supply sequencing is required. The recommended power supply de-coupling network is shown in the figure below. For improved conducted emissions, an optional ferrite bead may be placed between the supply and the PHY de-coupling network.

Typical TC-10 application block diagram along with supply and peripherals is shown below. TPS7B81-Q1 is the recommended part number to be used as 3.3V LDO for the VSLEEP rail. The low quiescent current of this LDO makes it ideal for TC-10 applications.

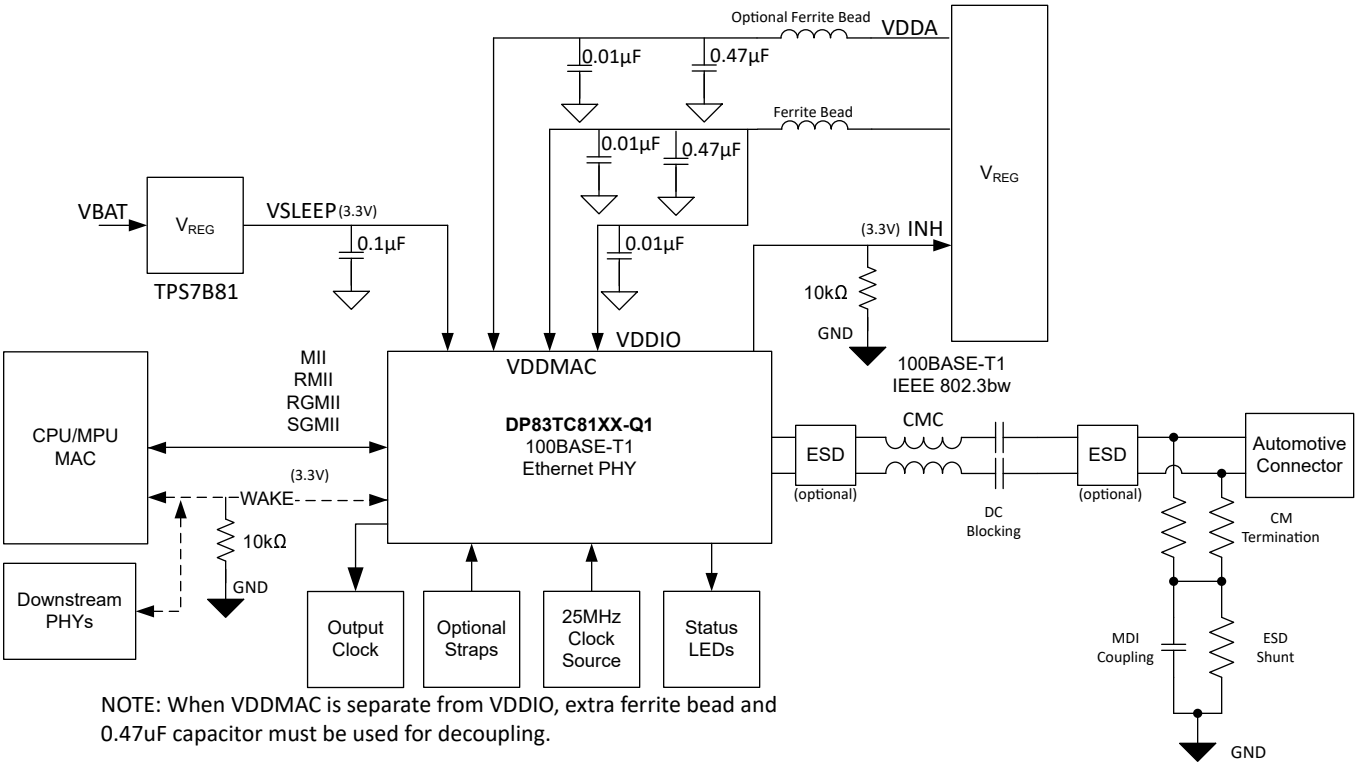


Figure 9-1. Typical TC-10 Application with peripherals

10 Layout

10.1 Layout Guidelines

10.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces must be 50-Ω, single-ended impedance. Differential traces must be 50-Ω single-ended and 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities will cause reflections leading to emissions and signal integrity issues. Stubs must be avoided on all signal traces, especially differential signal pairs.

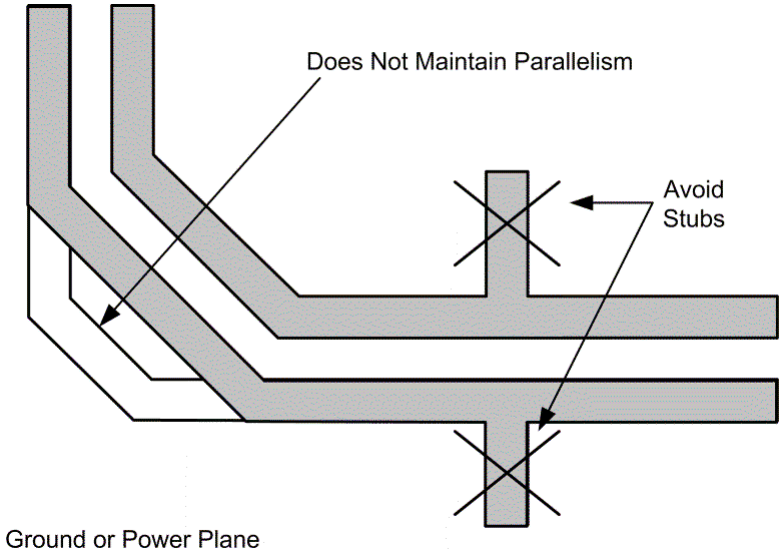


Figure 10-1. Differential Signal Trace Routing

Within the differential pairs, trace lengths must be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All transmit signal traces must be length matched to each other and all receive signal traces must be length matched to each other.

Ideally, there must be no crossover on signal path traces. High speed signal traces must be routed on internal layers to improved EMC performance. However, vias present impedance discontinuities and must be minimized when possible. Route trace pairs on the same layer. Signals on different layers must not cross each other without at least one return path plane between them. Differential pairs must always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

10.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces should be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

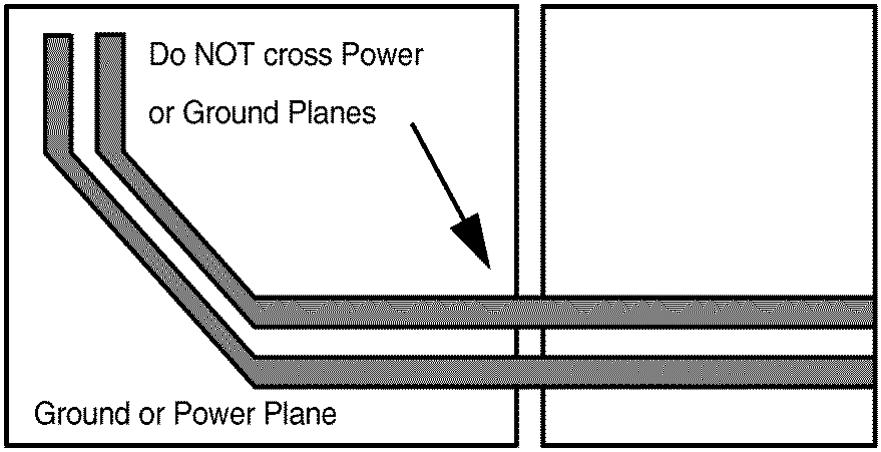


Figure 10-2. Power and Ground Plane Breaks

10.1.3 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

10.1.4 PCB Layer Stacking

To meet signal integrity and performance requirements, minimum four-layer PCB is recommended. However, a six-layer PCB and above must be used when possible.

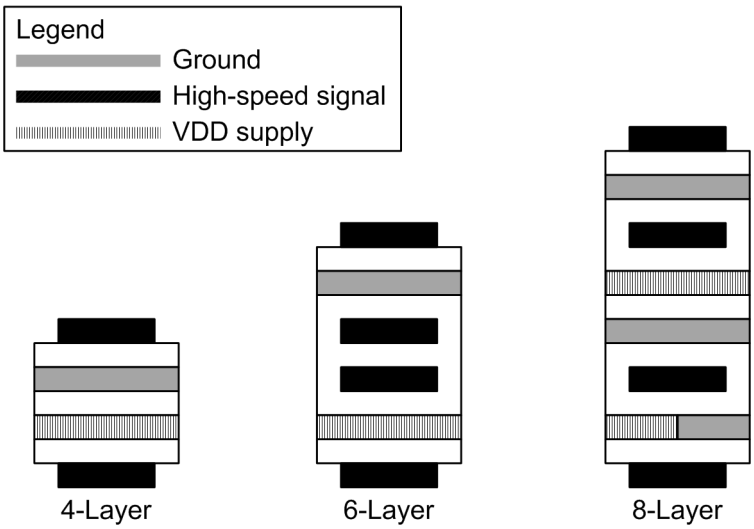


Figure 10-3. Recommended PCB Layer Stack-Up

10.2 Layout Example

There is a evaluation board references for the DP83TC812-Q1 ; the DP83TC812EVM-MC is a media converter board which can be used for interoperability and bit error rate testing.

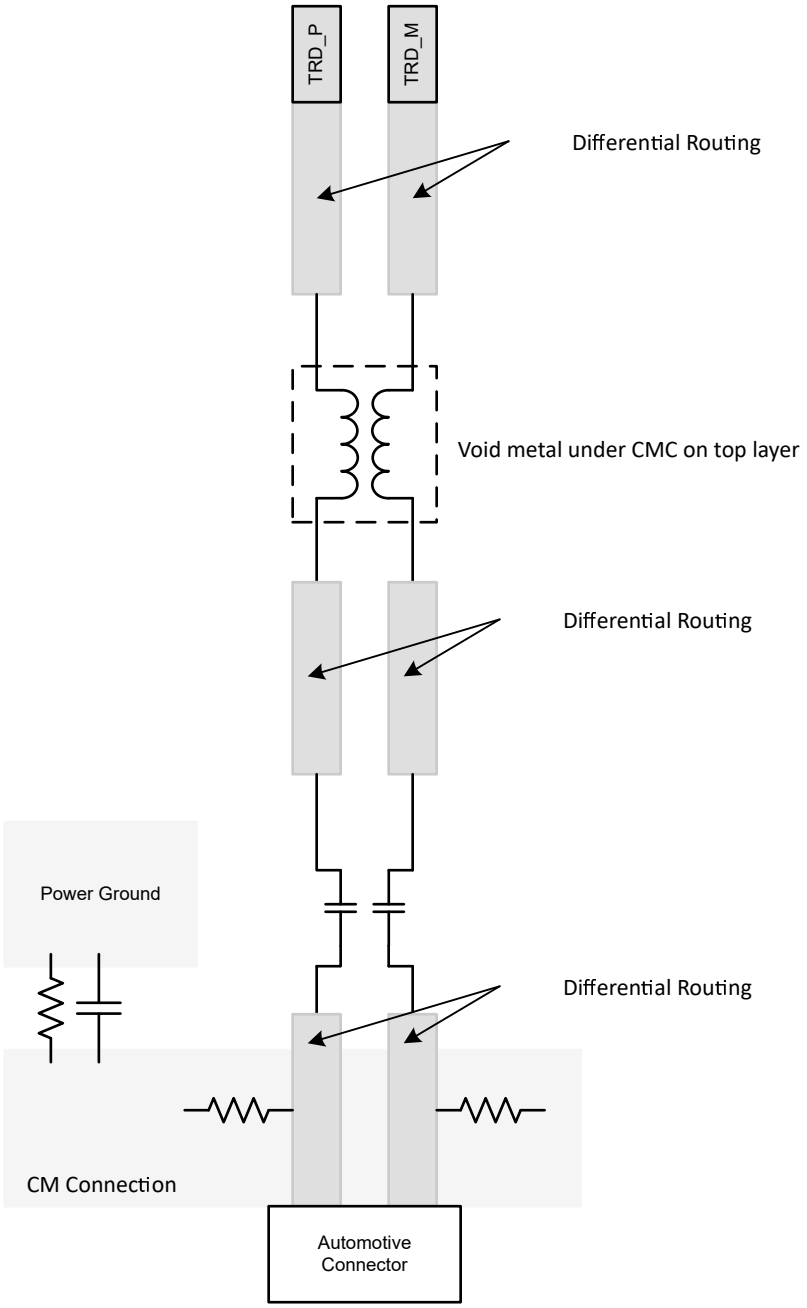


Figure 10-4. MDI Low-Pass Filter Layout Recommendation

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Community Resources

11.4 Trademarks

PHYTER™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
PDP83TC812SRHATQ1	EARLY SAMPLES	VQFN	RHA	36	250	RoHS	NIPDAU	MSL3-260°C	-40 to 125	TBD

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

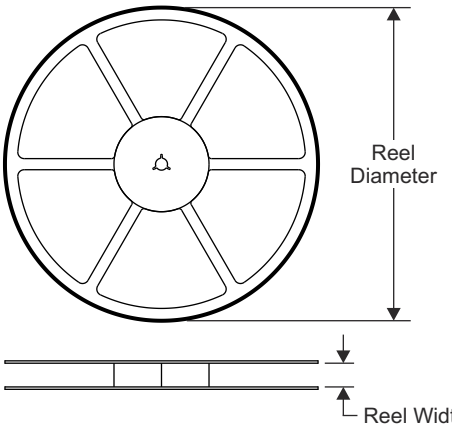
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

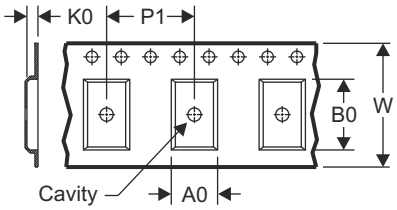
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

12.1.2 Tape and Reel Information

REEL DIMENSIONS

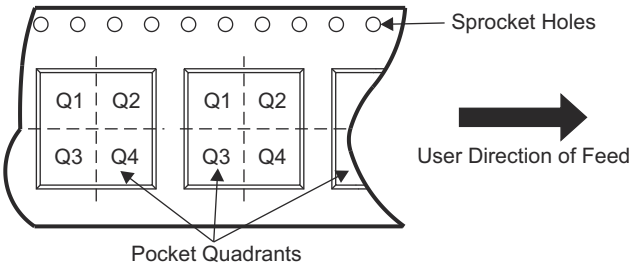


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

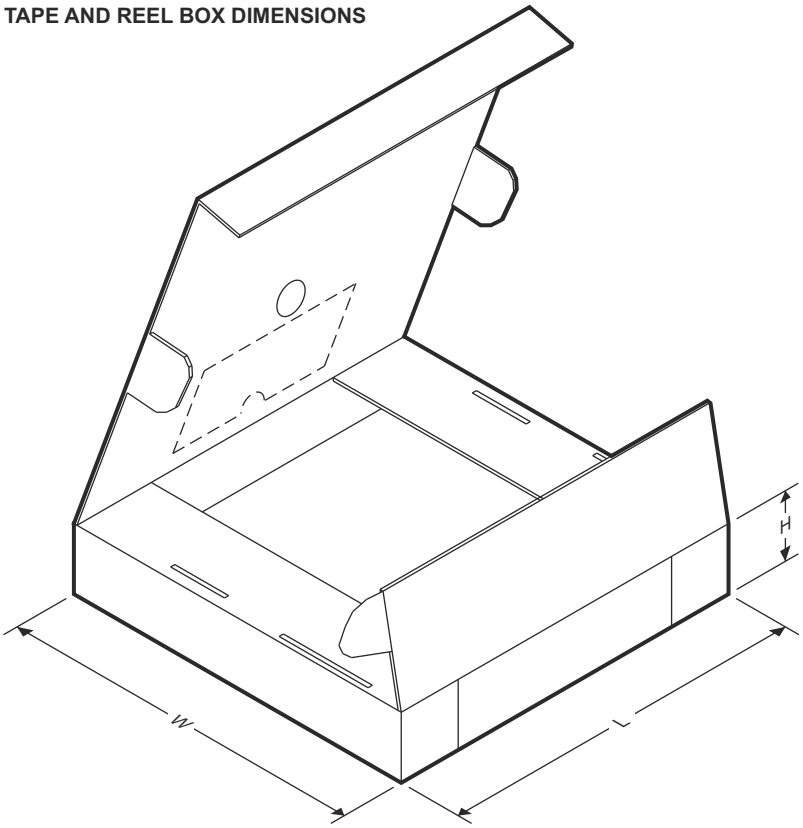
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDP83TC812SRHATQ1	VQFN	RHA	36	250	180	16.4	6.3	6.3	1.1	12	16	Q2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PDP83TC812SRHATQ1	VQFN	RHA	36	Call TI	Call TI	Call TI	Call TI

ADVANCE INFORMATION

ADVANCE INFORMATION

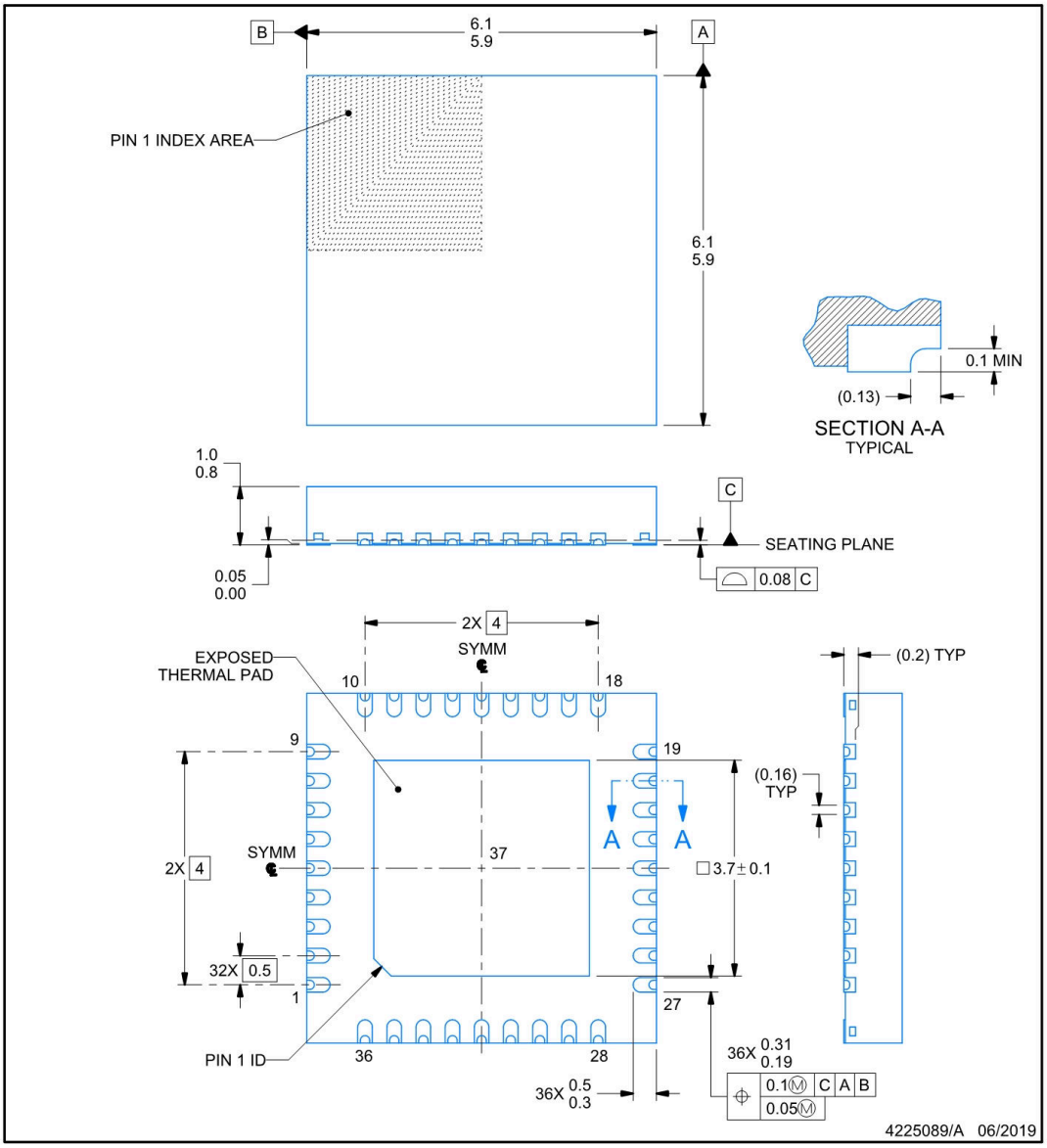
13 POD

RHA0036A

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



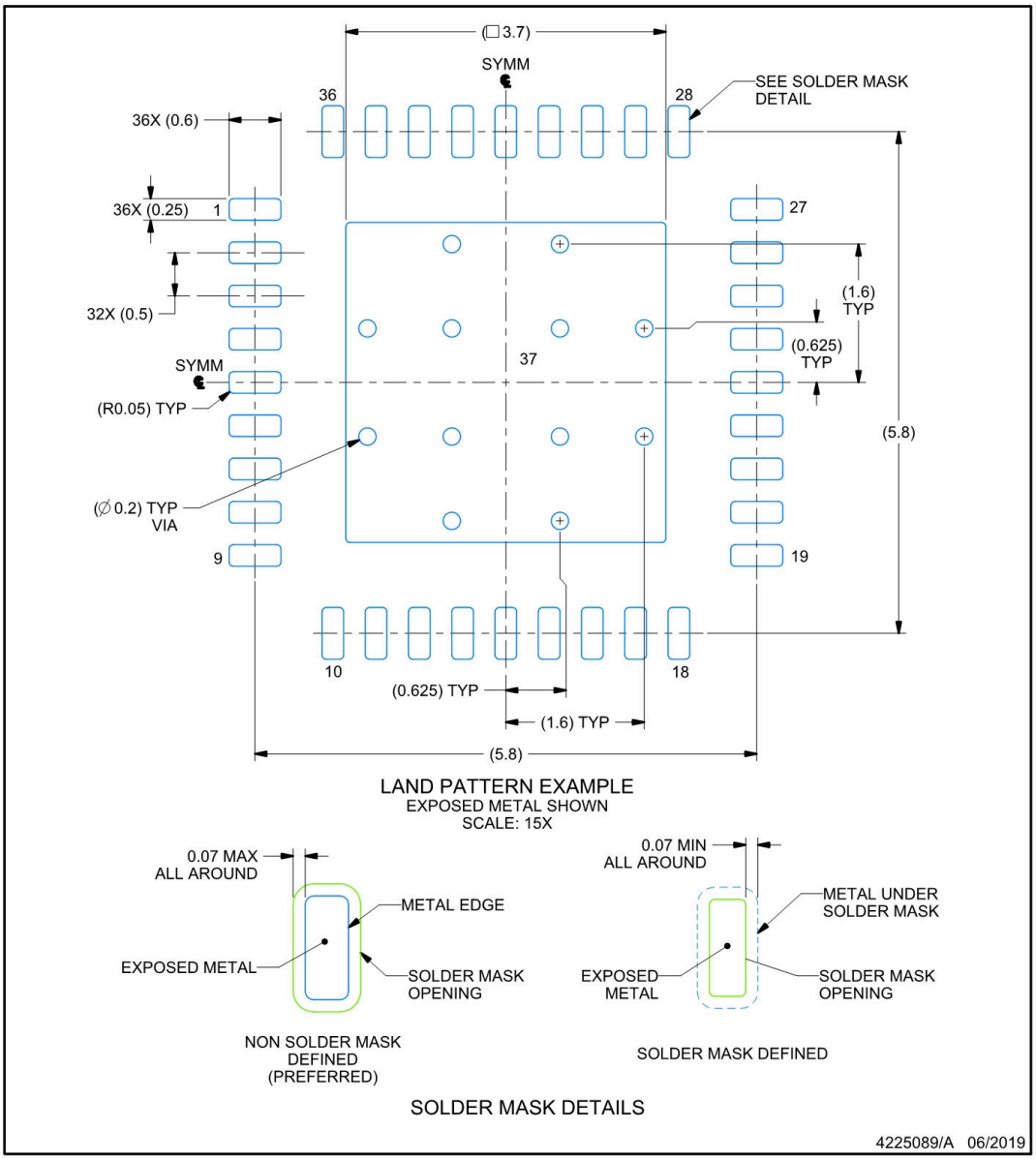
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHA0036A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



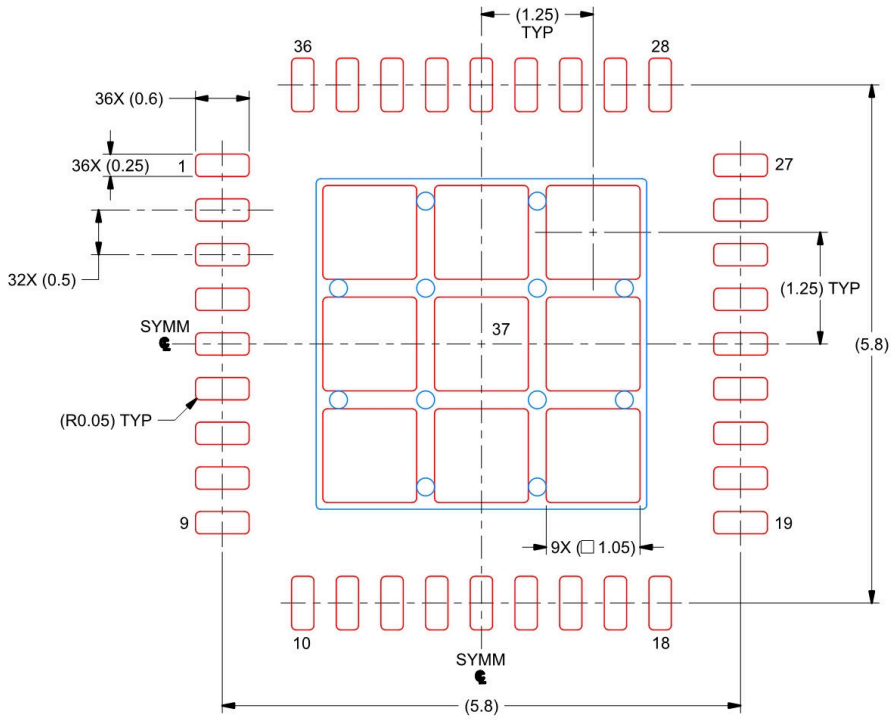
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0036A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225089/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PDP83TC812SRHATQ1	ACTIVE	VQFN	RHA	36	250	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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