

## SNx52x0 USB Port Transient Suppressors

### 1 Features

- Design to protect submicron 3-V or 5-V circuits from noise transients
- Port ESD protection capability exceeds:
  - 15-kV human body model
  - 2-kV machine model
- Available in a WCSP chip-scale package
- Stand-off voltage: 6 V (minimum)
- Low current leakage: 1- $\mu$ A maximum at 6 V
- Low capacitance: 35-pF (typical)

### 2 Applications

- USB full-speed host, HUB, or peripheral
- Ports

### 3 Description

The SN65220 device is a dual, and the SN65240 and SN75240 devices are quadruple, unidirectional transient voltage suppressors (TVS). These devices provide electrical noise transient protection to Universal Serial Bus (USB) low and full-speed ports. The input capacitance of 35 pF makes it unsuitable for high-speed USB 2.0 applications.

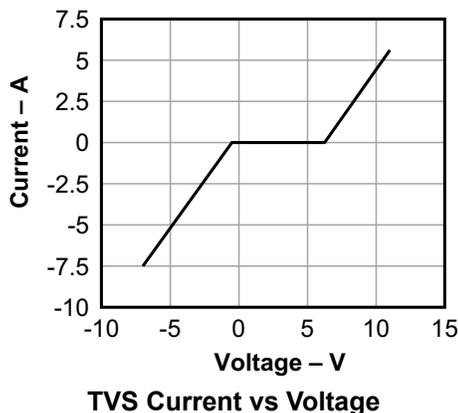
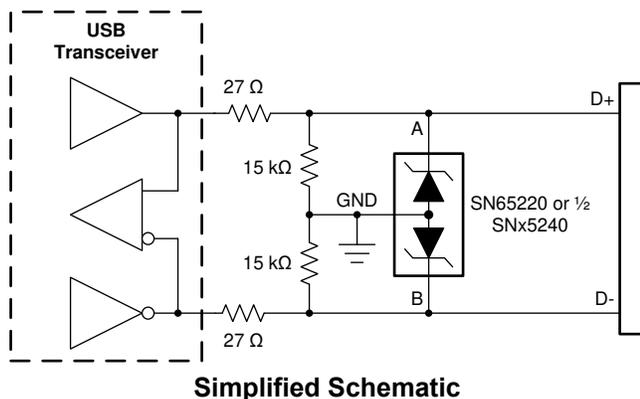
Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the USB transceiver or the USB ASIC if they are of sufficient magnitude and duration.

The SN65220, SN65240, and SN75240 devices ESD performance is measured at the system level, according to IEC61000-4-2; system design, however, impacts the results of these tests. To accomplish a high compliance level requires careful board design and layout techniques.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65220	SOT-23 (6)	2.90 mm × 1.60 mm
	DSBGA (4)	0.925 mm × 0.925 mm
SN65240 SN75240	PDIP (8)	9.09 mm × 6.35 mm
	TSSOP (8)	3.00 mm × 4.40 mm

- (1) See the orderable addendum at the end of the data sheet for all available packages.



## Table of Contents

<b>1 Features</b> .....	1	9.4 Device Functional Modes.....	7
<b>2 Applications</b> .....	1	<b>10 Application and Implementation</b> .....	8
<b>3 Description</b> .....	1	10.1 Application Information.....	8
<b>4 Revision History</b> .....	2	10.2 Typical Application.....	8
<b>5 Device Comparison Table</b> .....	3	<b>11 Power Supply Recommendations</b> .....	10
<b>6 Pin Configuration and Functions</b> .....	3	<b>12 Layout</b> .....	10
<b>7 Specifications</b> .....	4	12.1 Layout Guidelines.....	10
7.1 Absolute Maximum Ratings.....	4	12.2 Layout Example.....	10
7.2 ESD Ratings.....	4	<b>13 Device and Documentation Support</b> .....	11
7.3 Recommended Operating Conditions.....	4	13.1 Related Links.....	11
7.4 Thermal Information.....	4	13.2 Receiving Notification of Documentation Updates..	11
7.5 Electrical Characteristics.....	4	13.3 Support Resources.....	11
7.6 Typical Characteristics.....	5	13.4 Trademarks.....	11
<b>8 Parameter Measurement Information</b> .....	5	13.5 Electrostatic Discharge Caution.....	11
<b>9 Detailed Description</b> .....	6	13.6 Glossary.....	11
9.1 Overview.....	6	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	11
9.2 Functional Block Diagram.....	6		
9.3 Feature Description.....	7		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision H (May 2015) to Revision I (April 2021)</b>	<b>Page</b>
• Updated the numbering format for tables, figures and cross-references throughout the document .....	1
• Updated the units for resistance from <i>O</i> to $\Omega$ in the <i>Simplified Schematic</i> figure.....	1
• Updated the units from <i>O</i> to $\Omega$ in the <i>Typical Application Schematic for ESD Protection of USB Transceivers</i> figure .....	8
• Updated the units from <i>O</i> to $\Omega$ in the <i>Layout Example of a 4-Layer Board With SN65220</i> figure.....	10

<b>Changes from Revision G (August 2008) to Revision H (May 2015)</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1

## 5 Device Comparison Table

PRODUCT	SUPPRESSORS	T <sub>A</sub> - RANGE	PACKAGE
SN65220	1	–40°C to 85°C	WCSP-4
			SOT23-6
SN65240	2	–40°C to 85°C	DIP-8
			TSSOP-8
SN75240	2	0°C to 70°C	DIP-8
			TSSOP-8

## 6 Pin Configuration and Functions

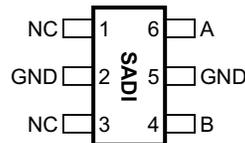


Figure 6-1. DBV Package 6-Pin SOT-23 Top View

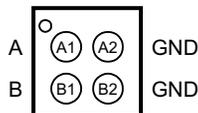


Figure 6-2. YZB Package 4-Pin DSBGA Top View

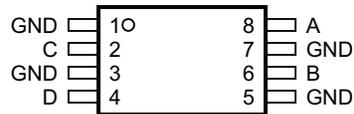


Figure 6-3. P, PW Packages 8-Pin PDIP, TSSOP Top View

Table 6-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DBV	YZB	P, PW		
A	6	A1	8	Analog input	Transient suppressor input – Line 1
B	4	B2	6	Analog input	Transient suppressor input – Line 2
C	—	—	2	Analog input	Transient suppressor input – Line 3
D	—	—	4	Analog input	Transient suppressor input – Line 4
GND	2, 5	A2, B2	1, 3, 5, 7	Power	Local device ground
NC	1, 3	—	—	—	Internally not connected

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$P_{D(\text{peak})}$	Peak power dissipation		60	W
$I_{\text{FSM}}$	Peak forward surge current		3	A
$I_{\text{RSM}}$	Peak reverse surge current		-9	A
$T_{\text{stg}}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 7.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic discharge		V
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±15000	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±2000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$T_A$	Ambient temperature			°C
	SN75240	0	70	
	SN65220, SN65240	-40	85	

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN65220		SN65240, SN75240		UNIT
		DBV (SOT-23)	YZB (DSBGA)	P (PDIP)	PW (TSSOP)	
		6 PINS	4 BALLS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	199.5	170	67.5	185.3	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	159.7	1.8	57.9	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.1	43.5	44.5	114.0	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	41	9.2	36.2	9.9	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	50.5	43.5	44.5	112.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

### 7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{\text{kg}}$	Leakage current			1	μA	
$V_{\text{(BR)}}$	Breakdown voltage		6.5	7	8	V
$C_{\text{IN}}$	Input capacitance to ground		35		pF	

## 7.6 Typical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted.

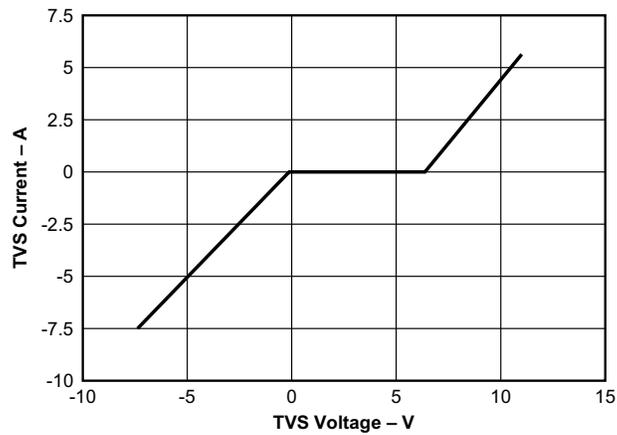


Figure 7-1. Transient-Voltage-Suppressor Current vs Voltage

## 8 Parameter Measurement Information

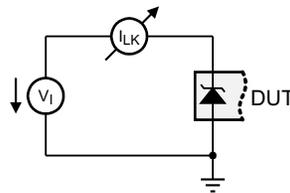


Figure 8-1. Measurement of Leakage Current

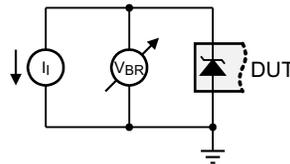


Figure 8-2. Measurement of Breakdown Voltage

## 9 Detailed Description

### 9.1 Overview

The SN65220, SN65240, and SN75240 devices integrate multiple unidirectional transient voltage suppressors (TVS). Figure 9-1 shows the equivalent circuit diagram of a single TVS diode.

For positive transient voltages, only the Q1 transistor determines the switching characteristic. When the input voltage reaches the Zener voltage,  $V_Z$ , Zener diode D1 conducts; therefore, allowing for the base-emitter voltage,  $V_{BE}$ , to increase. At  $V_{IN} = V_Z + V_{BE}$ , the transistor starts conducting. From then on, its on-resistance decreases linearly with increasing input voltage.

For negative transient voltages, only diode D2 determines the switching characteristic. Here, switching occurs when the input voltage exceeds the diode forward voltage,  $V_{FW}$ .

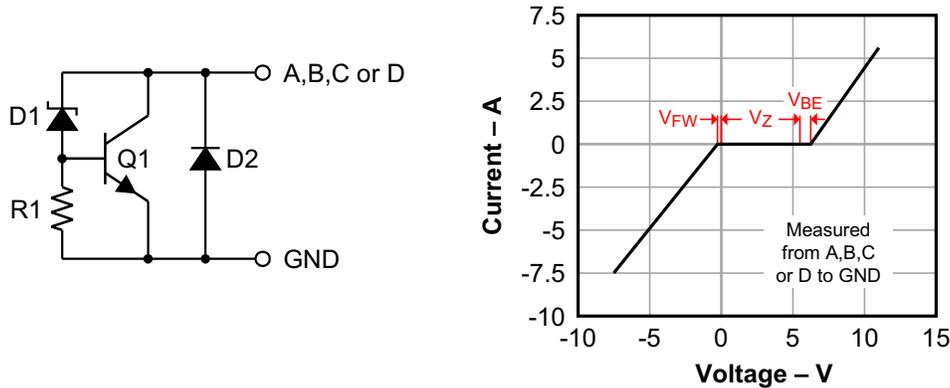
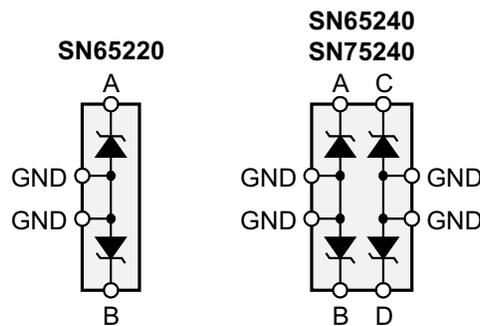


Figure 9-1. TVS Structure and Current — Voltage Characteristic

### 9.2 Functional Block Diagram



### 9.3 Feature Description

The SN65220, SN65240, and SN75240 family of unidirectional transient voltage suppressors provide transient protection to Universal Serial Bus low and full-speed ports. These TVS diodes provide a minimum breakdown voltage of 6.5V to protect USB transceivers and USB ASICs typically implemented in 3-V or 5-V digital CMOS technology.

### 9.4 Device Functional Modes

TVS diodes possess two functional modes, a high-impedance and a conducting mode.

During normal operating conditions, that is in the absence of high voltage transients, the breakdown voltage of TVS diodes is not exceeded and the devices remain high-impedance.

In the presence of high-voltage transients the breakdown voltage is exceeded. The TVS diodes then conduct and become low-impedance. In this mode excessive transient energy is shunted directly to local circuit ground, preventing USB transceivers from electrical damage.

## 10 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 10.1 Application Information

The universal serial bus (USB) has become a popular solution to connect PC peripherals. USB allows devices to be hot-plugged in and out of the existing PC system without rebooting or turning off the PC. Because frequent human interaction with the USB system occurs as a result of its attractive hot-plugging ability, there is the possibility for large ESD strikes and damage to crucial system elements. The ESD protection included on the existing hardware is typically in the 2-kV to 4-kV range for the human body model (HBD) and 200-V to 300-V for the machine model (MM). The ESD voltage levels found in a normal USB operating environment can exceed these levels. The SN75240, SN65240, and SN65220 devices will increase the robustness of the existing USB hardware to ESD strikes common to the environment in which USB is likely to be used.

### 10.2 Typical Application

Figure 10-1 illustrates a typical USB system and application of the SN75240, SN65240, and SN65220 devices. Connections to pin A from the D+ data line, pin B from the D- data line, and the device grounds from the GND line that already exists are necessary to increase the amount of ESD protection provided to the USB port.

The design of the suppressor gives it very low maximum current leakage of 1  $\mu$ A, a very low typical capacitance of 35 pF, and a standoff voltage minimum of 6 V. Because of these levels, the SN75240, SN65240, and SN65220 devices will provide added protection to the USB system hardware during ESD events without introducing the high capacitance and current leakage levels typical of external transient voltage suppressors. The addition of an SN75240, SN65240, or SN65220 device is beneficial to both full-speed and low-speed USB 1.1 bandwidth standards.

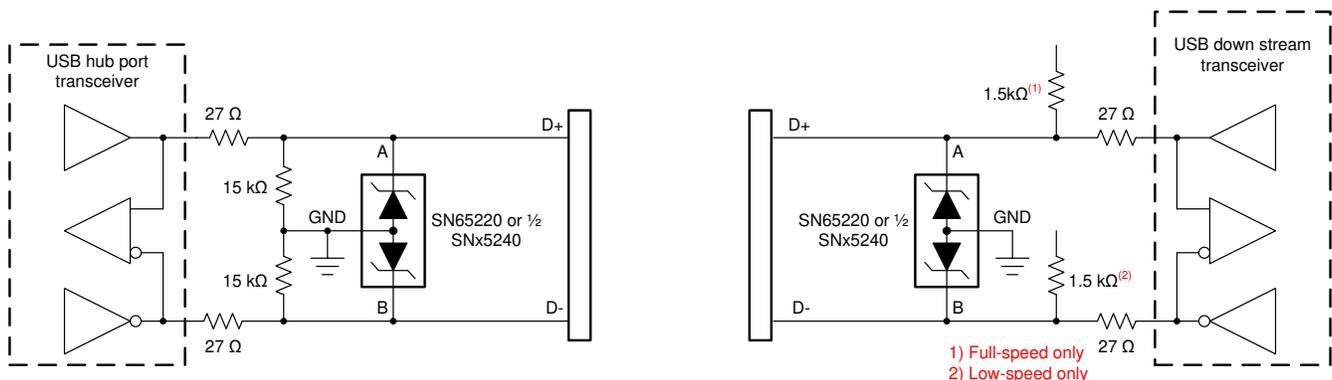


Figure 10-1. Typical Application Schematic for ESD Protection of USB Transceivers

### 10.2.1 Design Requirements

For this design example, use the parameters listed in [Table 10-1](#) as design parameters.

**Table 10-1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Minimum breakdown voltage (TVS)	6.5 V
Maximum supply voltage (USB transceiver)	5.5 V
Typical junction capacitance (TVS)	35 pF
Maximum data rate (USB transceiver)	12 Mbps

### 10.2.2 Detailed Design Procedure

To effectively protect USB transceivers, use TVS diodes with breakdown voltages close to 6 V, such as the SN65220, SN65240, or SN75220 devices.

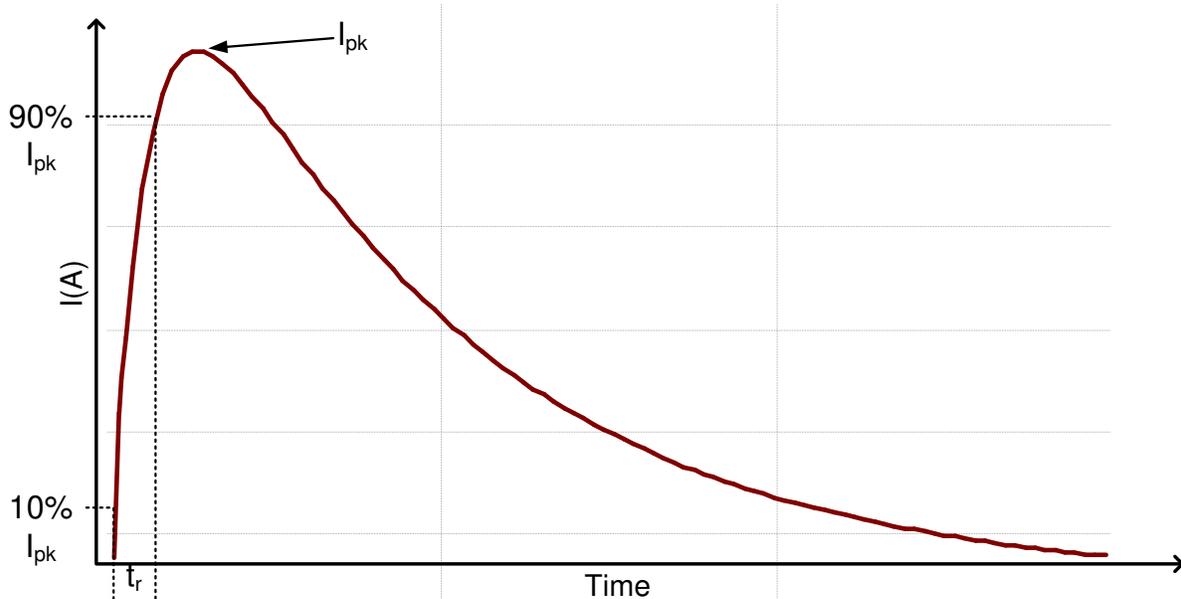
Because of the TVS junction capacitance of 35 pF, apply these TVS diodes only to USB transceivers with full-speed capability that is 12 Mbps maximum.

Place the TVS diodes as close to the board connector as possible to prevent transient energies from entering further board space.

Connect the TVS diode between the data lines (D+, D–) and local circuit ground (GND).

Because noise transient represents high-speed frequencies, ensure low-inductance return paths for the transient currents by providing a solid ground plane and using two VIAs connecting the TVS terminals to ground.

### 10.2.3 Application Curve



**Figure 10-2. HBM Curve**

## 11 Power Supply Recommendations

Unlike other semiconductor components that require a supply voltage to operate, the SN65220, SN65240, and SN75240 transient suppressors are combinations of multiple p-n diodes, activated by transient voltages. Therefore, these transient suppressors do not require external voltage supplies.

## 12 Layout

### 12.1 Layout Guidelines

The multiple ground pins provided lower the connection resistance to ground. In order to improve circuit operation, a connection to all ground pins must be provided on the system printed circuit board. Without proper device connection to ground, the speed and protection capability of the device will be degraded.

- The ground termination pads should be connected directly to a ground plane on the board for optimum performance. A single trace ground conductor will not provide an effective path for fast rise-time transient events including ESD due to parasitic inductance.
- Nominal inductive values of a PCB trace are approximately 20 nH/cm. This value may seem small, but an apparent *short length* of trace may be sufficient to produce significant  $L(di/dt)$  effects with fast rise-time ESD spikes.
- Mount the TVS as close as possible to the I/O socket to reduce radiation originating from the transient as it is routed to ground.

#### Note

Direct connective paths of the traces are taken to the suppressor mounting pads to minimize parasitic inductance in the surge-current conductive path, thus minimizing  $L(di/dt)$  effects.

### 12.2 Layout Example

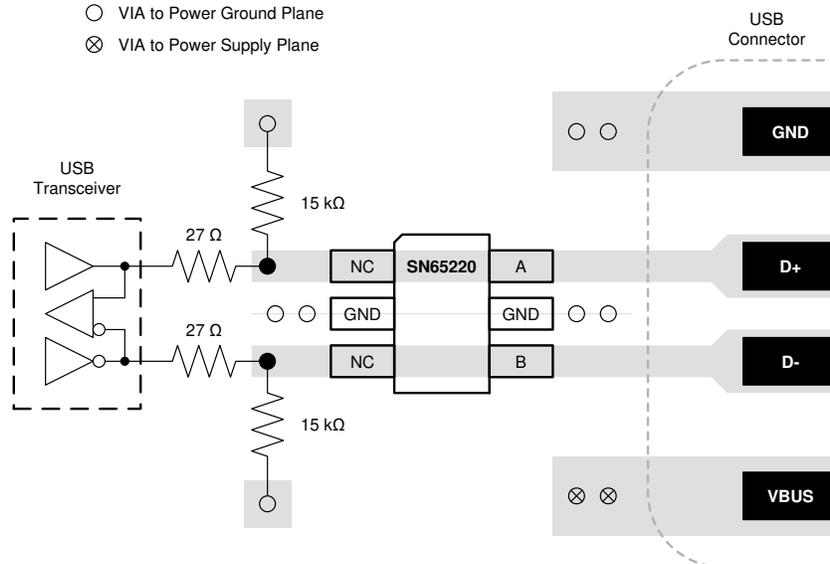


Figure 12-1. Layout Example of a 4-Layer Board With SN65220

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 13-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65220	<a href="#">Click here</a>				
SN65240	<a href="#">Click here</a>				
SN75240	<a href="#">Click here</a>				

### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65220DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI	<a href="#">Samples</a>
SN65220DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI	<a href="#">Samples</a>
SN65220DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI	<a href="#">Samples</a>
SN65220DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI	<a href="#">Samples</a>
SN65240P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65240P	<a href="#">Samples</a>
SN65240PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65240P	<a href="#">Samples</a>
SN65240PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240	<a href="#">Samples</a>
SN65240PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240	<a href="#">Samples</a>
SN65240PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240	<a href="#">Samples</a>
SN65240PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240	<a href="#">Samples</a>
SN75240P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75240P	<a href="#">Samples</a>
SN75240PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A75240	<a href="#">Samples</a>
SN75240PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A75240	<a href="#">Samples</a>
SN75240PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A75240	<a href="#">Samples</a>
SN75240PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A75240	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN65220 :**

- Automotive : [SN65220-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

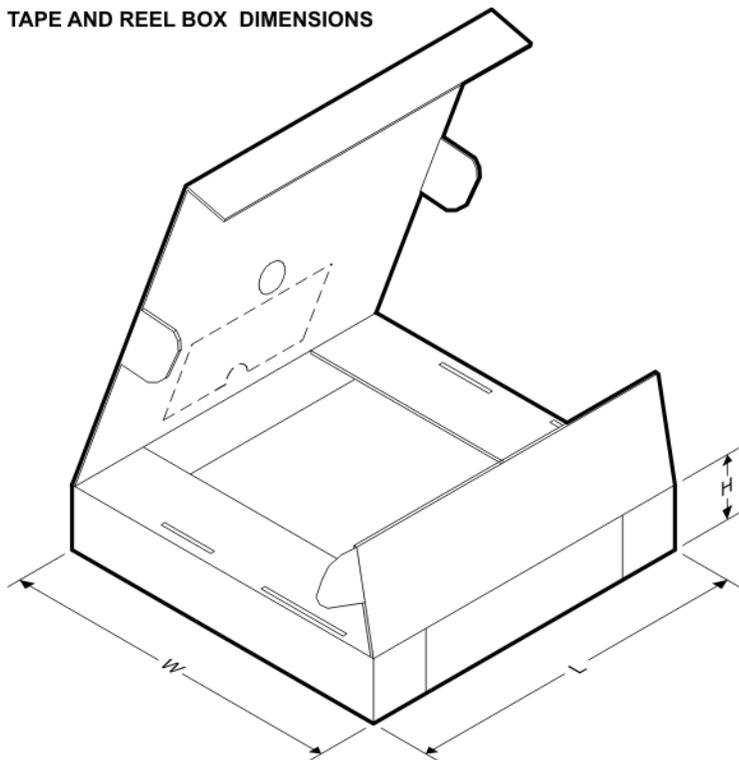
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65220DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN65220DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN65240PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN75240PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65220DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN65220DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN65240PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
SN75240PWR	TSSOP	PW	8	2000	853.0	449.0	35.0

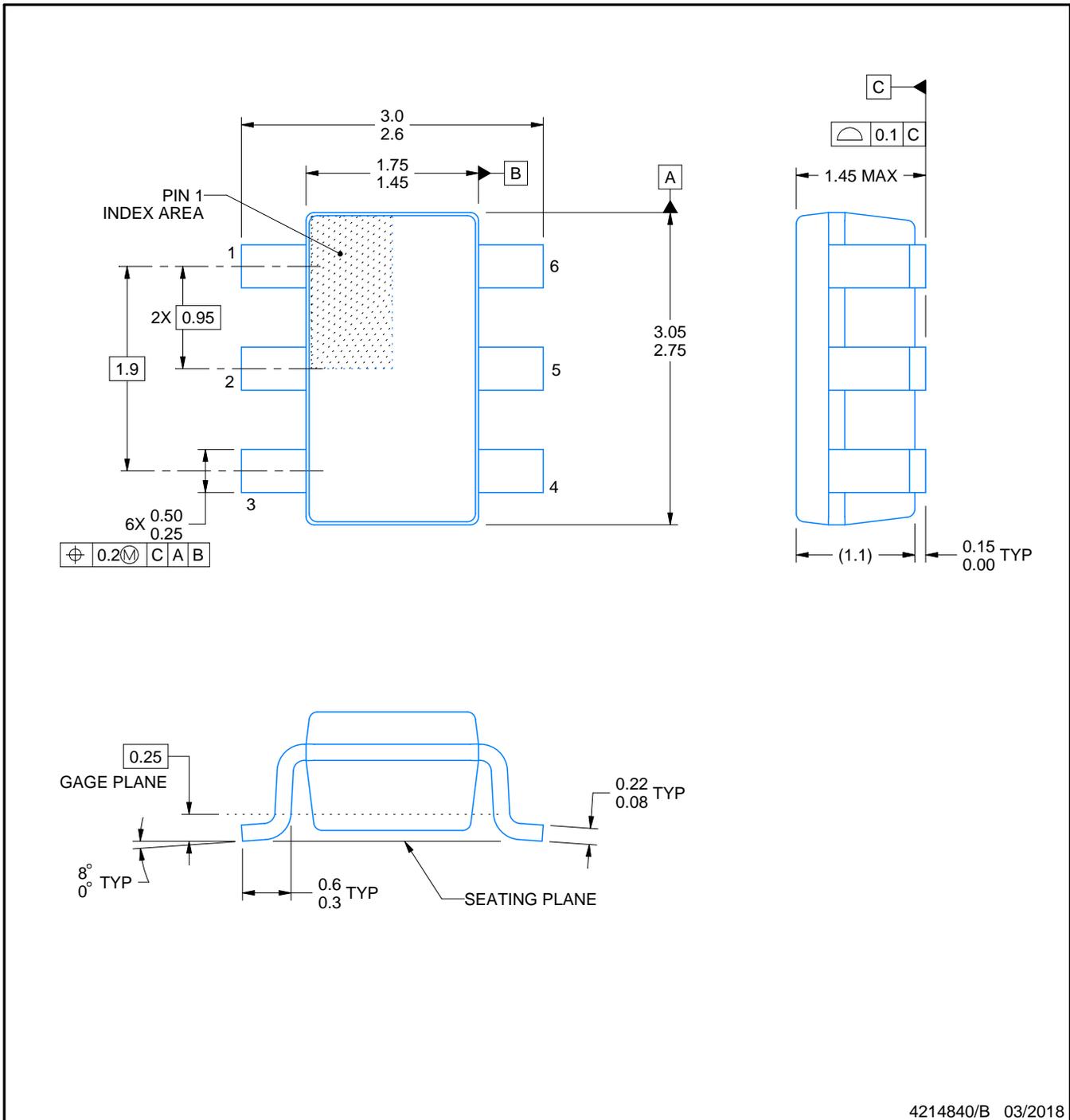
DBV0006A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/B 03/2018

NOTES:

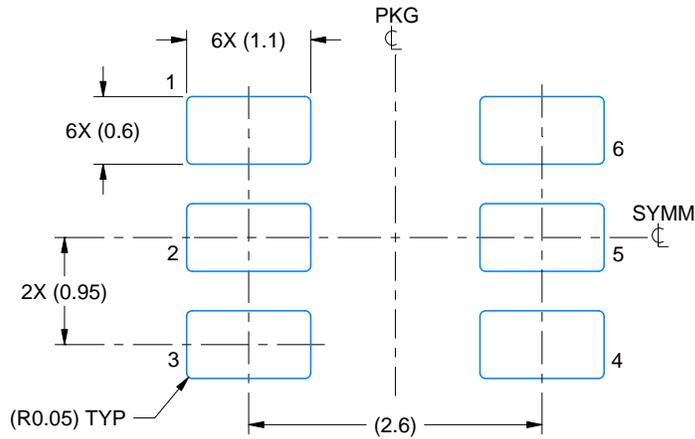
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

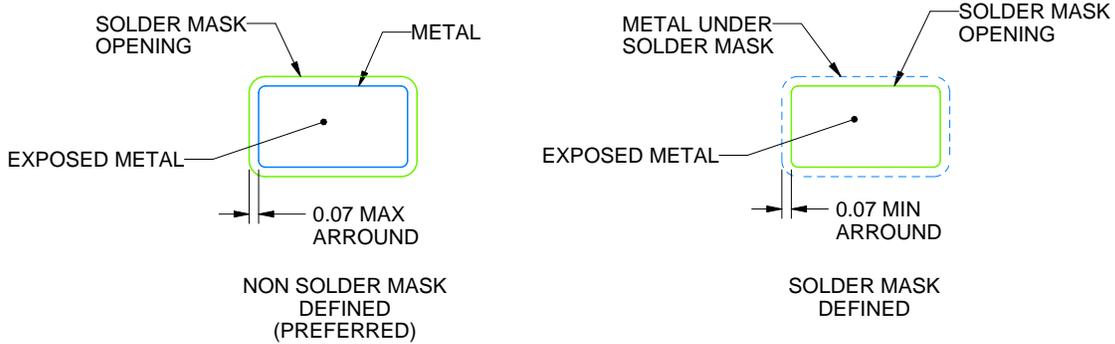
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

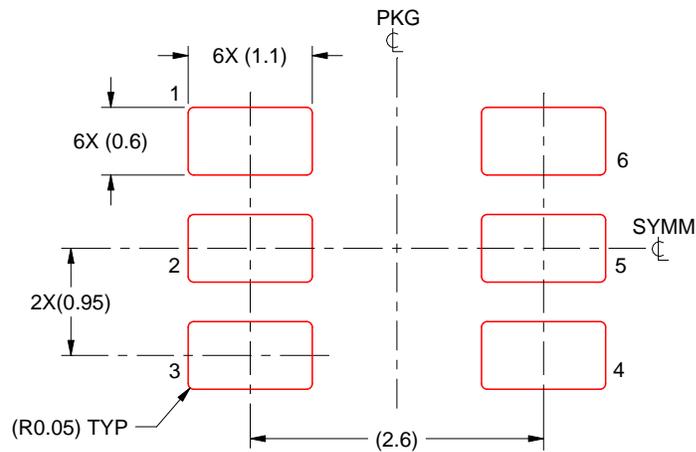
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

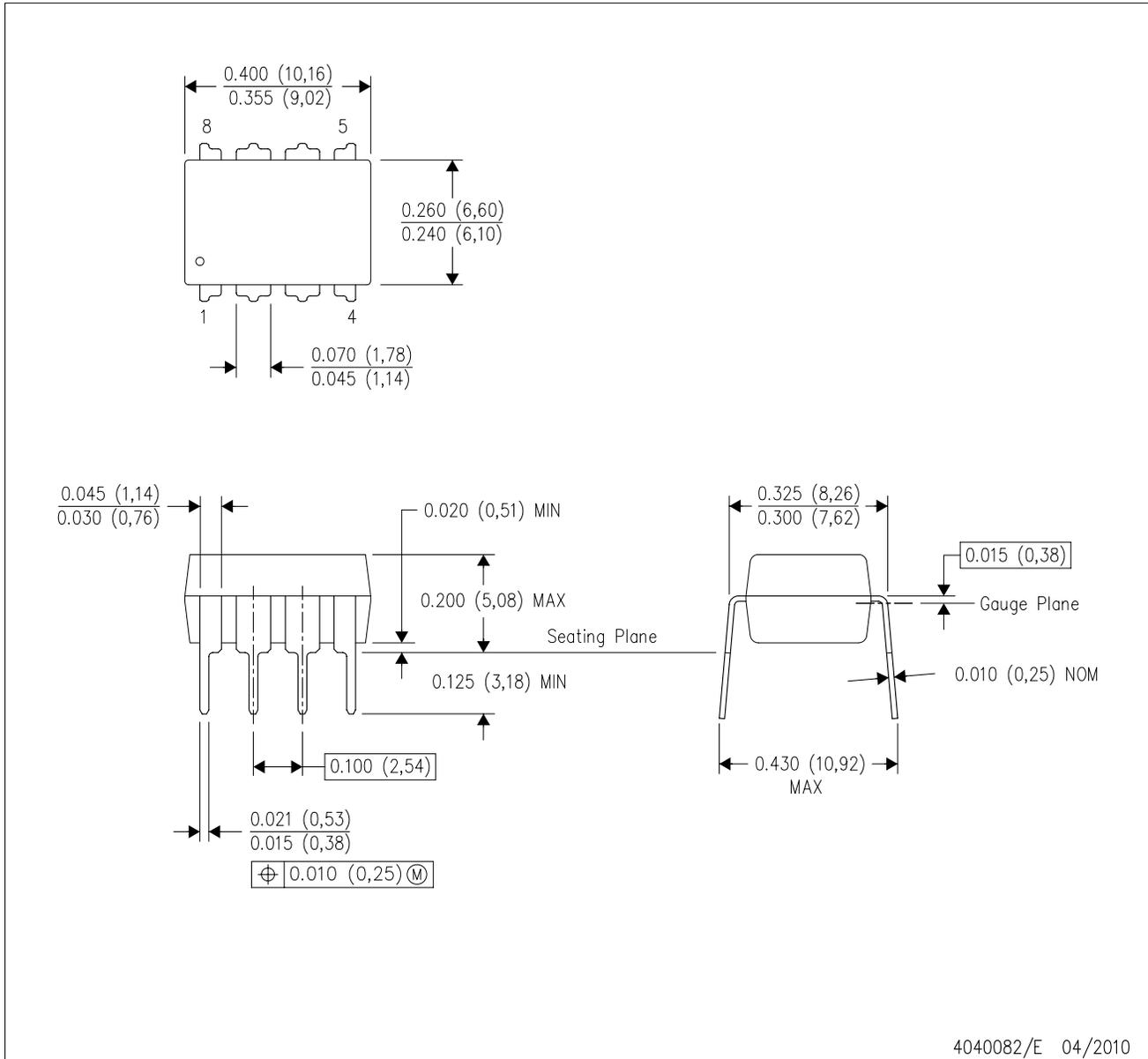
4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

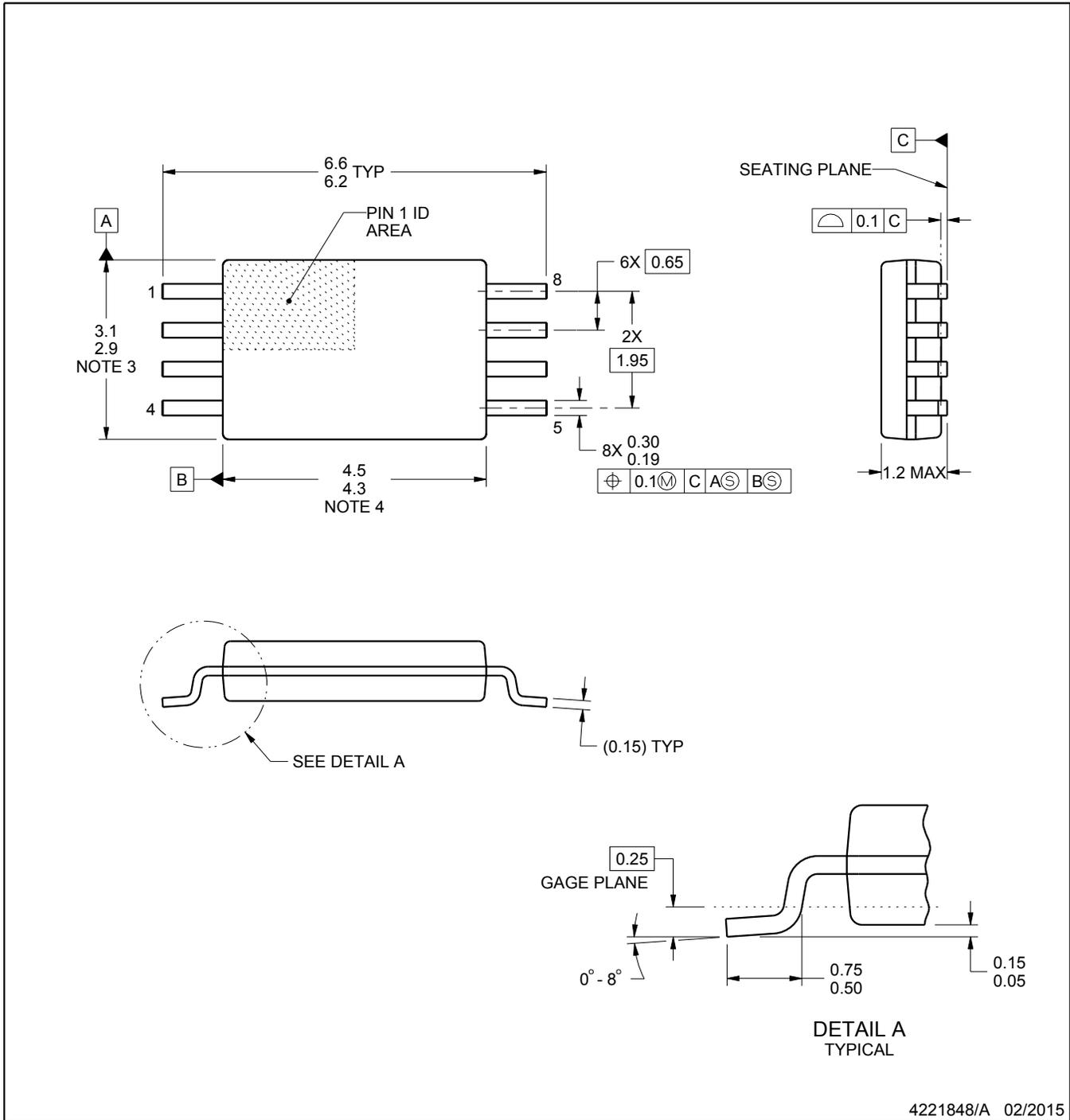
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

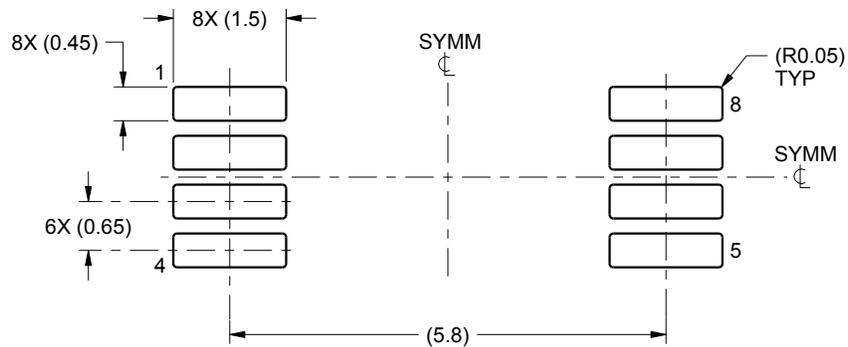
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

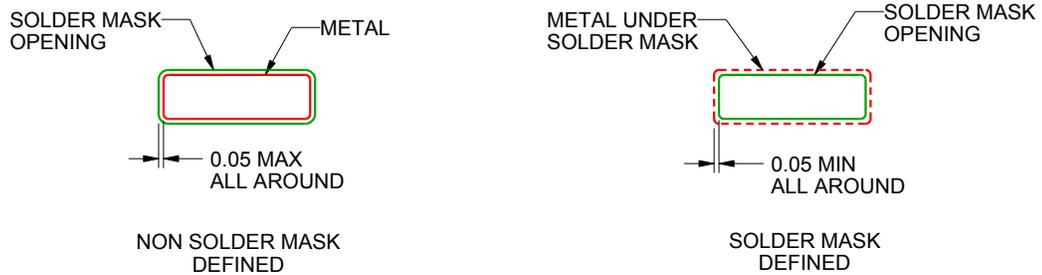
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

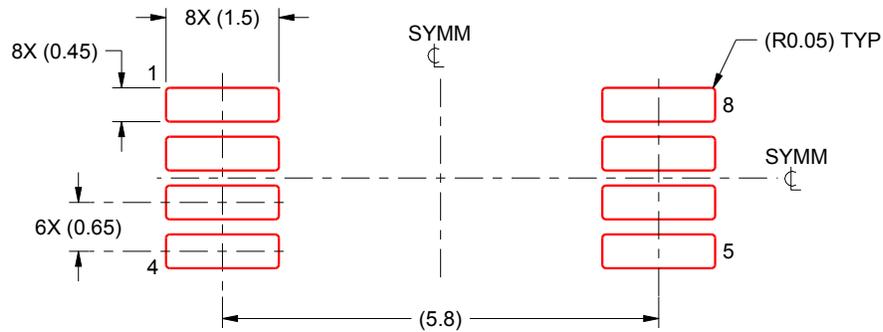
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated