具有显性状态超时且支持故障保护功能的 TLIN2029-Q1 局域互联网络 (LIN) 收发器

1 特性

- 符合面向汽车 标准
  - 温度等级 1：–40°C 至 125°C T_A
  - 器件 HBM 认证等级：±8kV
  - 器件 CDM 认证等级：±1.5kV
- 符合 LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2 A 和 ISO/DIS 17987–4.2 标准
- 符合适用于 LIN 的 SAE J2602 推荐实践的要求
- 支持 24V 应用
- LIN 传输数据速率高达 20kbps
- 宽工作范围
  - 4V 至 48V 电源电压
  - ±60V LIN 总线故障保护
- 休眠模式：超低电流消耗允许以下类型的唤醒事件：
  - LIN 总线
  - 通过 EN 引脚进行的本地唤醒
- 上电和断电无干扰运行
- 保护 特性：
  - V_{SUP} 欠压保护
  - TXD 显性超时 (DTO) 保护
  - 热关断保护
  - 系统级未供电节点或接地断开失效防护。
- 采用 SOIC (8) 和无引线 VSON (8) 封装，提高了自动光学检测 (AOI) 能力

2 应用

- 车身电子装置和照明
- 信息娱乐系统和仪表组
- 混合动力电动汽车和动力总成系统
- 被动安全
- 电器

3 说明

TLIN2029-Q1 是一款局域互联网络 (LIN) 物理层收发器，具有集成的唤醒和保护 功能，符合 LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2 A 和 ISO/DIS 17987–4.2 标准。LIN 是一根单线制双向总线，通常用于低速车载网络，数据传输速率高达 20kbps。TLIN2029-Q1 专为支持 24V 应用设计， 具有更宽的工作电压和额外的总线故障保护。LIN 接收器支持高达 100kbps 的数据传输速率，以更快速地执行内联编程。TLIN2029-Q1 使用一个可降低电磁辐射 (EME) 的限流波形整形驱动器将 TXD 输入上的 LIN 协议数据流转化为 LIN 总线信号。接收器将数据流转化为逻辑电平信号，此信号通过开漏 RXD 引脚发送到微处理器。休眠模式可实现超低电流消耗，允许通过 LIN 总线或引脚实现唤醒。

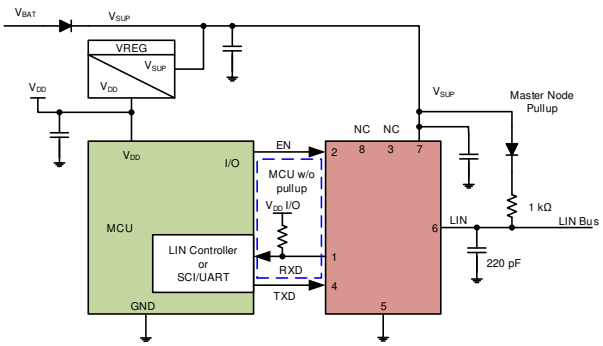
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLIN2029-Q1	SOIC (D) (8)	4.90mm x 3.91mm
	VSON (DRB) (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

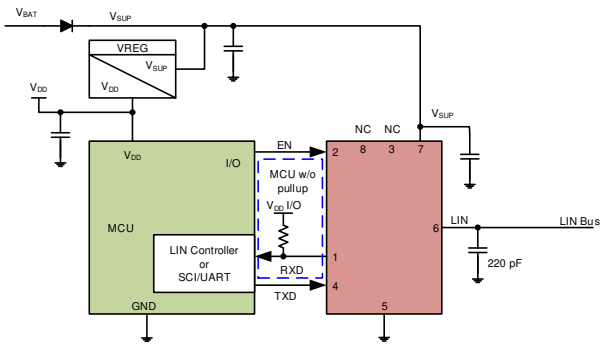
中的 220pF 电容器更改为 200pF 中的 200pF 电容器更改为 220pF

简化原理图，主模式



中的 220pF 电容器更改为 200pF 中的 200pF 电容器更改为 220pF

简化原理图，从模式



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4 说明 （续）

集成电阻器、静电放电 (ESD) 和故障保护功能有助于设计人员节约 应用中的布板空间。

5 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (July 2019) to Revision D **Page**

- 将特性中的“±58V LIN 总线故障保护”更改为“±60V LIN 总线故障保护” 1
- 将*简化原理图，主模式* 1
- 将*简化原理图，从模式* 1
- Changed V_{LIN} from MIN = –58, MAX = 58 To: MIN = –60, MAX = 60 in the Absolute Maximum Ratings 5
- Changed C_{LINPIN} from MAX = 45 pF To: MAX = 25 pF and added V_{SUP} = 14 V for Test Condition in Electrical Characteristics 7
- Changed text From: "For slave applications a 200 pF capacitor" To: "For slave applications a 220 pF capacitor" For Pin 6 (LIN) in the *Layout Guidelines* 27

Changes from Revision B (February 2018) to Revision C **Page**

- 将*器件信息* 中的 SOIC 封装尺寸从 4.90mm x 6.00mm 更改为 4.90mm x 3.9mm 1
- 将*简化原理图，主模式* 1
- 将*简化原理图，从模式* 1
- Changed V_{LOGIC} absolute maximum rating MAX from 5.5 V to 6 V 5
- Changed the title of 图 24 To: Recessive to Dominant Propagation 26
- Changed the title of 图 25 To: Dominant to Recessive Propagation 26
- Changed text From: "For slave applications a 220 pF capacitor" To: "For slave applications a 200 pF capacitor" For Pin 6 (LIN) in the *Layout Guidelines* 27

Changes from Revision A (December 2017) to Revision B **Page**

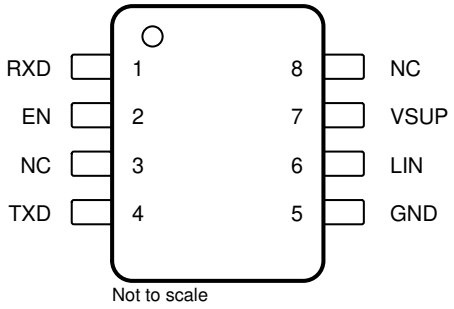
- 将“投诉 LIN 2.0...” 更改为“符合 LIN 2.0...”，位置为 *特性* 和*说明* 1
- Changed From: "complaint to LIN 2.0..." To: "compliant to LIN 2.0..." in the *Overview* section 19

Changes from Original (October 2017) to Revision A **Page**

- 将器件状态从“*预告信息*” 更改为“*生产数据*” 1

6 Pin Configuration and Functions

D Package
8-Pin (SOIC)
Top View



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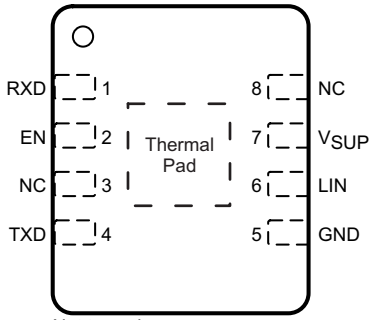
DRB Package
8-Pin (VSON)
Top View



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Pin Functions

PIN		Type	DESCRIPTION
Name	No.		
RXD	1	DO	RXD output (open-drain) interface reporting state of LIN bus voltage
EN	2	DI	Enable input - High put the device in normal operation mode and low put the device in sleep mode
NC	3	–	Not connected
TXD	4	DI	TXD input interface to control state of LIN output - Internal pulled to ground
GND	5	GND	Ground
LIN	6	HV I/O	LIN bus single-wire transmitter and receiver
V_{SUP}	7	HV Supply	Device supply voltage (connected to battery in series with external reverse blocking diode)
NC	8	–	Not connected
Thermal Pad		GND	Ground and should be soldered (DRB package only)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Symbol	Parameter	MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO/DIS 17987 Param 10)	–0.3	60	V
V_{LIN}	LIN bus input voltage (ISO/DIS 17987 Param 82)	–60	60	V
V_{LOGIC}	Logic pin voltage (RXD, TXD, EN)	–0.3	6	V
T_A	Ambient temperature range	–40	125	°C
T_J	Junction temperature range	–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

ESD Ratings				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) TXD, RXD, EN Pins, per AEC Q100-002(1)		±4000	V
		Human body model (HBM) LIN and V_{SUP} Pin, per AEC Q100-002(2)		±8000	
		Charged device model (CDM), per AEC Q100-011	All terminals	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) LIN bus a stressed with respect to GND.

7.3 ESD Ratings - IEC

ESD and Surge Protection Ratings			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	IEC 61000-4-2 contact discharge	±8000	V
$V_{(ESD)}$	Powered ESD Performance, per SAEJ2962-1(2)	contact discharge	±8000	V
		air-gap discharge	±25000	
ISO 7637-2 and IEC 62215-3 transients according to IBEE LIN EMC test specifications(3) (LIN and V_{SUP})		Pulse 1	–100	V
		Pulse 2	75	V
		Pulse 3a	–150	V
		Pulse 3b	100	V

(1) IEC 61000-4-2 is a system level ESD test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system level configurations may lead to different results
(2) SAEJ2962-1 Testing performed at 3rd party US3 approved EMC test facility, test report available upon request
(3) ISO 7637 is a system level transient test. Different systme level configurations may lead to diffrent results

7.4 Thermal Information

THERMAL METRIC(1)		TLIN2029D D (SOIC) 8-PINS	TLIN2029DRB DRB (VSON) 8-PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	115.5	48.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	58.7	55.5	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	58.9	22.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.1	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.2	22.2	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER - DEFINITION		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	4		48	V
V_{LIN}	LIN Bus input voltage	0		48	V
V_{LOGIC}	Logic Pin Voltage (RXD, TXD, EN)	0		5.25	V
TSD	Thermal shutdown temperature	165			°C
$TSD_{(HYS)}$	Thermal shutdown hysteresis		15		°C

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10, 53)	Device is operational beyond the LIN defined nominal supply voltage range See 图 1 and 图 2	4		48	V
V_{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10, 53)	Normal and Standby Modes: ramp V_{SUP} while LIN signal is a 10 kHZ square wave with 50 % duty cycle and 36V swing. See 图 1 and 图 2	4		48	V
		Sleep Mode	4		48	V
UV_{SUP}	Under voltage V_{SUP} threshold	Min is falling edge and Max is rising edge	2.9		3.85	V
UV_{HYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.2		V
I_{SUP}	Supply current	Normal Mode: EN = high, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF (See 图 7)		1.2	5	mA
		Standby Mode: EN = low, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF (See 图 7)		1	2.1	mA
I_{SUP}	Supply current	Normal Mode: EN = high, bus recessive: LIN = VSUP,		400	700	µA
		Standby Mode: EN = low, bus recessive: LIN = VSUP,		20	35	µA
		Sleep Mode: 4.0 V < VSUP ≤ 27 V, LIN = VSUP, EN = 0 V, TXD and RXD floating		9	15	µA
		Sleep Mode: 27 V < VSUP ≤ 48 V, LIN = VSUP, EN = 0 V, TXD and RXD floating			30	µA
TSD	Thermal shutdown		165			℃
$TSD_{(HYS)}$	Thermal shutdown hysteresis			15		℃
RXD OUTPUT PIN (OPEN DRAIN)						
V_{OL}	Output low voltage	Based upon external pull-up to V_{CC}			0.6	V
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{ILG}	Leakage current, high-level	LIN = V_{SUP}, RXD = 5 V	–5	0	5	µA
TXD INPUT PIN						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{ILG}	Low level input leakage current	TXD = low	–5	0	5	µA
R_{TXD}	Interal pull-down resitor value		125	350	800	kΩ
LIN PIN						

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	HIGH level output voltage	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 7 V to 48 V	0.85			V_{SUP}
		LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 4 V ≤ V_{SUP} < 7 V	3			V
V_{OL}	LOW level output voltage	LIN dominant, TXD = low, V_{SUP} = 7 V to 48 V			0.2	V_{SUP}
		LIN dominant, TXD = low, V_{SUP} = 4 V ≤ V_{SUP} < 7 V			1.2	V
$V_{SUP\_NON\_OP}$	VSUP where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11, 54/56)	TXD& RXD open LIN = 4 V to 58 V	–0.3		58	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12, 57)	TXD = 0 V, V_{LIN} = 36 V, R_{MEAS} = 440 Ω, V_{SUP} = 36 V, V_{BUSdom} < 4.518 V See 图 6	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13, 58)	LIN = 0 V, V_{SUP} = 24 V Driver off/recessive 图 7	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14, 59)	LIN > V_{SUP}, 4 V ≤ V_{SUP} ≤ 45 V Driver off; 图 8			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14, 59)	LIN = V_{SUP}, Driver off; 图 8	–5		5	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15, 60)	GND = V_{SUP}, V_{SUP} = 27 V, LIN = 0 V; 图 9	–1		1	mA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15, 60)	GND = V_{SUP}, V_{SUP} ≥ 36 V, LIN = 0 V; 图 9	–1.5		1.5	mA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16, 61)	LIN = 48 V, V_{SUP} = GND; 图 10			5	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17, 62)	LIN dominant (including LIN dominant for wake up) See 图 4, 图 3			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18, 63)	Lin recessive See 图 4, 图 3	0.6			V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19, 64)	V_{BUS_CNT} = (V_{IL} + V_{IH})/2 See 图 4, 图 3	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20, 65)	V_{HYS} = (V_{IL} - V_{IH}) See 图 4, 图 3			0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path	By design and characterization	0.4	0.7	1	V
R_{SLAVE}	Internal pull-up resistor to V_{SUP}	Normal and standby modes	20	45	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 27 V, LIN = GND	–2		–20	µA
C_{LINPIN}	Capacitance of the LIN pin	V_{SUP} = 14 V			25	pF
EN INPUT PIN						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
V_{IT}	Hysteresis voltage	By design and characterization		50	500	mV
I_{ILG}	Low level input current	EN = low	–5	0	5	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)(1)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 图 11, 图 12)	0.396			
$D1_{12V}$	Duty Cycle 1	$TH_{REC(MAX)}$ = 0.625 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 图 11, 图 12)	0.396			
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4.6 V to 18 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See 图 11, 图 12)			0.581	
$D3_{12V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 图 11, 图 12)	0.417			
$D3_{12V}$	Duty Cycle	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 图 11, 图 12)	0.417			
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 4.6 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See 图 11, 图 12)			0.59	
$D1_{24V}$	Duty Cycle 1 (ISO/DIS 17987 Param 72)(1)	$TH_{REC(MAX)}$ = 0.710 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.544 x V_{SUP}, V_{SUP} = 15 V to 36 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 图 11, 图 12)	0.33			
$D2_{24V}$	Duty Cycle 2 (ISO/DIS 17987 Param 73)	$TH_{REC(MAX)}$ = 0.446 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.302 x V_{SUP}, V_{SUP} = 15.6 V to 36 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See 图 11, 图 12)			0.642	
$D3_{24V}$	Duty Cycle 3 (ISO/DIS 17987 Param 74)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 36 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 图 11, 图 12)	0.386			
$D3_{24V}$	Duty Cycle	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 图 11, 图 12)	0.386			
$D4_{24V}$	Duty Cycle 4 (ISO/DIS 17987 Param 75)	$TH_{REC(MIN)}$ = 0.442 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4.6 V to 36 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See 图 11, 图 12)			0.591	

(1) Duty cycles: LIN driver bus load conditions (CLINBUS, RLINBUS): Load1 = 1 nF, 1 kΩ; Load2 = 10 nF, 500 Ω. Duty cycles 3 and 4 are defined for 10.4-kbps operation. The TLIN1029 also meets these lower data rate requirements, while it is capable of the higher speed 20-kbps operation as specified by duty cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAEJ2602 specification

7.8 Timing Requirements

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{rx_pdr}, t_{rx_pdf}	Receiver rising propagation delay time (ISO/DIS 17987 Param 31, 76)	R_{RXD} = 2.4 kΩ, $_{CRX}$D = 20 pF (See 图 13 and 图 14)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time	Rising edge with respect to falling edge, (trx_sym = trx_pdf – trx_pdr), $_{RRX}$D = 2.4 kΩ, $_{CR}$XD = 20 pF (See 图 13 and 图 14)	–2		2	µs
t_{LINBUS}	LIN wakeup time (Minimum dominant time on LIN bus for wakeup)	See 图 17, 图 20, and 图 21)	25	65	150	µs

Timing Requirements (continued)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bust stuck dominant fault)	See 图 21	8	25	50	µs
t_{DST}	Dominant state time out		20	45	80	ms
t_{MODE_CHANGE}	Mode change delay time	Time to change from standby mode to normal mode or normal mode to sleep mode through EN pin: See 图 15 and 图 22	2		15	µs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid See 图 15			35	µs
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms

7.9 Typical Characteristics

8 Parameter Measurement Information

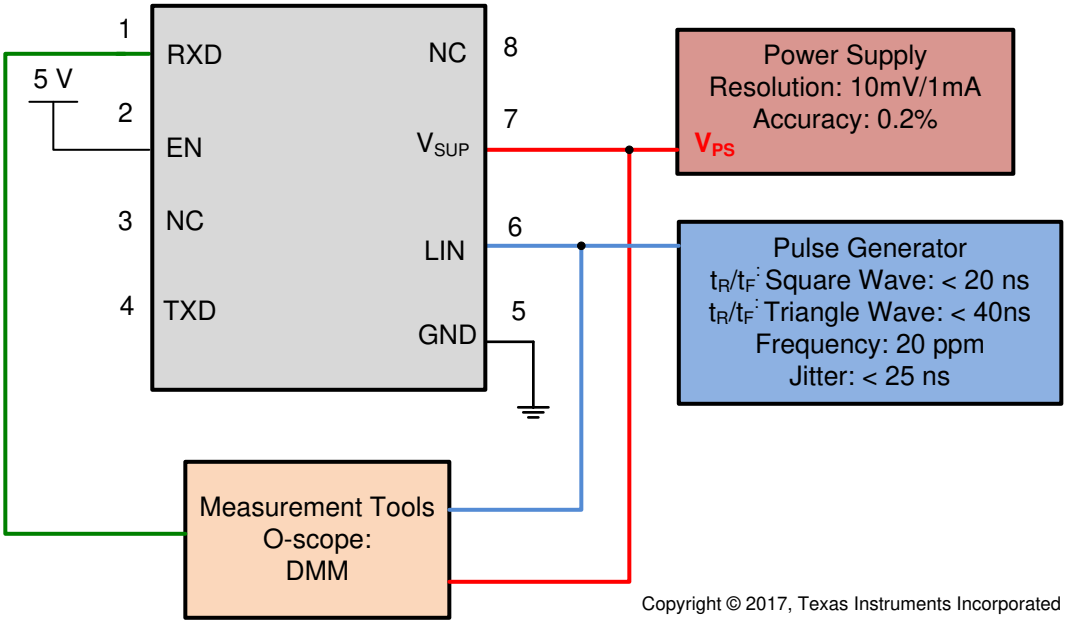


图 1. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10

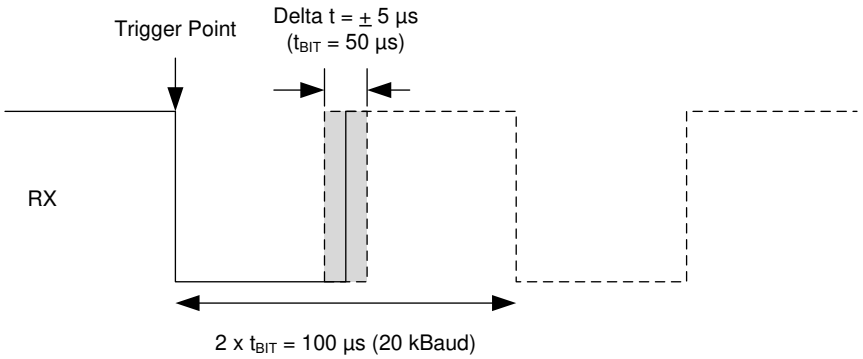


图 2. RX Response: Operating Voltage Range

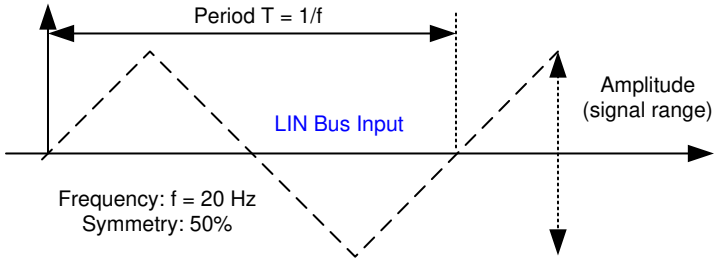


图 3. LIN Bus Input Signal

Parameter Measurement Information (接下页)

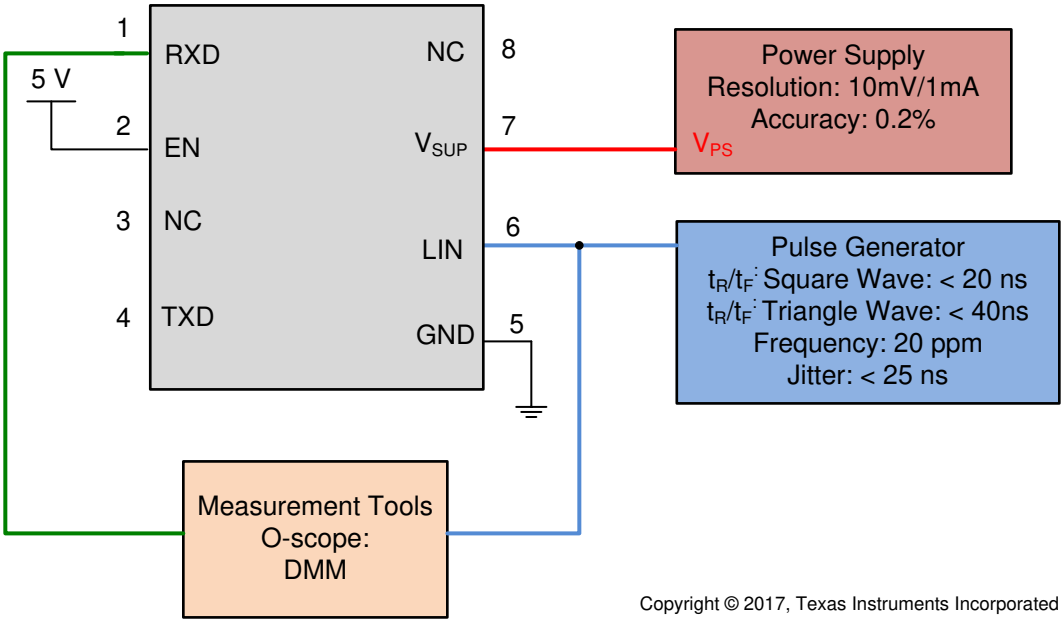


图 4. LIN Receiver Test with RX access Param 17, 18, 19, 20

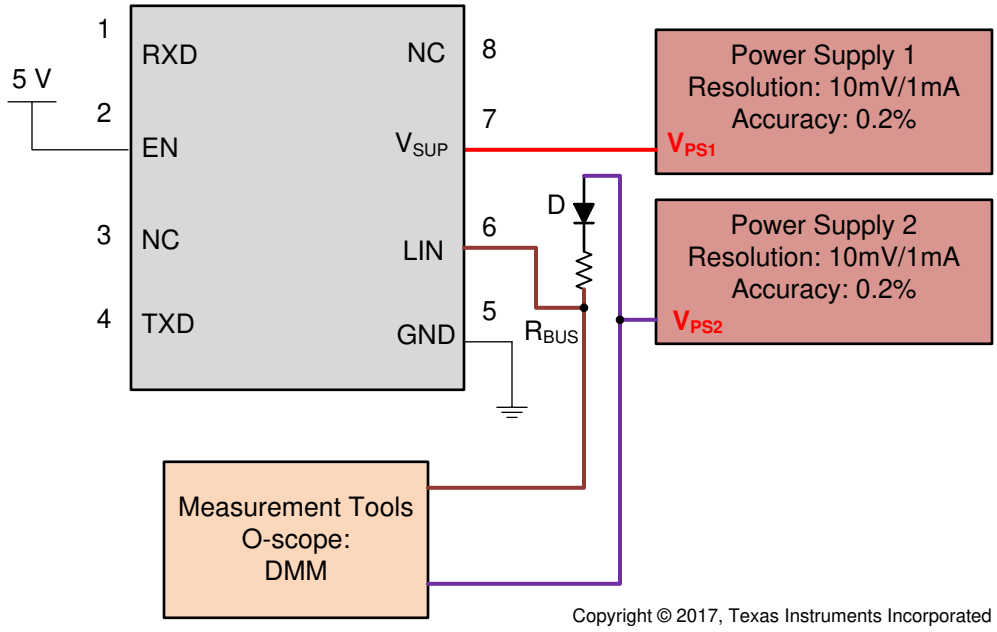


图 5. $V_{SUP\_NON\_OP}$ Param 1154/56

Parameter Measurement Information (接下页)

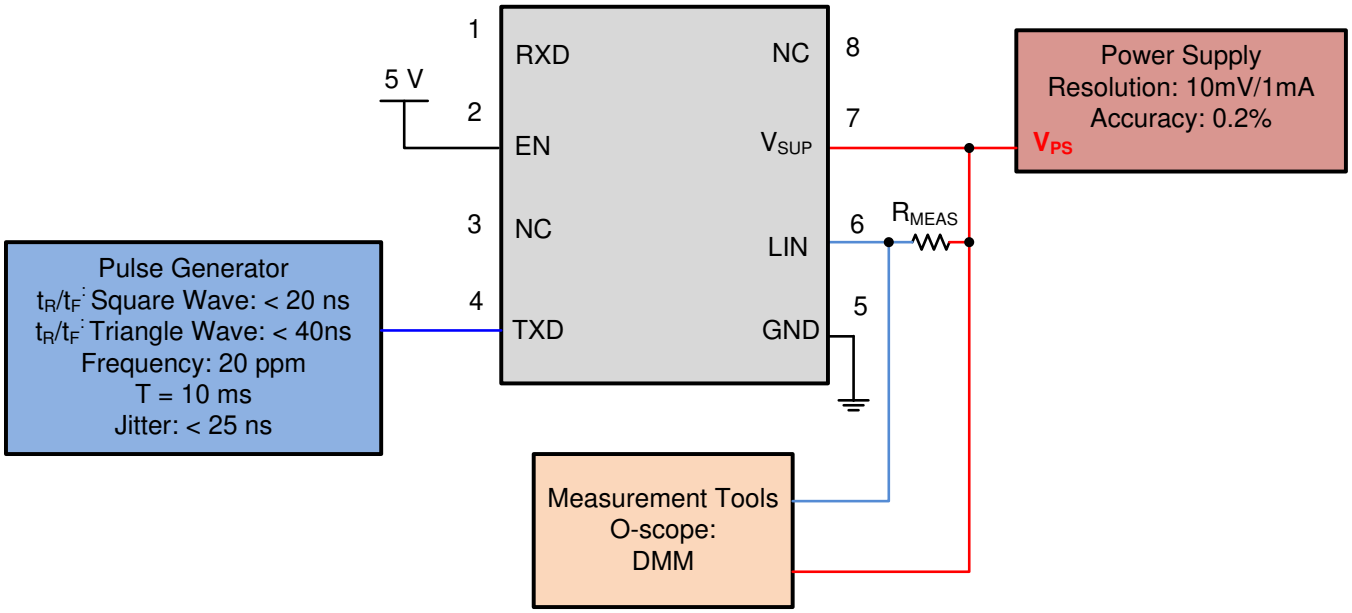


图 6. Test Circuit for I_{BUS_LIM} at Dominant State (Driver on) Param 12

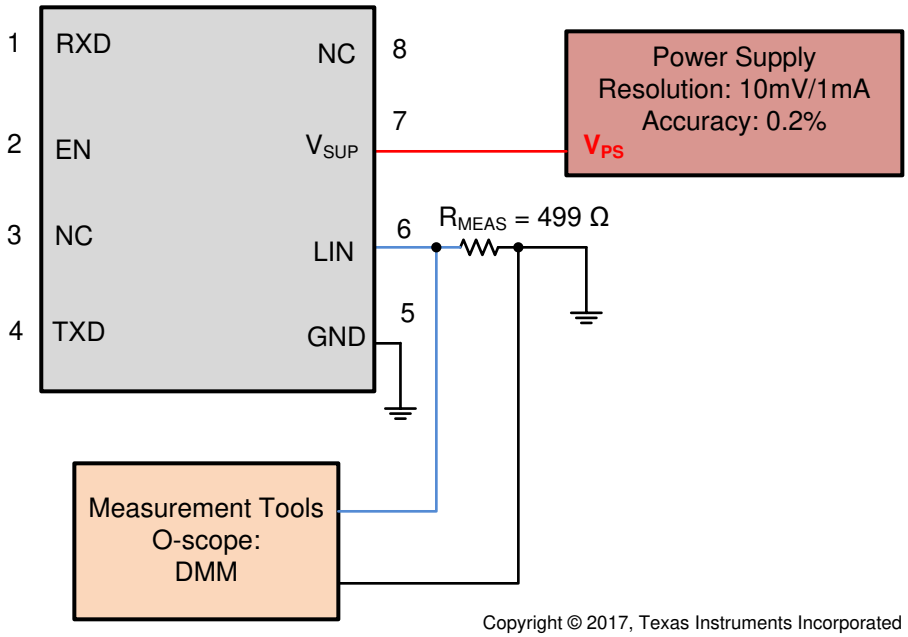


图 7. Test Circuit for $I_{BUS\_PAS\_dom}$; TXD = Recessive State V_{BUS} = 0 V, Param 13

Parameter Measurement Information (接下页)

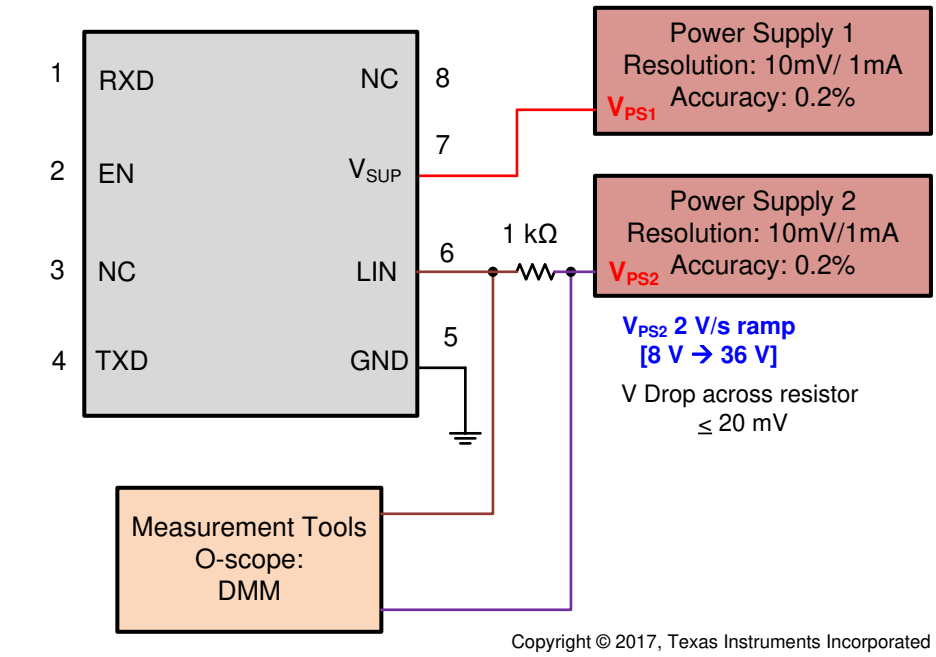


图 8. Test Circuit for $I_{BUS\_PAS\_rec}$ Param 14

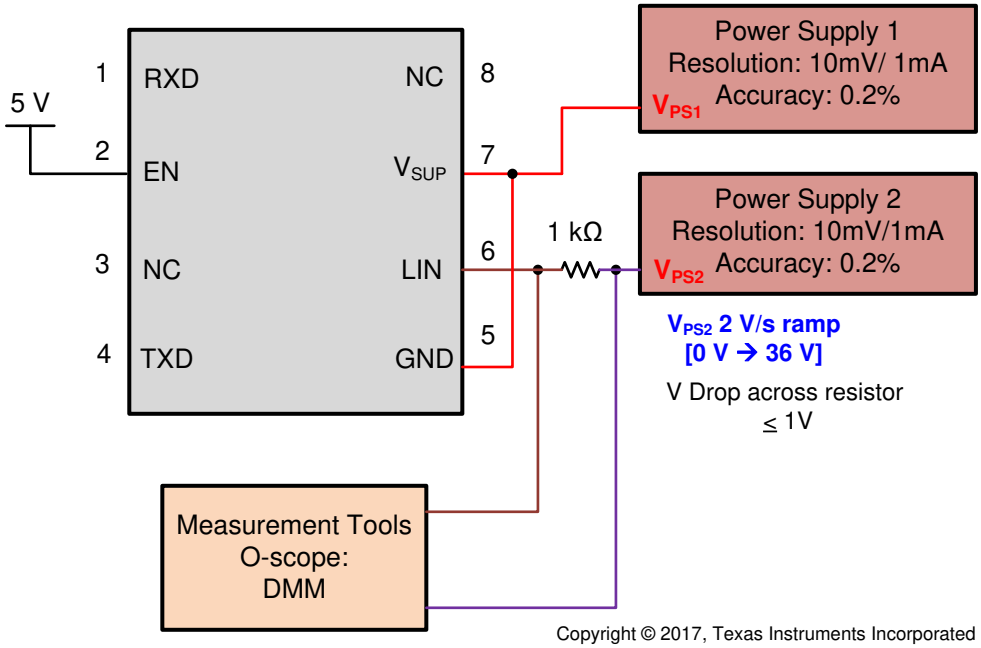


图 9. Test Circuit for $I_{BUS\_NO\_GND}$ Loss of GND

Parameter Measurement Information (接下页)

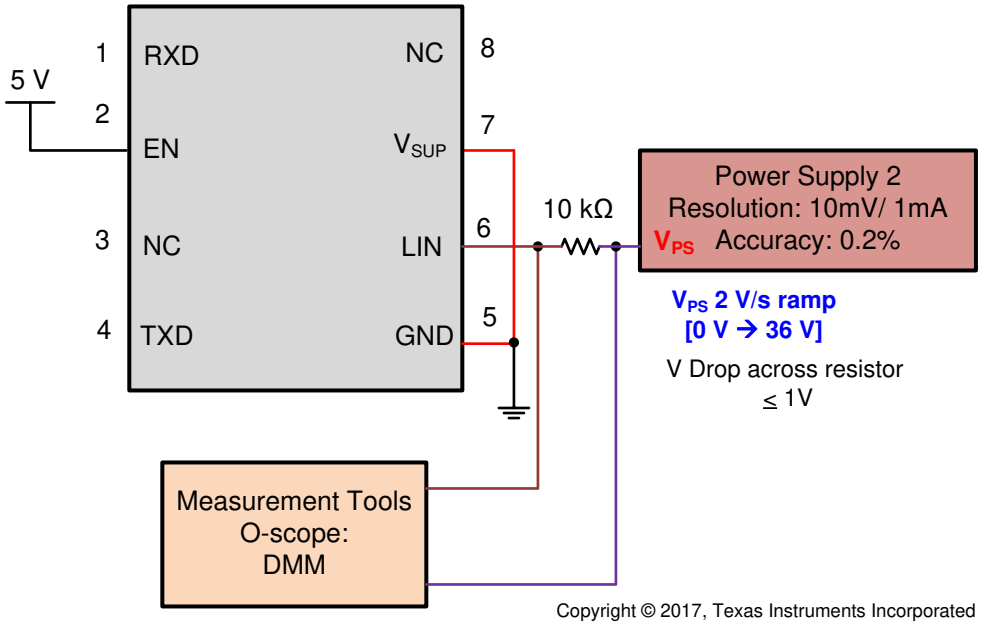


图 10. Test Circuit for $I_{BUS\_NO\_BAT}$ Loss of Battery

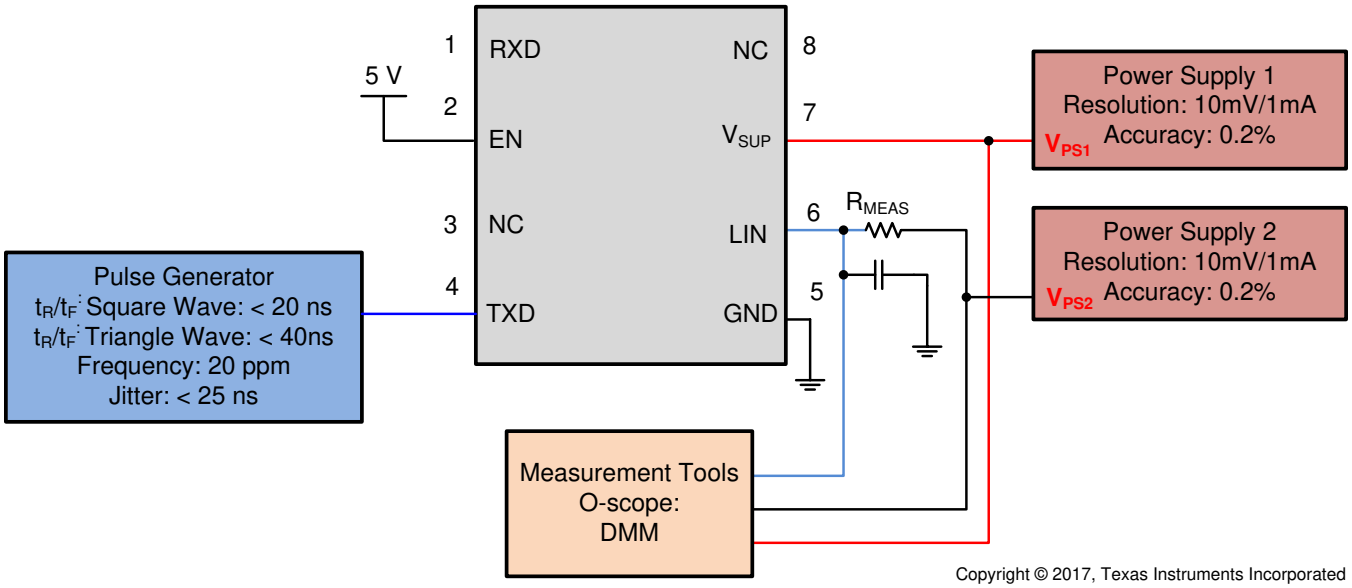


图 11. Test Circuit Slope Control and Duty Cycle Param 27, 28, 29, 30, 72, 73, 74, 75

Parameter Measurement Information (接下页)

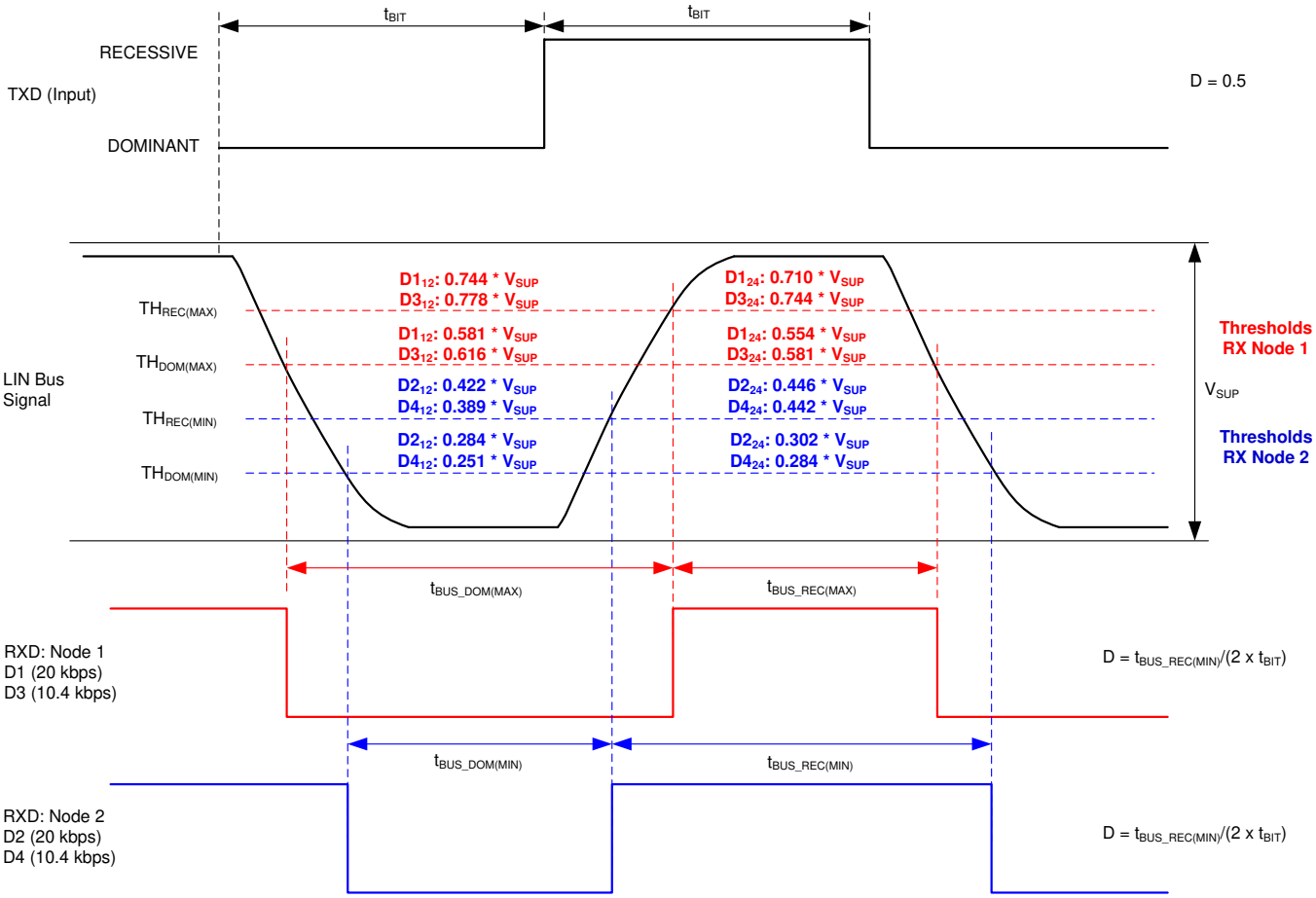


图 12. Definition of Bus Timing Parameters

Parameter Measurement Information (接下页)

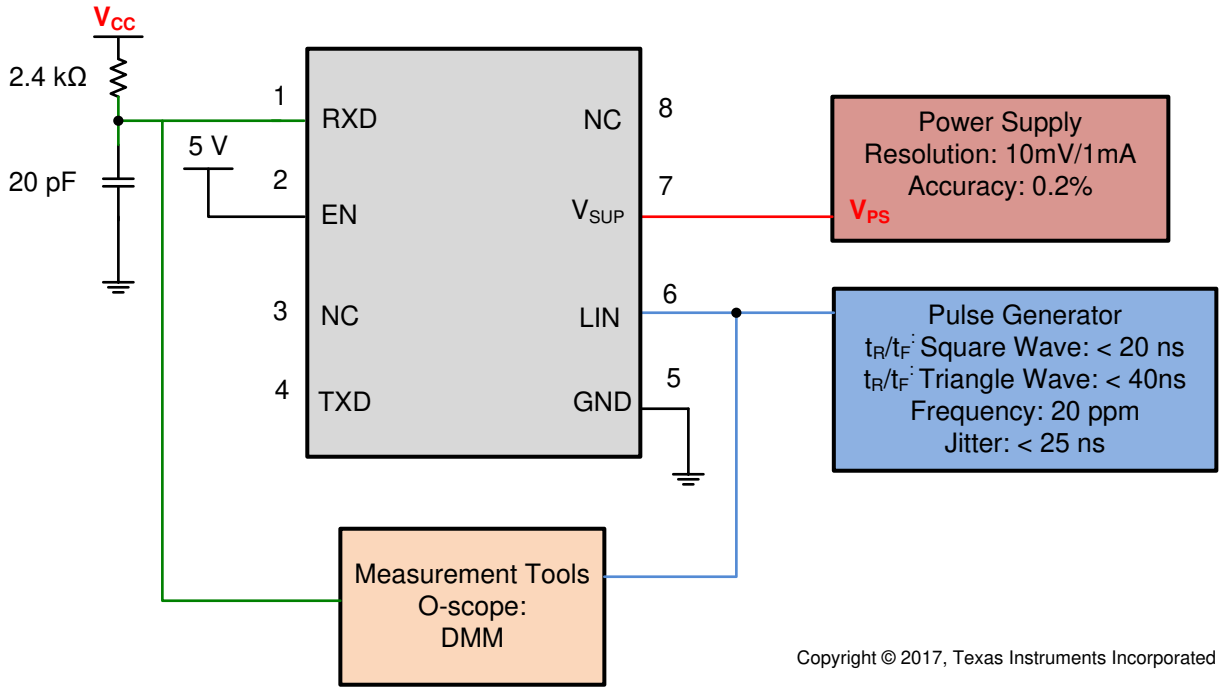


图 13. Propagation Delay Test Circuit; Param 31, 32

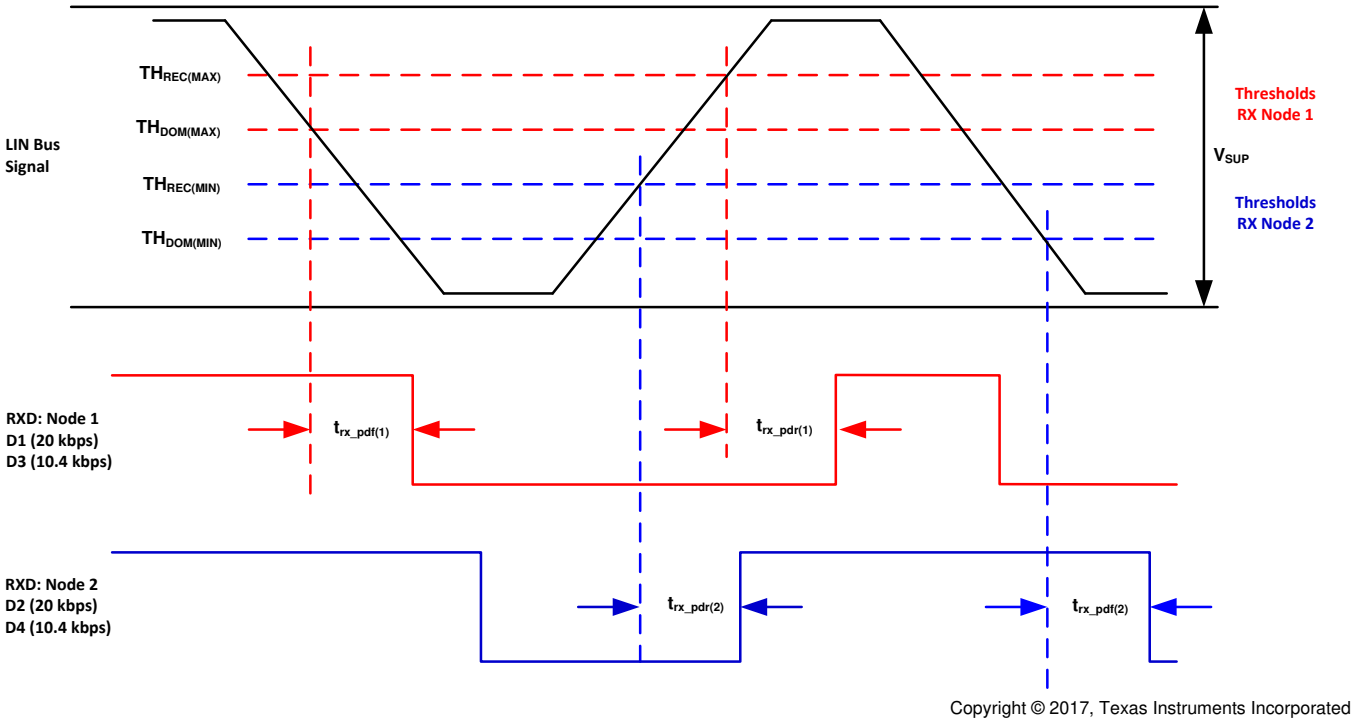


图 14. Propagation Delay

Parameter Measurement Information (接下页)

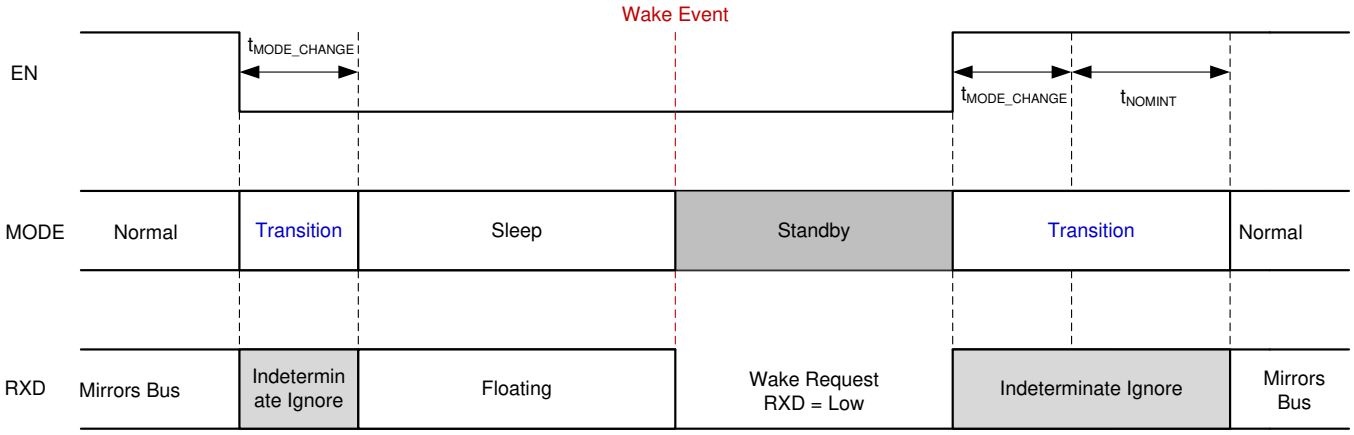


图 15. Mode Transitions

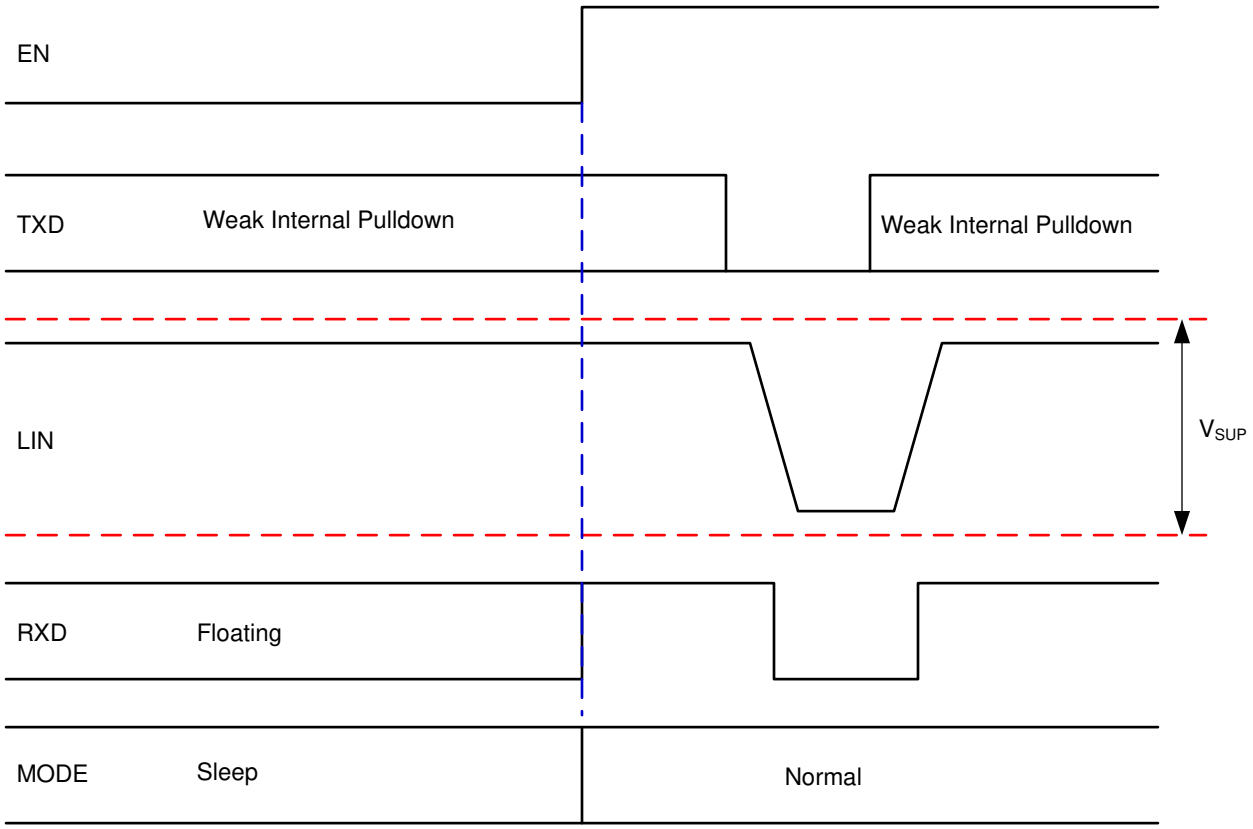


图 16. Wakeup Through EN

Parameter Measurement Information (接下页)

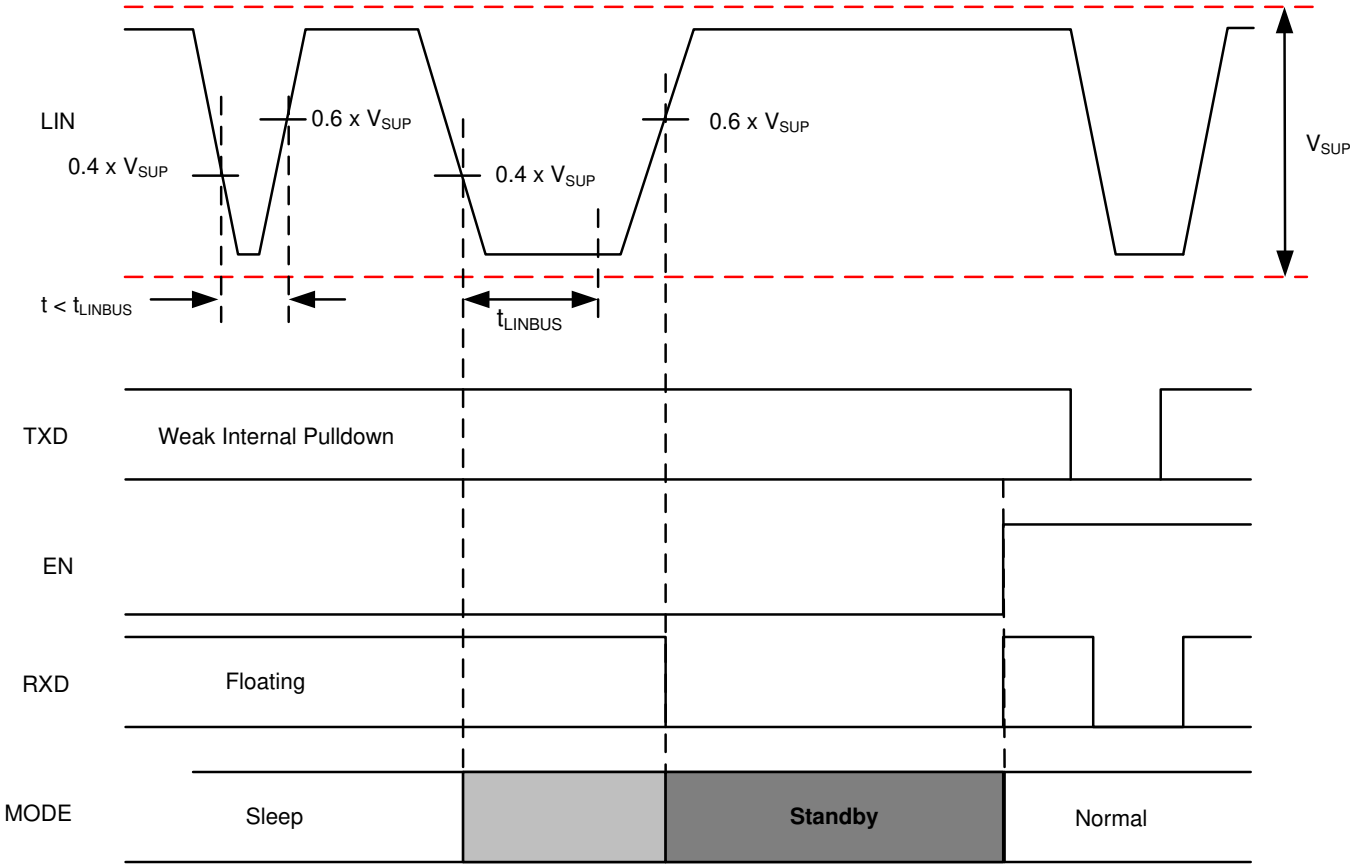


图 17. Wakeup through LIN

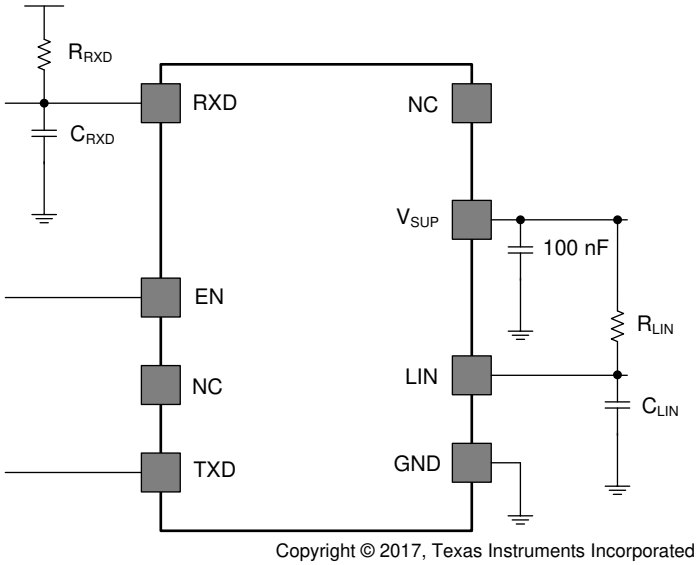


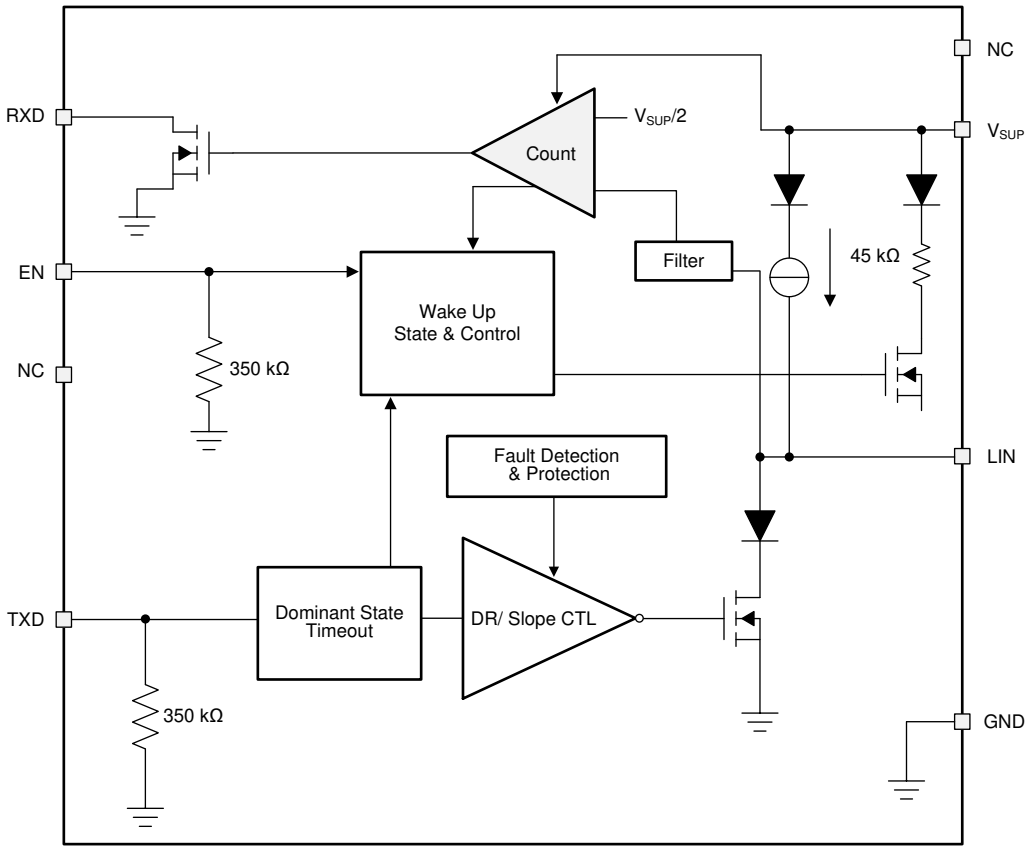
图 18. Test Circuit for AC Characteristics

9 Detailed Description

9.1 Overview

The TLIN2029-Q1 is a Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2 standards, with integrated wake-up and protection features. The LIN bus is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates from 2.4 kbps to 20 kbps. The TLIN2029-Q1 LIN receiver works up to 100 kbps supporting in-line programming. The LIN protocol data stream on the TXD input is converted by the TLIN2029-Q1 into a LIN bus signal using a current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for slave applications. Master applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification. The TLIN2029-Q1 provides many protection features such as immunity to ESD and high bus standoff voltage. The device also provides two methods to wake up: EN pin and from the LIN bus.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 LIN (Local Interconnect Network) Bus

This high voltage input/output pin is a single wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 60 V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

Feature Description (接下页)

9.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shut-down condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a master node application.

9.3.1.2 LIN Receiver Characteristics

The receiver's characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN2029-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pullup resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor (1 kΩ) and a series diode to V_{SUP} must be added when the device is used for master node applications as per the LIN specification.

图 19 shows a Master Node configuration and how the voltage levels are defined

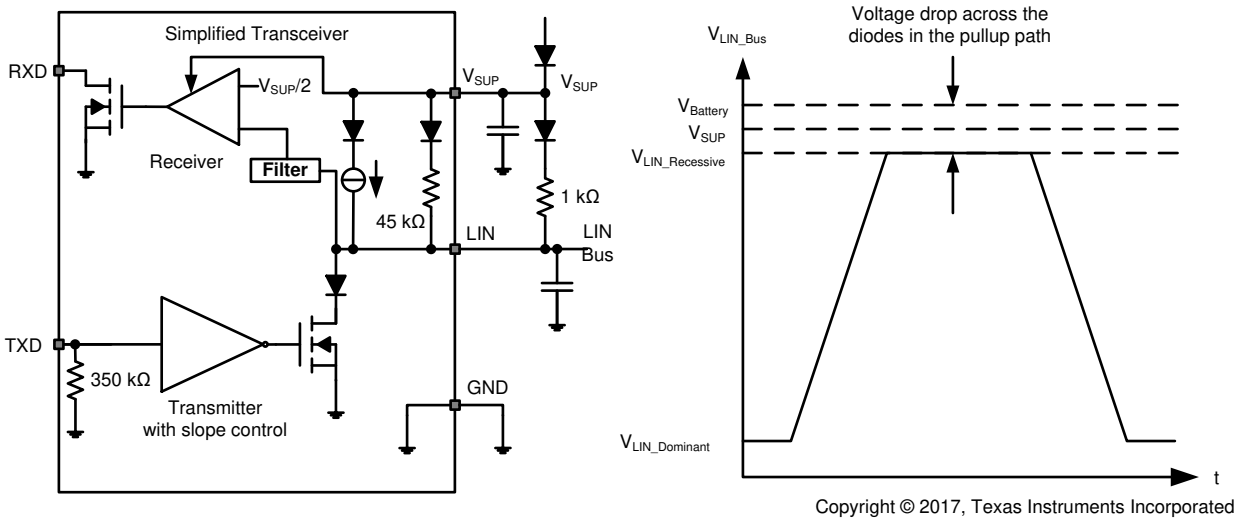


图 19. Master Node Configuration with Voltage Levels

9.3.2 TXD (Transmit Input and Output)

TXD is the interface to the MCU's LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground). When TXD is high the LIN output is recessive (near $V_{Battery}$). See 图 19. The TXD input structure is compatible with microcontrollers with 3.3 V and 5 V I/O. TXD has an internal pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timer-out timer.

Feature Description (接下页)

9.3.3 RXD (Receive Output)

RXD is the interface to the MCU's LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near $V_{Battery}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pullup, an external pullup resistor to the microcontroller I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake up request from the LIN bus.

9.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode (图 19). If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats.

9.3.7 Protection Features

The TLIN2029-Q1 has several protection features that will now be described.

9.3.8 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

9.3.9 Bus Stuck Dominant System Fault: False Wake Up Lockout

The TLIN2029-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake up logic is locked out until a valid recessive on the bus "clears" the bus stuck dominant, preventing excessive current use. 图 20 and 图 21 show the behavior of this protection.

Feature Description (接下页)

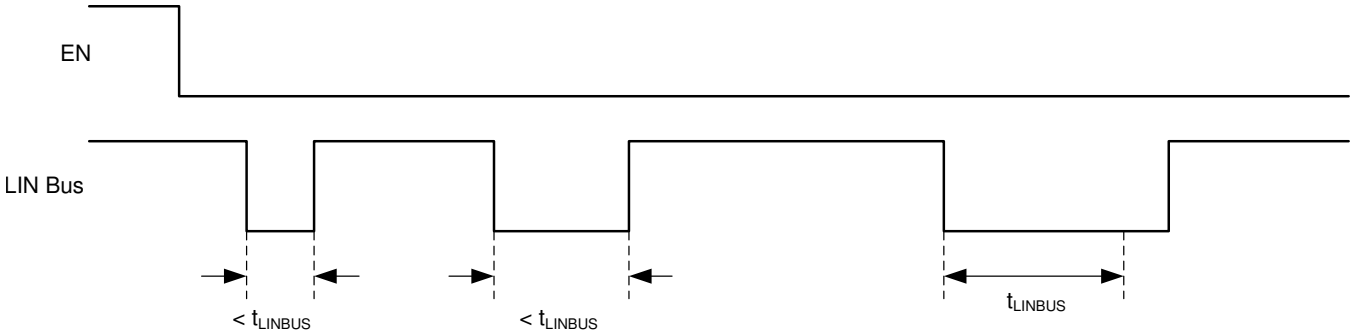


图 20. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

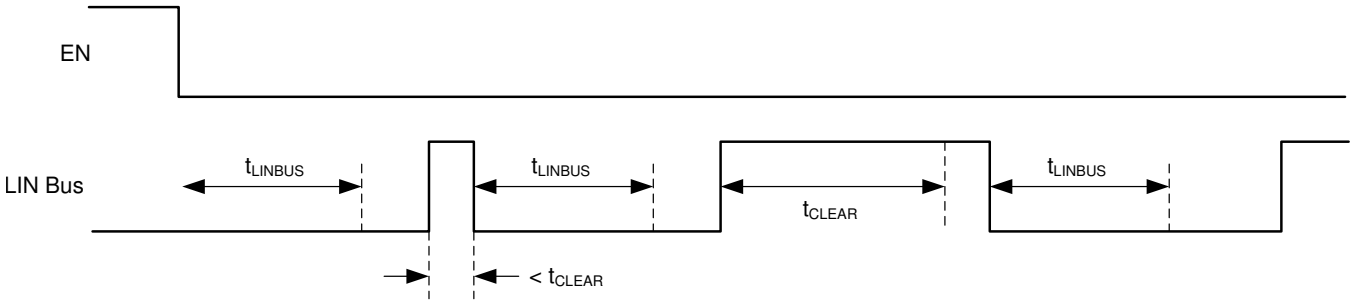


图 21. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

9.3.10 Thermal Shutdown

The LIN transmitter is protected by limiting the current; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pullup termination remains on.

9.3.11 Under Voltage on V_{SUP}

The TLIN2029-Q1 contains a power on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

9.3.12 Unpowered Device and LIN Bus

In automotive applications some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remains powered by the battery. The TLIN2029-Q1 has extremely low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

9.4 Device Functional Modes

The TLIN2029-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections will describe these modes as well as how the device moves between the different modes. 图 22 graphically shows the relationship while 表 1 shows the state of pins.

表 1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Floating	Weak Current Pullup	Off	
Standby	Low	Low	45 kΩ (typical)	Off	Wake up event detected, waiting on MCU to set EN
Normal	High	LIN Bus Data	45 kΩ (typical)	On	LIN transmission up to 20 kbps

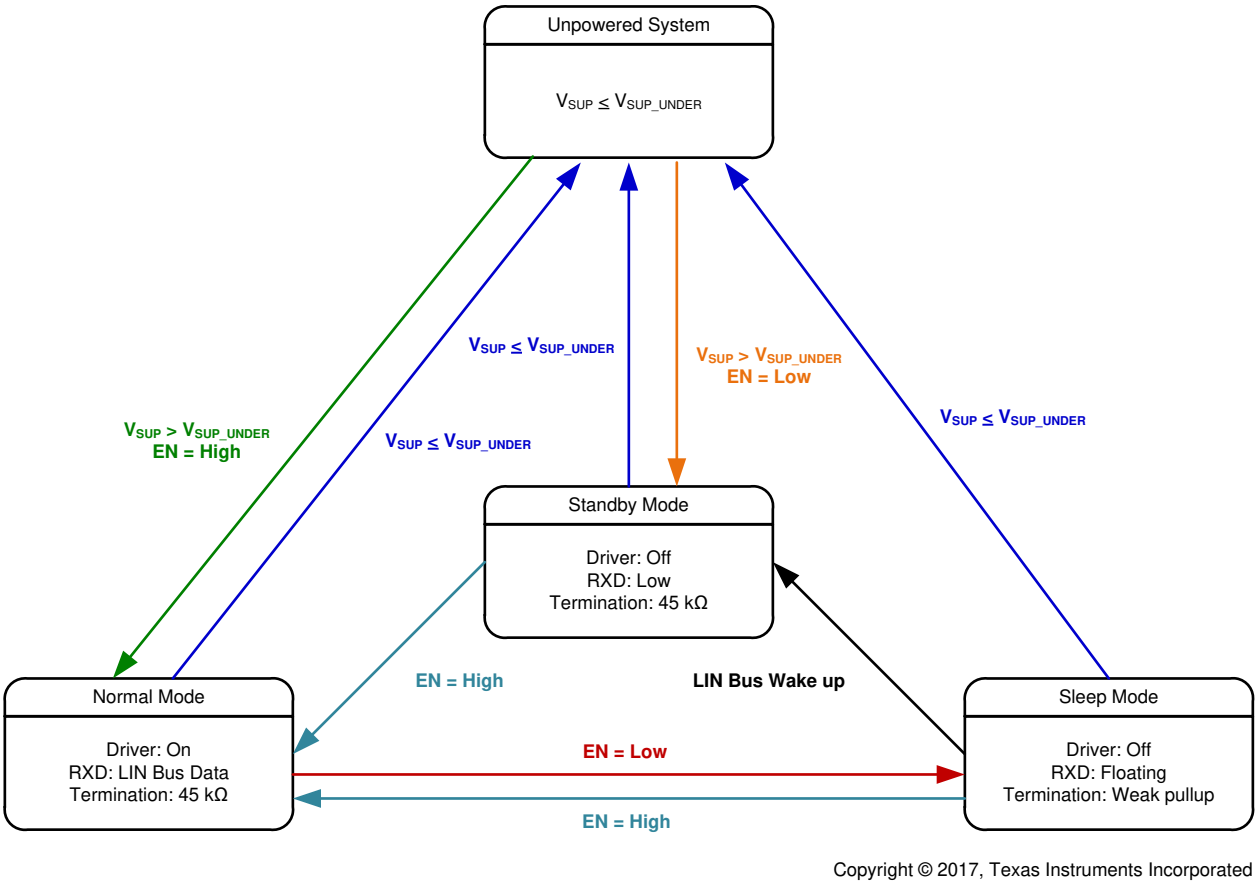


图 22. Operating State Diagram

9.4.1 Normal Mode

If the EN pin is high at power up the device will power up in normal mode and if low will power up in standby mode. The EN pin controls the mode of the device. In normal operational mode the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a logic high and a dominant signal on the LIN bus is a logic low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while theTLIN2029-Q1 is in sleep or standby mode for > t_{MODE_CHANGE} plus t_{NOMINT}.

9.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN2029-Q1. Sleep mode is only entered when the EN pin is low and from normal mode. Even with extremely low current consumption in this mode, the TLIN2029-Q1 can still wake up from LIN bus through a wake up signal or if EN is set high for > t_{MODE_CHANGE}. The LIN bus is filtered to prevent false wake up events. The wake up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE}.

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake up receiver are active.

9.4.3 Standby Mode

This mode is entered whenever a wake up event occurs through LIN bus while the device is in sleep mode. The LIN bus slave termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See *Standby Mode Application Note* for more application information.

When EN is set high for longer than t_{MODE_CHANGE} while the device is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

9.4.4 Wake Up Events

There are two ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is be held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event, eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than t_{MODE_CHANGE}.

9.4.4.1 Wake Up Request (RXD)

When the TLIN2029-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin is releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.4.2 Mode Transitions

When the TLIN2029-Q1 is transitioning from normal to sleep or standby modes the device needs the time t_{MODE_CHANGE} to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby to normal mode the device needs t_{MODE_CHANGE} plus t_{NOMINT}.

10 Application and Implementation

注

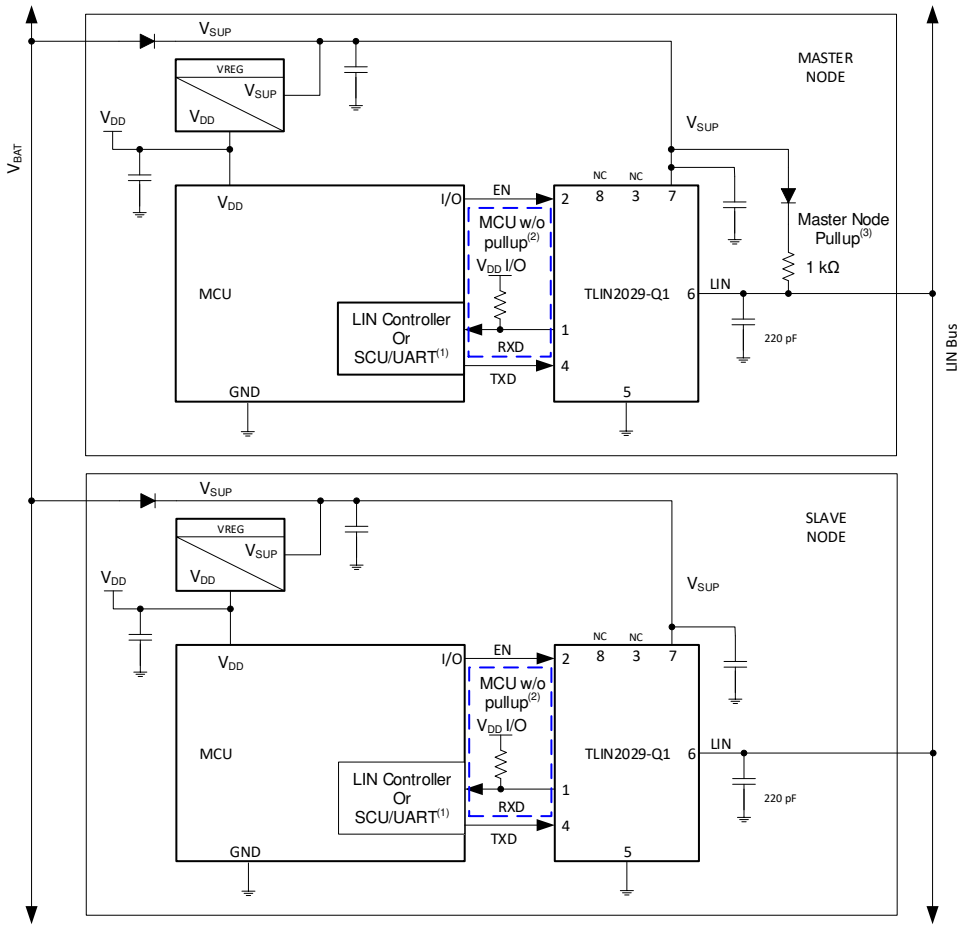
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLIN2029-Q1 can be used as both a slave device and a master device in a LIN network. The device comes with the ability to support both remote wake up request and local wake up request.

10.2 Typical Application

The device integrates a 45 kΩ pull-up resistor and series diode for slave applications. For master applications an external 1 kΩ pull-up resistor with series blocking diode can be used. 图 23 shows the device being used in both master and slave applications.



(1) If RXD on MCU on LIN slave has internal pullup; no external pullup resistor is needed.

(2) If RXD on MCU or LIN slave does not have an internal pullup requires external pullup resistor.

(3) Master node applications require and external 1 kΩ pullup resistor and serial diode.

(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥ 10 µF.

图 23. Typical LIN Bus

Typical Application (接下页)

10.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN2029-Q1 to be used with 3.3- V and 5-V I/O processor. If the RXD pin of the processor does not have an integrated pull-up, an external pull-up resistor to the processor I/O supply voltage is required. The select external pull-up resistor value should be between 1 kΩ to 10 kΩ. The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor as close to the supply pin of the device as possible. The system should include 1 µF and ≥ 10 µF decoupling capacitors on V_{SUP} as per each application requirements.

10.2.2 Detailed Design Procedures

10.2.2.1 Normal Mode Application Note

When using the TLIN2029-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until t_{MODE_CHANGE}. This is shown in 图 15

10.2.2.2 Standby Mode Application Note

If the TLIN2029-Q1 detects an under voltage on V_{SUP} the RXD pin transitions low and would signal to the software that the TLIN2029-Q1 is in standby mode and should be returned to sleep mode for the lowest power state.

10.2.2.2.1 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for master and slave applications thus there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

10.2.3 Application Curves

and show the propagation delay from the TXD pin to the LIN pin for both dominant to recessive and recessive to dominant stated under lightly loaded conditions.

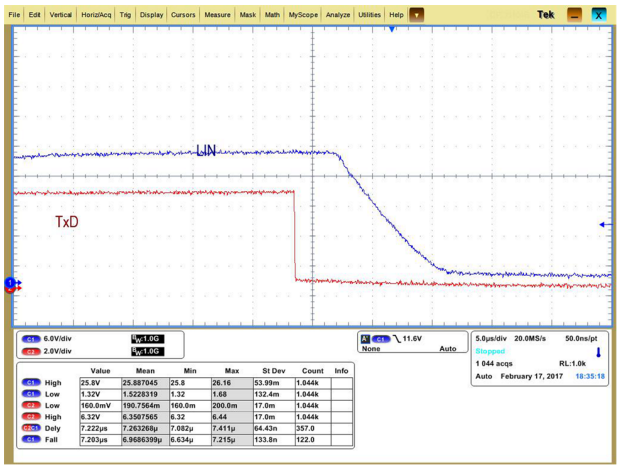


图 24. Recessive to Dominant Propagation

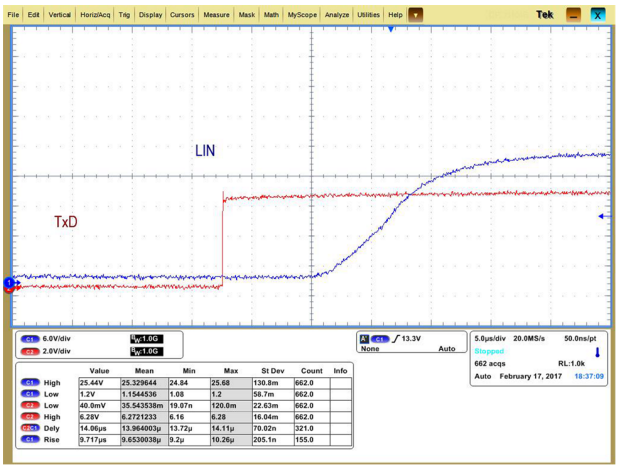


图 25. Dominant to Recessive Propagation

11 Power Supply Recommendations

The TLIN2029-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 4 V to 45 V. A 100 nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible.

12 Layout

In order for your PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1(RXD):** The pin is an open drain output and requires and external pull-up resistor in the range of 1 kΩ and 10 kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low power sleep mode. If this feature is not used the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (NC):** Not Connected.
- **Pin 4 (TXD):** The TXD pin is the transmit input signal to the device from the microcontroller. A series resistor can be placed to limit the input current to the device in the case of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** This pin connects to the LIN bus. For slave applications a 220 pF capacitor to ground is implemented. For maser applications and additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See 图 23.
- **Pin 7 (VSUP):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 8 (NC):** Not Connected.

注

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

12.2 Layout Example

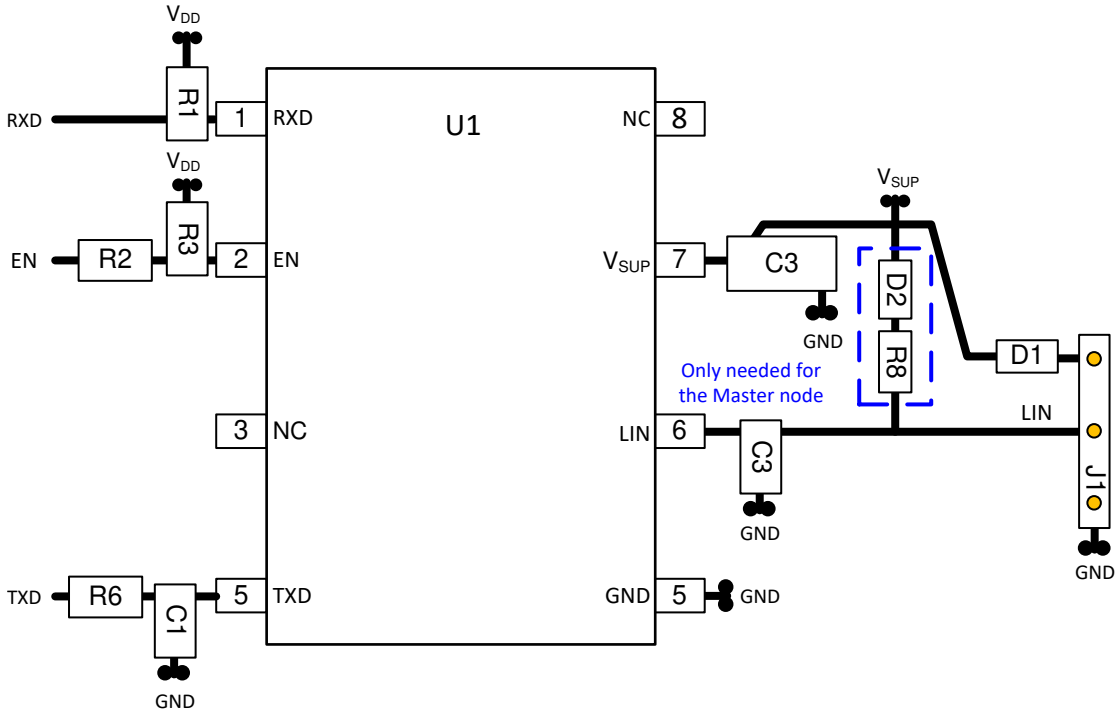


图 26. Layout Example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

LIN 标准：

- ISO/DIS 17987-1.2：道路车辆 - 局域互联网络 (LIN) - 第 1 部分：一般信息和用例定义
- ISO/DIS 17987-4.2：道路车辆 - 局域互联网络 (LIN) - 第 4 部分：电气物理层规格 (EPL) 12V/24V
- SAEJ2602-1：车用 LIN 网络 应用
- LIN 规范 LIN 2.0、LIN 2.1、LIN 2.2 和 LIN 2.2A

EMC 要求：

- SAEJ2962-1：通信收发器认证要求 - LIN
- ISO 10605：道路车辆 - 静电放电引起的电干扰的试验方法
- ISO 11452-4:2011：道路车辆 - 窄带辐射电磁能量的电子干扰组件试验方法 - 第 4 部分：线束激励方法
- ISO 7637-1:2015：道路车辆 - 传导和耦合造成的电干扰 - 第 1 部分：定义和一般描述
- ISO 7637-3：道路车辆 - 由传导和耦合引起的电干扰 - 第 3 部分：通过电容耦合和电感耦合经由非电源线线路的瞬间电传输
- IEC 62132-4:2006：集成电路 - 150kHz - 1GHz 电磁抗扰度的测量 - 第 4 部分：直接射频功率注入法
- IEC 61000-4-2
- IEC 61967-4
- CISPR25

符合性测试要求：

- ISO/DIS 17987-7.2：道路车辆 - 局域互联网络 (LIN) - 第 7 部分：电气物理层 (EPL) 符合性测试规格
- SAEJ2602-2：车辆应用的 LIN 网络 符合性测试

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 商标

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13.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLIN2029DQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TL029	Samples
TLIN2029DRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TL029	Samples
TLIN2029DRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TL029	Samples
TLIN2029DRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TL029	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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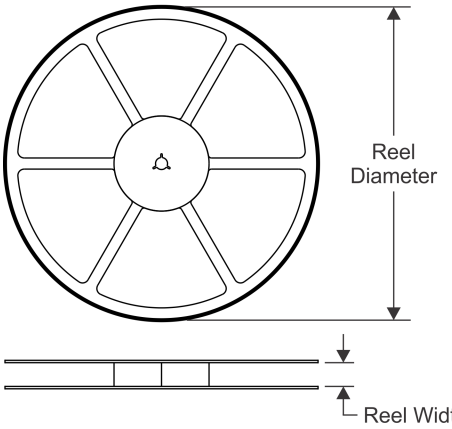
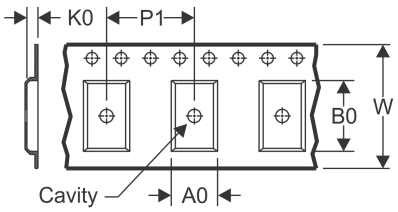
TAPE AND REEL INFORMATION

REEL DIMENSIONS

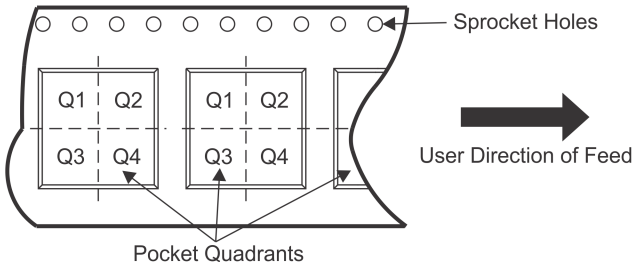


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

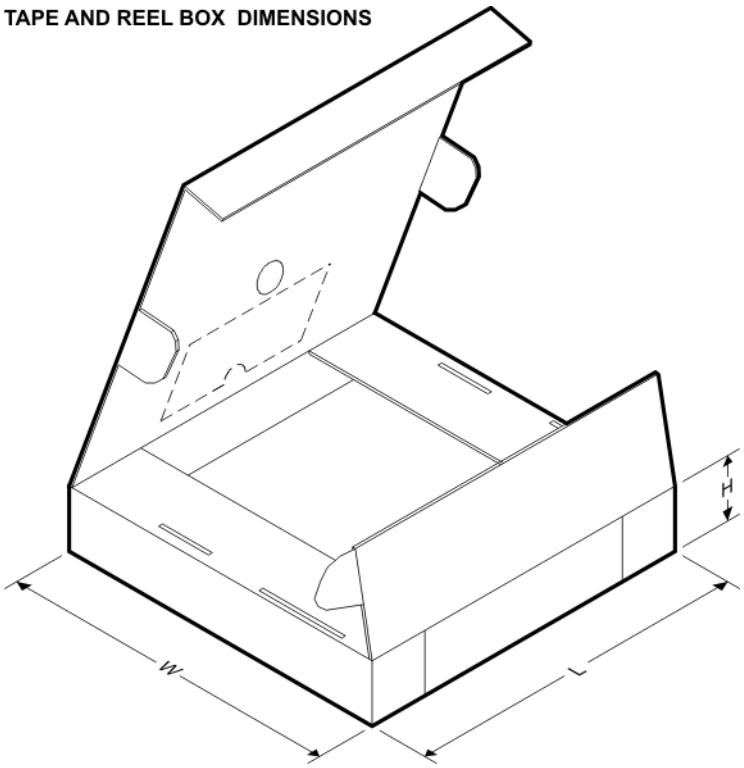
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN2029DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TLIN2029DRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TLIN2029DRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN2029DRBRQ1	SON	DRB	8	3000	367.0	367.0	38.0
TLIN2029DRBTQ1	SON	DRB	8	250	213.0	191.0	35.0
TLIN2029DRQ1	SOIC	D	8	2500	366.0	364.0	50.0

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