LP3950 Color LED Driver with Audio Synchronizer

Check for Samples: LP3950

FEATURES

- **Audio Synchronization for Color LEDs with Two Modes: Amplitude and Frequency**
- **Programmable Frequency and Amplitude Response with Tracking Speed Control**
- **Automatic Gain Control or Selectable Gain for Input Signal Optimization**
- **RGB Pattern Generator Similar to LP3933/LP3936**
- **Magnetic DC-DC Boost Converter with Programmable Boost Output Voltage**
- **Selectable SPI or I^2C Compatible Interface**
- **One Pin Default Enable for Non-Serial Interface Users. One Pin Selector for Synchronization Mode**
- **Space Efficient 32-Pin TLGA Package**

APPLICATIONS

- **Cellular Phones**
- **MP3/CD/Minidisc Players**
- **Toys**

DESCRIPTION

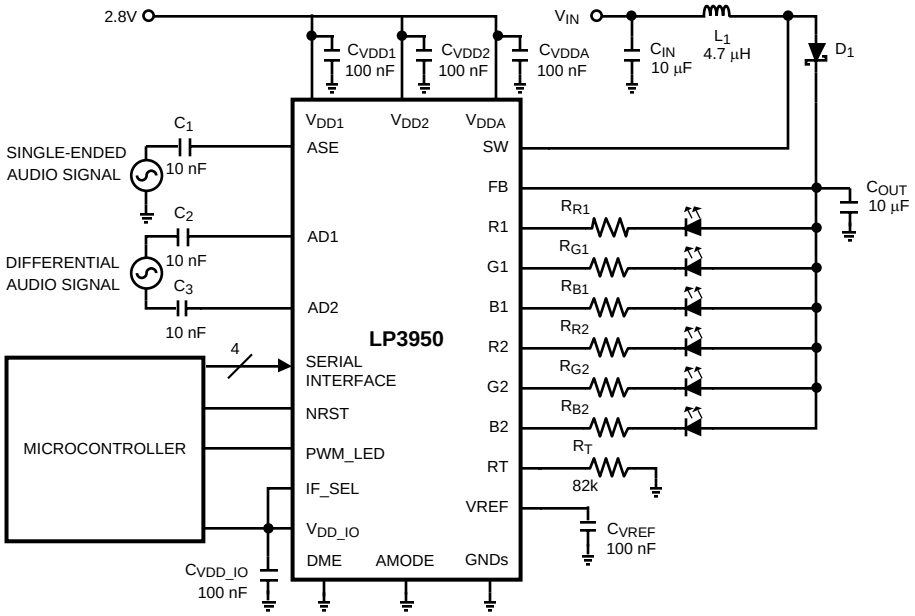
The LP3950 is a color LED driver with a built-in audio synchronization feature for any analog audio input such as polyphonic ring tones and MP3 music. LEDs can be synchronized to an audio signal with two methods - amplitude and frequency. Also several fine tuning options are available for differentiation purposes. The chip also has an unique AGC (Automatic Gain Control) feature which tracks the input signal level and automatically adjusts the gain to an optimal value.

The LP3950 has a high efficiency magnetic DC/DC converter with programmable output voltage and switching frequency. The converter has high output current capability so it is also able to drive flash LEDs in camera phone applications.

The LP3950 is similar to LP3933 and LP3936 in that the color LEDs (or RGB LEDs) can also be programmed to generate light patterns (programmable color, intensity, on/off timing, slope and blinking cycle).

All functions are software controllable through a SPI or I^2C compatible interface but the device also supports one pin control for enabling predefined (default) audio synchronization mode.

Typical Application



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Connection Diagrams

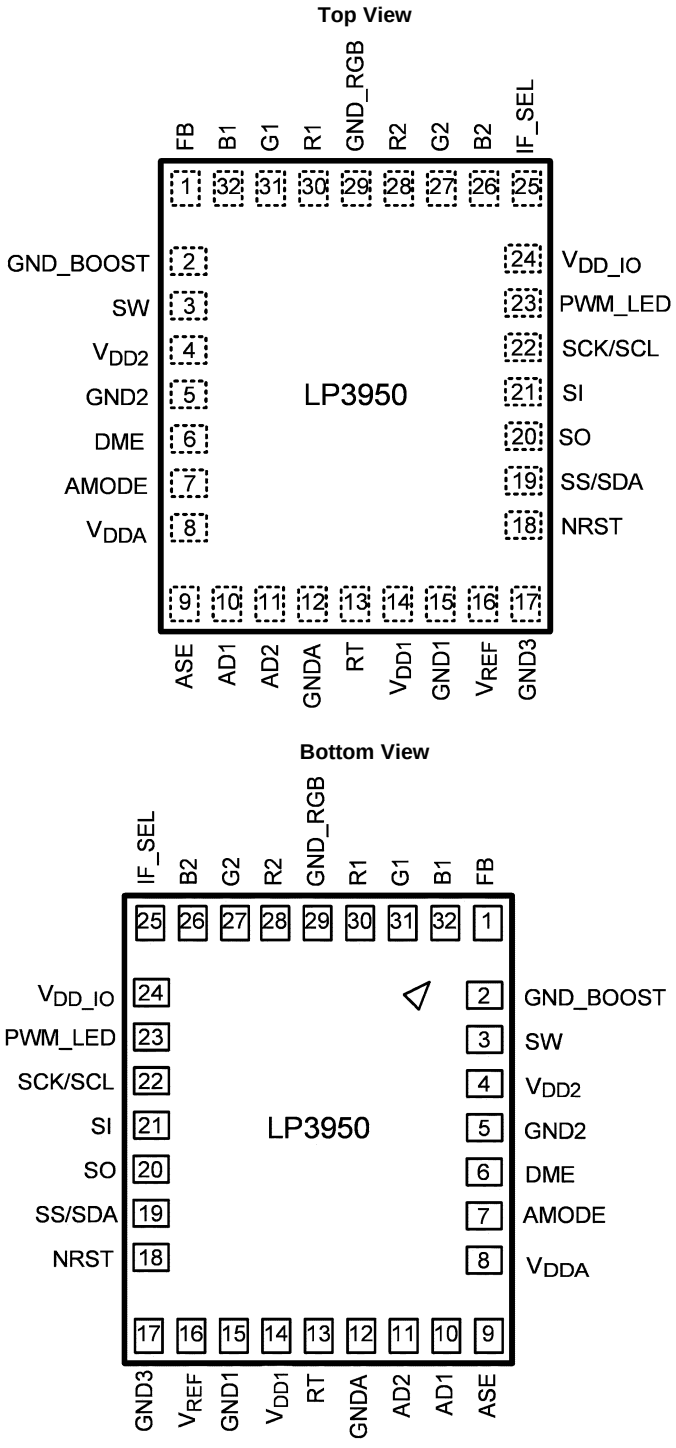


Figure 1. 32-Lead TLGA Package
4.5 x 5.5 x 0.8 mm, 0.5 mm Pitch, See Package Number NPC0032A

PIN DESCRIPTIONS

Pin #	Name	Type	Description
1	FB	Input	Boost converter feedback.
2	GND_BOOST	Ground	Power switch ground.
3	SW	Output	Open drain, boost converter power switch.
4	V_{DD2}	Power	Supply voltage for internal digital circuits.
5	GND2	Ground	Ground return for V_{DD2} (internal digital).
6	DME	Logic Input	Default mode enable (internal pull down 1 MΩ).
7	AMODE	Logic Input	Audio mode selection (internal pull down 1 MΩ).
8	V_{DDA}	Power	Supply voltage for audio circuits.
9	ASE	Input	Analog audio input, single-ended.
10	AD1	Input	Analog audio input, differential.
11	AD2	Input	Analog audio input, differential.
12	GNDA	Ground	Ground for analog audio inputs.
13	RT	Input	Oscillator resistor.
14	V_{DD1}	Power	Supply voltage for internal analog circuits.
15	GND1	Ground	Ground.
16	V_{REF}	Output	Internal reference bypass capacitor.
17	GND3	Ground	Ground.
18	NRST	Logic Input	Low active reset input.
19	SS/SDA	Logic I/O	SPI slave select/ I^2C data line.
20	SO	Logic Output	SPI serial data output.
21	SI	Logic Input	SPI serial data input.
22	SCK/SCL	Logic Input	SPI/ I^2C clock.
23	PWM_LED	Logic Input	Direct PWM control for LEDs.
24	V_{DDIO}	Power	Supply voltage for logic IO signals.
25	IF_SEL	Logic Input	SPI/I^2C select (IF_SEL = 1 in SPI mode).
26	B2	Output	Open drain output, blue LED2.
27	G2	Output	Open drain output, green LED2.
28	R2	Output	Open drain output, red LED2.
29	GND_RGB	Ground	RGB driver ground.
30	R1	Output	Open drain output, red LED1.
31	G1	Output	Open drain output, green LED1.
32	B1	Output	Open drain output, blue LED1.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

V (SW, FB, R1–2, G1–2, B1–2) (4) (5)	−0.3V to +7.2V
V_{DD1}, V_{DD2}, V_{DDIO}, V_{DDA}	−0.3V to +6.0V
Voltage on ASE, AD1, AD2	−0.3V to V_{DD1} +0.3V with 6.0V max
Voltage on Logic Pins	−0.3V to V_{DD_IO}+0.3V with 6.0V max
I (R1, G1, B1, R2, G2, B2) (6)	150 mA
I (V_{REF})	10 µA
Continuous Power Dissipation (7)	Internally Limited
Junction Temperature (T_{J-MAX})	125°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature	260°C
(Reflow soldering, 3 times) (8)	
ESD Rating (9)	
Human Body Model:	2 kV
Machine Model:	200V

(1) All voltages are with respect to the potential at the GND pins (GND1–3, GND_BOOST, GND_RGB, GNDA).
(2) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) Battery/Charger voltage should be above 6.0V no more than 10% of the operational lifetime.
(5) Voltage tolerance of LP3950 above 6.0V relies on fact that V_{DD1}, V_{DD2} and V_{DDA} (2.8V) are available (ON) at all conditions. If V_{DD1}, V_{DD2} and V_{DDA} are not available (ON) at all conditions, Texas Instruments does not guarantee any parameters or reliability for this device. Also, V_{DD1}, V_{DD2} and V_{DDA} must be at the same electric potential.
(6) The total load current of the boost converter should be limited to 300 mA.
(7) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 140°C (typ.).
(8) For detailed package and soldering specifications and information, please refer to Texas Instruments Application Note 1125 (SNAA002): Laminate CSP/FBGA.
(9) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1)(2)

V (SW, FB, R1–2, G1–2, B1–2)	0V to 6.0V
V_{DD1}, V_{DD2}, V_{DDA} (3)	2.7V to 2.9V
V_{DDIO}	1.65V to $V_{DD1,2}$ V
Voltage on ASE, AD1, AD2	0.1V to V_{DD1} - 0.1V
Recommended Load Current	0 mA to 300 mA
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range (4)	−40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins (GND1–3, GND_BOOST, GND_RGB, GNDA).
(3) Voltage tolerance of LP3950 above 6.0V relies on fact that V_{DD1}, V_{DD2} and V_{DDA} (2.8V) are available (ON) at all conditions. If V_{DD1}, V_{DD2} and V_{DDA} are not available (ON) at all conditions, Texas Instruments does not guarantee any parameters or reliability for this device. Also, V_{DD1}, V_{DD2} and V_{DDA} must be at the same electric potential.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), NPC0032A Package (1)	72°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics (1)(2)

Limits in standard typeface are for T_J = +25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise noted, specifications apply to Figure 2 with: V_{DD1} = V_{DD2} = V_{DDA} = 2.8V, C_{VDD1} = C_{VDD2} = C_{VDDA} = C_{VDDIO} = 100 nF, C_{OUT} = C_{IN} = 10 µF, C_{VREF} = 100 nF, L_1 = 4.7 µH and f_{BOOST} = 2.0 MHz (3).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VDD}	Standby Supply Current (V_{DD1} + V_{DD2} + V_{DDA} current)	NSTBY = L (register) SCK, SS, SI, NRST = H		1	**5**	µA
	No-Load Supply Current (V_{DD1} + V_{DD2} + V_{DDA} current, boost off)	NSTBY = H (reg.) EN_BOOST = L (reg.) SCK, SS, SI, NRST = H		300	**400**	µA
	Full Load Supply Current (V_{DD1} + V_{DD2} + V_{DDA} current, boost on) (4)	NSTBY = H (reg.) EN_BOOST = H (reg.) SCK, SS, SI, NRST = H All Outputs Active		850		µA
I_{VDDIO}	V_{DDIO} Supply Current	1.0 MHz SCK Frequency C_L = 50 pF at SO Pin		20		µA
I_{VDDA}	Audio Circuitry Supply Current (5)	INPUT_SEL = [10] (register)		550		µA
V_{REF}	Reference Voltage (6)	I_{REF} ≤ 1.0 nA Only for Test Purpose		1.230		V

(1) All voltages are with respect to the potential at the GND pins (GND1–3, GND_BOOST, GND_RGB, GNDA).
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) Low-ESR Surface-Mount Ceramic Capacitors are used in setting electrical characteristics.
(4) Audio block inactive.
(5) In single-ended and in differential mode one audio buffer only is active and I_{VDDA} will be reduced by 90 µA (typ).
(6) V_{REF} pin (Bandgap reference output) is for internal use only. A capacitor should always be placed between V_{REF} and GND1.

Block Diagram

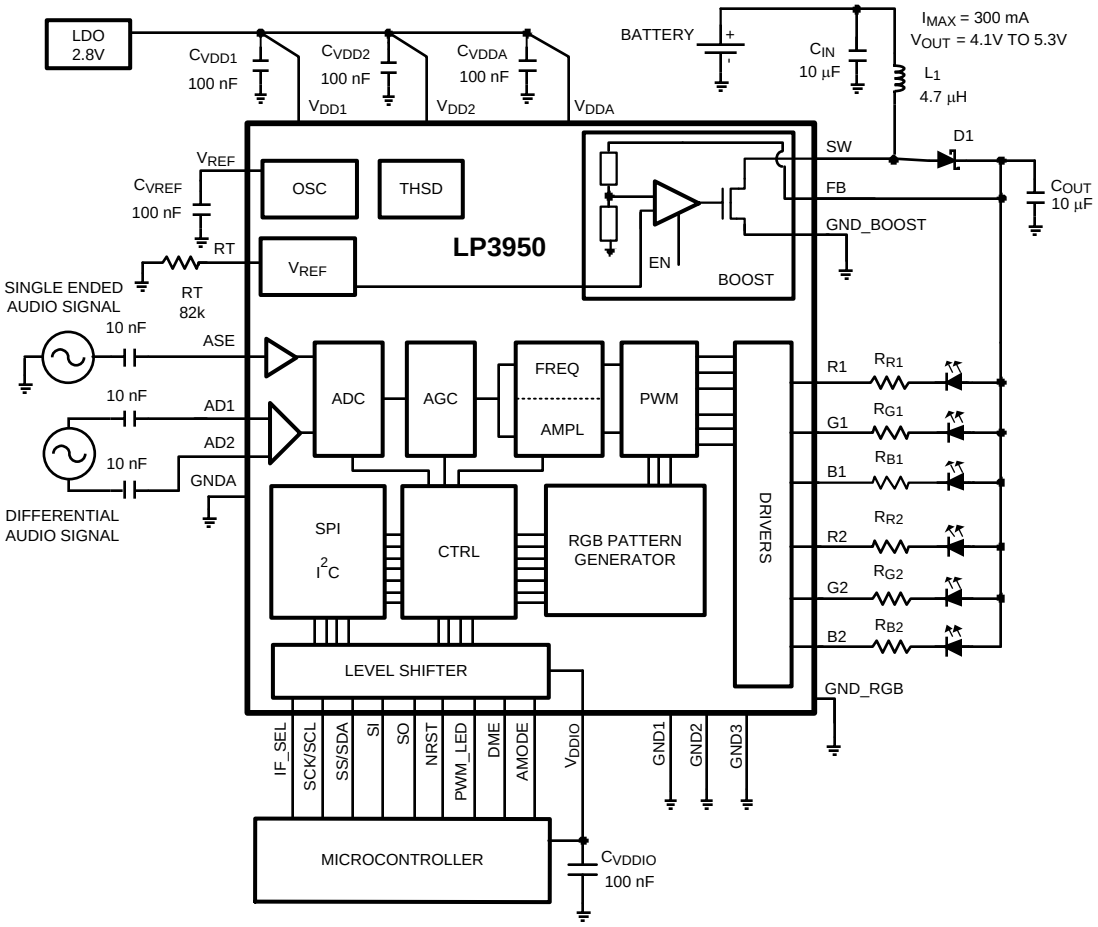


Figure 2. LP3950 Block Diagram

Modes of Operation

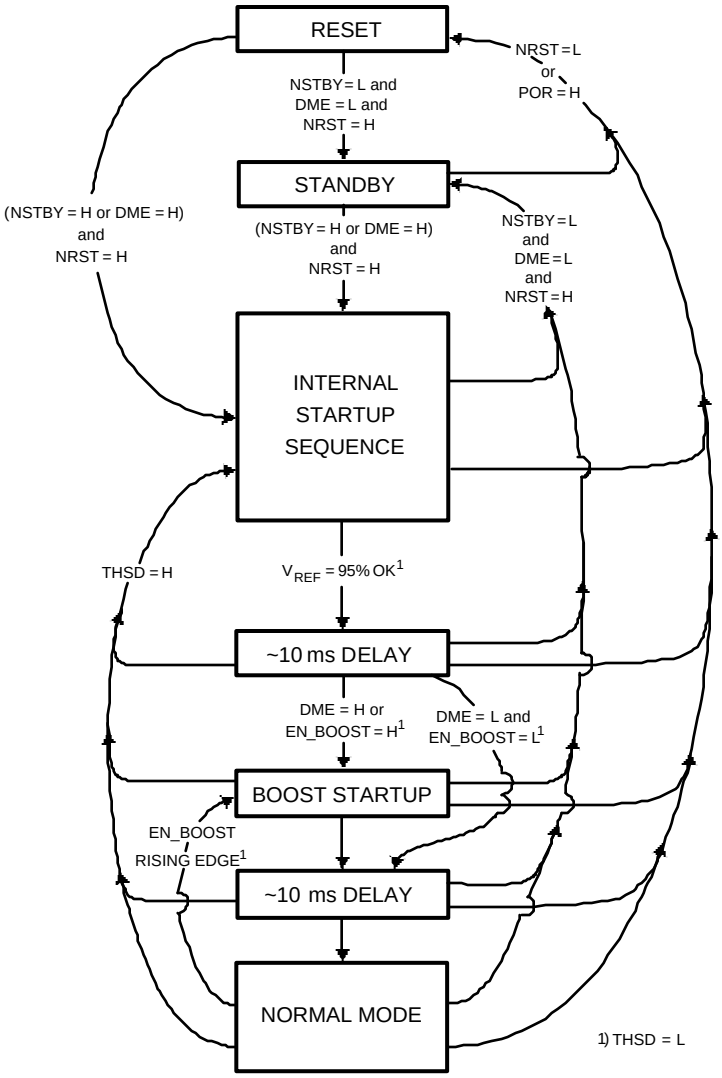
RESET: In the RESET mode all the internal registers are reset to the default values. RESET is entered always if input NRST is LOW or internal Power On Reset is active.

STANDBY: The STANDBY mode is entered if the register bit NSTBY is LOW and RESET is not active. This is the low power consumption mode, when all the circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after start up.

STARTUP: INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (V_{REF}, oscillator, etc.). To ensure the correct oscillator initialization, a 10 ms delay is generated by the internal state-machine. Thermal shutdown (THSD) disables the chip operation and Startup mode is entered until no thermal shutdown event is present.

BOOST STARTUP: Soft start for boost output is generated in the BOOST STARTUP mode. In this mode the boost output is raised in PFM mode during the 10 ms delay generated by the state-machine. All RGB outputs are off during the 10 ms delay to ensure smooth startup. The Boost startup is entered from Internal Startup Sequence if EN_BOOST is HIGH or from Normal mode when EN_BOOST is written HIGH.

NORMAL: During the NORMAL mode the user controls the chip using the control registers. Registers can be written in any sequence and any number of bits can be altered in a register within one write cycle . If the default mode is selected, default control register values are used.


RESET
NRST = L or POR = H
NSTBY = L and DME = L and NRST = H
STANDBY
(NSTBY = H or DME = H) and NRST = H
NSTBY = L and DME = L and NRST = H
(NSTBY = H or DME = H) and NRST = H
INTERNAL STARTUP SEQUENCE
THSD = H
VREF = 95% OK1
~10 ms DELAY
DME = H or EN_BOOST = H1
DME = L and EN_BOOST = L1
BOOST STARTUP
EN_BOOST RISING EDGE1
~10 ms DELAY
NORMAL MODE
1) THSD = L

Logic Interface Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIC INPUTS SS, SI, SCK/SCL, PWM_LED, IF_SEL						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**V_{DDIO} − 0.5**			V
I_I	Logic Input Current		**−1.0**		**1.0**	µA
f_{SCL}	Clock Frequency	I^2C Mode			**400**	kHz
		SPI Mode			**8**	MHz
LOGIC OUTPUT SO						
V_{OL}	Output Low Level	I_{SO} = 3.0 mA		0.3	**0.5**	V
V_{OH}	Output High Level	I_{SO} = −3.0 mA	**V_{DDIO} − 0.5**	V_{DDIO} − 0.3		V
I_L	Output Leakage Current	V_{SO} = 2.8V			**1.0**	µA
LOGIC I/O SDA						
V_{OL}	Output Low Level	I_{SDA} = 3.0 mA		0.3	**0.5**	V
LOGIC INPUTS DME, AMODE (Internal pull down 1 MΩ)						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**V_{DDIO} − 0.5**			V
I_I	Logic Input Current		**−1.0**		**6.0**	µA

(1) (1.80V ≤ V_{DDIO} ≤ $V_{DD1,2}$V). Limits in standard typeface are for T_J = +25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C ≤ T_A ≤ +85°C).

Logic Interface Characteristics, Low I/O Voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIC INPUTS SCL, PWM_LED, IF_SEL						
V_{IL}	Input Low Level				**0.35**	V
V_{IH}	Input High Level		**V_{DDIO} − 0.35**			V
I_I	Logic Input Current		**−1.0**		**1.0**	µA
f_{SCL}	Clock Frequency	I^2C Mode			**200**	kHz
LOGIC I/O SDA						
V_{OL}	Output Low Level	I_{SDA} = 3.0 mA		0.3	**0.5**	V
LOGIC INPUTS DME, AMODE (Internal pull down 1 MΩ)						
V_{IL}	Input Low Level				**0.35**	V
V_{IH}	Input High Level		**V_{DDIO} − 0.35**			V
I_I	Logic Input Current		**−1.0**		**6.0**	µA

(1) (1.65V ≤ V_{DDIO} < 1.80V) . I^2C compatible interface only.

Logic Input NRST Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**1.3**			V
I_I	Logic Input Current		**−1.0**		**1.0**	µA
t_{NRST}	Reset Pulse Width	Note: Guaranteed by design	**10**			µs

(1) (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V).

Control Interface

The LP3950 supports three different interface modes:

1. SPI interface (4 wire, serial)
2. I^2C compatible interface (2 wire, serial)
3. Direct enable (2 wire, enable lines)

User can define the serial interface by the IF_SEL pin. The following table shows the pin configuration for both interface modes. Note that the pin configurations will be based on the status of the IF_SEL pin.

IF_SEL	Interface	Pin Configuration		Comment
HIGH	SPI	SCK SI SO SS	(clock) (data in) (data out) (chip select)	
LOW	I^2C Compatible	SCL SDA SI SO	(clock) (data in/out) (I^2 address) (NC)	Use pull up resistor for SCL. Use pull up resistor for SDA. SI HIGH → address is 51'h; SI LOW → address is 50'h; Unused pin SO can be left unconnected.

SPI Interface

The transmission consists of 16-bit write and read cycles. One cycle consists of seven address bits, one read/write (R/W) bit and eight data bits. R/W bit high state defines a write cycle and low defines a read cycle. SO output is normally in high-impedance state and it is active only during when data is sent out during a read cycle. A pull-up or pull-down resistor may be needed for SO line if a floating logic signal can cause unintended current consumption in the circuitry.

The address and data are transmitted Most Significant Byte (MSB) first. The Slave Select signal (SS) must be low during the cycle transmission. SS resets the interface when high and it has to be taken high between successive cycles. Data is clocked in on the rising edge of the SCK clock signal, while data is clocked out on the falling edge of SCK.

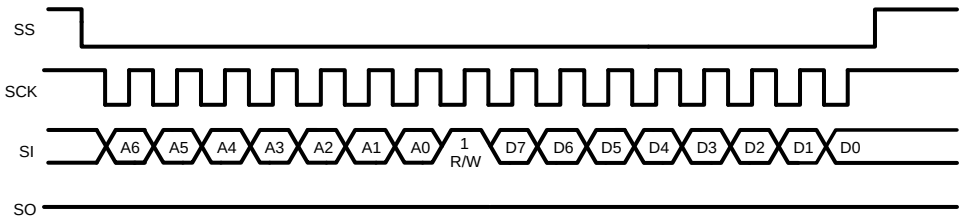


Figure 3. SPI Write Cycle

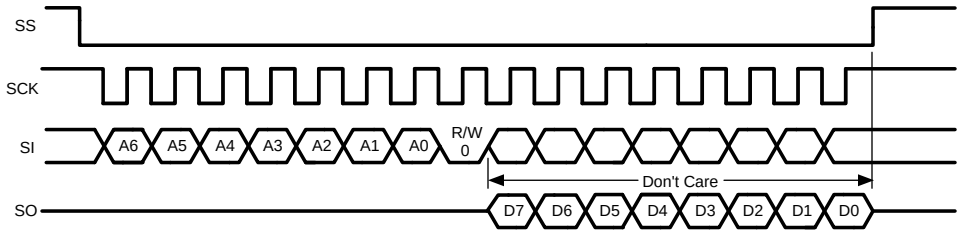


Figure 4. SPI Read Cycle

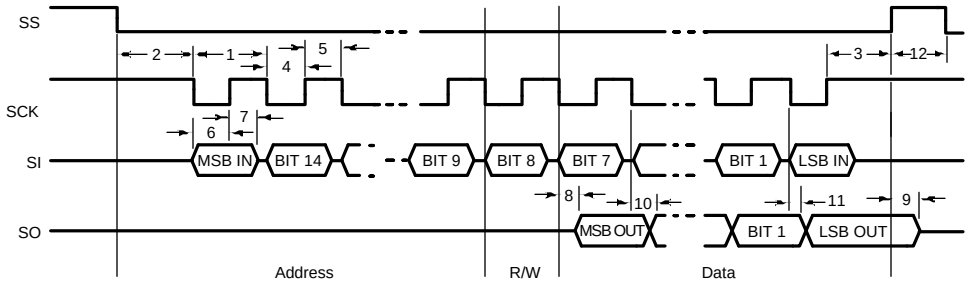


Figure 5. SPI Timing Diagram

Table 1. SPI Timing Parameters(1)

Symbol	Parameter	Limit		Units
		Min	Max	
1	Cycle Time	80		ns
2	Enable Lead Time	40		ns
3	Enable Lag Time	40		ns
4	Clock Low Time	40		ns
5	Clock High Time	40		ns
6	Data Setup Time	0		ns
7	Data Hold Time	20		ns
8	Data Access Time		27	ns
9	Output Disable Time		27	ns
10	Output Data Valid		37	ns
11	Output Data Hold Time	0		ns
12	SS Inactive Time	15		ns

(1) Data guaranteed by design.

I²C Compatible Interface

I²C SIGNALS

In I²C compatible mode, the LP3950 pin SCL is used for the I²C clock and the SDA pin is used for the I²C data. Both these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistors are determined by the capacitance of the bus (typ. 1.8k). Signal timing specifications are shown in Table 2. Unused pin SO can be left unconnected and pin SI must be connected to V_{DDIO} or GND (address selector). Maximum bit rate is 400 kbit/s (V_{DDIO} 1.80V to $V_{DD1,2}$V). I²C compatible interface can be used down to 1.65 V_{DDIO} with maximum bit rate of 200 kbit/s.

I²C DATA VALIDITY

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

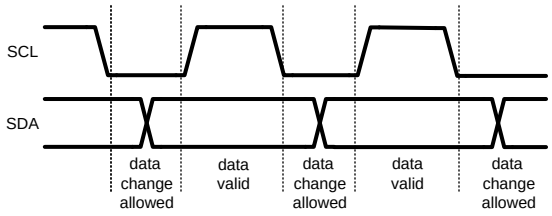


Figure 6. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transition from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

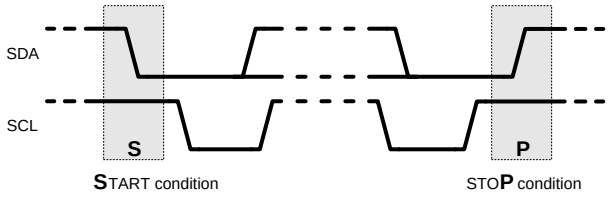


Figure 7. Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3950 address is 50'h or 51'h. The selection of the address is done by connecting SI pin to V_{DDIO} (51 hex) or GND (50 hex). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

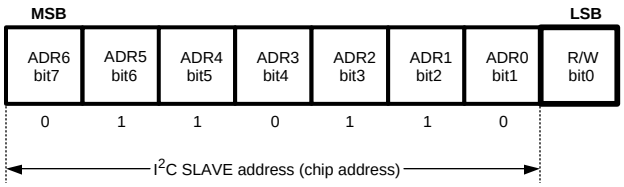
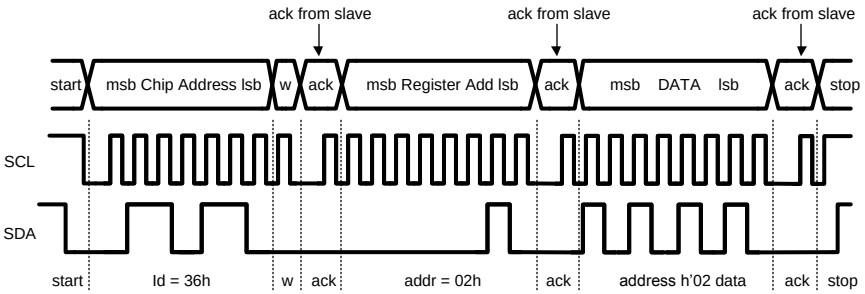


Figure 8. I²C Chip Address



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = chip address, 50'h or 51'h for LP3950.

Figure 9. I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in Figure 10 .

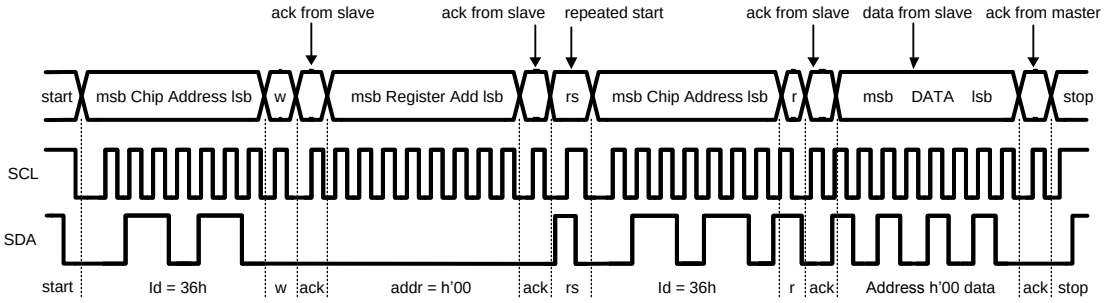


Figure 10. I²C Read Cycle

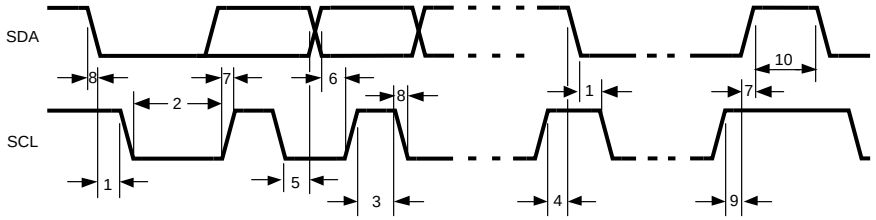


Figure 11. I²C Timing Diagram

Table 2. I²C Timing Parameters(1)

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time ($1.65V \le V_{DDIO} < 1.80V$)	3.2		µs
2	Clock Low Time ($1.80V \le V_{DDIO} \le V_{DD1,2}V$)	1.3		µs
3	Clock High Time ($1.65V \le V_{DDIO} < 1.80V$)	1200		ns
3	Clock High Time ($1.80V \le V_{DDIO} \le V_{DD1,2}V$)	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (data output, delay generated by LP3950)	300	900	ns
5	Data Hold Time (data input)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load Parameter for Each Bus Line. Load of One Picofarad Corresponds to One Nanosecond.	10	200	ns

(1) Data guaranteed by design

Magnetic Boost DC/DC Converter

The boost DC/DC converter generates a 4.1V–5.3V output voltage to drive LEDs from a single Li-Ion battery (3.0V to 4.5V). The output voltage is controlled with an eight-bit register in nine steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The converter has three options for switching frequency, 1.0 MHz, 1.67 MHz and 2.0 MHz (default), when the timing resistor RT is 82 kΩ.

The LP3950 boost converter uses an unique pulse-skipping elimination method to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is fed to the inductor. An internal active load is used to remove the excess charge from the output capacitor when needed (see **NOTE** below). The boost converter should be disabled when there is no load to avoid idle current consumption.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The output voltage control changes the resistor divider in the feedback loop.

Figure 12 shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage
   - Keeps the output below breakdown voltage
   - Prevents boost operation if the battery voltage is much higher than desired output
2. Over current protection, limits the maximum inductor current
   - Voltage over switching NMOS is monitored; too high voltages turn the switch off
3. Feedback (FB) protection for no connection
4. Duty cycle limit function, done with digital control

NOTE

When the battery voltage is close to the output voltage, the output voltage may rise slightly over programmed value if the load on output is small and pulse-skipping elimination is active.

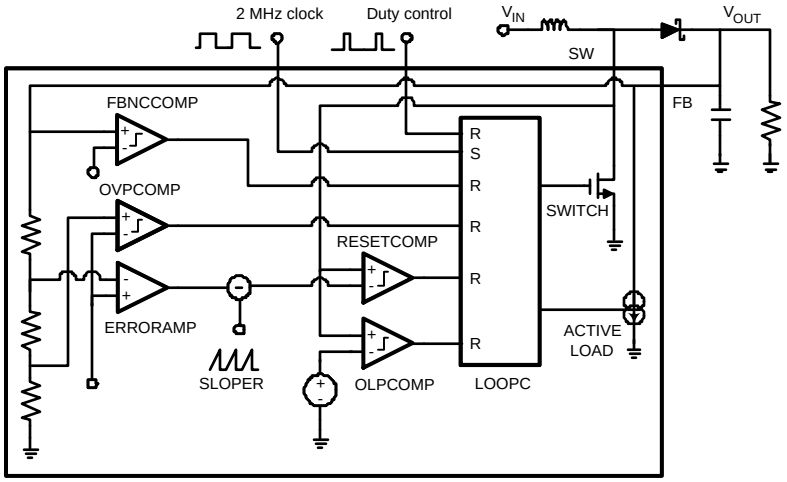


Figure 12. Boost Converter Functional Block Diagram

Magnetic Boost DC/DC Converter Electrical Characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LOAD}	Load Current	3.0V ≤ V_{IN} ≤ 4.5V V_{OUT} = 5.0V	0		300	mA
V_{OUT}	Output Voltage Accuracy (FB Pin)	1.0 mA ≤ I_{LOAD} ≤ 300 mA 3.0V ≤ V_{IN} ≤ 4.5V V_{OUT} = 5.0V (target value), autoload OFF	**−5**		**+5**	%
	Output Voltage (FB Pin)	1.0 mA ≤ I_{LOAD} ≤ 300 mA 3.0V < V_{IN} < 5.0V + $V_{(SCHOTTKY)}$, autoload OFF		5.0		V
		1.0 mA ≤ I_{LOAD} ≤ 300 mA V_{IN} > 5V + $V_{(SCHOTTKY)}$		V_{IN}–$V_{(SCHOTTKY)}$		V
RDS_{ON}	Switch ON Resistance	$V_{DD1,2}$ = 2.8V, I_{SW} = 0.5A		0.4	**0.7**	Ω
f_{PWF}	PWM Mode Switching Frequency	RT = 82 kΩ freq_sel[2:0] = 1XX		2.0		MHz
	Frequency Accuracy	2.7 ≤ $VDD_{1,2}$ ≤ 2.9	−6	±3	+6	%
		RT = 82 kΩ	**−9**		**+9**	
t_{PULSE}	Switch Pulse Minimum Width	No Load		25		ns
$t_{STARTUP}$	Startup Time			15		ms
I_{CL_OUT}	SW Pin Current Limit		700	800	900	mA
			500		**1000**	

(1) Limits in standard typeface are for T_J = +25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise noted, specifications apply to Figure 2 with: V_{DD1} = V_{DD2} = V_{DDA} = 2.8V, C_{VDD1} = C_{VDD2} = C_{VDDA} = C_{VDDIO} = 100 nF, C_{OUT} = C_{IN} = 10 µF, C_{VREF} = 100 nF, L_1 = 4.7 µH and f_{BOOST} = 2.0 MHz.
(2) Low-ESR Surface-Mount Ceramic Capacitors are used in setting electrical characteristics.

Boost Standby Mode

User can set the boost converter to STANDBY mode by writing the register bit EN_BOOST low when there is no load to avoid idle current consumption. When EN_BOOST is written high, the converter starts in PFM (Pulse Frequency Modulation) mode for 10 ms and then goes to PWM (Pulse Width Modulation) mode. All RGB outputs are off during the 10 ms delay.

Boost Output Voltage Control

User can control the boost output voltage by eight-bit boost output voltage register according to the following table.

BOOST[7:0] Register 0D'h		BOOST Output Voltage (typical)
Binary	Hex	
0000 0000	00	4.10
0000 0001	01	4.25
0000 0011	03	4.40
0000 0111	07	4.55
0000 1111	0F	4.70
0001 1111	1F	4.85
0011 1111	**3F**	**5.00 Default**
0111 1111	7F	5.15
1111 1111	FF	5.30

Boost Frequency Control

The register 'boost frequency' has address 0C'h. The default value after reset is 07'h. 'x' means don't care.

FREQ_SEL[2:0]	Frequency
1xx	2.00 MHz
01x	1.67 MHz
001	1.00 MHz

Boost Converter Typical Performance Characteristics

V_{IN} = 3.6V, V_{OUT} = 5.0V if not otherwise stated.

Boost Converter Efficiency

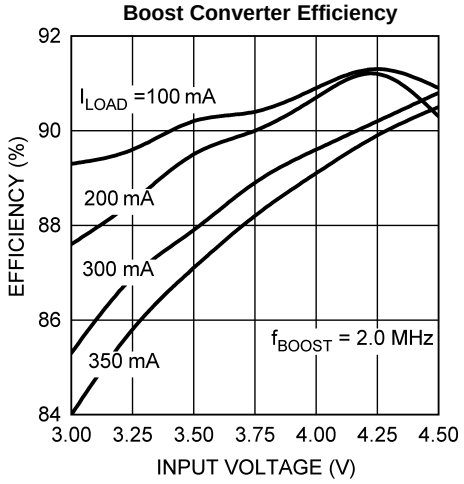


Figure 13.

Boost Frequency vs RT Resistor

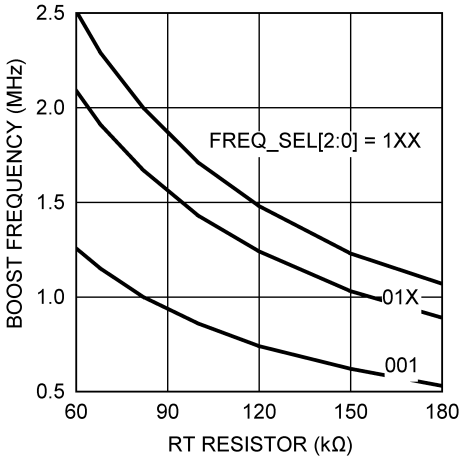


Figure 14.

Battery Current vs Voltage

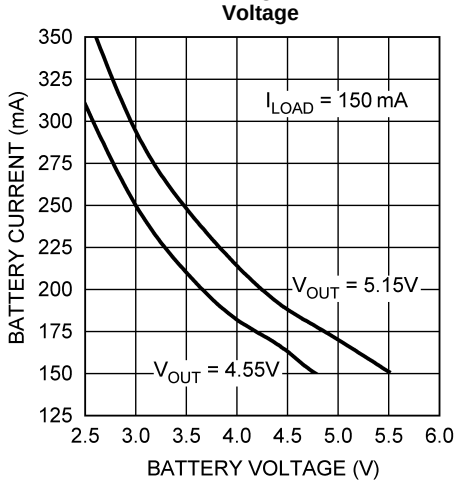


Figure 15.

Battery Current vs Voltage

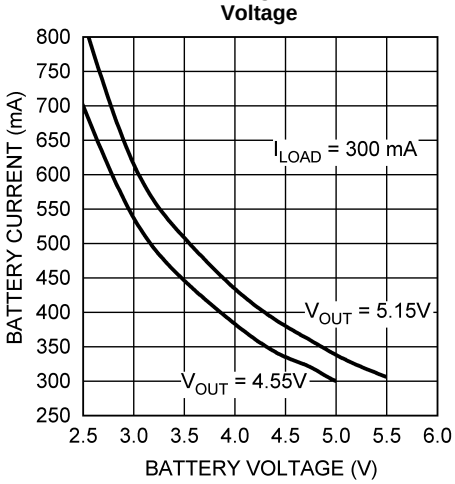


Figure 16.

Boost Converter Typical Performance Characteristics (continued)

V_{IN} = 3.6V, V_{OUT} = 5.0V if not otherwise stated.

Boost Typical Waveforms at 100 mA Load

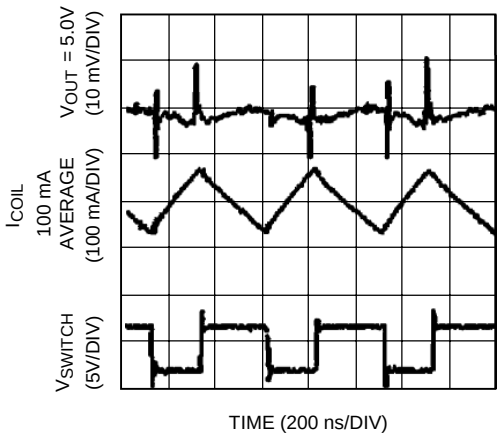


Figure 17.

Boost Startup with No Load

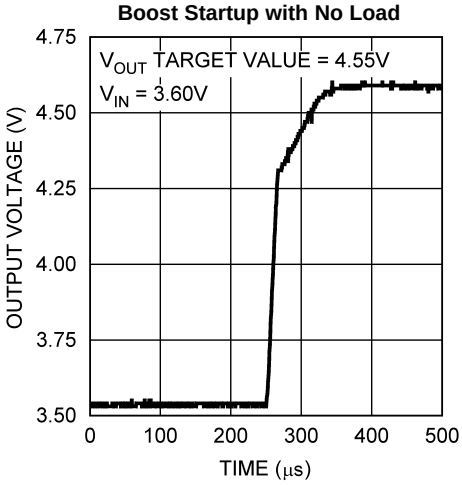


Figure 18.

Boost Line Regulation

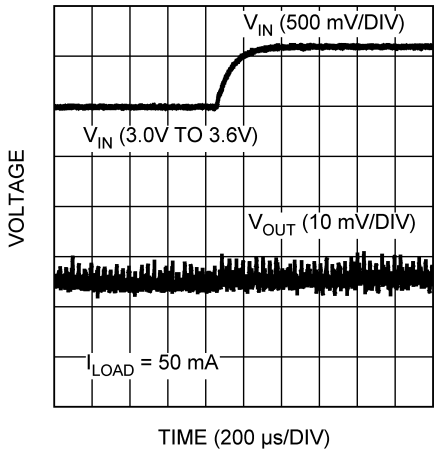


Figure 19.

Boost Load Transient Response, 50 mA to 100 mA

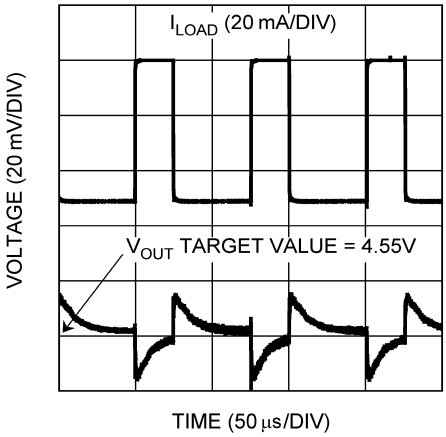


Figure 20.

RGB LED Pattern Generator

The LP3950 RGB outputs can be controlled either with audio synchronization or with RGB pattern generator.

The pattern generator of LP3950 drives three independently controlled LED outputs (for example, R1, G1 and B1). The functionality is similar compared to RGB functionality of LP3936 and LP3933.

The output of RGB pattern generator can be selected to drive RGB1 (R1-G1-B1), RGB2 (R2-G2-B2) or RGB1 and RGB2 (R1&R2 – G1&G2 – B1&B2) outputs.

Programmable Pattern Mode

User has control over the following parameters separately for each LED:

ON and OFF (start and stop time in blinking cycle)

DUTY (PWM brightness control)

SLOPE (dimming slope)

ENABLE (output enable control)

The main blinking cycle is controlled with three-bit CYCLE control (0.25 / 0.5 / 1.0 / 2.0 / 4.0s).

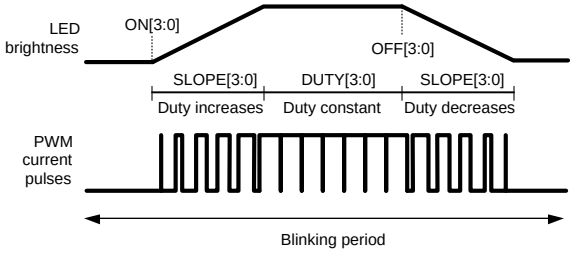


Figure 21. RGB PWM Operating Principle

RGB_START is the master control for the whole RGB function. The internal PWM and blinking control can be disabled by setting the RGB_PWM control LOW. In this case the individual enable controls can be used to switch outputs on and off. PWM_EN input can be used for external hardware PWM control.

In the normal PWM mode the R, G and B switches are controlled in 3 phases (one phase per driver). During each phase the peak current set by an external ballast resistor is driven through the LED for the time defined by DUTY setting (0 µs to 50 µs). As a time averaged current this means 0% to 33% of the peak current. The PWM period is 150 µs and the pulse frequency is 6.67 kHz in normal mode.

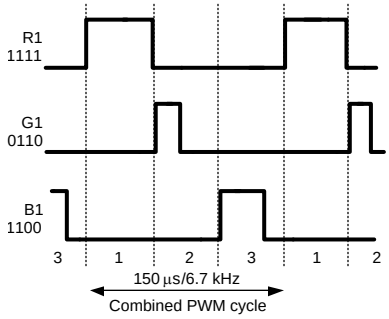


Figure 22. Normal Mode PWM Waveforms at Different Duty Settings

In the FLASH mode all the outputs are controlled in one phase and the PWM period is 50 µs. The time averaged FLASH mode current is three times the normal mode current at the same DUTY value.

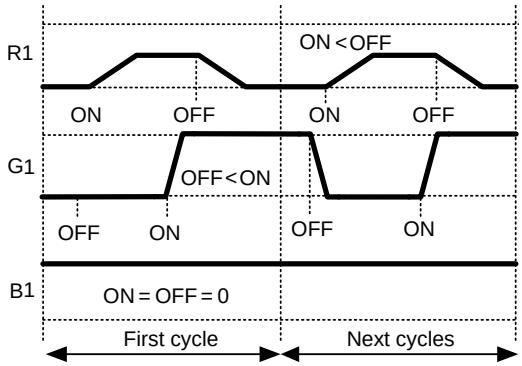


Figure 23. Example Blinking Waveforms

RGB Driver Characteristics

(R1, G1, B1, R2, G2, B2 outputs). Limits in standard typeface are for T_J = +25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C ≤ T_A ≤ +85°C).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{DS-ON}	ON Resistance			3.5	**6.0**	Ω
$I_{LEAKAGE}$	Off State Leakage Current	V_{FB} = 5.0V, LED driver off		0.03	**1.0**	µA
t_{SMAX}	Maximum Slope Period	At Maximum Duty Setting		0.93		s
t_{SMIN}	Minimum Slope Period	At Maximum Duty Setting		31		ms
t_{SRES}	Slope Resolution	At Maximum Duty Setting		62		ms
$t_{START/STOP}$	Start/Stop Resolution	Cycle 1.0s		1/16		s
Duty	Duty Step Size			1/16		
t_{BLINK}	Blinking Cycle Accuracy		−6	±3	+6	%
D_{CYCF}	Duty Cycle Range	EN_FLASH = 1	0		99.6	%
D_{CYC}	Duty Cycle Range	EN_FLASH = 0	0		33.2	%
D_{RESF}	Duty Resolution	EN_FLASH = 1 (4-bit)		6.64		%
D_{RES}	Duty Resolution	EN_FLASH = 0 (4-bit)		2.21		%
f_{PWMF}	PWM Frequency	EN_FLASH = 1		20		kHz
f_{PWM}	PWM Frequency	EN_FLASH = 0		6.67		kHz

Table 3. RGB LED PWM Control (1)

RDUTY[3:0] GDUTY[3:0] BDUTY[3:0]	DUTY sets the brightness of the LED by adjusting the duty cycle of the PWM driver. The minimum DUTY cycle is 0% [0000] and the maximum in the flash mode is 100% [1111]. The peak pulse current is determined by the external resistor, LED forward voltage drop and the boost voltage. In the normal mode the maximum duty cycle is 33%.
RSLOPE[3:0] GSLOPE[3:0] BSLOPE[3:0]	SLOPE sets the turn-on and turn-off slopes. Fastest slope is set by [0000] and slowest by [1111]. SLOPE changes the duty cycle at constant, programmable rate. For each slope setting the maximum slope time appears at maximum DUTY setting. When DUTY is reduced, the slope time decreases proportionally. For example, in case of maximum DUTY, the sloping time can be adjusted from 31 ms [0000] to 930 ms [1111]. For DUTY [0111] the sloping time is 14 ms [0000] to 434 ms [1111]. The blinking cycle has **no** effect on SLOPE.
RON[3:0] GON[3:0] BON[3:0]	ON sets the beginning time of the turn-on slope. The on-time is relative to the selected blinking cycle length. On-setting N (N = 0–15) sets the on-time to N/16 * cycle length.
ROFF[3:0] GOFF[3:0] BOFF[3:0] ROFF[3:0] GOFF[3:0] BOFF[3:0]	OFF sets the beginning time of the turn-off slope. Off-time is relative to blinking cycle length in the same way as on-time.
	If **ON = 0, OFF = 0** and **RGB_PWM = 1**, then RGB outputs are continuously on (no blinking), the DUTY setting controls the brightness and the SLOPE control is ignored. **If ON and OFF are the same, but not 0, RGB outputs are turned off.**
CYCLE[2:0]	CYCLE sets the blinking cycle: [000] for 0.25s, [001] for 0.5s, [010] for 1.0s, [011] for 2.0s. and [1XX] for 4.0s CYCLE effects to all RGB LEDs.
RSW1 GSW1 BSW1 RSW2 GSW2 BSW2	Enable for R1 switch Enable for G1 switch Enable for B1 switch Enable for R2 switch Enable for G2 switch Enable for B2 switch
RGB_START	Master Switch for both RGB drivers: RGB_START = 0 → RGB OFF RGB_START = 1 → RGB ON, starts the new cycle from t = 0
RGB_PWM	RGB_PWM = 0 → RSW, GWS and BSW control directly the RGB outputs (on/off control only) RGB_PWM = 1 → Normal PWM RGB functionality (duty, slope, on/off times, cycle)
EN_FLASH	Flash mode enable control for RGB1 and RGB2. In the flash mode (EN_FLASH = 1) RGB outputs are PWM controlled simultaneously, not in 3-phase system as in the normal mode.
R1_PWM G1_PWM B1_PWM R2_PWM G2_PWM B2_PWM	xx_PWM = 0 → External PWM control from PWM_LED pin is disabled xx_PWM = 1 → External PWM control from PWM_LED pin is enabled Internal PWM control (DUTY) can be used independently of external PWM control. External PWM has the same effect on all enabled outputs.

(1) The LP3933 shares the same pattern generator. Application Note AN-1291 (SNVA069), “Driving RGB LEDs Using LP3933 Lighting Management System” contains a thorough description of the RGB driver functionality including programming examples.

PWM_LED input can be used as a direct on/off or PWM brightness control for selected RGB outputs. For example it can trigger the flash using a flash signal from the camera. If PWM_LED input is not used, it must be tied to V_{DDIO}.

AUDIO SYNCHRONIZATION

The LEDs connected to the RGB outputs can be synchronized to incoming audio signal with Audio Synchronization feature. Audio Synchronization has two modes. **Amplitude mode** synchronizes LEDs based on the peak amplitude of the input signal. In the amplitude mode the user can select one of three amplitude mapping options. The **frequency mode** synchronizes the LEDs based on bass, middle and treble amplitudes (= low pass, band pass and high pass filters). The user can select between two different responses of frequency for best audio-visual user experience. Both of the modes provide a control for speed of the mapping with four different speed configurations. Programmable gain and AGC (Automatic Gain Control) function are also available for adjustment of the optimum audio signal mapping. The Audio Synchronization functionality is described more closely below.

INPUT SIGNAL TYPE

The LP3950 support four types of analog audio input signals for audio synchronization

1. Single ended audio
2. Differential audio
3. Stereo
4. Single ended and differential audio.

Figure 24 shows how to wire the LP3950 audio inputs case by case (NC = Not Connected).

USING A DIGITAL PWM AUDIO SIGNAL AS AN AUDIO SYNCHRONIZATION SOURCE

If the input signal is a PWM signal, use a first or second order low pass filter to convert the digital PWM audio signal into an analog waveform. There are two parameters that need to be known to get the filter to work successfully: frequency of the PWM signal and the voltage level of the PWM signal. Suggested cut-off frequency (-3dB) should be around 2 kHz to 4 kHz and the stop-band attenuation at sampling frequency should be around -48dB or better. Use a resistor divider to reduce the digital signal amplitude to meet the specification of the analog audio input. Because a low-order low-pass filter attenuates the high-frequency components from audio signal, MODE_CONTROL=[01] selection is recommended when frequency synchronization mode is enabled. Figure 33 shows an example of a second order RC-filter for 29 kHz PWM signal with 3.3V amplitude. Active filters, such as a Sallen-Key filter, may also be applied. An active filter gives better stop-band attenuation and cut-off frequency can be higher than for a RC-filter.

To make sure that the filter rolls off sufficiently quickly, connect your filter circuit to the audio input(s), turn on the audio synchronization feature, set manual gain to maximum, apply the PWM signal to the filter input and keep an eye on LEDs. If they are blinking without an audio signal (modulation), a sharper roll-off after the cut-off frequency, more stop-band attenuation, or smaller amplitude of the PWM signal is required.

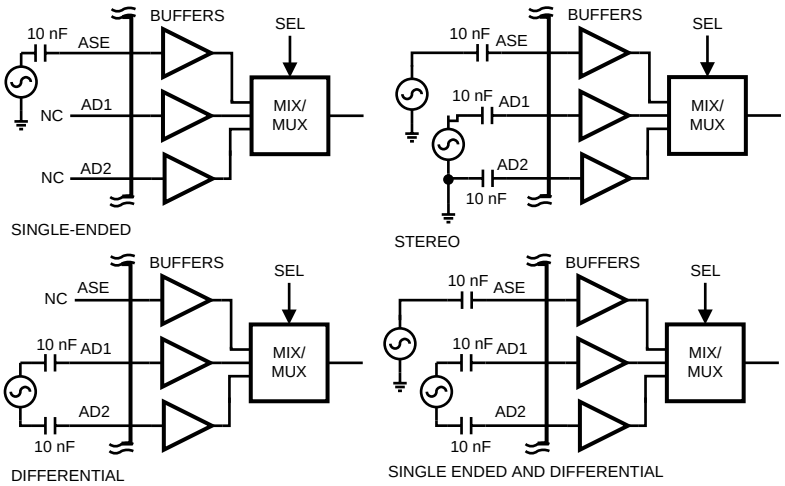


Figure 24. Wiring Diagram for LP3950 Audio Inputs

INPUT BUFFERING

Figure 25 describes the LP3950 audio input buffering structure in high level. The electric parameters of the buffers are described in Table 4. Operational amplifiers for both buffers are rail-to-rail input opamps. The single ended buffer is simply a voltage follower. DC level of the input signal is generated by a resistor divider. The differential amplifier is a basic differential-to-single-ended converter.

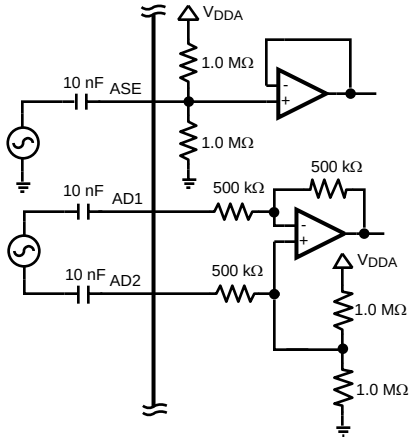


Figure 25. Audio Input Buffer Structure

AUDIO SYNCHRONIZATION SIGNAL PATH

LP3950 audio synchronization is mainly done digitally and it consists of the following signal path blocks (see Figure 26):

- Input buffers
- Multiplexer
- AD converter
- DC remover
- Automatic gain control (AGC) / programmable gain
- 3 band digital filter
- Peak detector
- Look-up tables (LUT)
- Mode selector
- Integrators
- PWM generator

Functional Block Diagram

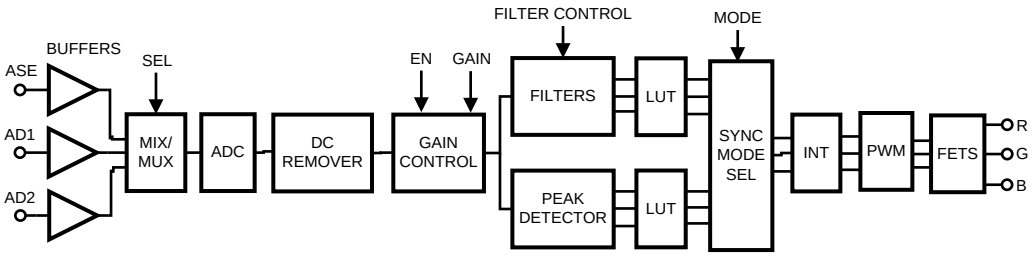


Figure 26. Signal Path Block Diagram

The digitized input signal has a DC component that is removed by the digital **DC REMOVER** (-3 dB @ 400 Hz). The automatic **GAIN CONTROL** adjusts the input signal to suitable range automatically. User can disable AGC and the gain can be set manually with **PROGRAMMABLE GAIN**. The LP3950 has two audio synchronization modes: amplitude and frequency. For amplitude based synchronization the **PEAK DETECTION** method is used. For frequency based synchronization the three-way crossover **FILTER** separates high pass, low pass and band pass signals. For both modes, a predefined lookup table (LUT) is used to match the audio visual effect. The **MODE SELECTOR** selects the synchronization mode. Reaction speed can be selected using **INTEGRATOR** speed variables. Finally **PWM GENERATOR** sets the driver FETs duty cycles.

Table 4. Audio Synchronization Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Zin	Input Impedance of AD1, AD2, ASE pins		200	500		kΩ
A_{IN_SINGLE}	Audio Input Level Range (peak-to-peak), Single Ended Audio		0.1		V_{DDA} −0.1	V
A_{IN_DIFF}	Audio Input Level Range (peak-to-peak), Differential Audio		0.1		V_{DDA} −0.1	V
$f_{3\ dB}$	Crossover Frequencies (−3 dB)					kHz
	Narrow Frequency Response	Low Pass Band Pass High Pass		0.5 1.0 and 1.5 2.0		
	Wide Frequency Response	Low Pass Band Pass High Pass		1.0 2.0 and 3.0 4.0		

CONTROL OF AUDIO SYNCHRONIZATION

The following table describes the controls required for audio synchronization. Note that these controls are functional when using serial interface (I^2C or SPI) for device control. Also LP3950 audio synchronization functionality is illustrated in Figure 27.

Table 5. Audio Synchronization Control

EN_SYNC	Audio synchronization enabled. Set EN_SYNC = 1 to enable audio synchronization or 0 to disable.			
SYNC_MODE	Synchronization mode selector. Set SYNC_MODE = 0 for amplitude synchronization. Set SYNC_MODE = 1 for frequency synchronization.			
MODE_CTRL[1:0]	See below: Mode control			
EN_AGC	Automatic gain control. Set EN_AGC = 1 to enable automatic control or 0 to disable. When EN_AGC is disabled, the audio input signal gain value is defined by GAIN_SEL.			
GAIN_SEL[2:0]	Input signal gain control. Gain has a range from 0 dB to 21 dB with 3 dB steps:			
	[000] ... 0 dB	[011] ... 9 dB	[110] ... 18 dB	
	[001] ... 3 dB	[100] ... 12 dB	[111] ... 21 dB	
	[010] ... 6 dB	[101] ... 15 dB		
INPUT_SEL[1:0]	[00] ... Single ended input signal, ASE. [01] ... Differential input signal, AD1 and AD2. [10] ... Stereo input or single ended and differential input signal. Note: Sum of input signals divided by 2. [11] ... No input Please see Figure 24 for wiring.			
SPEED_CTRL[1:0]	Control for speed of the mapping. Sets the reaction speed (or "sampling rate") for the audio input signal:			
	[00] ... FASTEST	[01] ... FAST	[10] ... MEDIUM	
	[11] ... SLOW			
	In the amplitude mode f_{MAX} = 3.8 Hz, in the frequency mode f_{MAX} = 7.6 Hz.			

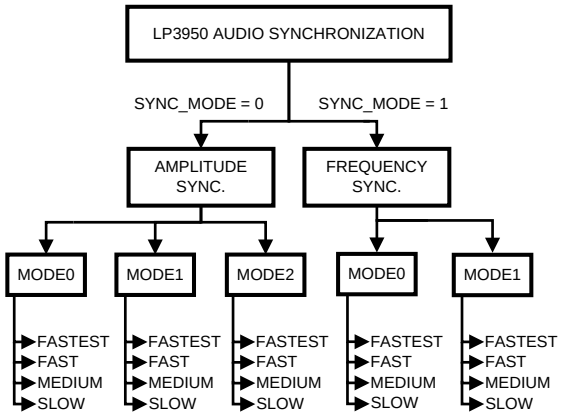


Figure 27. LP3950 Audio Synchronization Functionality

MODE CONTROL IN THE FREQUENCY MODE

During the frequency mode (SYNC_MODE = 1) the user can select between two filter options by MODE_CTRL[1:0] as shown below (Figure 29). User can select the filters based on the music type and light effect requirements. Filter options: Left figure, wide frequency response; MODE_CTRL[1:0] is set to [00], [10] or [11]. Right figure, narrow frequency response: MODE_CTRL[1:0] set to [01]. Signal passed through the lowpass filter is used to control the duty cycle of red LEDs (R1 and/or R2 PWM outputs), the signal passed through the bandpass filter is used to control green LEDs (G1 and/or G2 PWM outputs) and high pass signal controls blue LEDs (B1 and/or B2 PWM outputs). Finally, the user can select the desired mapping speed by SPEED_CTRL[1:0]. Of course, the user can connect any color LED to any output in his/her own application (i.e. the red output does not need to drive a red LED). Maximum duty cycle is 100% as in the Flash mode (not 33% as in the normal mode of the pattern generator, which is described in Table 3).

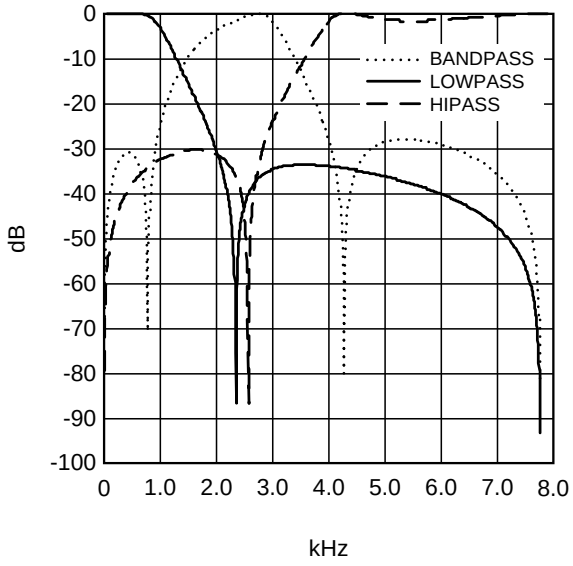


Figure 28. Cross-over Frequency Left: Wide Frequency Response

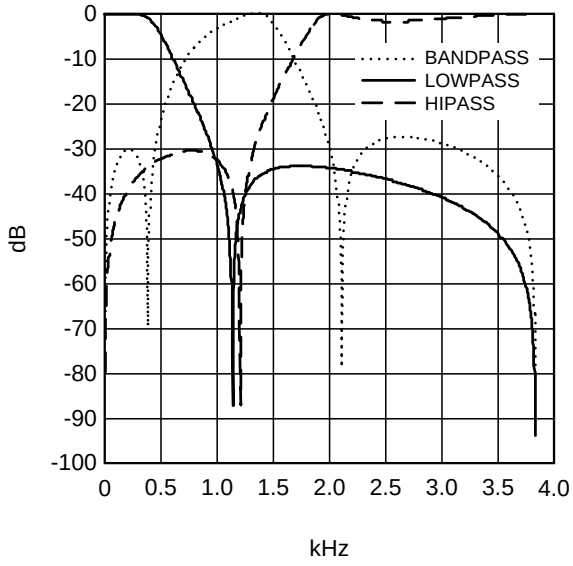
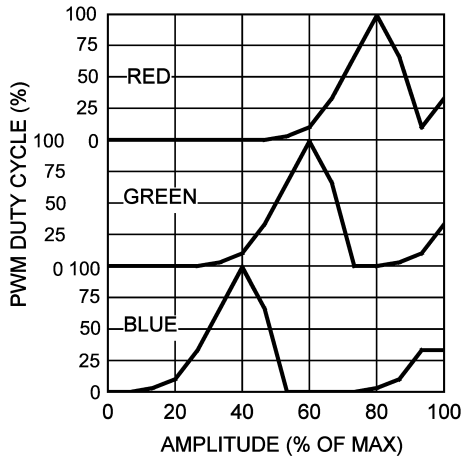


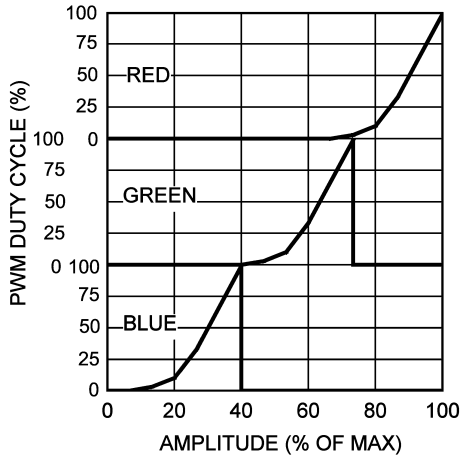
Figure 29. Cross-over Frequency Right: Narrow Frequency Response

MODE CONTROL IN THE AMPLITUDE MODE

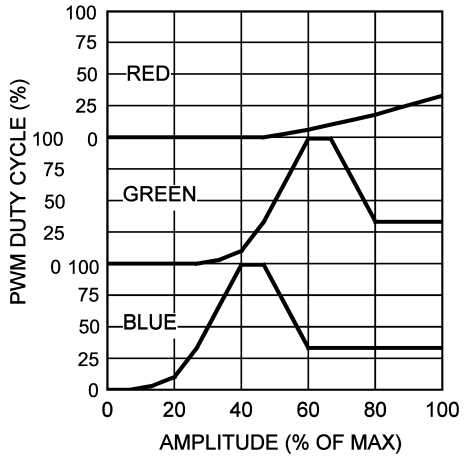
During the amplitude synchronization mode (SYNC_MODE = 0) the user can select between three different amplitude mappings by using MODE_CTRL[1:0] select. These three mapping options give different light responses as shown in Figure 30. Again, the user can select the desired mapping speed by SPEED_CTRL[1:0]. Maximum duty cycle is 100%. If MODE_CTRL[1:0] = 11 and SYNC_MODE = 0, audio synchronization is inactive.



MODE_CTRL[1:0] = [00] = MODE0



MODE_CTRL[1:0] = [01] = MODE1



MODE_CTRL[1:0] = [10] = MODE2

This figure is for illustrating purpose only and does not necessarily represent the accurate function of the circuit.

Figure 30. Amplitude Synchronization Mapping Options

MODE CONTROL IN THE DEFAULT MODE

One of the main benefits of LP3950 is the default mode, which enables user to build applications without I^2C or SPI control. The LP3950 is set to the default mode when DME pin is high. DME pin high –state forces registers NSTBY and EN_SYNC to the high [1] state so that the start-up sequence get started (see start-up sequence on Modes of Operation). Function of LP3950 in the default mode of operation is controlled by AMODE pin. If AMODE is pulled low the LP3950 is in the amplitude synchronization mode. If the AMODE pin is pulled high the LP3950 is in the frequency synchronization mode. In the default mode default control register values are used, see Table 8. Please refer to Figure 32 in Typical Applications for wiring.

RGB OUTPUT SELECTOR

The usage of RGB outputs (RGB1 and RGB2) can be selected with RGB_SEL[1:0] control bits. Audio synchronization and RGB pattern generator output can be connected to RGB ports as shown in the following table.

Table 6. RGB Output Control

RGB_SEL[0]	RGB_SEL[1]	RGB1 Output Control	RGB2 Output Control
0	0	Pattern Generator	Pattern Generator
1	0	Audio Sync	Pattern Generator
0	1	Pattern Generator	Audio Sync
1	1	Audio Sync	Audio Sync

Recommended External Components

OUTPUT CAPACITOR, C_{OUT}

The output capacitor C_{OUT} directly affects the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR (Equivalent Series Resistance) are the best choice. At the lighter loads, the low ESR ceramics offer a much lower V_{OUT} ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower V_{OUT} ripple magnitude than the tantalums of the same value. However, the dv/dt of the V_{OUT} ripple with the ceramics is much lower that the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 10V is recommended.

Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied voltage. The capacitance value can fall to below half of the nominal capacitance. Too low output capacitance can make the boost converter unstable.

INPUT CAPACITOR, C_{IN}

The input capacitor C_{IN} directly affects the magnitude of the input ripple voltage and to a lesser degree the V_{OUT} ripple. A higher value C_{IN} will give a lower V_{IN} ripple. Capacitor voltage rating must be sufficient, 10V is recommended.

OUTPUT DIODE, D_1

A Schottky diode should be used for the output diode. To maintain high efficiency the average current rating of the schottky diode should be larger than the peak inductor current (1.0A). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

INDUCTOR, L_1

LP3950's high switching frequency enables the use of a small surface mount inductor. A 4.7 µH shielded inductor is suggested for 2.0 MHz switching frequency. Values below 2.2 µH should not be used at 2.0 MHz. At lower switching frequencies 4.7 µH inductors should always be used. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation (1.0A). Less than 300 mΩ ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and, thus, may interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the SW pin as close to the IC as possible. Examples of suitable inductors are TDK type VLF4012AT- 4R7M1R1 and Coilcraft type MSS4020-472MLD.

Table 7. List of Recommended External Components

Symbol	Symbol Explanation	Value	Unit	Type
C_{VDD1}	V_{DD1} Bypass Capacitor	100	nF	Ceramic, X5R
C_{VDD2}	V_{DD2} Bypass Capacitor	100	nF	Ceramic, X5R
C_{OUT}	Output Capacitor from FB to GND	10 ± 10%	µF	Ceramic, X5R
C_{IN}	Input Capacitor from Battery Voltage to GND	10 ± 10%	µF	Ceramic, X5R
C_{VDDIO}	V_{DD_IO} Bypass Capacitor	100	nF	Ceramic, X5R
C_{VDDA}	V_{DDA} Bypass Capacitor	100	nF	Ceramic, X5R
$C_{1,2,3}$	Audio Input Capacitors	10	nF	Ceramic, X5R
R_T	Oscillator Frequency Bias Resistor	82	kΩ	1% (1)
R_{SO}	SO Output Pull-up Resistor	100	kΩ	
C_{VREF}	Reference Voltage Capacitor, between V_{REF} and GND	100	nF	Ceramic, X5R
L_1	Boost Converter Inductor	4.7	µH	Shielded, Low ESR, I_{SAT}1.0A
D_1	Rectifying Diode, V_F @ Maxload	0.3	V	Schottky Diode
	RGB LED	User Defined		
	Red, Green, Blue or White LEDs			
R_{RX}, R_{GX}, R_{BX}	Current Limit Resistors			

(1) Resistor RT tolerance change will change the timing accuracy of RGB block. Also the boost converter switching frequency will be affected.

PCB Design Guidelines

Printed circuit board layout is critical to low noise operation and good performance of the LP3950. Bypass capacitors should be close to the V_{DD} pins of the integrated circuit. Special attention must be given to the routing of the switching loops. Lengths of these loops should be minimized. It is essential to place the input capacitor, the output capacitor, the inductor and the schottky diode very close to the integrated circuit and use wide routings for those components. Sensitive components should be placed far from those components with high pulsating current. A ground plane is recommended.

The power switch loop (the switch is on) has the greatest affect on noise generation. The loop is formed by the input capacitor, the inductor, the SW pin, the GND_BOOST pin and the ground plane, as shown by the dashed line in Figure 31. The other switching loop, the rectifier loop, is formed by the input capacitor, the inductor, the diode, the output capacitor and the ground plane, as shown by the dotted line. Arrange the components so that the switching current loops curl in the same direction (see arrows in Figure 31). See also Application Note AN 1149, Layout Guidelines for Switching Mode Power Supplies.

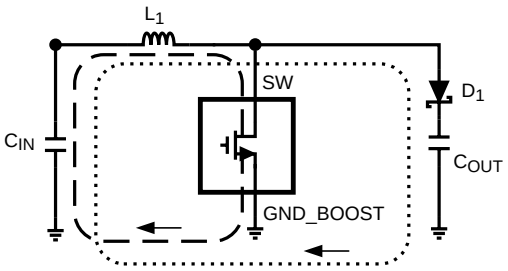


Figure 31. The Current Loops

Typical Applications

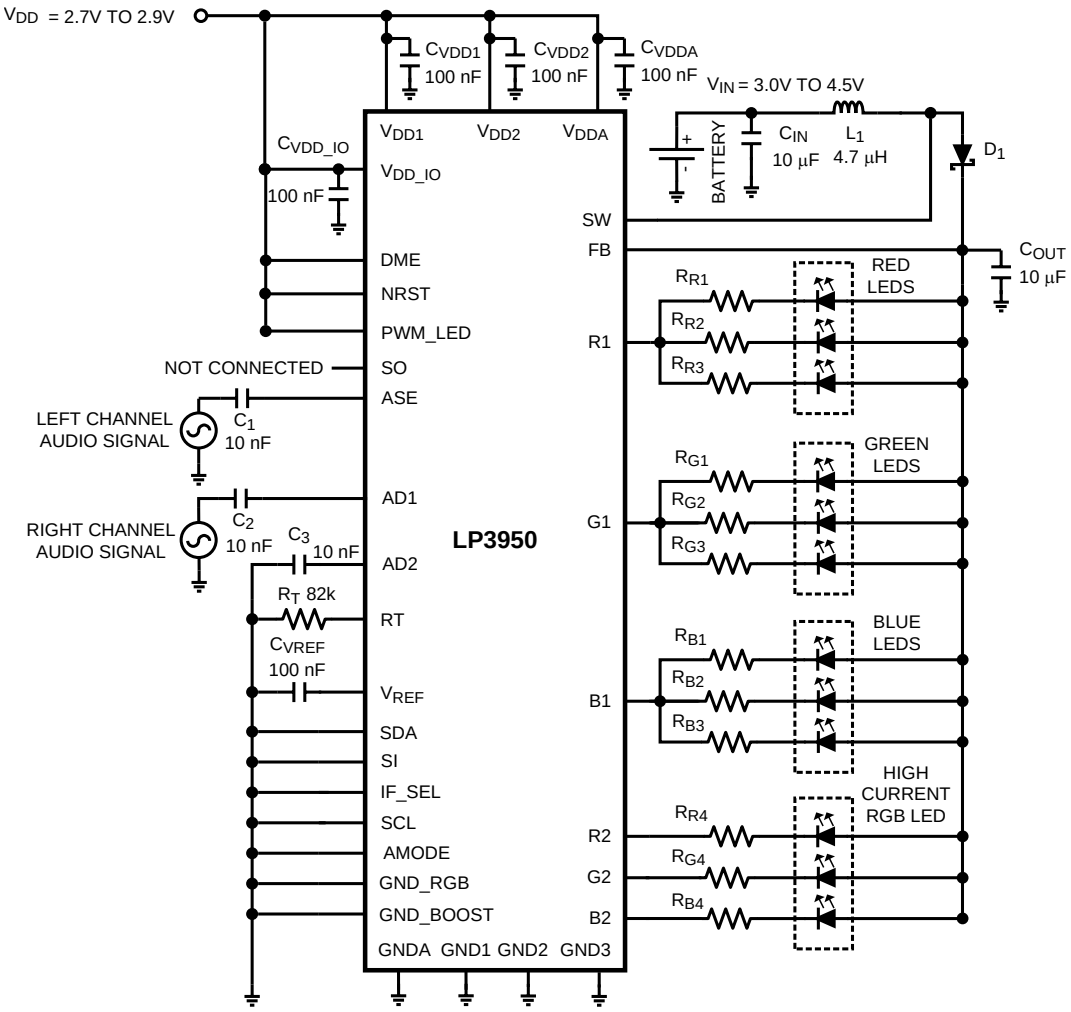
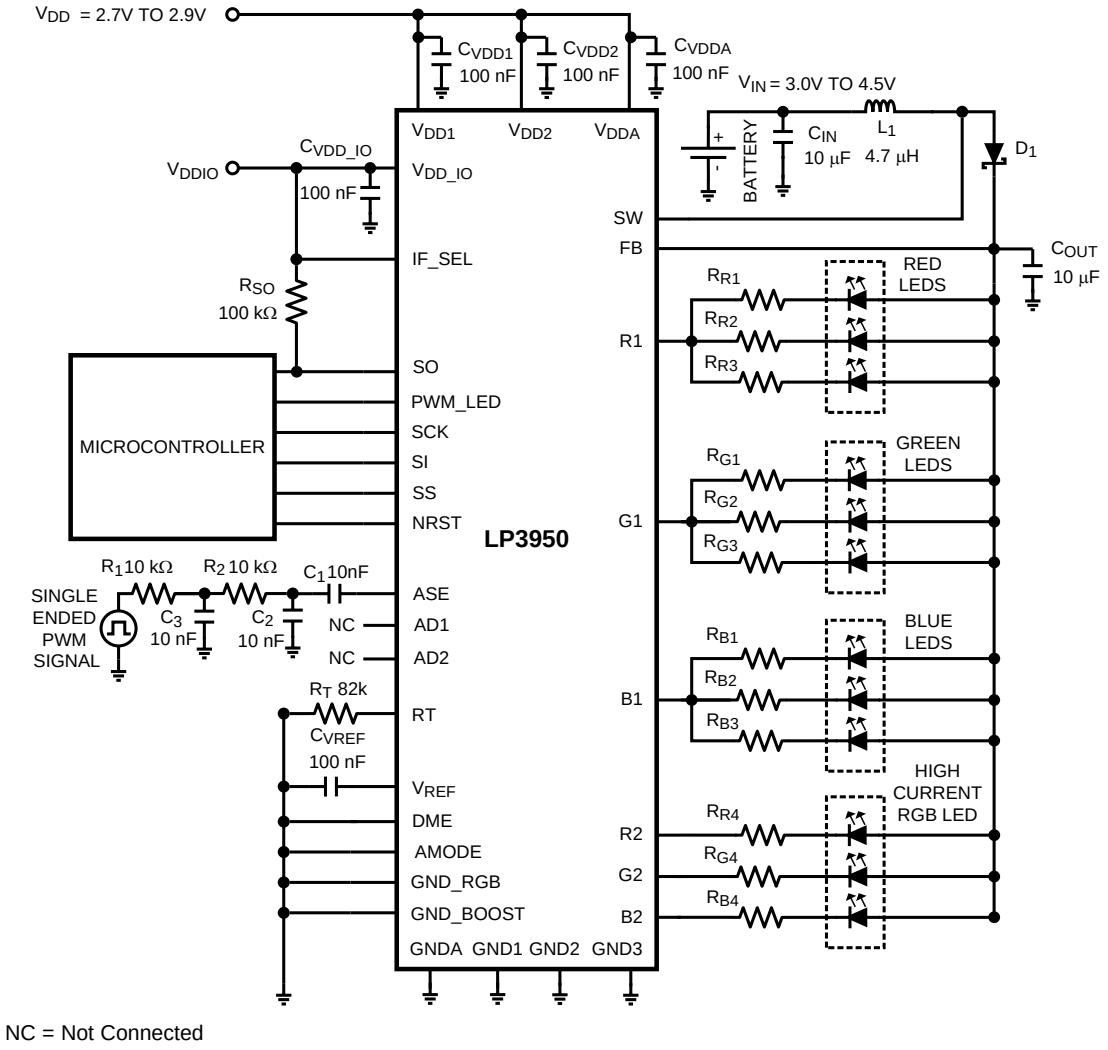


Figure 32. The LP3950 Set to the Default Mode



NC = Not Connected

Figure 33. Typical Application of LP3950 When the SPI Interface Is Used

Here, a second order RC-filter is used on the ASE input to convert a PWM signal to an analog waveform.

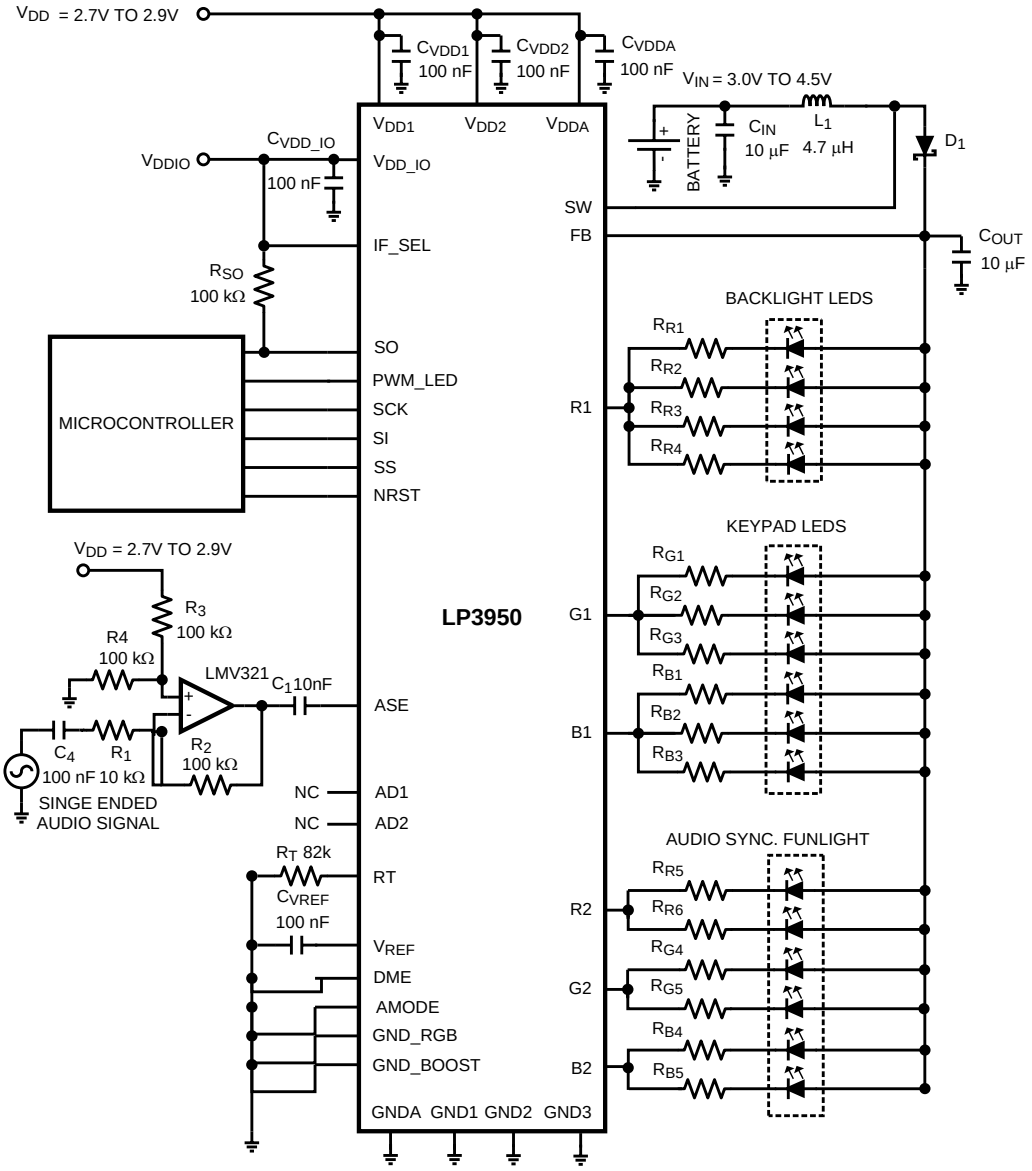


Figure 34. Backlight and Keypad LEDs Controlled by the Pattern Generator Funlight LEDs Controlled by Audio Synchronization

There may be cases where the audio input signal going into the LP3950 is too weak for audio synchronization. This figure presents a single-supply inverting amplifier connected to the ASE input for audio signal amplification. The amplification is +20 dB, which is well enough for 20 mV_{p-p} audio signal. Because the amplifier (LMV321) is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the input signal is within the input common-mode voltage range of the amplifier. The capacitor C_4 is placed between the inverting input and resistor R_1 to block the DC signal going into the audio signal source. The values of R_1 and C_4 affect the cutoff frequency, $f_c = 1/(2*Pi*R_1*C_4)$, in this case it is around 160 Hz. As a result, the LMV321 output signal is centered around mid-supply, that is $V_{DD}/2$. The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system

Table 8. LP3950 Control Register Names and Default Values

ADDR (HEX)	SETUP	D7	D6	D5	D4	D3	D2	D1	D0
00	RGB CONTROL	RGB PWM **0**	RGB START **0**	RSW1 **0**	GSW1 **0**	BSW1 **0**	RSW2 **0**	GSW2 **0**	BSW2 **0**
01	RED ON/OFF	RON[3] **0**	RON[2] **0**	RON[1] **0**	RON[0] **0**	ROFF[3] **0**	ROFF[2] **0**	ROFF[1] **0**	ROFF[0] **0**
02	GREEN ON/OFF	GON[3] **0**	GON[2] **0**	GON[1] **0**	GON[0] **0**	GOFF[3] **0**	GOFF[2] **0**	GOFF[1] **0**	GOFF[0] **0**
03	BLUE ON/OFF	BON[3] **0**	BON[2] **0**	BON[1] **0**	BON[0] **0**	BOFF[3] **0**	BOFF[2] **0**	BOFF[1] **0**	BOFF[0] **0**
04	RED SLOPE & DUTY CYCLE	RSLOPE[3] **0**	RSLOPE[2] **0**	RSLOPE[1] **0**	RSLOPE[0] **0**	RDUTY[3] **0**	RDUTY[2] **0**	RDUTY[1] **0**	RDUTY[0] **0**
05	GREEN SLOPE & DUTY CYCLE	GSLOPE[3] **0**	GSLOPE[2] **0**	GSLOPE[1] **0**	GSLOPE[0] **0**	GDUTY[3] **0**	GDUTY[2] **0**	GDUTY[1] **0**	GDUTY[0] **0**
06	BLUE SLOPE & DUTY CYCLE	BSLOPE[3] **0**	BSLOPE[2] **0**	BSLOPE[1] **0**	BSLOPE[0] **0**	BDUTY[3] **0**	BDUTY[2] **0**	BDUTY[1] **0**	BDUTY[0] **0**
07	CYCLE PWM	CYCLE[1] **0**	CYCLE[0] **0**	R1_PWM **0**	G1_PWM **0**	B1_PWM **0**	R2_PWM **0**	G2_PWM **0**	B2_PWM **0**
0B	ENABLES	CYCLE[2] **0**	NSTBY **0**	EN_BOOST **0**	EN_FLASH **0**		AUTOLOAD_EN **1**	RGB_SEL[1] **1**	RGB_SEL[0] **1**
0C	BOOST FREQUENCY						FREQ_SEL[2] **1**	FREQ_SEL[1] **1**	FREQ_SEL[0] **1**
0D	BOOST OUTPUT VOLTAGE	BOOST[7] **0**	BOOST[6] **0**	BOOST[5] **1**	BOOST[4] **1**	BOOST[3] **1**	BOOST[2] **1**	BOOST[1] **1**	BOOST[0] **1**
2A	AUDIO SYNC CONTROL 1	GAIN_SEL[2] **1**	GAIN_SEL[1] **0**	GAIN_SEL[0] **1**	SYNC_MODE **0**	EN_AGC **1**	EN_SYNC **0**	INPUT_SEL[0] **1**	INPUT_SEL[0] **0**
2B	AUDIO SYNC CONTROL 2					MODE_CTRL[1] **0**	MODE_CTRL[0] **1**	SPEED_CTRL[1] **0**	SPEED_CTRL[0] **1**

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	32

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3950SL/NOPB	ACTIVE	TLGA	NPC	32	1000	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LP3950SL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

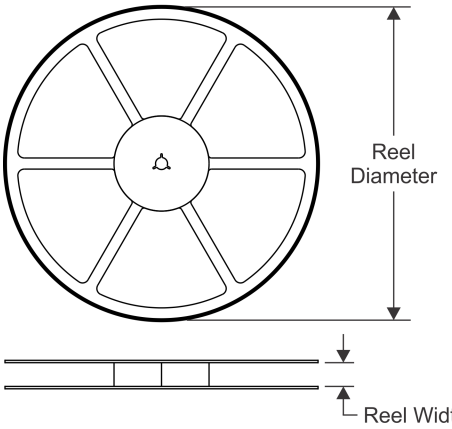
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

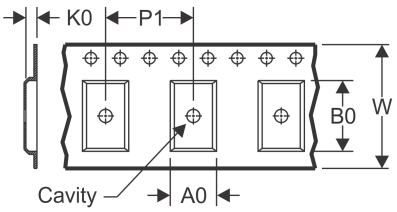
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

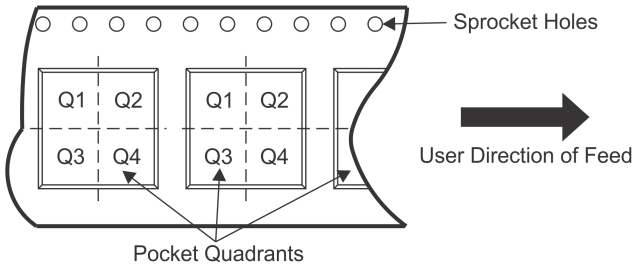


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

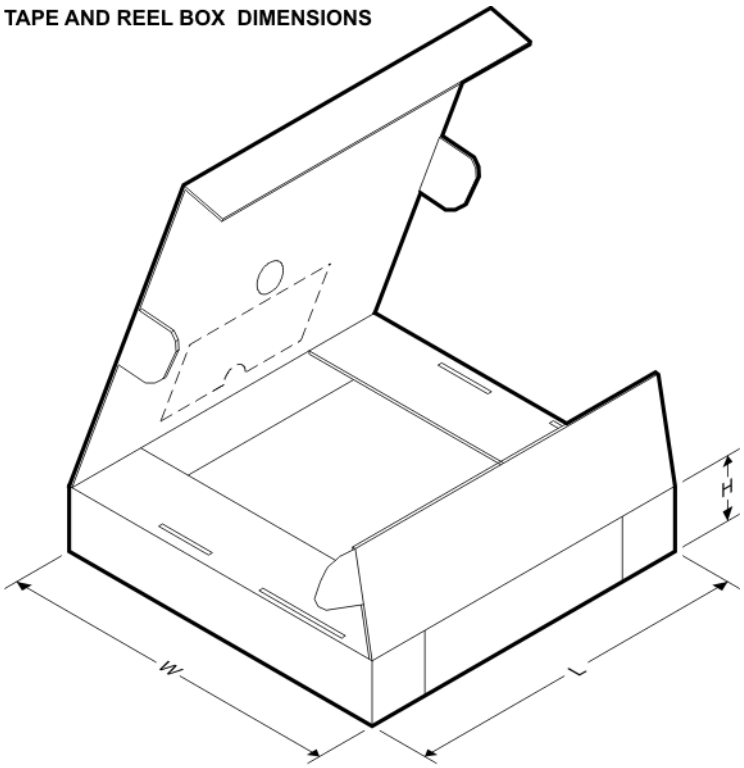
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3950SL/NOPB	TLGA	NPC	32	1000	178.0	12.4	4.8	5.8	1.3	8.0	12.0	Q1

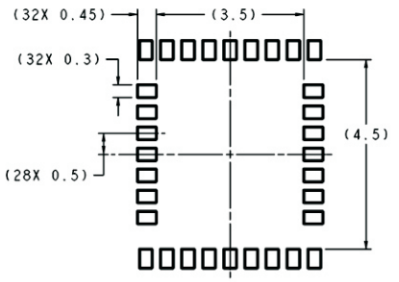
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

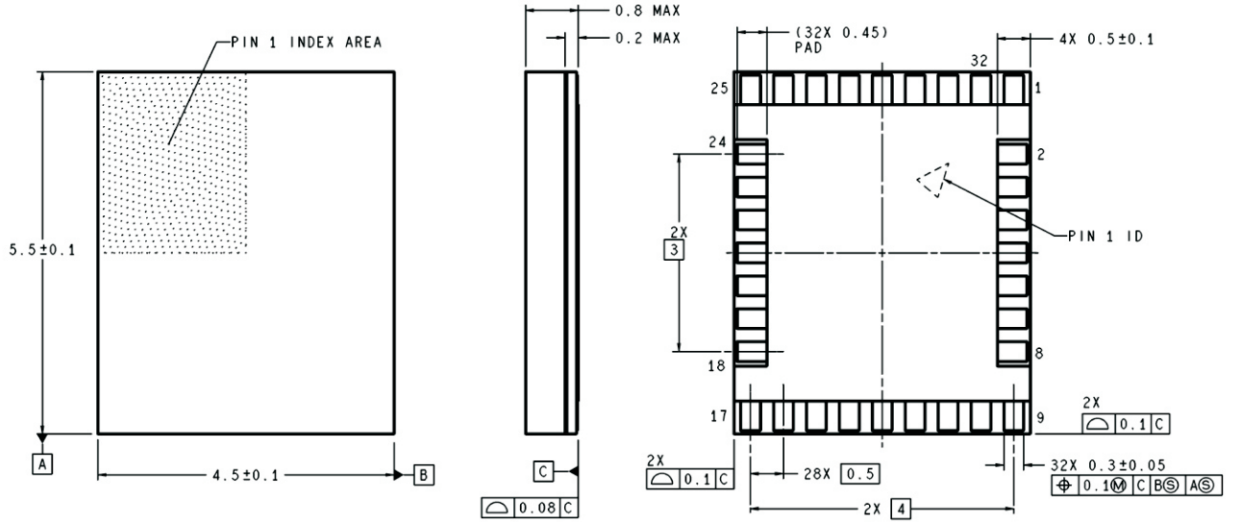
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3950SL/NOPB	TLGA	NPC	32	1000	210.0	185.0	35.0

NPC0032A



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



SLD32A (Rev A)

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