TPSM63603
SLVSFS5 – MARCH 2021

TPSM63603 High-Density, 3-V to 36-V Input, 1-V to 16-V Output, 3-A Power Module

1 Features

- Integrated controller, MOSFETs, and inductor
- 4.0-mm × 6.0-mm × 1.8-mm overmolded package
- Wide input voltage range: 3.0 V to 36 V
- Wide output voltage range: 1.0 V to 16 V
- Best in-class efficiency
- Switching frequency range: 200 kHz to 2.2 MHz
- Frequency synchronization
- FPWM mode of operation
- 1% total output voltage accuracy
- Low I_Q current of 9-µA (non-switching)
- –40°C to 105°C ambient temperature range
- Undervoltage and overvoltage power good
- Optimized for ultra-low EMI requirements
  - Spread spectrum (S suffix) reduces peak emissions
  - Adjustable SW node slew rate
  - Meets CISPR22 and CISPR32 class B emissions
- Monotonic start-up into prebiased output
- No external loop-compensation components
- Precision enable with hysteresis for external UVLO
- Thermal shutdown protection with hysteresis
- Create a custom design using the TPSM63603 with the WEBENCH® Power Designer

2 Applications

- Test and measurement
- Factory automation and control
- Aerospace and defense
- General purpose power supplies

3 Description

The TPSM63603 power module is a highly integrated 3-A power solution that combines a 36-V input, step-down DC/DC converter with power MOSFETs, a shielded inductor, and passives in a thermally enhanced QFN package. The 30-pin QFN package has enhanced thermal performance, small footprint, and low EMI. The package footprint has all signal and power pins accessible from the perimeter as well as four larger thermal pads beneath the device for simple layout and easy handling in manufacturing.

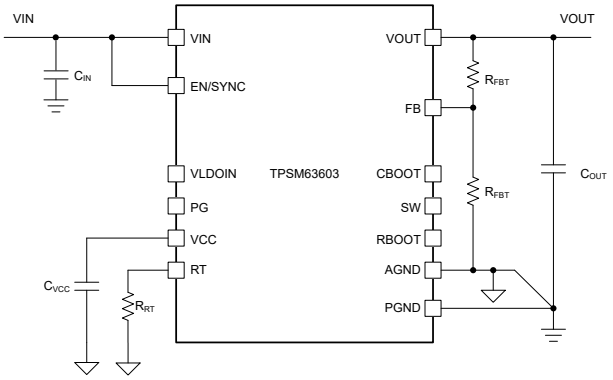
The TPSM63603 is a compact, easy-to-use power module with a wide output voltage range of 1.0 V to 16 V. The module is designed to quickly and easily implement a power design in a small PCB footprint. The total solution requires as few as four external components and eliminates the loop compensation and magnetics part selection from the design process.

Although designed for small size and simplicity, the TPSM63603 offers many features: precision enable with hysteresis allows external adjustable UVLO, adjustable SW node slew rate for improving EMI, and a power-good indicator allows sequencing and output voltage monitoring. The small package size is a good fit for space-constrained applications.

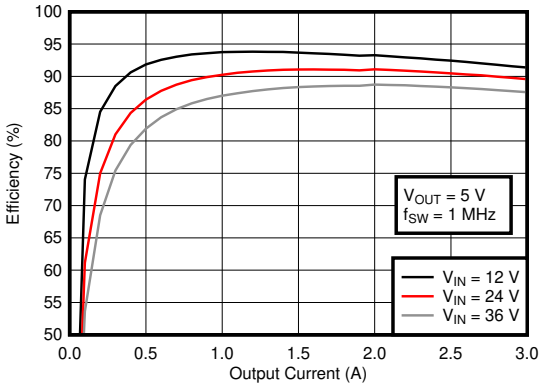
Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPSM63603	QFN-RDH (30)	4.0 mm × 6.0 mm
TPSM63603S		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Schematic



Typical Efficiency, V_{OUT} = 5 V

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4 Revision History

DATE	REVISION	NOTES
March 2021	*	Initial Release

5 Pin Configuration and Functions

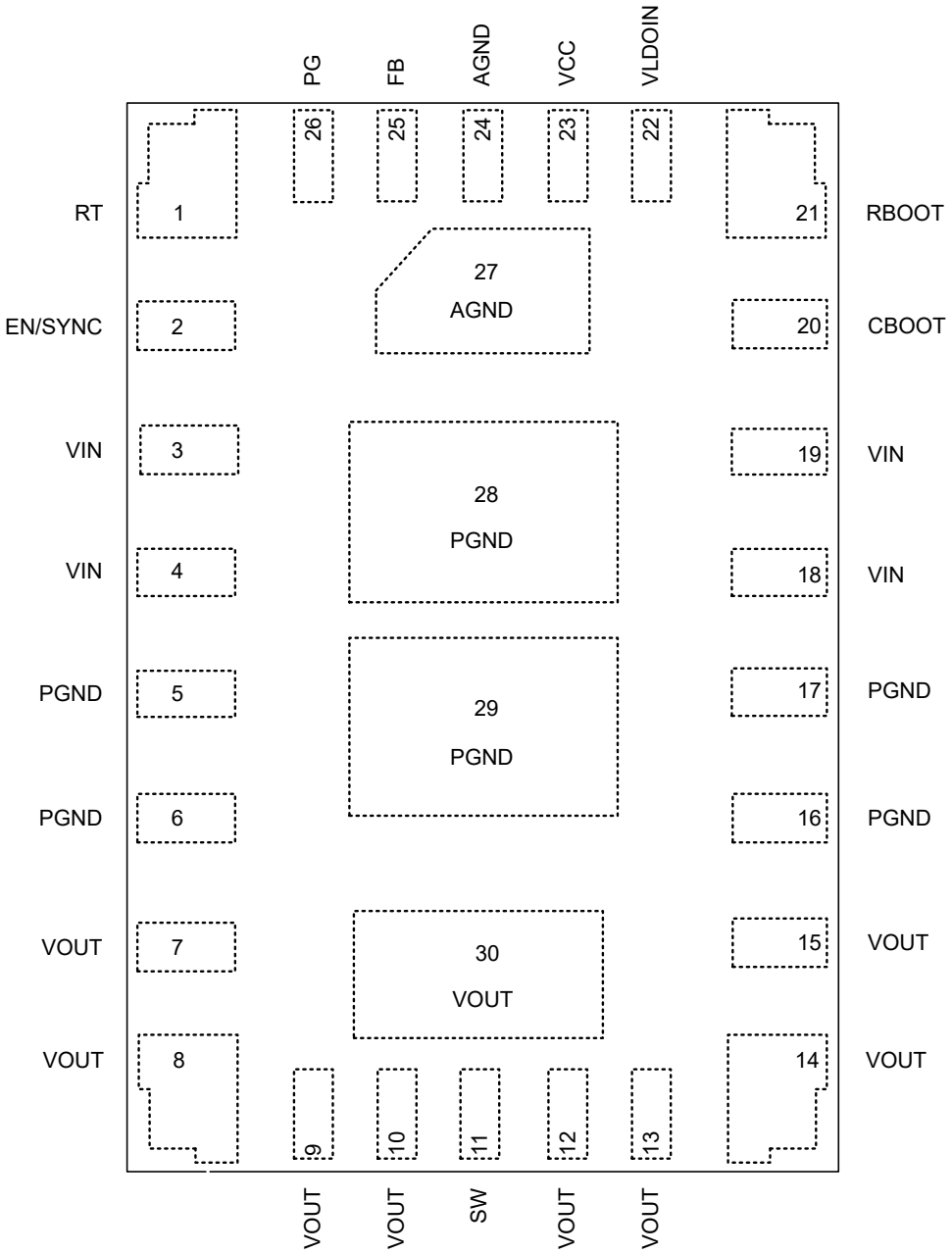

Figure 5-1. 30-Pin QFN RDH Package, (Top View)

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Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
24, 27	AGND	G	Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. **This pin must be connected to PGND at a single point.** See Section 10.2 for a recommended layout.
20	CBOOT	I/O	Bootstrap pin for internal high-side driver circuitry. A bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage. This pin is brought out to use in conjunction with RBOOT to effectively lower the value of the internal RBOOT resistor to adjust the SW node slew rate, if necessary.
2	EN/SYNC	I	Precision enable input pin. High = on, Low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. It also functions as the synchronization input pin. Used to synchronize the device switching frequency to a system clock. Triggers on the rising edge of an external clock. A capacitor can be used to AC couple the synchronization signal to this pin. When synchronized to an external clock, the device functions in Forced PWM. The converter can be turned off by using an open-drain/collector device to connect this pin to AGND. An external voltage divider can be placed between this pin, AGND, and VIN to create an external UVLO.
25	FB	I	Feedback input. Connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND. Do not leave open or connect to ground.
26	PG	O	Power-good pin. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required to a suitable pullup voltage. If not used, this pin can be left open or connected to PGND.
5, 6, 16, 17, 28, 29	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect this pad to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins. See Section 10.2 for a recommended layout.
21	RBOOT	I/O	External bootstrap resistor connection. Internal to the device, a 100-Ω bootstrap resistor is connected between this pin and the CBOOT pin. This pin is brought out to use in conjunction with CBOOT to effectively lower the value of the internal RBOOT resistor to adjust the SW node slew rate, if necessary.
1	RT	I	Frequency setting pin. This analog pin is used to set the switching frequency between 200 kHz and 2200 kHz by placing an external resistor from this pin to AGND. Do not leave open or connect to ground.
11	SW	O	Switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on these pins must be kept to a minimum to prevent issues with noise and EMI.
23	VCC	O	Internal LDO output. Used as supply to internal control circuits. Do not connect to any external loads. Connect a high-quality 1-µF capacitor from this pin to AGND.
3, 4, 18, 19	VIN	I	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device.
22	VLDOIN	P	Input bias voltage. Supplies the control circuitry of the power converter. Input to internal LDO. Connect to an output voltage point to improve efficiency. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. If output voltage is above 12 V, connect this pin to ground.
7-10, 12–15, 30	VOUT	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.

(1) G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Limits apply over T_A = –40°C to +105°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to AGND, PGND	–0.3	40	V
	EN/SYNC to AGND, PGND	–0.3	40	V
	PG to AGND, PGND	0	20	V
	VLDOIN to AGND, PGND	–0.3	16	V
	FB to AGND, PGND	–0.3	16	V
	RT to AGND, PGND	–0.3	5.5	V
	CBOOT to SW	–0.3	5.5	V
	RBOOT to SW	–0.3	5.5	V
	PGND to AGND	–1	2	V
Output voltage	SW to AGND, PGND	–0.3	40	V
	VOUT to AGND, PGND	–0.3	16	V
	VCC to AGND, PGND	–0.3	5.5	V
Sink Current	PG sink current	–	10	mA
T_A	Operating ambient temperature(2)	–40	105	°C
T_J	Operating IC junction temperature(2)	–40	150	°C
T_{stg}	Storage temperature	-55	150	°C
Peak reflow case temperature			–	°C
Maximum number of reflows allowed			3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted			G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz			G

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±TBD	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Limits apply over T_A = –40°C to +105°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN (Input voltage range after start-up)	3		36	V
Output voltage	VOUT	1		16	V
Output current	IOUT	0		3	A
Frequency	F_{SW} set by RT or SYNC	200		2200	kHz
PG input current	PG			TBD	mA
PG pullup voltage	V_{PG-PU}	0		16	V
T_A	Operating ambient temperature	-40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPSM63603 RDH (QFN) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	33.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter(3)	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(4)	21.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 64-mm × 83-mm four-layer PCB with 2-oz. copper and natural convection cooling. Additional airflow and PCB copper area reduces $R_{\theta JA}$. For more information see the *Layout* section.

(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$, where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.

(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$, where Pdis is the power dissipated in the device and T_B is the temperature of the board 1 mm from the device.

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6.5 Electrical Characteristics

Limits apply over T_A = –40°C to +105°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, F_{SW} = 800 kHz, I_{OUT} = 3.0 A, (unless otherwise noted); minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input operating voltage range	Needed to start up (over I_{OUT} range)	3.95		36.0	V
		Once operating (Over I_{OUT} range)	3.0		36.0	V
V_{IN_HYS}	Hysteresis(1)			1.0		
I_{Q_VIN}	Input operating quiescent current (non-switching)	V_{EN} = 3.3 V, V_{FB} = 1.5 V		TBD		µA
I_{SDN_VIN}	V_{IN} shutdown quiescent current	V_{EN} = 0 V, T_A = 25°C		TBD		µA
ENABLE						
V_{EN_RISE}	EN voltage rising threshold		1.161	1.263	1.365	V
V_{EN_FALL}	EN voltage falling threshold			TBD		V
V_{EN_HYS}	EN voltage hysteresis		0.303	0.353	0.404	V
V_{EN_WAKE}	EN wake-up threshold		0.4			V
t_{EN}	EN HIGH to start of switching delay(1)			0.7		ms
INTERNAL LDO VCC						
V_{CC}	Internal LDO VCC output voltage	3.4 V ≤ V_{LDOIN} ≤ 12.5 V		3.3		V
		V_{LDOIN} = 3.1 V, non-switching		3.1		V
V_{CC_UVLO}	VCC UVLO rising threshold	V_{LDOIN} < 3.1 V(1)		3.6		V
		V_{IN} < 3.6 V(2)		3.6		V
$V_{CC\_UVLO\_HYS}$	VCC UVLO hysteresis(2)			1.1		V
FEEDBACK						
V_{OUT}	Adjustable output voltage range	Over I_{OUT} range	1.0		16.0	V
V_{FB}	Feedback voltage	T_A = 25°C, I_{OUT} = 0 A		1.0		V
V_{FB_ACC}	Feedback voltage accuracy	Across V_{IN} range, V_{OUT} = 1.0 V, I_{OUT} = 0 A, F_{SW} = 200 kHz, –40°C ≤ T_A ≤ 105°C	–1%		+1%	
V_{FB}	Load regulation	T_A = 25°C, 0 A ≤ I_{OUT} ≤ 3 A		TBD%		
V_{FB}	Line regulation	T_A = 25°C, I_{OUT} = 0 A, 4.0 V ≤ V_{IN} ≤ 36 V		TBD%		
I_{FB}	Input current into FB pin	V_{FB} = 1.0 V		10		nA
CURRENT						
I_{OUT}	Output current		0		3.0	A
I_{OCL}	Output overcurrent (DC) limit threshold			TBD		A
I_{L_HS}	High side switch current limit	Duty cycle approaches 0%	TBD	6.2	TBD	A
I_{L_LS}	Low side switch current limit		TBD	3.4	TBD	A
I_{L_NEG}	Negative current limit			–3		A
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage to enter hiccup	Not during soft start		40%		
t_W	Short circuit wait time before soft start (hiccup)(1)			80		ms
SOFT-START						
t_{SS}	Time from first SW pulse to V_{REF} at 90%	V_{IN} ≥ 4.2 V	3.5	5	7	ms
t_{SS2}	Time from first SW pulse to release of FPWM lockout if output not in regulation(1)	V_{IN} ≥ 4.2 V	9.5	13	17	ms

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6.5 Electrical Characteristics (continued)

Limits apply over T_A = –40°C to +105°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, F_{SW} = 800 kHz, I_{OUT} = 3.0 A, (unless otherwise noted); minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
PG_{OV}	PG upper threshold — rising	% of V_{OUT} setting	105%	107%	110%	
PG_{UV}	PG upper threshold — falling	% of V_{OUT} setting	92%	94%	96.5%	
PG_{HYS}	PG upper threshold hysteresis (rising and falling)	% of V_{OUT} setting		1.3%		
$V_{IN\_PG\_VALID}$	Input voltage for valid PG output	46-µA pullup, EN = 0 V	1.0			V
V_{PG_LOW}	Low level PG function output voltage	2-mA pullup to PG pin, EN = 0 V			0.4	V
I_{PG}	Input current into PG pin when open drain output is high	V_{PG} = 3.3 V		TBD		µA
$t_{PG\_FLT\_RISE}$	Delay time to PG high signal		1.5	2.0	2.5	ms
$t_{PG\_FLT\_FALL}$	Glitch filter time constant for PG function			120		µs
SWITCHING FREQUENCY						
f_{SW_RANGE}	Switching frequency range by R_T or SYNC		200		2200	kHz
f_{SW_RT}	Default switching frequency by R_T	R_T = 66.5 kΩ	180	200	220	kHz
f_{SW_RT}	Default switching frequency by R_T	R_T = 5.76 kΩ	1980	2200	2420	kHz
SYNCHRONIZATION						
V_{EN_SYNC}	Edge height necessary to synchronize	Rise/fall time < 30 ns			2.4	V
t_B	Blanking of EN after rising or falling edges(1)		4		28	µs
t_{SYNC_EDGE}	Sync signal hold time after edge for edge recognition(1)		100			ns
POWER STAGE						
t_{ON_MIN}	Minimum ON pulse width	V_{OUT} = 1 V, I_{OUT} = 1 A, RBOOT short to CBOOT		55	70	ns
t_{ON_MAX}	Maximum ON pulse width			9		µs
t_{OFF_MIN}	Minimum OFF pulse width	V_{IN} = 4 V, I_{OUT} = 1 A, RBOOT short to CBOOT		65	85	ns
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Temperature rising	158	168	180	°C
T_{HYST}	Thermal shutdown hysteresis (1)			10		°C
PERFORMANCE						
η	Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 1.5 A, T_A = 25°C		TBD%		
η	Efficiency	V_{OUT} = 5.0 V, I_{OUT} = 1.5 A, T_A = 25°C		TBD%		

(1) Specified by design; not production tested.

(2) Production tested with V_{IN} = 3.0 V

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6.6 Typical Characteristics (V_{IN} = 12 V)

Refer to Section 8.2 for circuit designs.

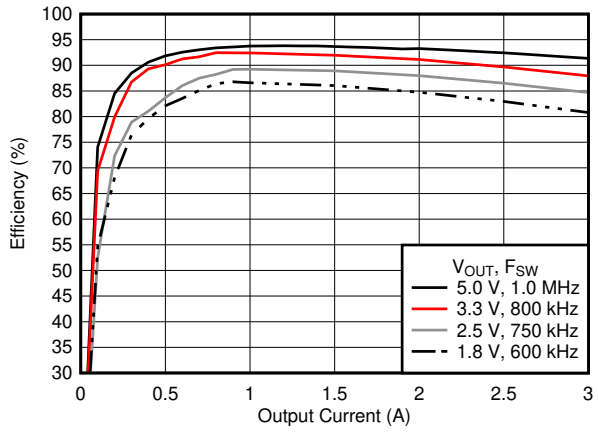


Figure 6-1. Efficiency

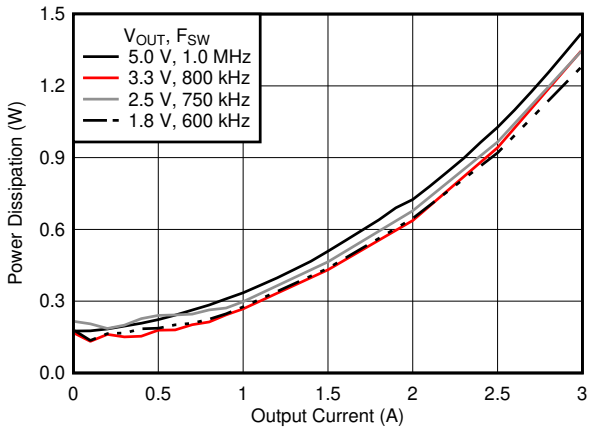
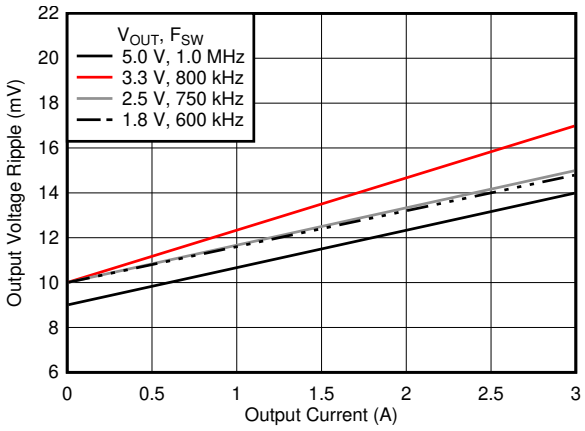
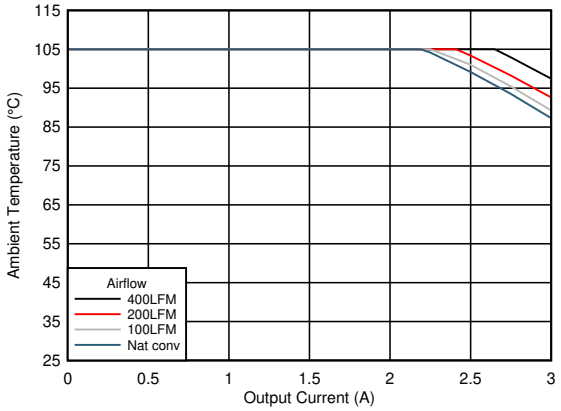


Figure 6-2. Power Dissipation



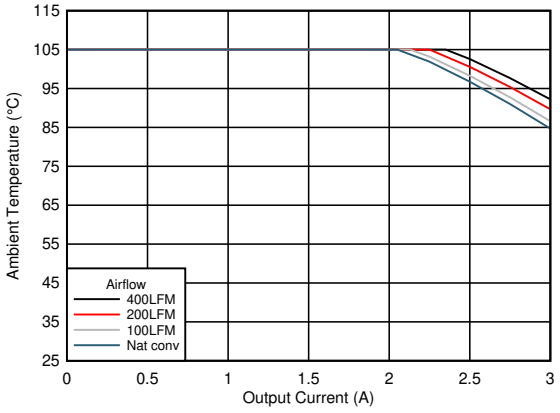
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-3. Output Voltage Ripple



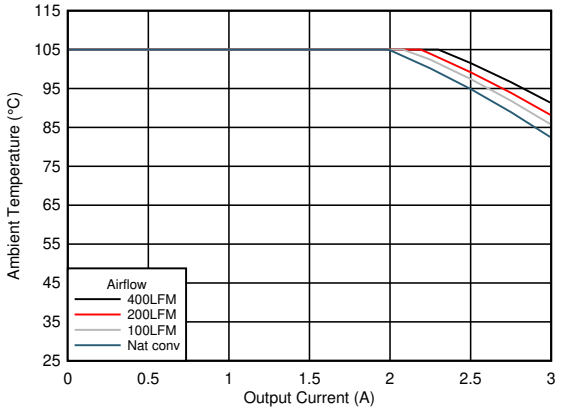
Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-4. Safe Operating Area (V_{OUT} = 1.8 V)



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-5. Safe Operating Area (V_{OUT} = 3.3 V)



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-6. Safe Operating Area (V_{OUT} = 5.0 V)

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6.7 Typical Characteristics (V_{IN} = 24 V)

Refer to Section 8.2 for circuit designs.

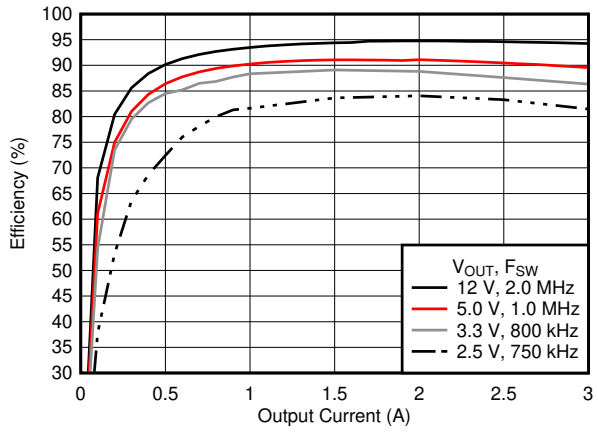


Figure 6-7. Efficiency

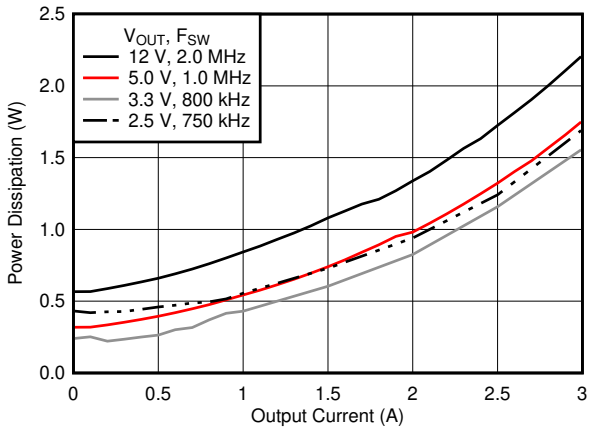
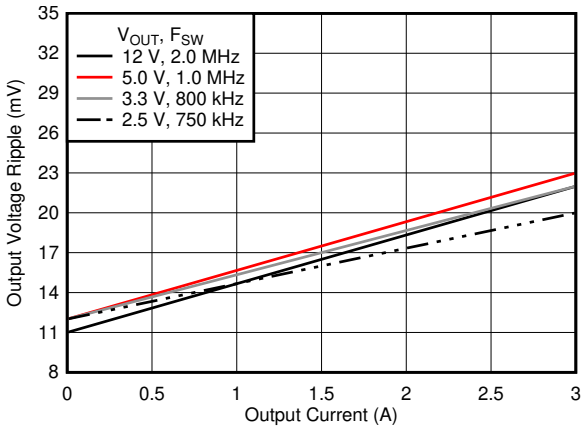
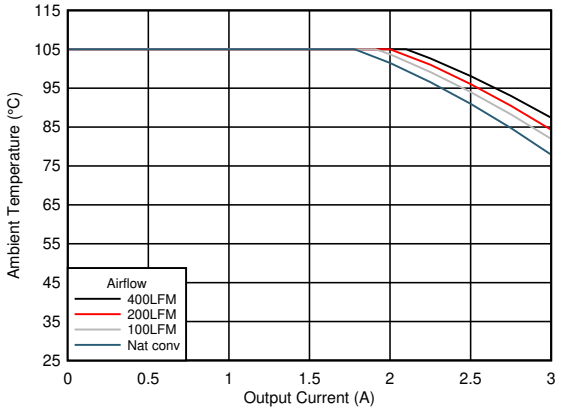


Figure 6-8. Power Dissipation



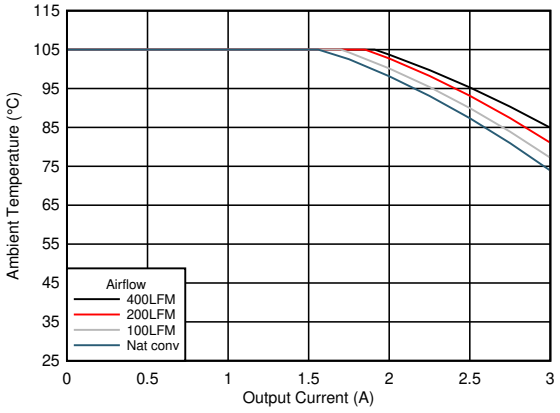
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-9. Output Voltage Ripple



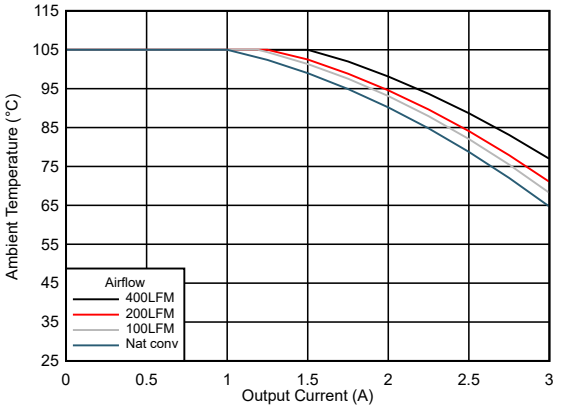
Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-10. Safe Operating Area (V_{OUT} = 3.3 V)



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-11. Safe Operating Area (V_{OUT} = 5.0 V)



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-12. Safe Operating Area (V_{OUT} = 12 V)

6.8 Typical Characteristics (V_{IN} = 36 V)

Refer to Section 8.2 for circuit designs.

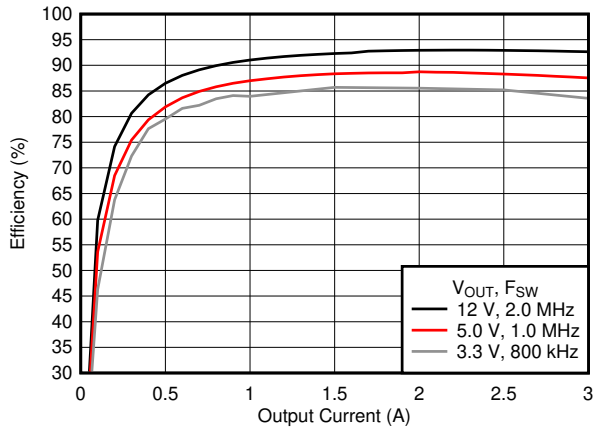


Figure 6-13. Efficiency

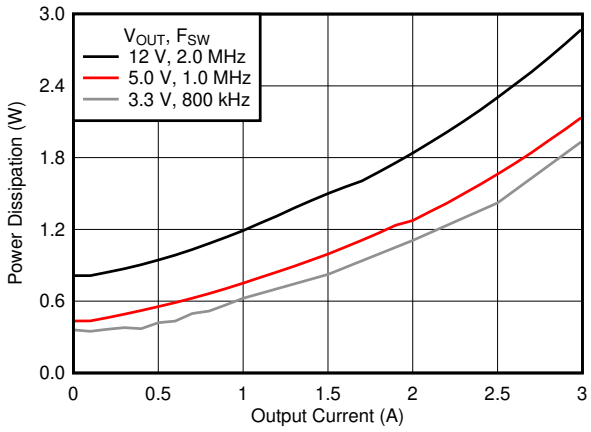
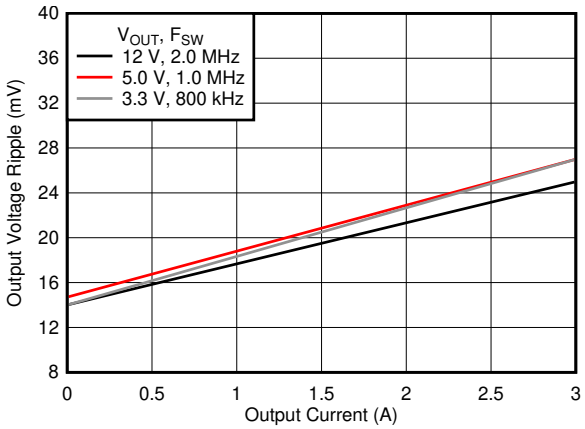
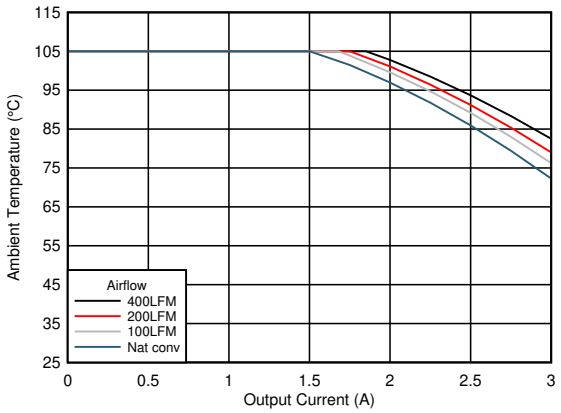


Figure 6-14. Power Dissipation



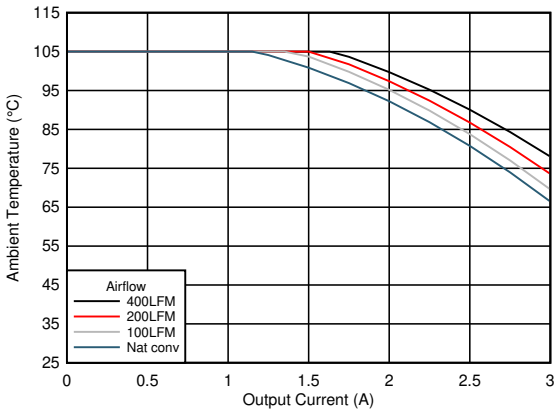
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-15. Output Voltage Ripple



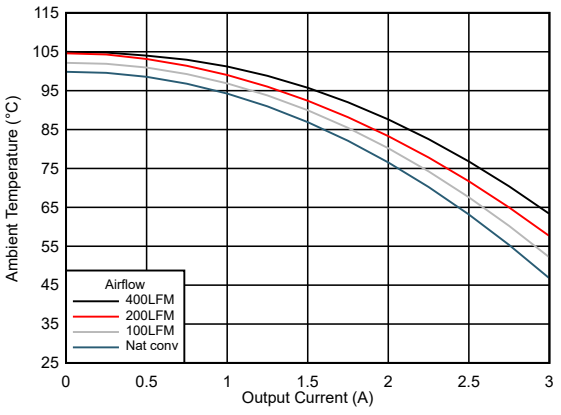
Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-16. Safe Operating Area (V_{OUT} = 3.3 V)



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-17. Safe Operating Area (V_{OUT} = 5.0 V)



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-18. Safe Operating Area (V_{OUT} = 12 V)

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7 Detailed Description

7.1 Overview

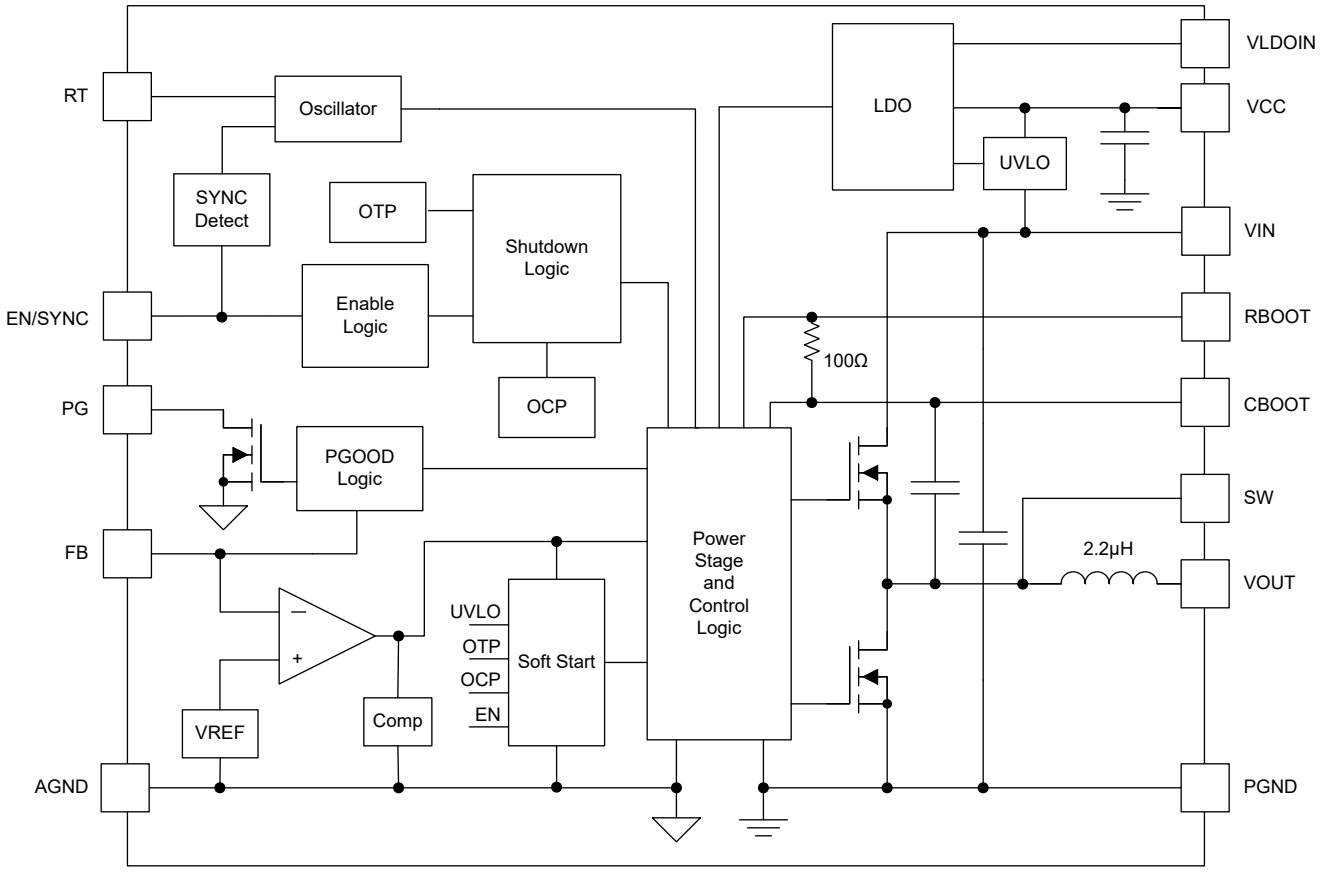
The TPSM63603 is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 36-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, and 24-V supply rails. With an integrated power controller, inductor, and MOSFETs, the TPSM63603 delivers up to 3-A DC load current, with high efficiency and ultra-low input quiescent current, in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

The TPSM63603 incorporates many features for comprehensive system requirements. The adjustable SW node rise time as well as the spread spectrum variant improve EMI performance. Other features include the following:

- Wide frequency synchronization from 200 kHz to 2.2 MHz
- An open-drain Power-Good circuit for power-rail sequencing and fault reporting
- Monotonic start-up into prebiased loads
- Precision enable for programmable line undervoltage lockout (UVLO)
- Thermal shutdown with automatic recovery

These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple layout, requiring few external components. See Section 10.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjustable Output Voltage (FB)

The TPSM63603 has an adjustable output voltage range of 1.0 V to 16 V. Setting the output voltage requires two resistors, R_{FBT} and R_{FBB} (see Figure 7-1). Connect R_{FBT} between VOUT, at the regulation point, and the FB pin. Connect R_{FBB} between the FB pin and AGND (pin 10). The recommended value of R_{FBT} is 10 kΩ. The value for R_{FBB} can be calculated using Equation 1. Table 7-1 lists the standard resistor values for several output voltages and the recommended switching frequency. The minimum required output capacitance for each output voltage is also included in Table 7-1. The capacitance values listed represent the effective capacitance, taking into account the effects of DC bias and temperature variation.

$$R_{FBB} = \frac{1.0}{V_{OUT} - 1.0} \times R_{FBT} \quad (1)$$

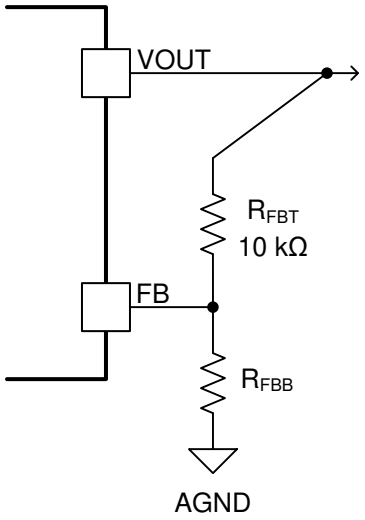


Figure 7-1. FB Resistor Divider

Table 7-1. Standard R_{FBB} Values, Recommended F_{SW} and Minimum C_{OUT}

V_{OUT} (V)	R_{FBB} (kΩ) (1)	RECOMMENDED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)	V_{OUT} (V)	R_{FBB} (kΩ) (1)	RECOMMENDED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)
1.0	open	400	300	3.3	4.32	800	40
1.2	49.9	500	200	5.0	2.49	1000	25
1.5	20.0	500	160	7.5	1.54	1300	20
1.8	12.4	600	120	10	1.10	1500	15
2.0	10.0	600	100	12	0.909	2000	5
2.5	6.65	750	65	15	0.715	2200	4
3.0	4.99	750	50	16	0.665	2200	3

(1) R_{FBT} = 10 kΩ

Selecting a R_{FBT} value of 10 kΩ is recommended for most applications. A larger R_{FBT} consumes less DC current, which is mandatory if light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see Section 10.

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7.3.2 Input Capacitors

The TPSM63603 requires a minimum of 2 × 4.7 µF of ceramic type input capacitance. Only use high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. Additional capacitance can be required for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. Table 7-2 includes a preferred list of capacitors by vendor.

Table 7-2. Recommended Input Capacitors

VENDOR(1)	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				WORKING VOLTAGE (V)	CAPACITANCE (2) (µF)
TDK	X7R	C3216X7R1H475K160AC	1206	50	4.7
Murata	X7R	GRM31CR71H475KA12L	1206	50	4.7
TDK	X7S	C3225X7S2A475K200AB	1210	100	4.7
Murata	X7S	GCM32DC72A475KE02L	1210	100	4.7

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.

(2) Specified capacitance values

7.3.3 Output Capacitor Selection

Table 7-1 lists the TPSM63603 minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance above $C_{OUT(MIN)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See Table 7-3 for a preferred list of output capacitors by vendor.

Table 7-3. Recommended Output Capacitors

VENDOR(1)	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE (V)	CAPACITANCE (µF)(2)
TDK	X7R	CGA5L1X7R1C106K160AC	1206	16	10
Murata	X7R	GCM31CR71C106KA64L	1206	16	10
TDK	X7R	C3216X7R1E106K160AB	1206	25	10
Murata	X7S	GCJ31CC71E106KA15L	1206	25	10
TDK	X5R	C3225X5R1C226M	1210	16	22
Murata	X5R	GRM32ER61C226K	1210	16	22
TDK	X5R	C3216X5R1E226M160AB	1206	25	22
Murata	X6S	GRM31CC81E226K	1206	25	22
Murata	X7R	GRM32ER71E226M	1210	25	22
TDK	X5R	C3225X5R1A476M	1210	10	47
Murata	X5R	GRM32ER61C476K	1210	16	47

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in Table 7-3.

(2) Specified capacitance values

7.3.4 Switching Frequency (RT)

The switching frequency range of the TPSM63603 is 200 kHz to 2.2 MHz. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin and AGND. Use Equation 2 to calculate the R_{RT} value for a desired frequency or simply select from Table 7-4. Note that a resistor value outside of the recommended range can cause the device to shut down. This prevents unintended operation if RT pin is shorted to ground or left open. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, refer to Section 7.3.6.

The switching frequency must be selected based on the output voltage setting of the device. See Table 7-4 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for common input voltages.

$$R_{RT}(k\Omega) = \left(\frac{1.0}{f_{SW}(kHz)} - 3.3\times10^{-5}\right) \times 1.346\times10^{4} \quad (2)$$

Table 7-4. Switching Frequency vs Output Voltage (I_{OUT} = 3 A)

F_{SW} (kHz)	R_{RT} (kΩ)	V_{IN} = 5 V		V_{IN} = 12 V		V_{IN} = 24 V		V_{IN} = 36 V	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
200	66.5	1.0	2.0	1.0	2.0	1.0	1.5	1.0	1.5
400	33.2	1.0	3.0	1.0	4.0	1.0	3.3	1.2	3.0
600	22.1	1.0	3.5	1.0	6.0	1.5	6.0	1.8	5.0
800	16.5	1.0	3.5	1.0	7.0	1.5	9.0	2.5	7.0
1000	13.0	1.0	3.0	1.0	8.0	2.0	12.0	3.0	10.0
1200	10.7	1.0	3.0	1.5	9.0	2.5	13.0	3.5	14.0
1400	9.09	1.0	3.0	1.5	9.5	3.0	14.0	4.0	16.0
1600	8.06	1.0	3.0	1.5	9.0	3.0	15.0	4.5	16.0
1800	6.98	1.0	3.0	2.0	9.0	3.5	16.0	5.0	16.0
2000	6.34	1.2	2.5	2.0	9.0	4.0	16.0	5.5	16.0
2200	5.626	1.2	2.5	2.0	9.0	4.5	16.0	6.0	16.0

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7.3.5 Output ON/OFF Enable (EN/SYNC) and V_{IN} UVLO

The EN/SYNC pin provides precision ON and OFF control for the TPSM63603. Once the EN/SYNC pin voltage exceeds the threshold voltage and V_{IN} is above the minimum turn-on threshold, the device starts operation. The simplest way to enable the TPSM63603 is to connect EN/SYNC directly to VIN. This allows the TPSM63603 to start up when V_{IN} is within its valid operating range. However, many applications benefit from the employment of an enable divider network as shown in Figure 7-2, which establishes a precision input undervoltage lockout (UVLO). This can be used for sequencing, to prevent re-triggering the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. An external logic signal can also be used to drive the enable input to toggle the output on and off and for system sequencing or protection.

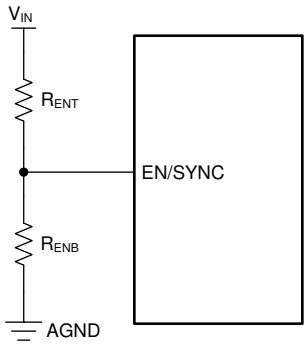

Figure 7-2. VIN UVLO Using the EN/SYNC Pin

R_{ENB} can be calculated using Equation 3.

$$R_{ENB} = R_{ENT} \cdot \frac{V_{EN}}{V_{ON} - V_{EN}} \tag{3}$$

where

- A typical value for R_{ENT} is 100 kΩ
- V_{EN} is 1.263 (typical)
- V_{ON} is the desired start-up input voltage

Note

The EN/SYNC pin can also be used as an external synchronization clock input. See Section 7.3.6 for additonal information. A blanking time of 4 µs to 28 µs is applied to the enable logic after a clock edge is detected. To effectively disable the output, the EN/SYNC input must stay low for longer than 28 µs. Any logic change within the blanking time is ignored. Blanking time is not applied when the device is in Shutdown mode.

7.3.6 Synchronization (EN/SYNC)

The TPSM63603 can be synchronized to an external clock using the EN/SYNC pin. The synchronization frequency range is 200 kHz to 2.2 MHz The internal oscillator can be synchronized by AC coupling a positive clock edge into the EN/SYNC pin, as shown in Figure 7-3. It is recommended to keep the parallel combination value of R_{ENT} and R_{ENB} in the 100-kΩ range. R_{ENT} is required for synchronization, but R_{ENB} can be left open. The external clock must be off before start-up to allow proper start-up sequencing. After a valid synchronization signal is applied for 2048 cycles, the clock frequency changes to that of the applied signal.

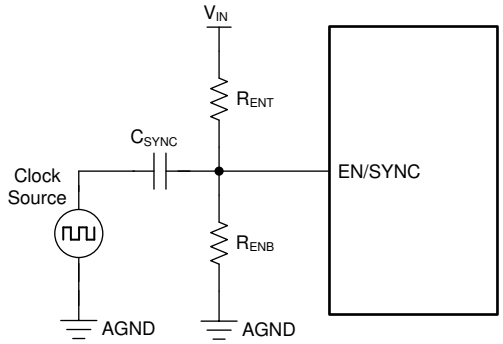

Figure 7-3. Typical synchronization Using the EN/SYNC pin

Referring to Figure 7-4, the AC-coupled voltage edge at the EN/SYNC pin must exceed the SYNC amplitude threshold, V_{EN_SYNC}, of 2.4 V to trip the internal synchronization pulse detector. In addition, the minimum EN/SYNC rising pulse and falling pulse durations must be longer than the SYNC signal hold time, t_{SYNC_EDGE}, of 100 ns and shorter than the minimum blanking time, t_B. A 3.3-V or higher amplitude pulse signal coupled through a 1-nF capacitor, C_{SYNC}, is suggested.

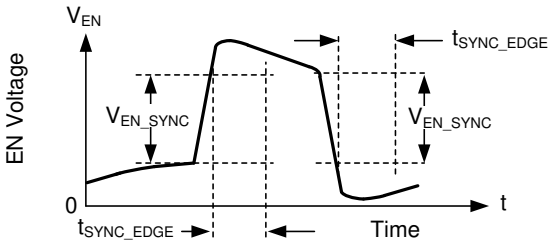

Figure 7-4. Typical SYNC Waveform

7.3.7 Power Good (PGOOD)

The TPSM63603 provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. The PGOOD pin voltage goes low when the feedback voltage is outside of the PGOOD thresholds. This occurs during the following:

- While the device is disabled
- In current limit
- In thermal shutdown
- During normal start-up

A glitch filter prevents false flag operation for short excursions (120 µs typical) of the output voltage, such as during line and load transients.

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PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 20 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 1 V (typical).

7.3.8 Adjustable SW Node Slew Rate (RBOOT/CBOOT)

The SW node slew rate of TPSM63603 can be adjusted to slow the SW node voltage rise time and optimize EMI. However, slowing the rise time decreases efficiency slightly. Care must be taken to balance the improved EMI versus the decreased efficiency.

Internal to the device, a bootstrap resistor of 100 Ω is connected between the RBOOT pin and the CBOOT pin as shown in Figure 7-5. Leaving these pins open incorporates the 100-Ω resistor in the BOOT circuit, slowing the SW voltage slew rate and optimizing EMI. However, if improved EMI is not required, connecting RBOOT to CBOOT shorts the internal resistor, resulting in higher efficiency. Placing a resistor across RBOOT and CBOOT allows adjustment of the internal resistor to balance EMI and efficiency.

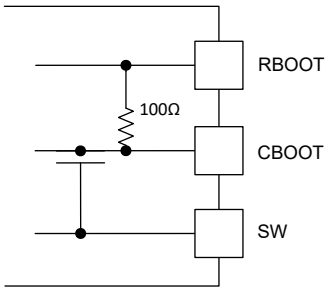

Figure 7-5. Internal BOOT resistor

7.3.9 Internal LDO Output (VCC)

The TPSM63603 has an internal LDO to power internal circuitry. The VCC pin is the output of the internal LDO. This pin must not be used to power external circuitry. Connect a high-quality, 1-µF capacitor from this pin to AGND, close to the device pins.

7.3.10 LDO Input Bias Voltage (VLDOIN)

The VLDOIN pin is an optional input to the internal LDO. This input can be connected to V_{OUT} or other supply voltage to improve efficiency. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity.

If the VLDOIN voltage is less than 3.1 V, the LDO is powered internally from V_{IN}. If V_{OUT} is above 12 V, or if this pin is unused, connect this pin to ground.

7.3.11 Overcurrent Protection (OCP)

The TPSM63603 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TPSM63603 employs hiccup overcurrent protection if there is an extreme overload. In Hiccup mode, the regulator is shut down and kept off for 80 ms (typical) before the TPSM63603 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation.

7.3.12 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 165°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM63603 attempts to restart when the junction temperature falls to 155°C (typical).

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TPSM63603. When $V_{EN/SYNC}$ is below approximately 0.4 V, the device is in Shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in Shutdown mode drops to 0.6 µA (typical). The TPSM63603 also employs internal undervoltage protection. If the input voltage is below its UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal LDO has a lower enable threshold than the regulator itself. When V_{EN} is above 1.1 V (maximum) and below the precision enable threshold of 1.263 V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UVLO threshold. The switching action and voltage regulation are not enabled until V_{EN} rises above the precision enable threshold.

7.4.3 Active Mode

The TPSM63603 is in Active mode when V_{IN} and V_{EN} are above their relevant thresholds and no fault conditions are present. The simplest way to enable the operation is to connect the EN/SYNC pin to V_{IN} which allows self start-up when the applied input voltage exceeds the minimum start-up voltage.

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM63603 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. The following section describes the design procedure to configure the TPSM63603 power module. To expedite and streamline the design process, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases.

As mentioned previously, the TPSM63603 also integrates several optional features to meet system design requirements, including the following:

- Precision enable with hysteresis
- External adjustable UVLO
- Adjustable SW node slew rate
- Power-good indicator

The following application circuit detailed shows the TPSM63603 configuration options suitable for several application use cases. Refer to the *TPSM63603EVM User's Guide* for more detail.

8.2 Typical Applications

Figure 8-1 shows the schematic diagram of a 5-V, 3-A output converter.

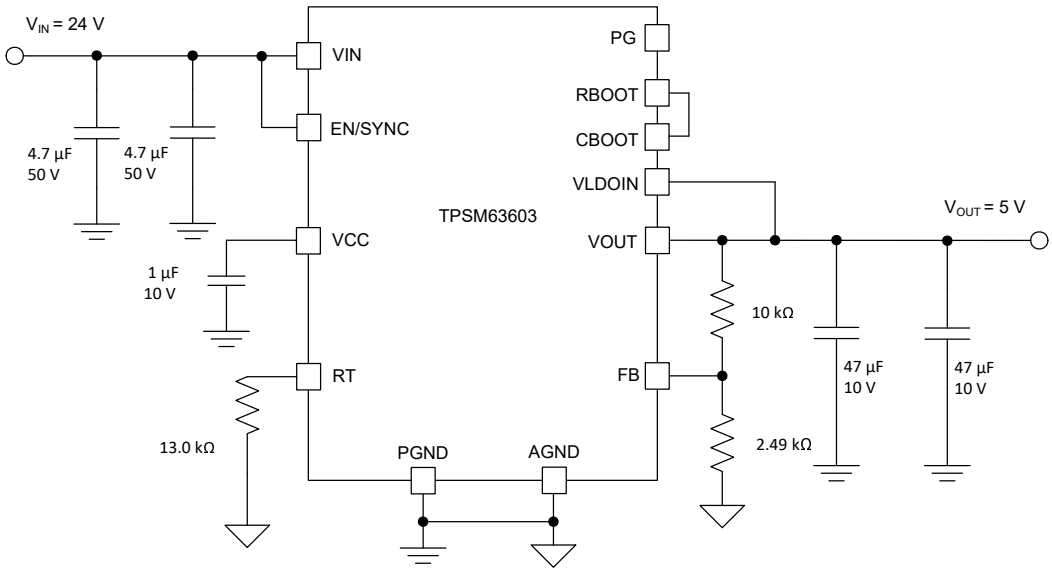

Figure 8-1. TPSM63603 Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters and follow the design procedures in Section 8.2.2.

Table 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	3 A

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63603 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM63603 device is externally adjustable using a resistor divider. The recommended value of R_{FBT} is 10 kΩ. The value for R_{FBB} can be selected from Table 7-1 or calculated using Equation 4:

$$R_{FBB} = \frac{1.0}{V_{OUT} - 1.0} \times R_{FBT} \quad (4)$$

For the desired output voltage of 5 V, the formula yields a value of 2.5 kΩ. Choose the closest available standard value of 2.49 kΩ for R_{FBB}.

8.2.2.3 Switching Frequency Selection

The recommended switching frequency for standard output voltages can be found in Table 7-1. For 5-V output, the recommended switching frequency is 1 MHz. To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND.

8.2.2.4 Input Capacitor Selection

The TPSM63603 requires a minimum input capacitance of 2 × 4.7-µF ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, two 4.7-µF, 50-V ceramic capacitors are selected.

8.2.2.5 Output Capacitor Selection

The TPSM63603 requires a minimum of 25 µF of effective output capacitance for proper operation. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, a two 47-µF, 10-V, ceramic capacitors are used which have a total effective capacitance of approximately 48 µF at 5 V.

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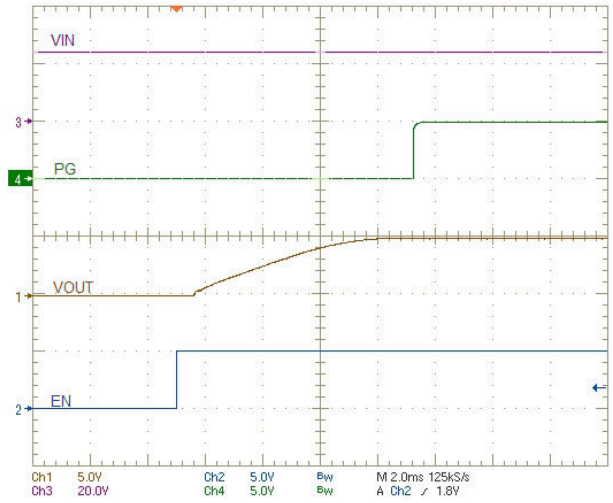
8.2.2.6 Other Connections

RBOOT and CBOOT were shorted together for best efficiency.

VLDOIN is connected to VOUT to improve efficiency.

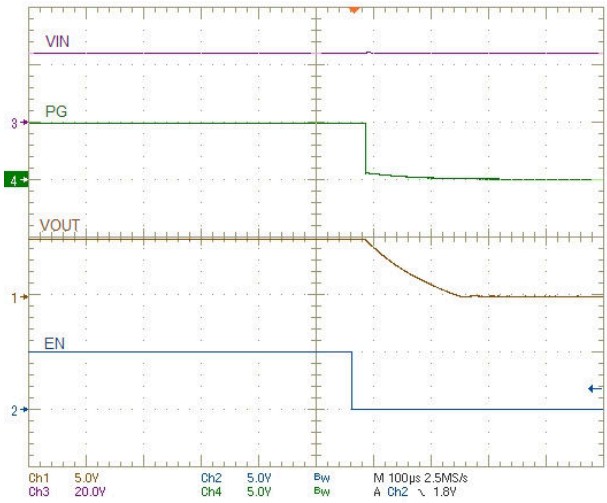
A 1-µF capacitor was placed on the VCC pin.

8.2.3 Application Curves



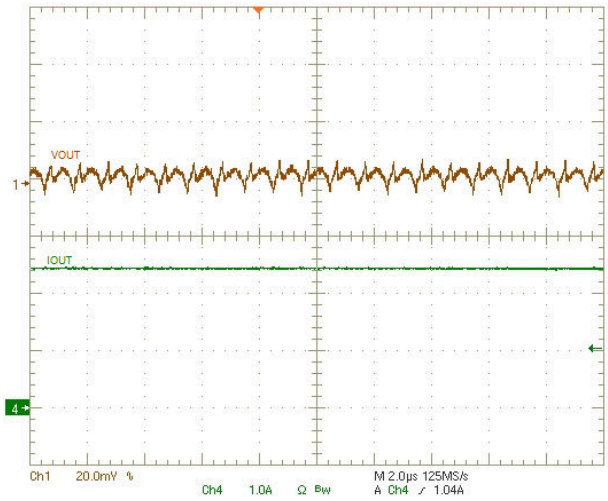
V_{IN} = 24 V V_{OUT} = 5 V

Figure 8-2. Start-up Waveforms



V_{IN} = 24 V V_{OUT} = 5 V

Figure 8-3. Shut-down Waveforms



I_{OUT} = 2.5 A C_{OUT} = 2 × 47 µF

Figure 8-4. Output Voltage Ripple

9 Power Supply Recommendations

The TPSM63603 is designed to operate from an input voltage supply range between 3 V and 36 V. This input supply must be able to provide the maximum input current and maintain a voltage above the set UVLO voltage. Ensure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the TPSM63603 supply rail to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPSM63603, additional bulk capacitance can be required in addition to the ceramic input capacitance. A 47-µF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 10-1 and Figure 10-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Connect AGND to PGND at a single point.
- Place R_{FBT} and R_{FBB} as close as possible to the FB pin.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

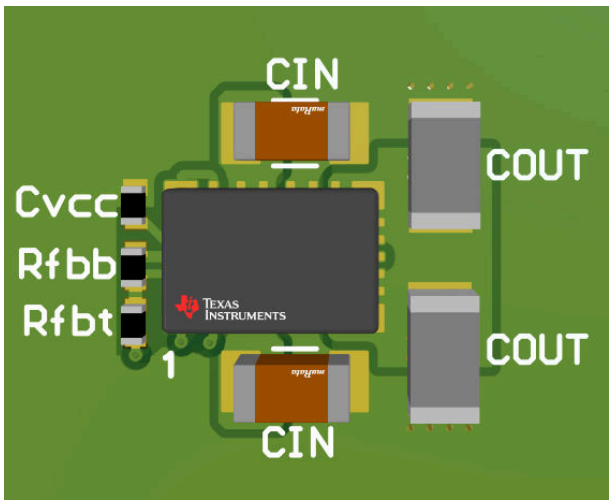


Figure 10-1. Typical Top-Layer Layout

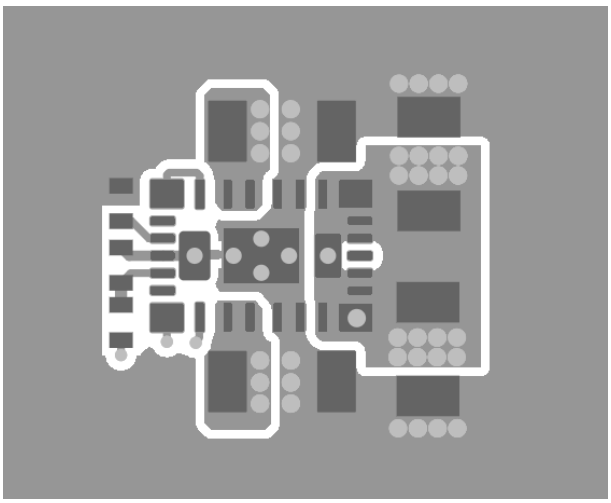


Figure 10-2. Typical Top-Layer

10.2.1 Package Specifications

Table 10-1. Package Specifications Table

TPSM63603		VALUE	UNIT
Weight		123	mg
Flammability	Meets UL 94 V-O		
MTBF calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	tbd	MHrs

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

For development support, see the following:

- For TI's reference design library, visit TI Reference Design library.
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center.
- To view a related device of this product, see the LM5166.

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63603 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPSM63603EVM User's Guide*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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ADVANCE INFORMATION

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

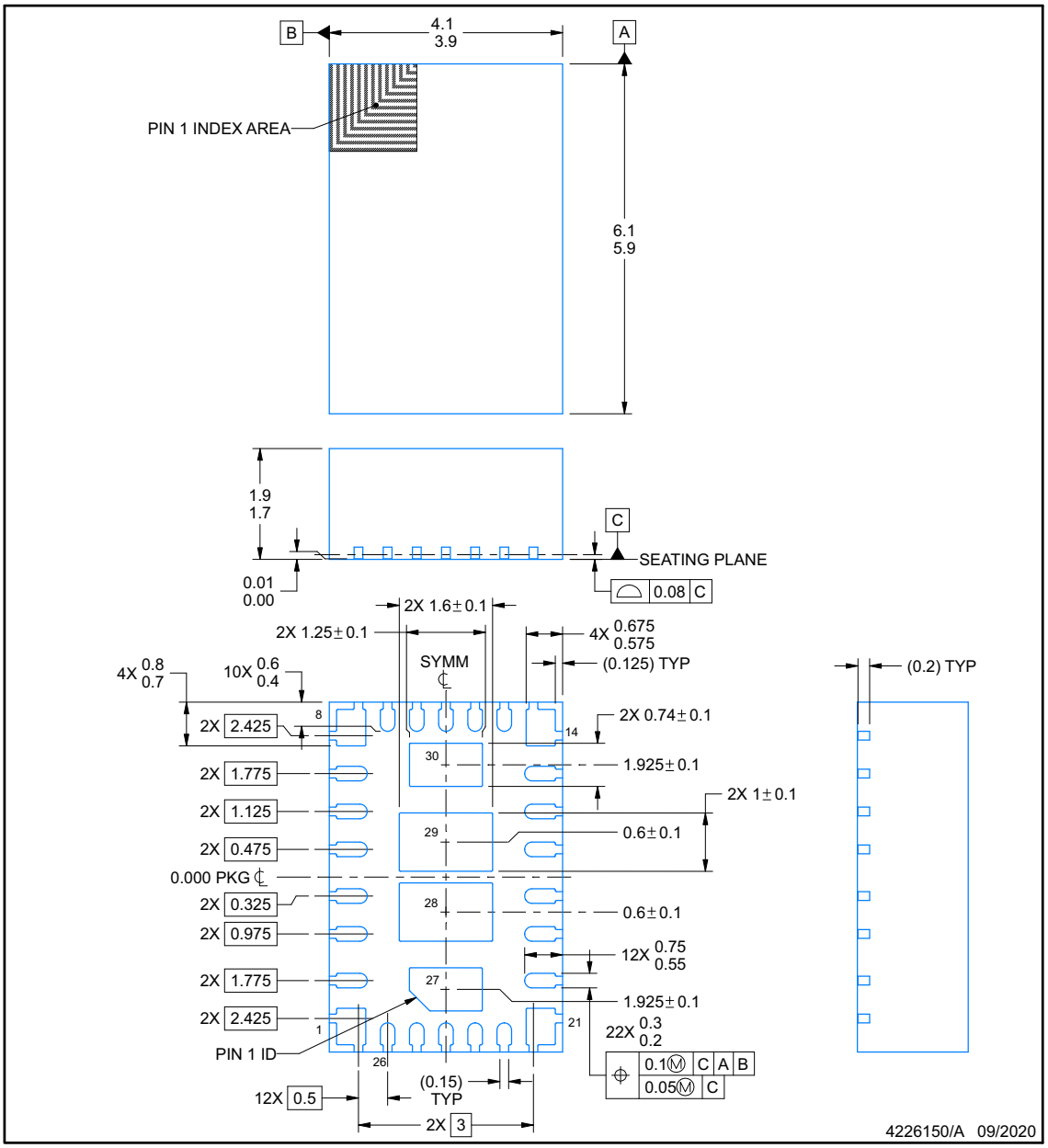
ADVANCE INFORMATION

PACKAGE OUTLINE

RDH0030A

B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

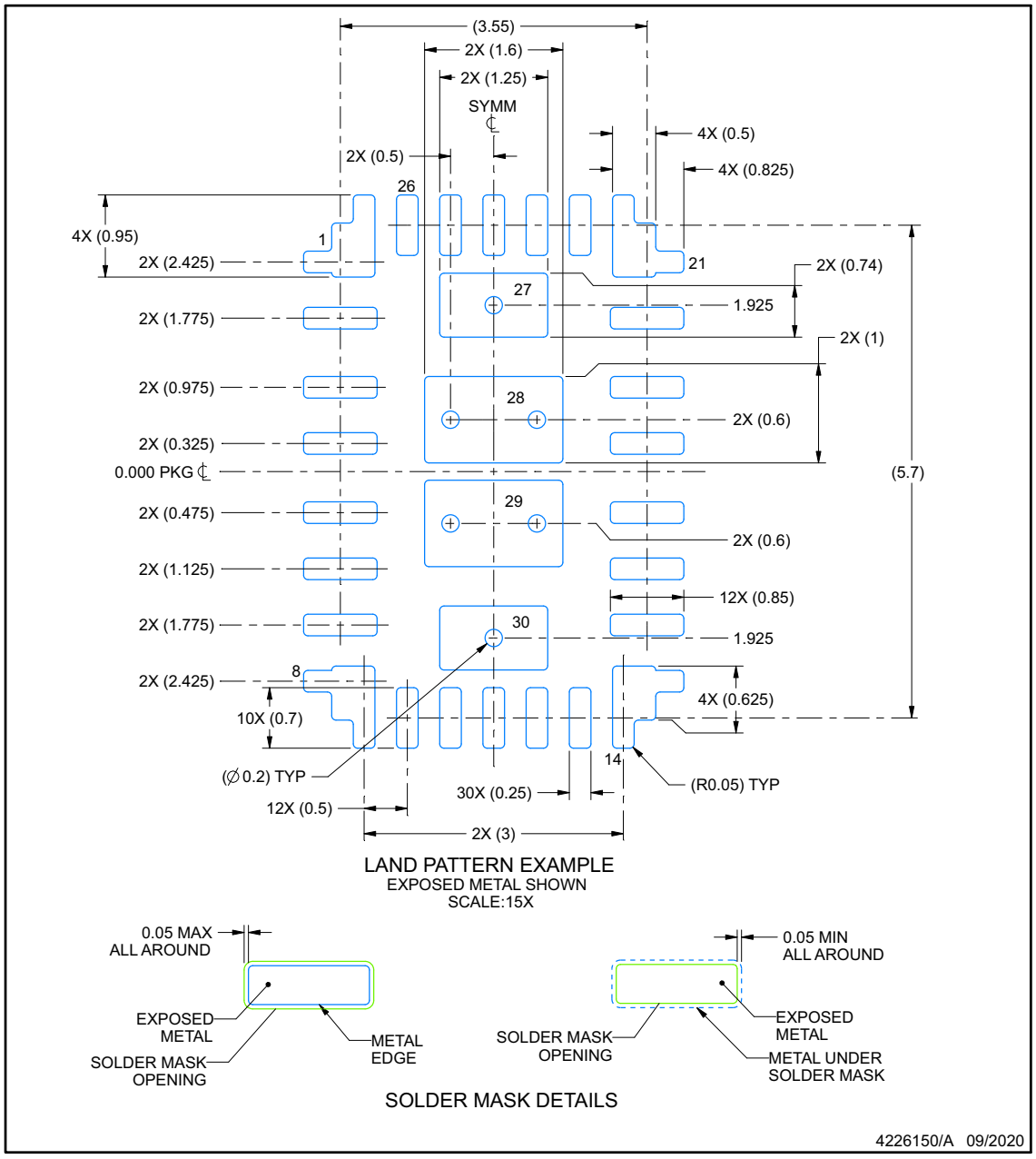
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RDH0030A

B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

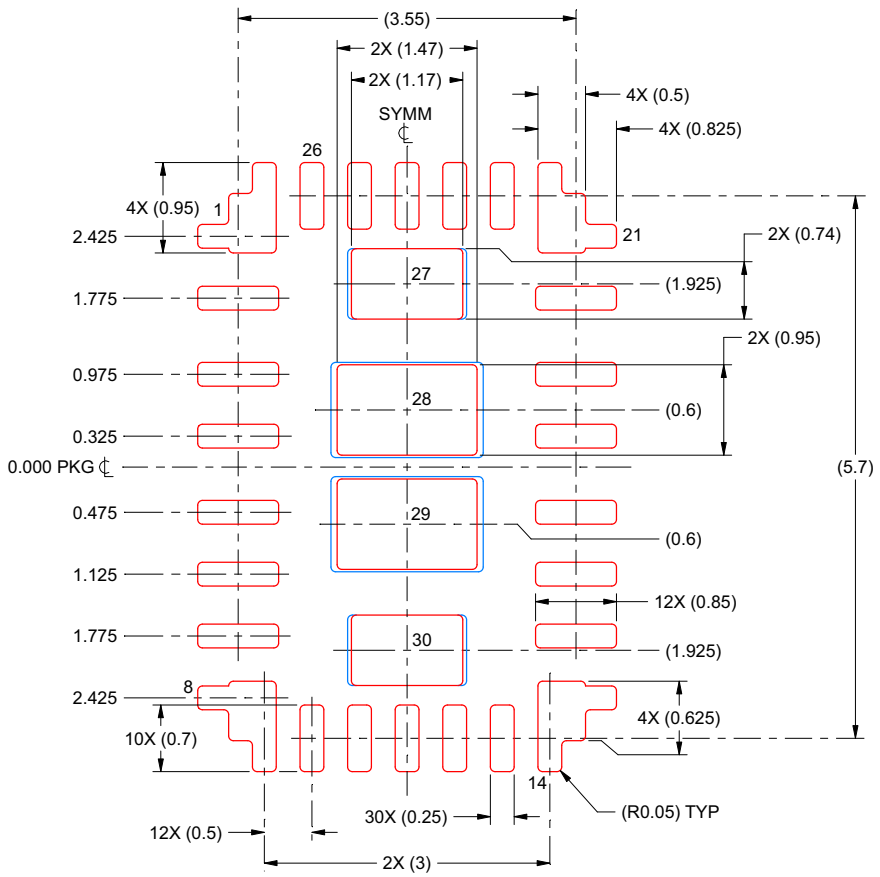
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RDH0030A

B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 27 & 30:
94% PRINTED SOLDER COVERAGE BY AREA

EXPOSED PAD 28 & 29
87% PRINTED SOLDER COVERAGE BY AREA

SCALE:15X

4226150/A 09/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPSM63603RDHR	ACTIVE	B0QFN	RDH	30	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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