

## LOW-INPUT HIGH-EFFICIENCY SYNCHRONOUS BUCK CONTROLLER

### FEATURES

- Operating Input Voltage 2.25 V to 5.5 V
- Output Voltage as Low as 0.7 V
- 1% Internal 0.7 V Reference
- Predictive Gate Drive™ N-Channel MOSFET Drivers for Higher Efficiency
- Externally Adjustable Soft-Start and Overcurrent Limit
- Fixed-Frequency Voltage-Mode Control
  - TPS40007, 300 kHz
  - TPS40009, 600 kHz
- Source/Sink with  $V_{OUT}$  Prebias
- 10-Lead MSOP PowerPad™ Package for Higher Performance
- Thermal Shutdown
- Internal Bootstrap Diode

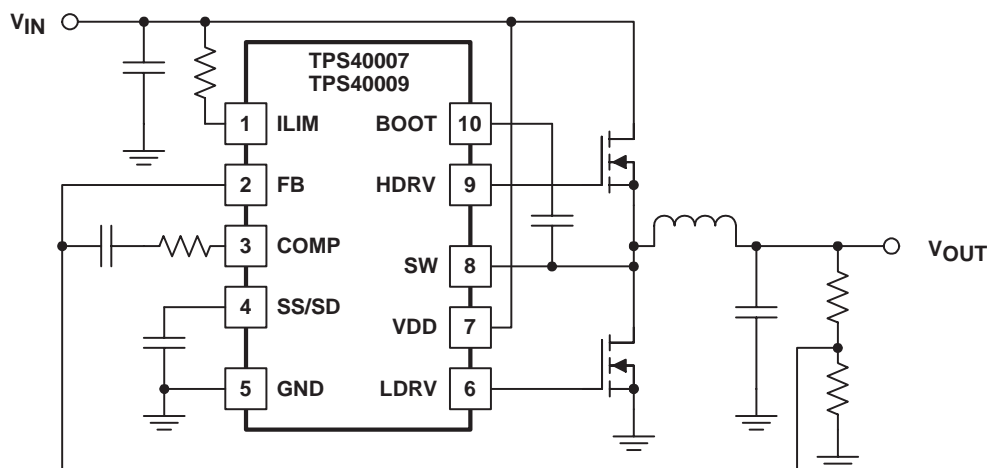
### APPLICATIONS

- Networking Equipment
- Telecom Equipment
- Base Stations
- Servers
- DSP Power
- Power Modules

### DESCRIPTION

The TPS4000x are controllers for low-voltage, non-isolated synchronous buck regulators. These controllers drive an N-channel MOSFET for the primary buck switch, and an N-channel MOSFET for the synchronous rectifier switch, thereby achieving very high-efficiency power conversion. In addition, the device controls the delays from main switch off to rectifier turn-on and from rectifier turn-off to main switch turn-on in such a way as to minimize diode losses (both conduction and recovery) in the synchronous rectifier with TI's proprietary Predictive Gate Drive™ technology. The reduction in these losses is significant and increases efficiency. For a given converter power level, smaller FETs can be used, or heat sinking can be reduced or even eliminated.

### SIMPLIFIED APPLICATION DIAGRAM



UDG–03161

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## DESCRIPTION (continued)

The current-limit threshold is adjustable with a single resistor connected to the device. The TPS4000x controllers implement a closed-loop soft start function. Startup ramp time is set by a single external capacitor connected to the SS/SD pin. The SS/SD pin is also used for shutdown.

## ORDERING INFORMATION

T <sub>A</sub>	FREQUENCY	PACKAGED DEVICES MSOP <sup>(1)</sup> (DGQ)
–40°C to 85°C	300 kHz	TPS40007DGQ
	600 kHz	TPS40009DGQ

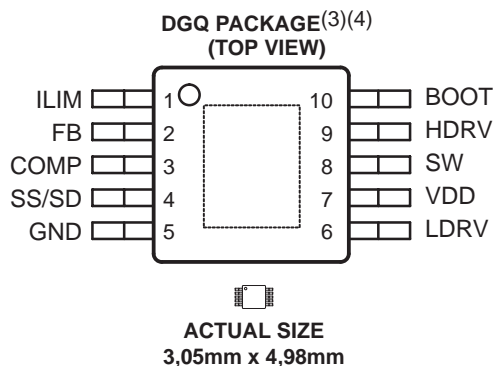
- (1) The DGQ package is available taped and reeled. Add R suffix to device type (e.g. TPS40007DGQR) to order quantities of 2,500 devices per reel and 80 units per tube.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(2)</sup>

		TPS4000x	UNIT
Input voltage range, V <sub>IN</sub>	BOOT	V <sub>SW</sub> + 6.5	V
	COMP, FB, ILIM, SS/SD	–0.3 to 6.5	
	SW	–3 to 10.5	
	SW <sub>T</sub> (SW transient < 50 ns)	–5	
	VDD	6.5	
Operating junction temperature range, T <sub>J</sub>		–40 to 150	°C
Storage temperature, T <sub>stg</sub>		–55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

- (2) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



- (3) See technical brief SLMA002 for PCB guidelines for PowerPAD packages.

- (4) PowerPAD™ heat slug should be connected to GND (pin 5).

## ELECTRICAL CHARACTERISTICS

temperature range,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $T_A = T_J$ ; all parameters measured at zero power dissipation (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY							
V <sub>DD</sub>	Input voltage range			2.25		5.5	V
V <sub>HGATE</sub>	High-side gate voltage		V <sub>BOOT</sub> – V <sub>SW</sub>			6	
I <sub>DD</sub>	Shutdown current		SS/SD = 0 V,      Outputs off		0.25	0.45	mA
	Quiescent current		FB = 0.8 V		1.4	2.0	
	Switching current		No load at HDRV/LDRV		1.5	4.0	
UVLO	Minimum on-voltage			1.95	2.05	2.15	V
	Hysteresis			80	150	220	mV
OSCILLATOR							
f <sub>OSC</sub>	Oscillator frequency	TPS40007	2.25 V ≤ V <sub>DD</sub> ≤ 5.00 V	250	300	350	kHz
		TPS40009		500	600	700	
V <sub>RAMP</sub>	Ramp voltage		V <sub>PEAK</sub> – V <sub>VALLEY</sub>	0.80	0.93	1.07	V
	Ramp valley voltage			0.24	0.31	0.44	
PWM							
	Maximum duty cycle(2)	TPS40007	FB = 0 V,      V <sub>DD</sub> = 3.3 V	87.0%	94.0%		
		TPS40009		83.0%	93.0%		
	Minimum duty cycle					0%	
	Minimum controllable pulse width(1)(3)				100	150	ns
ERROR AMPLIFIER							
V <sub>FB</sub>	FB input voltage		Line,      Temperature	0.690	0.700	0.711	V
			T <sub>A</sub> = 25°C	0.693	0.700	0.707	
I <sub>FB</sub>	FB input bias current				30	130	nA
V <sub>OH</sub>	High-level output voltage		FB = 0 V,      I <sub>OH</sub> = 1.0 mA	2.0	2.5		V
V <sub>OL</sub>	Low-level output voltage		FB = V <sub>DD</sub> ,      I <sub>OL</sub> = 0.5 mA		0.08	0.15	
I <sub>OH</sub>	Output source current		COMP = 0.7 V,      FB = GND	2	6		mA
I <sub>OL</sub>	Output sink current		COMP = 0.7 V,      FB = V <sub>DD</sub>	3	8		
GBW	Gain bandwidth(1)			5	10		MHz
AOL	Open loop gain			55	85		dB
SHORT CIRCUIT CURRENT PROTECTION							
I <sub>SINK</sub>	ILIM sink current		V <sub>DD</sub> = 5 V	11	15	19	μA
I <sub>SINK</sub>	ILIM sink current		V <sub>DD</sub> = 2.25 V	9.5	13.0	16.5	μA
V <sub>OS</sub>	Offset voltage SW vs ILIM(1)		2.25 V ≤ V <sub>DD</sub> ≤ 5.00	–20	0	20	mV
V <sub>ILIM</sub>	Input voltage range			2		V <sub>DD</sub>	V
t <sub>ON</sub>	Minimum HDRV pulse time in overcurrent		V <sub>DD</sub> = 3.3 V		220	330	ns
	SW leading edge blanking pulse in over-current detection(1)				100		ns
t <sub>SS</sub>	Soft-start capacitor cycles as fault timer(1)				6		

(1) Ensured by design. Not production tested.

(2) Derate the maximum duty cycle by 3% for  $V_{DD} < 3\text{ V}$

(3) Operating at PWM on-times of less than 100 ns could lead to overlap between HDRV and LDRV pulses.

## ELECTRICAL CHARACTERISTICS

temperature range,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $T_A = T_J$ ; all parameters measured at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVER						
R <sub>HDI</sub>	HDRV pull-up resistance	V <sub>BOOT</sub> –V <sub>SW</sub> = 3.3 V, I <sub>SOURCE</sub> = –100 mA		3	5.5	Ω
R <sub>HDLO</sub>	HDRV pull-down resistance	V <sub>BOOT</sub> – V <sub>SW</sub> = 3.3 V, I <sub>SINK</sub> = 100 mA		1.5	3	
R <sub>LDI</sub>	LDRV pull-up resistance	V <sub>DD</sub> = 3.3 V, I <sub>SOURCE</sub> = –100 mA		3	5.5	
R <sub>LDLO</sub>	LDRV pull-down resistance	V <sub>DD</sub> = 3.3 V, I <sub>SINK</sub> = 100 mA		1.0	2.0	
t <sub>RLD</sub>	LDRV rise time	C <sub>LOAD</sub> = 1 nF		15	35	ns
t <sub>FLD</sub>	LDRV fall time			10	25	
t <sub>RHD</sub>	HDRV rise time			15	35	
t <sub>FHD</sub>	HDRV fall time			10	25	
PREDICTIVE DELAY						
V <sub>SWP</sub>	Sense threshold to modulate delay time			–350		mV
T <sub>LDHD</sub>	Maximum delay modulation range time	LDRV OFF – to – HDRV ON	45	70	95	ns
	Predictive counter delay time per bit	LDRV OFF – to – HDRV ON	2.8	4.3	6.2	
T <sub>HDLD</sub>	Maximum delay modulation range	HDRV OFF – to – LDRV ON	50	80	110	
	Predictive counter delay time per bit	HDRV OFF – to – LDRV ON	3.0	4.8	6.6	
SHUTDOWN						
V <sub>SD</sub>	Shutdown threshold voltage	Outputs OFF	0.21	0.26	0.31	V
V <sub>EN</sub>	Device active threshold voltage		0.25	0.29	0.35	
SOFTSTART						
I <sub>SS</sub>	Soft-start source current	Outputs OFF	2.0	3.7	5.4	μA
V <sub>SS</sub>	Soft-start voltage to begin V <sub>OUT</sub> start		0.35	0.65	0.95	V
BOOTSTRAP						
R <sub>BOOT</sub>	Bootstrap switch resistance	V <sub>DD</sub> = 3.3 V		50	100	Ω
		V <sub>DD</sub> = 5 V		35	70	
V <sub>OUT</sub> PRE-BIAS						
	Recommended V <sub>OUT</sub> pre-bias level as % of final regulation <sup>(1)(4)</sup>	FB percent of 700 mV		90%		
SW NODE						
I <sub>SW</sub>	Leakage current in shutdown			2		μA
THERMAL SHUTDOWN						
t <sub>SD</sub>	Shutdown temperature <sup>(1)</sup>			165		°C
	Restart from thermal shutdown <sup>(1)</sup>			–15		

(1) Ensured by design. Not production tested.

(2) Derate the maximum duty cycle by 3% for  $V_{DD} < 3\text{ V}$ .

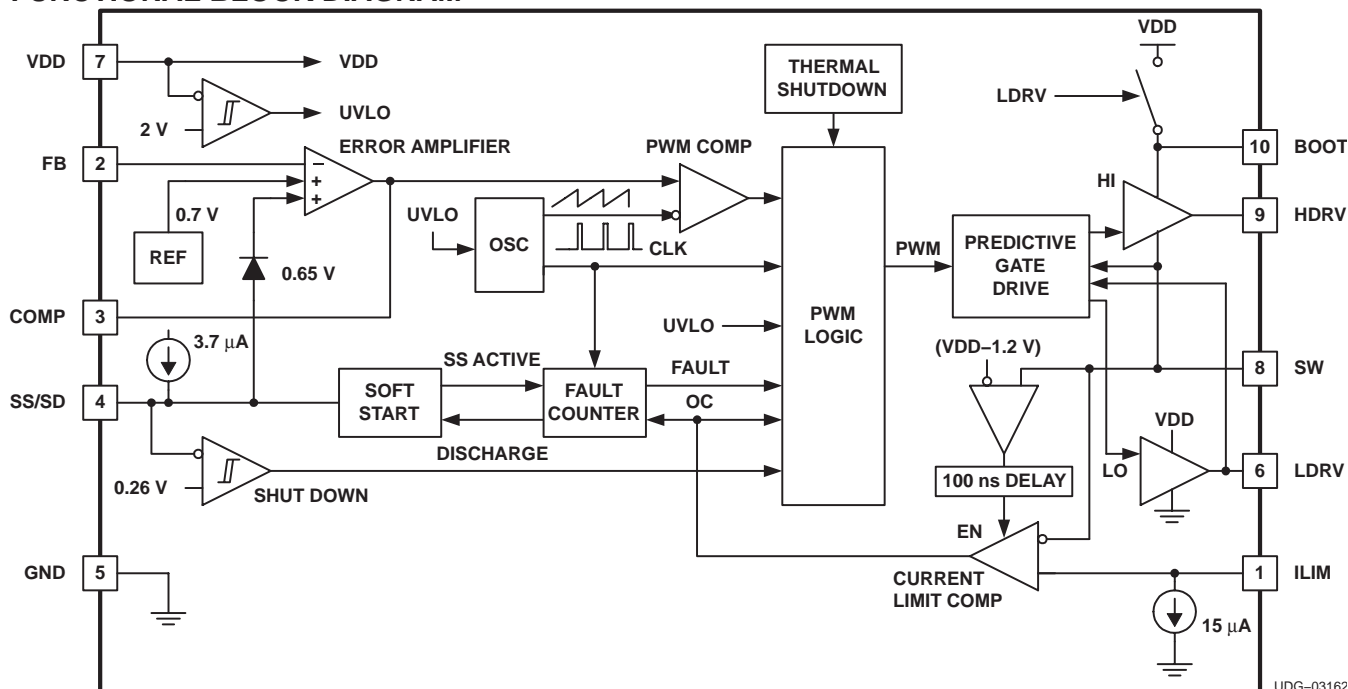
(3) Operating at PWM on-times of less than 100 ns could lead to overlap between HDRV and LDRV pulses.

(4) Prebiased output greater than 90% of final regulation may lead to sinking current from the prebias output.

## Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT	10	O	Provides a bootstrapped supply for the topside MOSFET driver, enabling the gate of the topside MOSFET to be driven above the input supply rail
COMP	3	O	Output of the error amplifier
FB	2	I	Inverting input of the error amplifier. In normal operation the voltage at this pin is the internal reference level of 700 mV.
GND	5	–	Power supply return for the device. The power stage ground return on the board requires a separate path from other sensitive signal ground returns.
HDRV	9	O	This is the gate drive output for the topside N-channel MOSFET. HDRV is bootstrapped to near $2 \times V_{DD}$ for good enhancement of the topside MOSFET.
ILIM	1	I	A resistor is connected between this pin and VDD to set up the over current threshold voltage. A 15- $\mu$ A current sink at the pin establishes a voltage drop across the external resistor that represents the drain-to-source voltage across the top side N-channel MOSFET during an over current condition. The ILIM over current comparator is blanked for the first 100 ns to allow full enhancement of the top MOSFET. Set the ILIM voltage level such that it is within 800 mV of VDD; that is, $(V_{DD} - 0.8) \leq I_{ILIM} \leq V_{DD}$ .
LDRV	6	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET
SS/SD	4	I	Soft-start and overcurrent fault shutdown times are set by charging and discharging a capacitor connected to this pin. A closed loop soft-start occurs when the internal 3- $\mu$ A current source charges the external capacitor. There is a 0.65-V offset between external SS pin and internal soft-start voltage at the error amplifier input. This allows the device to be enabled before starting $V_{OUT}$ , thus ensuring that $V_{OUT}$ soft starts smoothly. When the SS/SD voltage is less than 0.25 V, the device is shutdown and the HDRV and LDRV are driven low. In normal operation, the capacitor is charged to VDD. When a fault condition is asserted, the soft-start capacitor goes through six charge/discharge cycles, restarting the converter on the seventh cycle.
SW	8	O	Connect to the switched node on the converter. This pin is used for overcurrent sensing in the topside N-channel MOSFET, and level sensing for predictive delay circuit. Overcurrent is determined, when the topside N-channel MOSFET is on, by comparing the voltage on SW with respect to VDD and the voltage on the ILIM with respect to VDD. This pin is also used for the return of the topside N-channel MOSFET driver.
VDD	7	I	Power input for the chip, 5.5-V maximum. Decouple close to the pin with a low-ESR capacitor, 1- $\mu$ F or larger.

## FUNCTIONAL BLOCK DIAGRAM

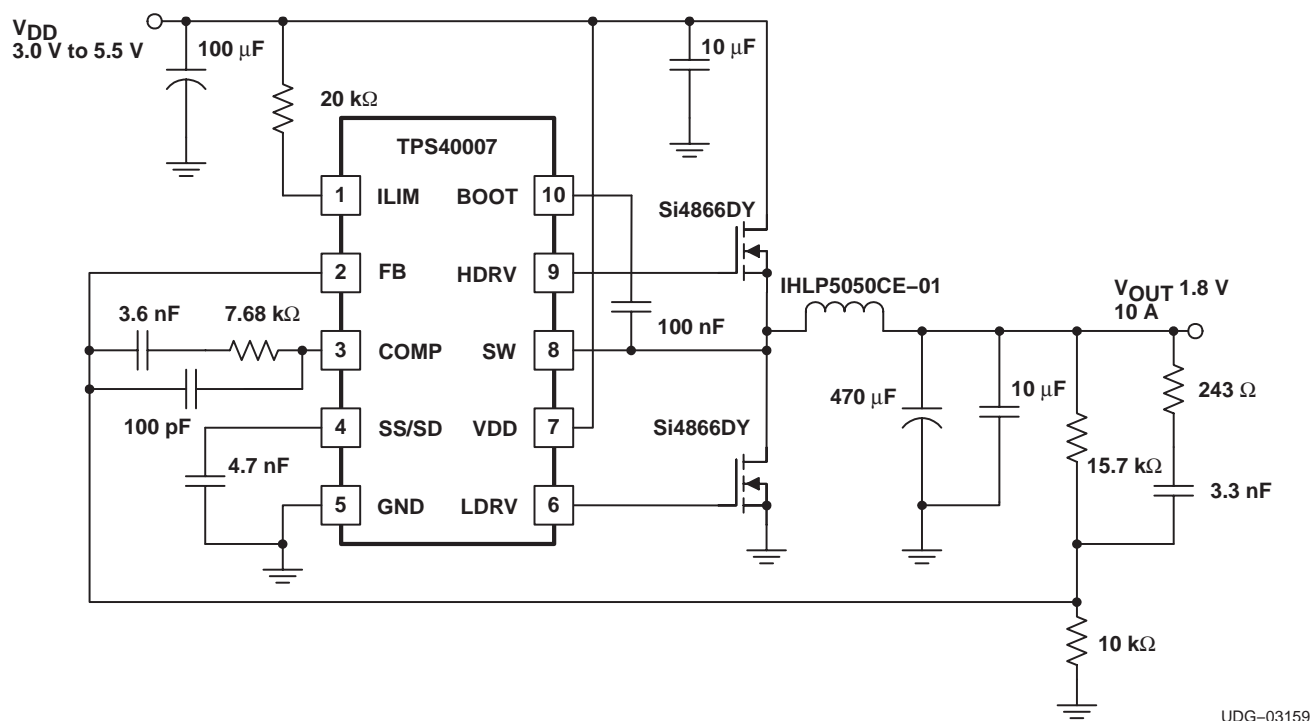


UDG-03162

## APPLICATION INFORMATION

The TPS4000x series of synchronous buck controller devices is optimized for high-efficiency dc-to-dc conversion in non-isolated distributed power systems. A typical application circuit is shown in Figure 1.

The TPS40007 and TPS40009 are the controllers of choice for general-purpose synchronous buck designs. They are designed to startup into applications where the output voltage is pre-biased, and without having the synchronous rectifier interfere with the pre-bias condition. PWM pulses are enabled when the soft-start voltage crosses the feedback level dictated by the pre-bias output. Moreover, the pre-biased output ramps up smoothly from its pre-bias value and into regulation.



UDG-03159

Figure 1. Typical Application Circuit

## APPLICATION INFORMATION

### ERROR AMPLIFIER

The error amplifier has a bandwidth of greater than 5 MHz, with open loop gain of at least 55 dB. The COMP output voltage is clamped to a level above the oscillator ramp in order to improve large-scale transient response.

### OSCILLATOR

The oscillator uses an internal resistor and capacitor to set the oscillation frequency. The ramp waveform is a sawtooth at the PWM frequency with a peak voltage of 1.25 V, and a valley of 0.31 V. The PWM duty cycle is limited to a maximum of 94%, allowing the bootstrap capacitor to charge during every cycle.

### BOOTSTRAP/CHARGE PUMP

There is an internal switch between VDD and BOOT. This switch charges the external bootstrap capacitor for the floating supply. If the resistance of this switch is too high for the application, an external schottky diode between VDD and BOOT can be used. The peak voltage on the bootstrap capacitor is approximately equal to VDD.

### DRIVER

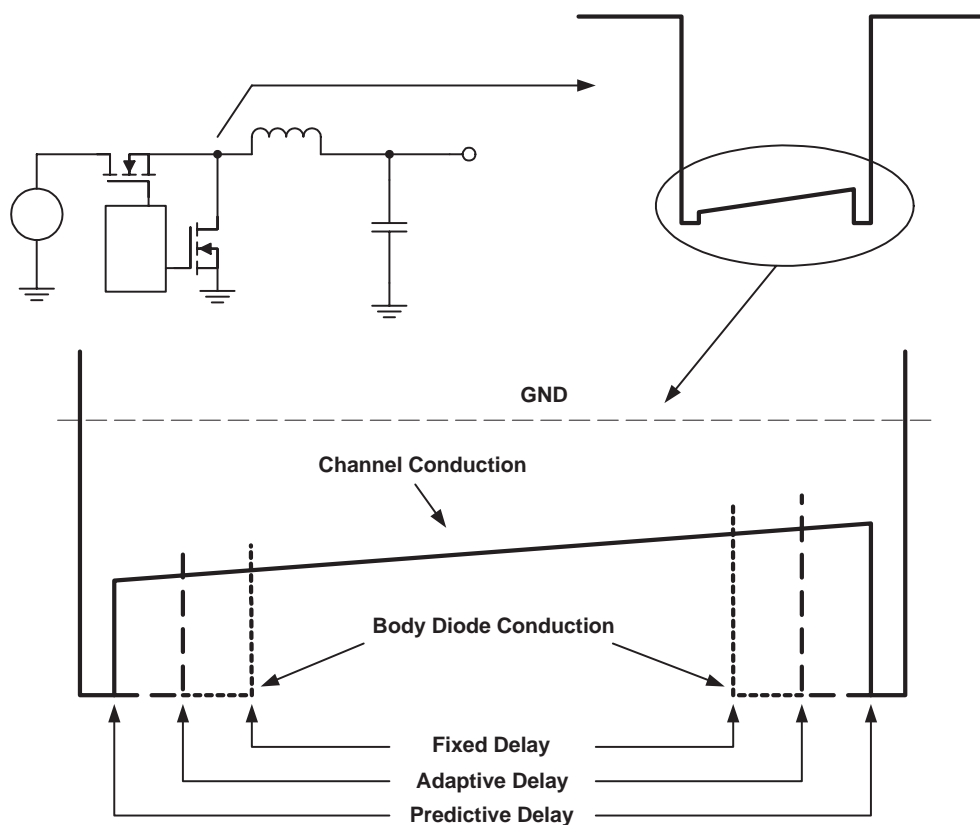
The HDRV and LDRV MOSFET drivers are capable of driving gate-to-source voltages up to 5.5 V. At  $V_{IN} = 5$  V and using appropriate MOSFETs, a 20-A converter can be achieved. The LDRV driver switches between VDD and ground, while the HDRV driver is referenced to SW and switches between BOOT and SW.

### SYNCHRONOUS RECTIFICATION AND PREDICTIVE DELAY

In a normal buck converter, when the main switch turns off, current is flowing to the load in the inductor. This current cannot be stopped immediately without using infinite voltage. In order to provide a path for current to flow and maintain voltage levels at a safe level, a rectifier or catch device is used. This device can be either a conventional diode, or it can be a controlled active device if a control signal is available to drive it. The TPS4000x provides a signal to drive an N-channel MOSFET as a rectifier. This control signal is carefully coordinated with the drive signal for the main switch so that there is minimum delay from the time that the rectifier MOSFET turns off and the main switch turns on, and minimum delay from when the main switch turns off and the rectifier MOSFET turns on. This scheme, Predictive Gate Drive™ delay, uses information from the current switching cycle to adjust the delays that are to be used in the next cycle. Figure 2 shows the switch-node voltage waveform for a synchronously rectified buck converter. Illustrated are the relative effects of a fixed-delay drive scheme (constant, pre-set delays for the turn-off to turn-on intervals), an adaptive delay drive scheme (variable delays based upon voltages sensed on the current switching cycle) and the predictive delay drive scheme.

Note that the longer the time spent in diode conduction during the rectifier conduction period, the lower the efficiency. Also, not described in Figure 2 is the fact that the predictive delay circuit can prevent the body diode from becoming forward biased at all. This results in a significant power savings when the main MOSFET turns on, and minimizes reverse recovery loss in the body diode of the rectifier MOSFET.

## APPLICATION INFORMATION



UDG-03166

**Figure 2. Switch Node Waveforms for Synchronous Buck Converter**

## SHORT CIRCUIT PROTECTION

Overcurrent conditions in the TPS4000x are sensed by detecting the voltage across the main MOSFET while it is on.

### Basic Description

If the voltage exceeds a pre-set threshold, the current pulse is terminated, and a counter inside the device is incremented. If this counter fills up, a fault condition is declared and the device disables switching for a period of time and then attempts to restart the converter with a full soft-start cycle.

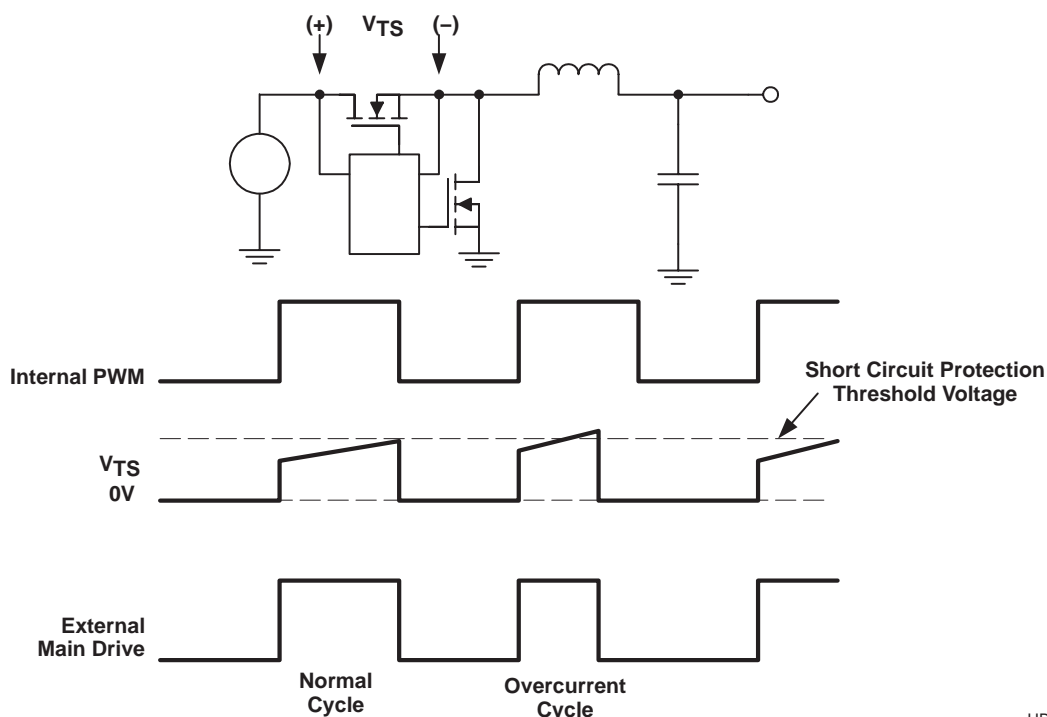


## APPLICATION INFORMATION

### Detailed Description

During each switching cycle, a comparator looks at the voltage across the top side MOSFET while it is on. This comparator is enabled after the SW node reaches a voltage greater than ( $V_{DD}-1.2\text{ V}$ ) followed by a 100-ns blanking time. If the voltage across that MOSFET exceeds the programmed voltage, the current-switching pulse is terminated and a 3-bit counter is incremented by one count. If, during the switching cycle, the topside MOSFET voltage does not exceed a preset threshold, then this counter is decremented by one count. (The counter does not wrap around from 7 to 0 or from 0 to 7). If the counter reaches a full count of 7, the device declares that a fault condition exists at the output of the converter. In this fault state, HDRV and LDRV are turned off, and the soft-start capacitor is discharged. LDRV is maintained OFF during fault timeout to effectively support pre-bias applications. The counter is decremented by one by the soft start capacitor ( $C_{SS}$ ) discharge. When the soft-start capacitor is fully discharged, the discharging circuit is turned off and the capacitor is allowed to charge up at the nominal charging rate. When the soft-start capacitor reaches approximately 1.3 V, it is discharged again and the overcurrent counter is decremented by one count. The capacitor is charged and discharged, and the counter decremented until the count reaches zero (a total of six times). When this happens, the outputs are again enabled as the soft-start capacitor generates a reference ramp for the converter to follow while attempting to restart.

During this soft-start interval (whether or not the controller is attempting to do a fault recovery or starting for the first time), pulse-by-pulse current limiting is in effect, but overcurrent pulses are not counted to declare a fault until the soft-start cycle has been completed. It is possible to have a supply attempt to bring up a short circuit for the duration of the soft start period plus seven switching cycles. Power stage designs should take this into account if it makes a difference thermally. Figure 3 shows the details of the overcurrent operation.

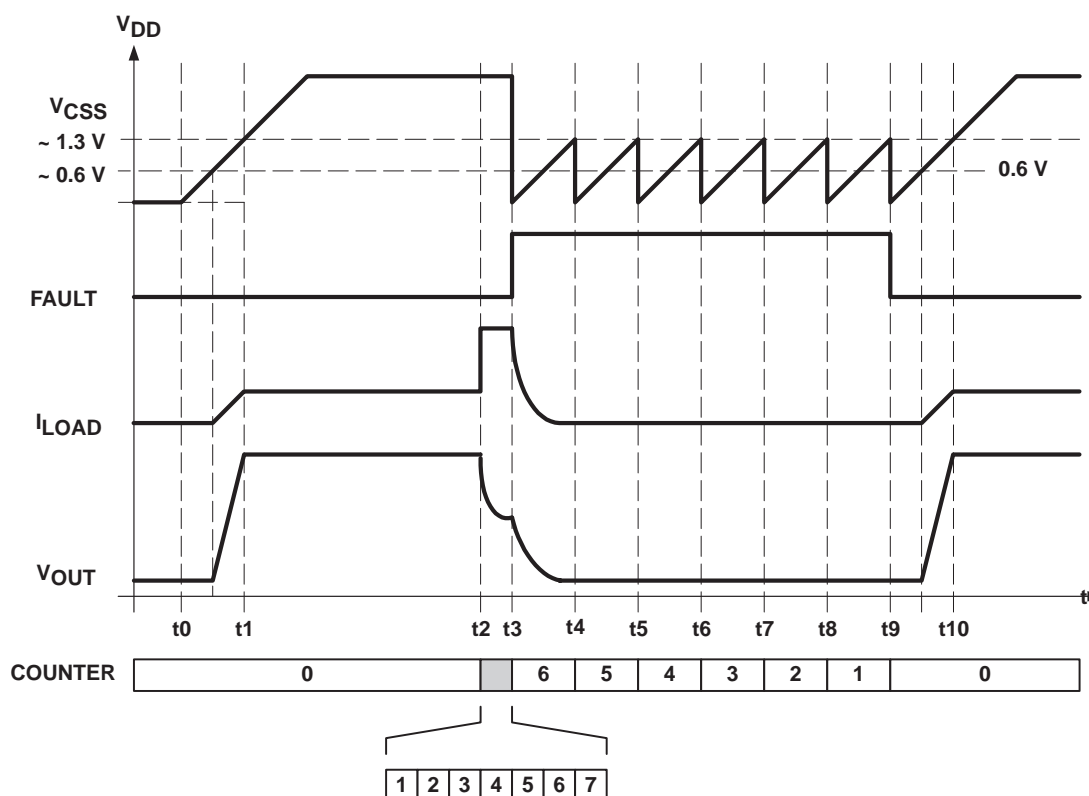


UDG-03165

Figure 3. Short Circuit Operation

## APPLICATION INFORMATION

Figure 4 shows the behavior of key signals during initial startup, during a fault and a successfully fault recovery. At time  $t_0$ , power is applied to the converter. The voltage on the soft-start capacitor ( $V_{CSS}$ ) begins to ramp up. At  $t_1$ , the soft-start period is completed and the converter is regulating its output at the desired voltage level. From  $t_0$  to  $t_1$ , pulse-by-pulse current limiting is in effect, and from  $t_1$  onward, overcurrent pulses are counted for purposes of determining a possible fault condition. At  $t_2$ , a heavy overload is applied to the converter. This overload is in excess of the overcurrent threshold. The converter starts limiting current and the output voltage falls to some level depending on the overload applied. During the period from  $t_2$  to  $t_3$ , the counter is counting overcurrent pulses, and at time  $t_3$  reaches a full count of 7. The soft-start capacitor is then discharged, the counter is decremented, and a fault condition is declared.



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**Figure 4. Overcurrent/Fault Waveforms**

When the soft start capacitor is fully discharged, it begins charging again at the same rate that it does on startup, with a nominal 3.7- $\mu$ A current source. When the capacitor voltage crosses 1.3 V, it is discharged again and the counter is decremented by one count. These transitions occur at  $t_3$  through  $t_9$ . Not shown in Figure 4 is that between  $t_3$  and  $t_9$ , LDRV is maintained OFF. At  $t_9$ , the counter has been decremented to 0. The fault logic is then cleared, the outputs are enabled, and the converter attempts to restart with a full soft-start cycle. The converter comes into regulation at  $t_{10}$ .

## APPLICATION INFORMATION

### SETTING THE CURRENT LIMIT

Connecting a resistor from VDD to ILIM sets the current limit. A 15- $\mu$ A current sink internal to the device causes a voltage drop at ILIM that becomes the short circuit threshold. Ensure that  $(V_{DD}-0.8\text{ V}) \leq V_{ILIM} \leq V_{DD}$ . The tolerance of the current sink is too loose to do an accurate current limit. The main purpose is for hard fault protection of the power switches. Given the tolerance of the ILIM sink current, and the  $R_{DS(on)}$  range for a MOSFET, it is generally possible to apply a load that thermally damages the converter. This device is intended for embedded converters where load characteristics are defined and can be controlled.

A local capacitor (with a value 50 pF to 150 pF) placed across the resistor between VDD and ILIM may improve coupling a common mode noise between VDD and ILIM.

### SOFT-START AND SHUTDOWN

These two functions are combined on the SS/SD pin. There is a VBE offset (0.65-V) between the external SS/SD pin and internal soft-start voltage at the error amplifier input, allowing the device to be enabled before starting  $V_{OUT}$  as shown in Figure 5. This reduces the transient current required to charge the output capacitor at startup, and allows for a smooth startup with no overshoot of the output voltage.

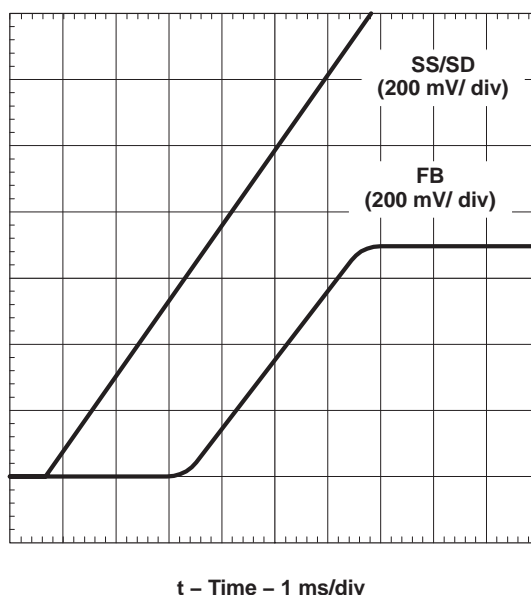
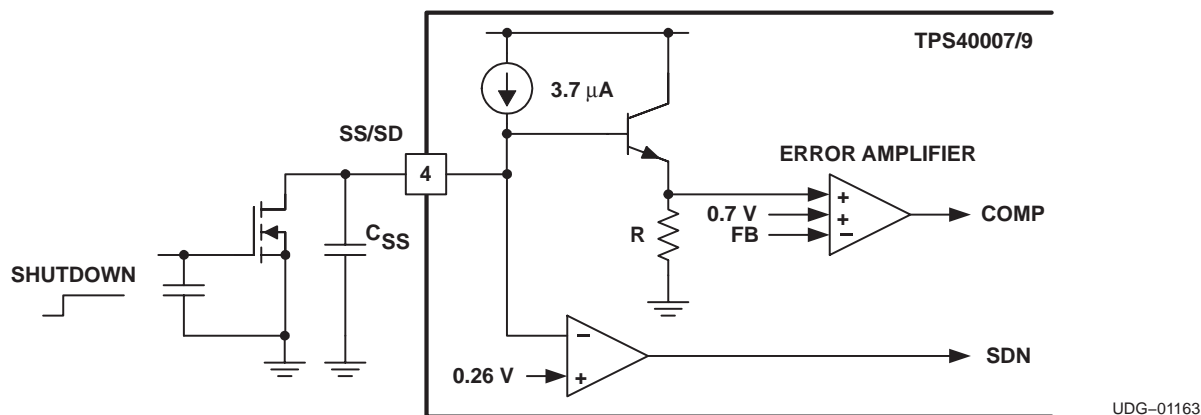


Figure 5. Offset Between SS/SD and FB at Startup

## APPLICATION INFORMATION

A shutdown feature can be implemented as shown in Figure 6. The device shuts down when the voltage at the SS/SD pin falls below 260 mV. Because of this limitation, it is recommended that a MOSFET be used as the controlling device, as in Figure 6. During shutdown, the total leakage current on the SW pin ( $I_{SW}$ ) is less than 2  $\mu$ A. When  $V_{SS/SD}$  is greater than 290 mV, the device is enabled with normal SW active bias currents.



**Figure 6. Shutdown Implementation**

Long soft start times may experience extended regions where the PWM pulse width is less than 100 ns. This could lead to momentary overlap between HDRV and LDRV. As a result, there is a momentary increase in ground or supply noise. It is important to ensure that the ground return of the synchronous rectifier be connected directly to the ground return of the input bank of bypass capacitors, in order to minimize ground noise from interfering with the controller during soft start. Also, if an external shutdown transistor is used in the application, it is important to place a local bypass capacitor between its gate and source on the board in order to minimize noise from interfering with the controller during soft-start.

## OUTPUT PRE-BIAS

The TPS4000x supports pre-biased  $V_{OUT}$  voltage applications. In cases, where the  $V_{OUT}$  voltage is held up by a pre-biasing supply while the controller is off, full synchronous rectification is disabled during the initial phase of soft starting the  $V_{OUT}$  voltage. When the first PWM pulses are detected during soft-start, the controller slowly activates synchronous rectification by starting the first LDRV pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by  $(1-D)$ , where  $D$  is the duty cycle of the converter. This scheme prevents the initial sinking the pre-bias output, and ensures that the  $V_{OUT}$  voltage starts and ramps up smoothly into regulation. Note, if the  $V_{OUT}$  voltage is pre-biased, PWM pulses start when the error amplifier soft-start input voltage rises above the commanded FB voltage.

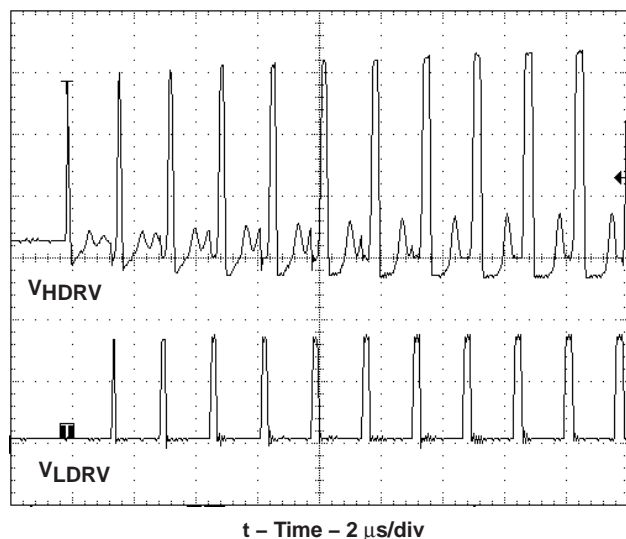
Figure 7 depicts the waveforms of the HDRV and LDRV output signals at the beginning PWM pulses. When HDRV turns off, diode rectification is enabled. Before the next PWM cycle starts, LDRV is turned on for a short pulse. With every cycle, the leading edge of LDRV is modulated, and the on-time of the synchronous rectifier is increased. Eventually, the leading edge of LDRV coincides with the falling edge of HDRV to achieve full synchronous rectification.

At most, synchronous rectifier modulation takes place for the first 128 cycles after PWM pulses start. Note that during the synchronous rectifier modulation region, the controller monitors pulse skipping. If the main HDRV skips a pulse, the controller also skips a LDRV pulse. Pulse skipping could be experienced if the loop response is much faster than the commanding soft-start ramp, especially when soft start times are long. The output voltage ratchets up as the soft-start ramp catches up to it. Appropriate setting of loop response curbs this effect.

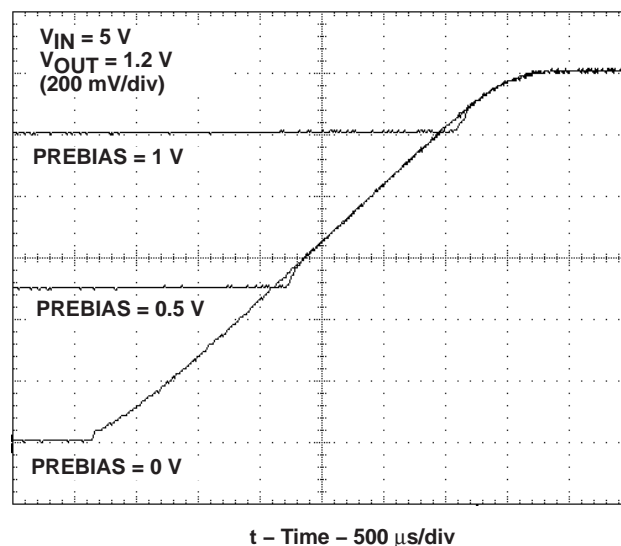
During normal regulation of the  $V_{OUT}$  voltage, the controller operates in full two-quadrant source/sink mode.

## APPLICATION INFORMATION

Figure 8 shows startup waveforms of a 1.2-V  $V_{OUT}$  voltage under different pre-bias scenarios. The first trace is when the output voltage starts with zero pre-bias. The second and third traces, respectively, the pre-bias levels are 0.5 V and 1.0 V.



**Figure 7.**  
**MOSFET Drivers at Beginning of Soft-Start**

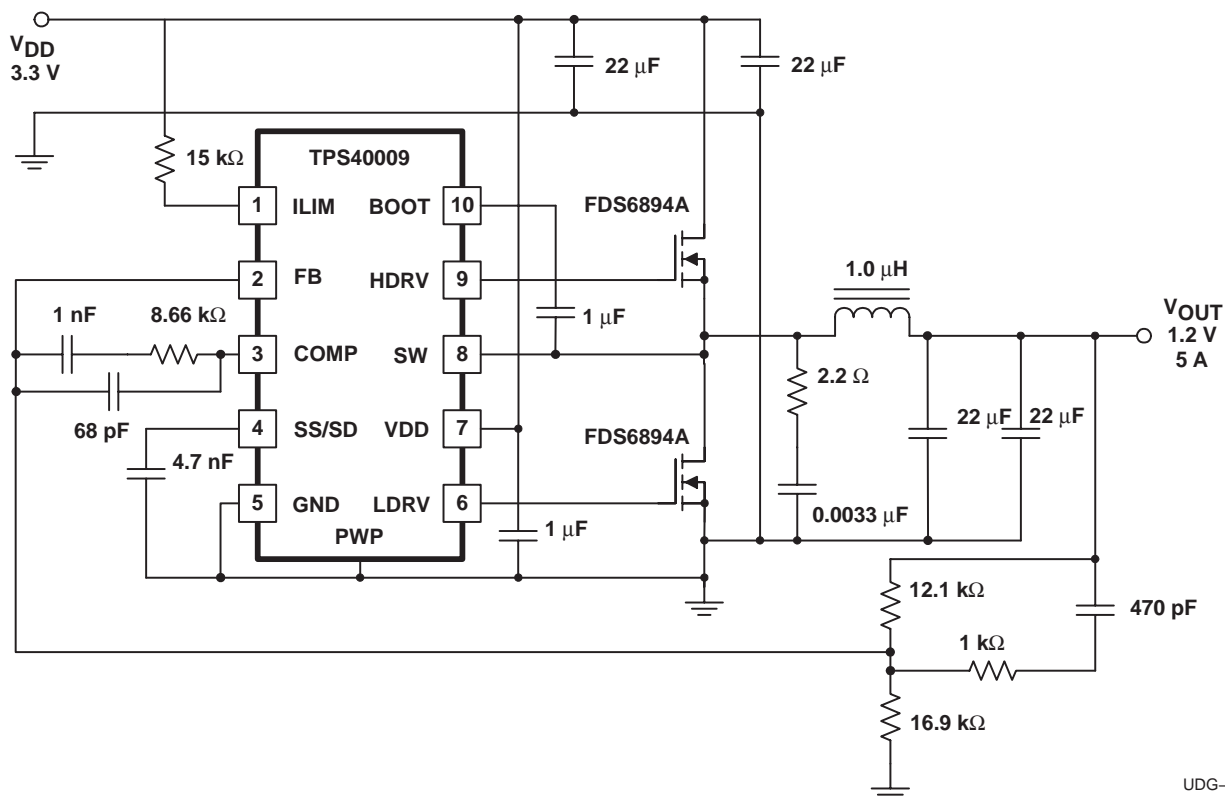


**Figure 8.**  
**Startup Waveforms**

The recommended  $V_{OUT}$  voltage pre-bias range is less than or equal to 90% of final regulation. That is, a pre-bias level between 90% and 100% of final regulation could lead to sinking the pre-bias supply. If the  $V_{OUT}$  voltage is initially set to higher than 100% of final regulation, the controller forces sinking current at the end of soft-start in order to bring the output quickly into regulation.

The following pages include design ideas for a few applications. For more ideas, detailed design information, and helpful hints, visit the TPS40000 resources at <http://power.ti.com>.

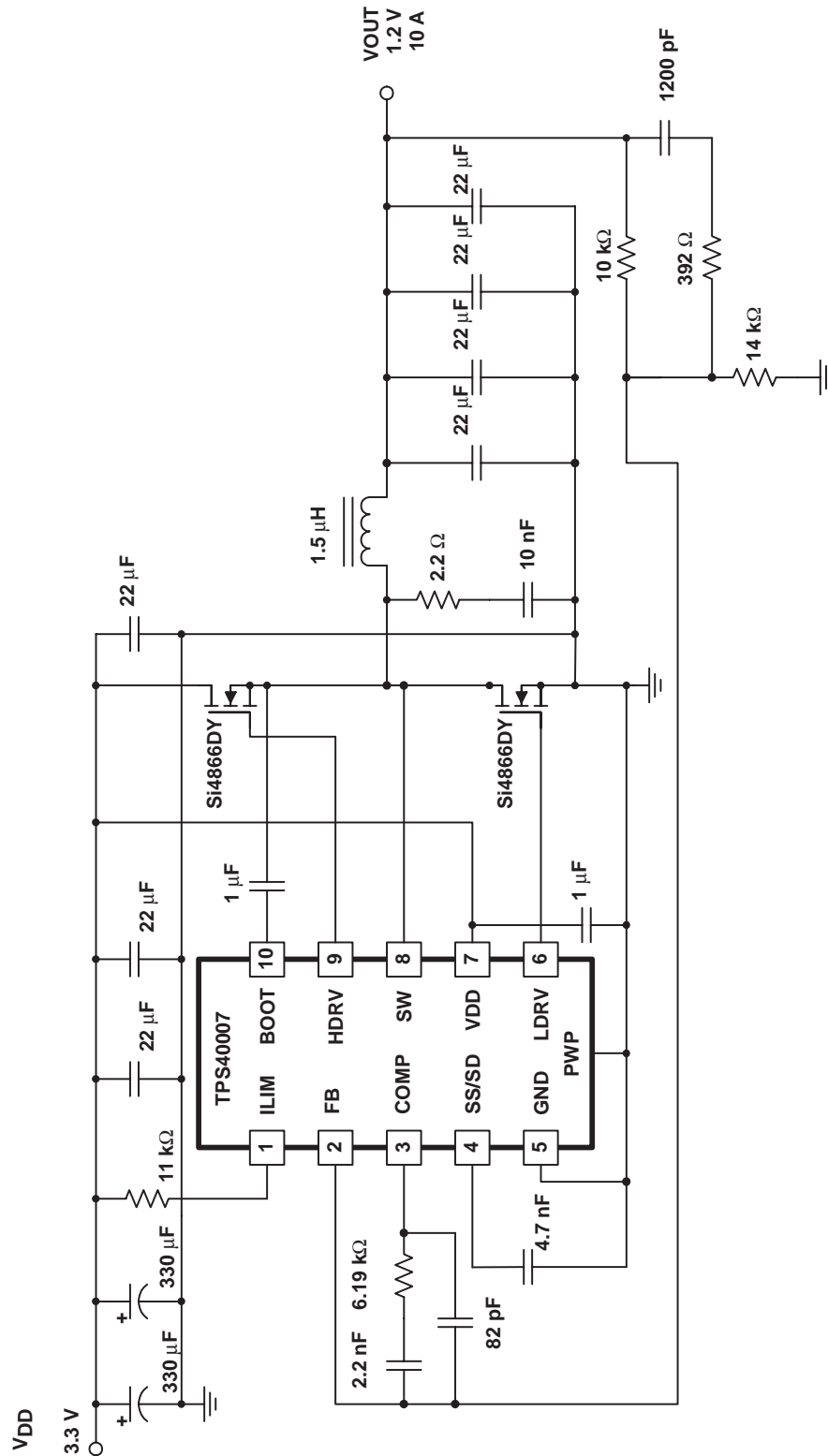
## APPLICATION INFORMATION



UDG-03164

**Figure 9. Small-Form Factor Converter for 3.3 V to 1.2 V at 5 A.**

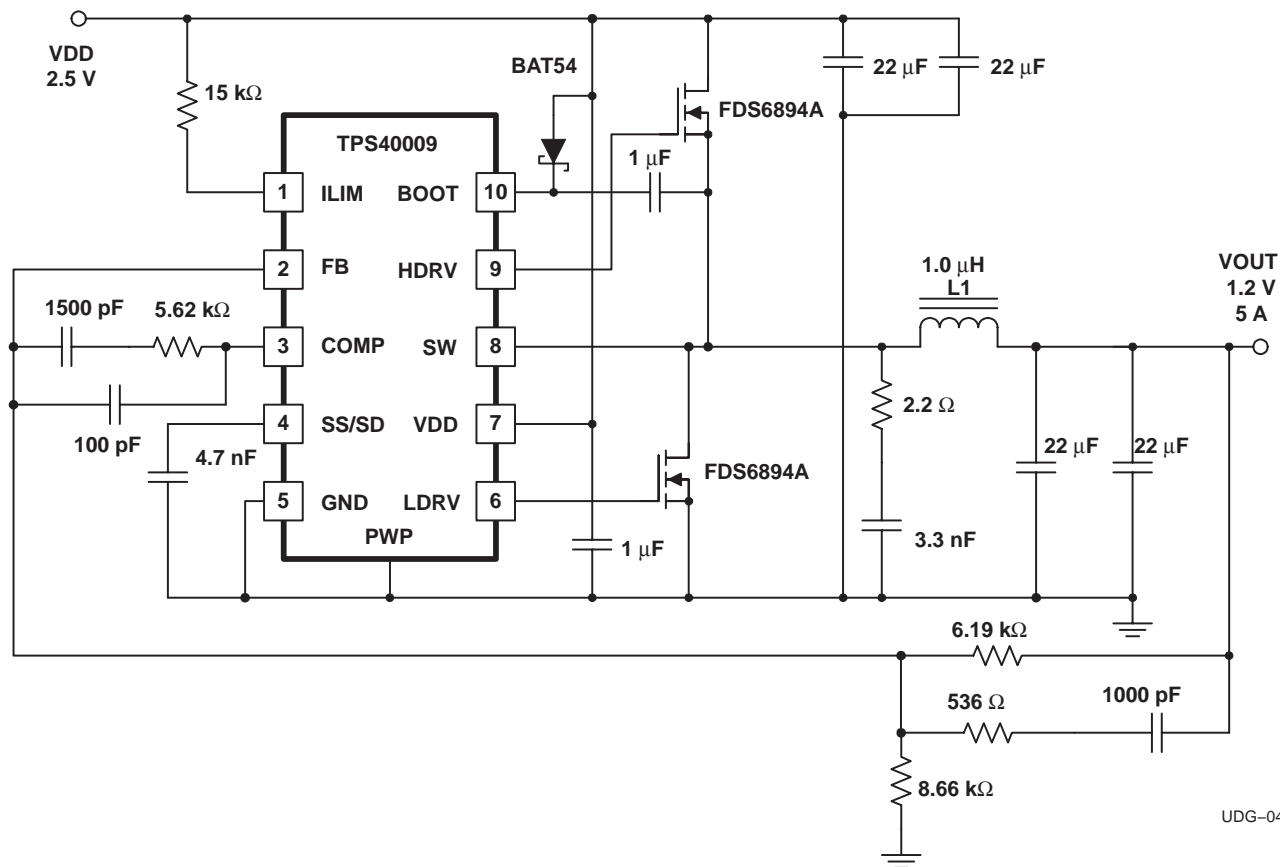
## APPLICATION INFORMATION



UDG-04014

Figure 10. High-Current Converter for 3.3 V to 1.2 V at 10 A.

## APPLICATION INFORMATION



UDG-04028

**Figure 11. Ultra-Low-Input Voltage Converter for 2.5 V to 1.2 V at 5 A**



## APPLICATION INFORMATION

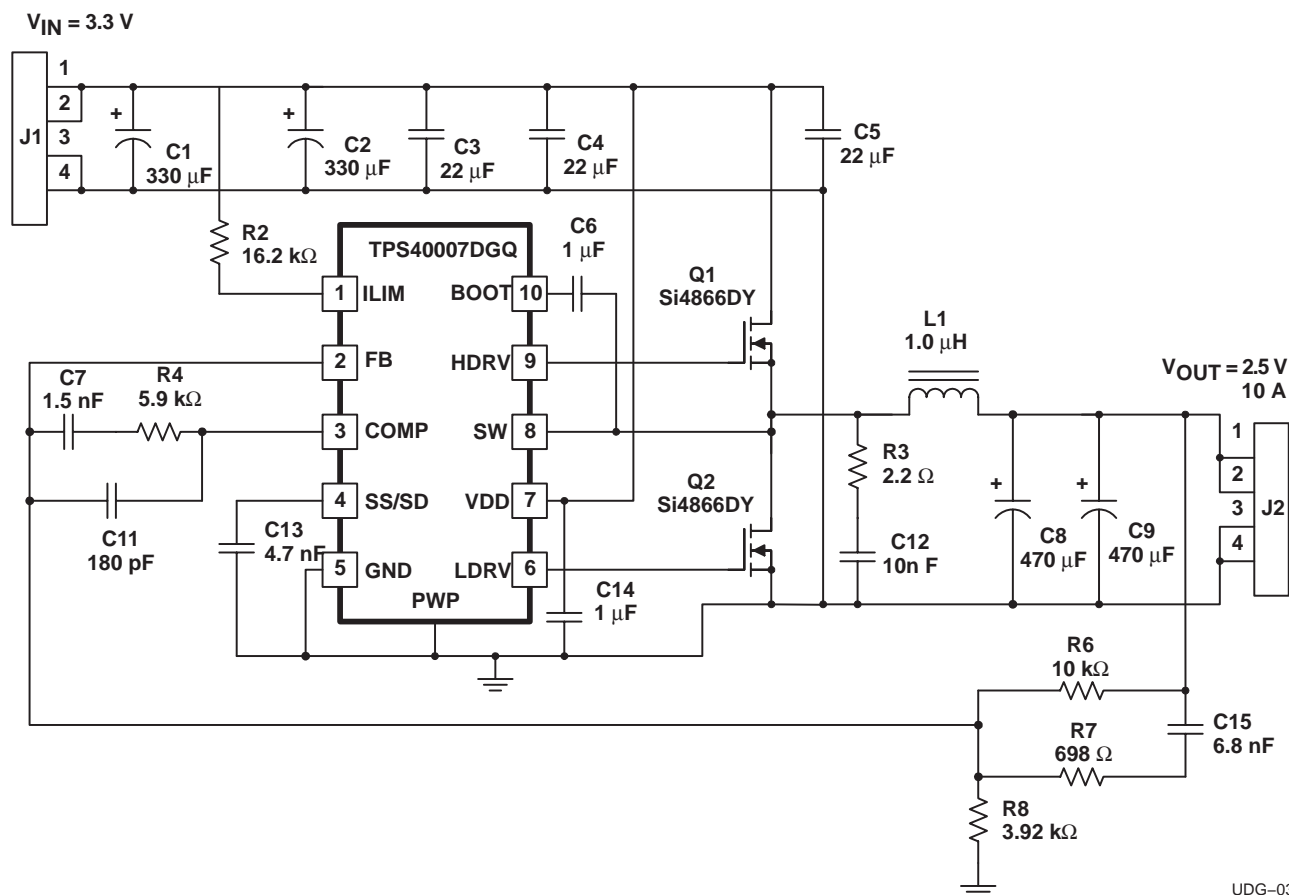


Figure 12. TPS40007EVM-001 Ultra-High-Efficiency Converter for 3.3 V to 2.5 V at 10 A

## APPLICATION INFORMATION

### Layout Considerations

Successful operation of the TPS4000x controllers is dependent upon proper converter layout and grounding techniques. High current returns for the SR MOSFET's source, and ground connection of the input and output capacitors, should be kept on a single ground plane. Bypassing capacitors at the device should return closely to the GND (pin 5) of the device. The GND (pin 5) and PowerPAD™ should connect together at the device and return to the main ground plane.

Proper operation of the Predictive Gate Drive™ circuits is dependent upon detecting low-voltage thresholds on the SW node. To ensure that the signal at the SW pin accurately represents the voltage at the main switching node, the connection from SW (pin 8) to the main switching node of the converter should be kept as short and as wide as possible. If the SW trace should traverse multiple board layers between the device and the MOSFETs, multiple vias should be used.

Gate drive outputs, LDRV and HDRV, should be kept as short as possible to minimize inductances of the traces. While the controller does not require the usage of external resistors between the driver pins and the gates of the MOSFETs, adding small resistors in series with very high gate charge MOSFETs could minimize the effects of high frequency ringing.

The PowerPAD™ package provides low thermal impedance for heat removal from the device. The PowerPAD™ derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD™ package (See Thermal Pad Mechanical Data on page 21)

## TYPICAL CHARACTERISTICS

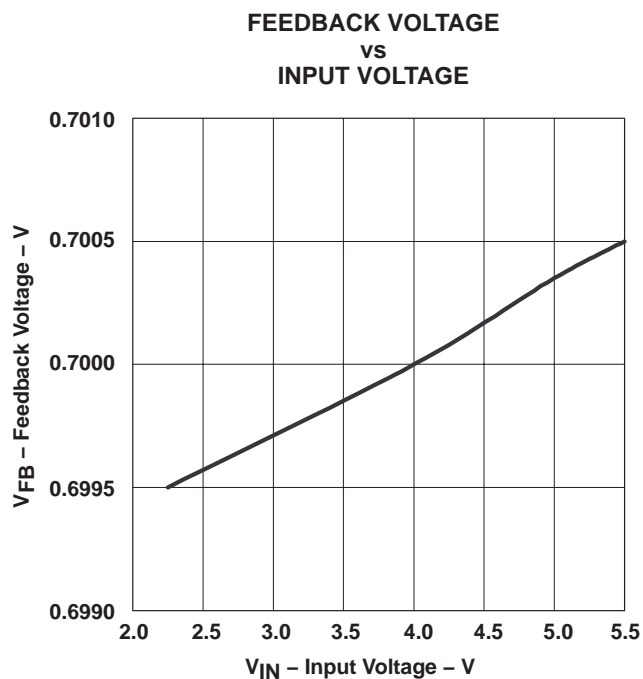
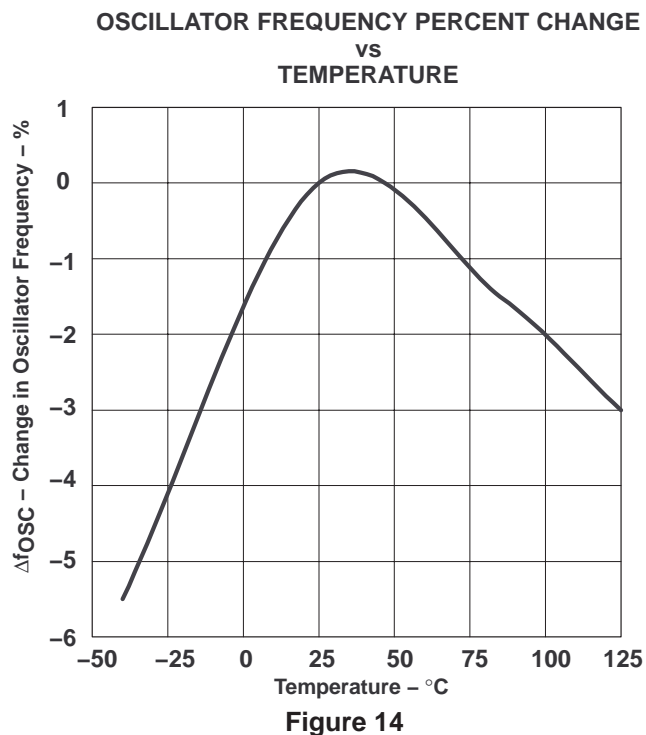
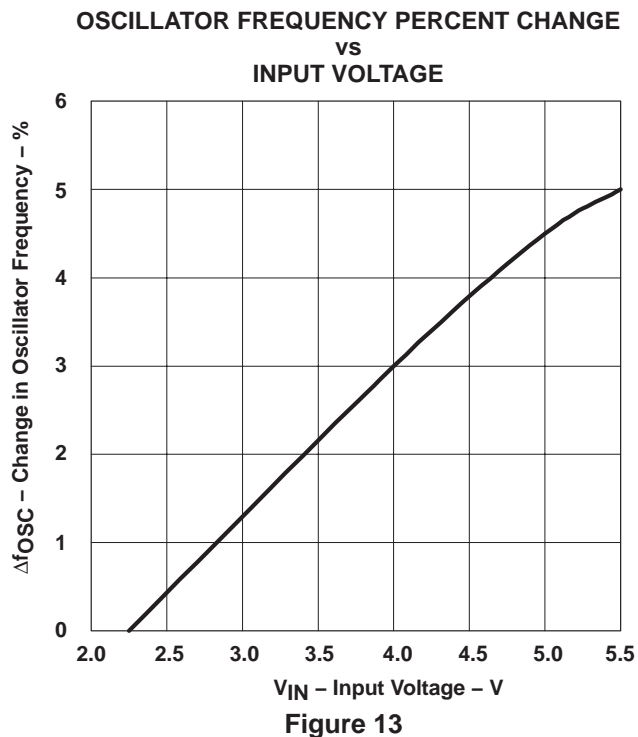


Figure 15

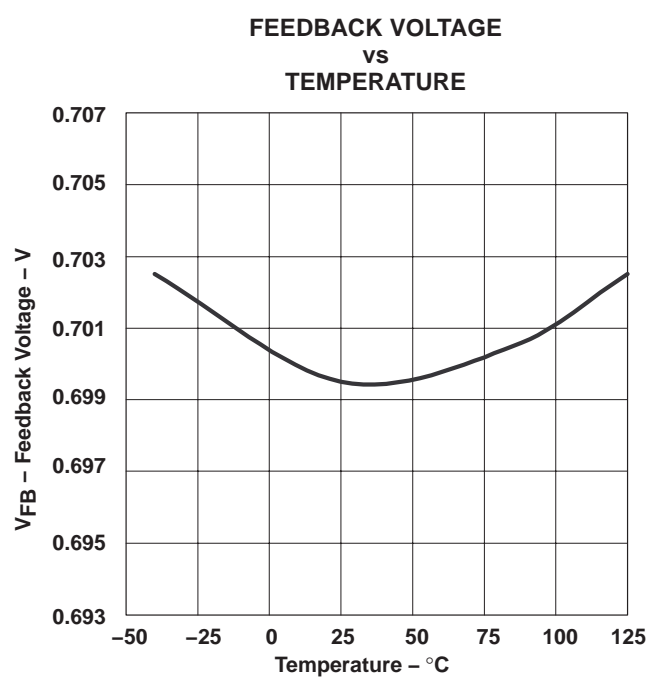
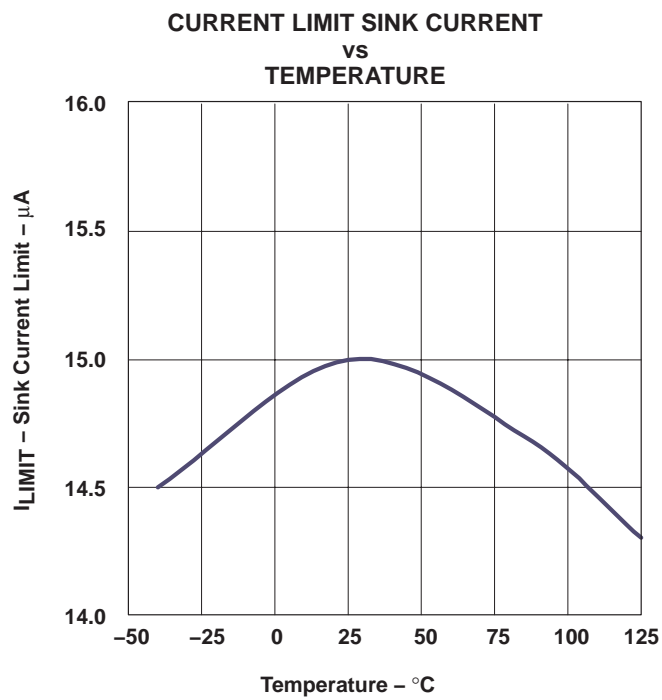
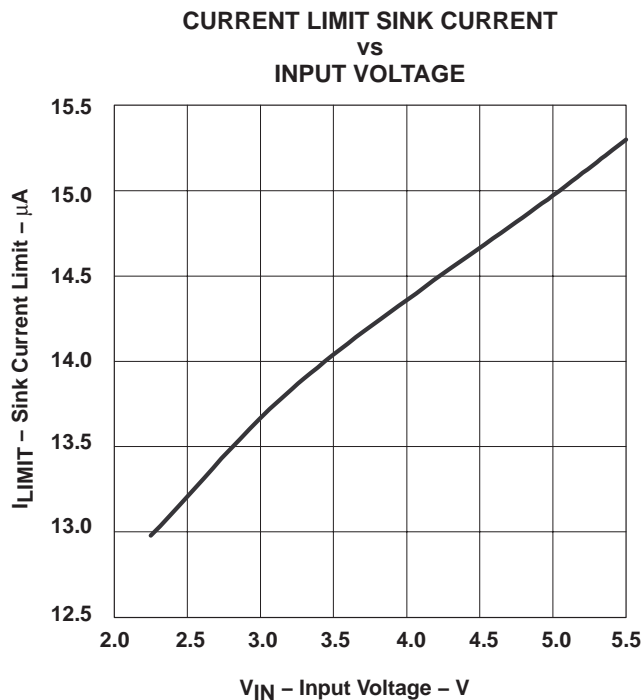
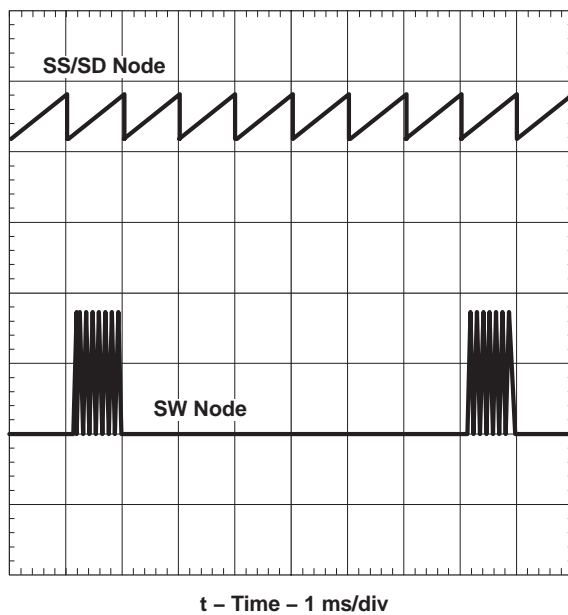


Figure 16

## TYPICAL CHARACTERISTICS



## SHORT CIRCUIT PROTECTION



**Figure 19**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40007DGQ	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40007	<a href="#">Samples</a>
TPS40007DGQG4	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40007	<a href="#">Samples</a>
TPS40007DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40007	<a href="#">Samples</a>
TPS40007DGQRG4	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40007	<a href="#">Samples</a>
TPS40009DGQ	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40009	<a href="#">Samples</a>
TPS40009DGQG4	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40009	<a href="#">Samples</a>
TPS40009DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40009	<a href="#">Samples</a>
TPS40009DGQRG4	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40009	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40007DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS40009DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40007DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
TPS40009DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0



## GENERIC PACKAGE VIEW

**DGQ 10**

**PowerPAD™ HVSSOP - 1.1 mm max height**

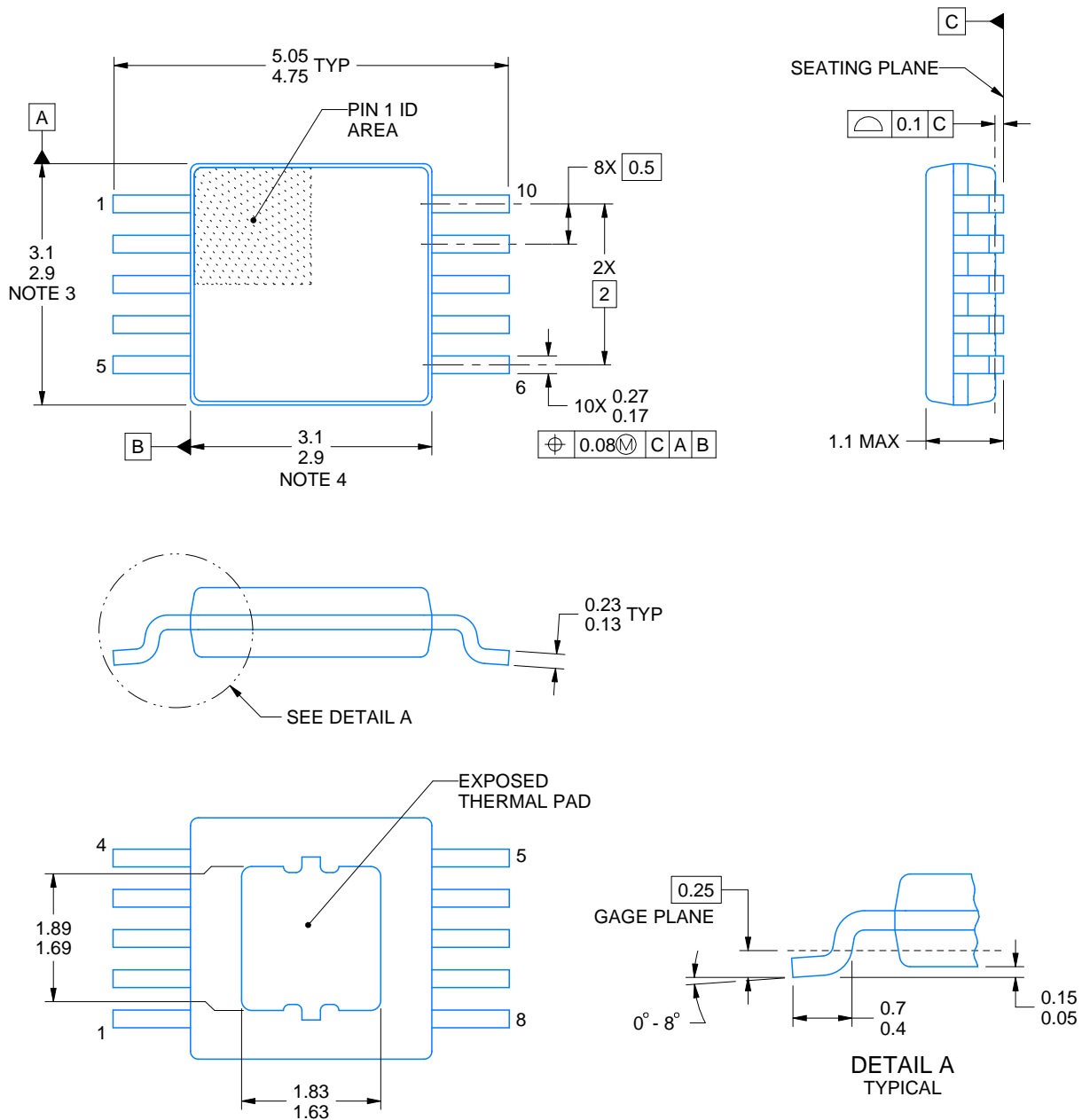
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224775/A

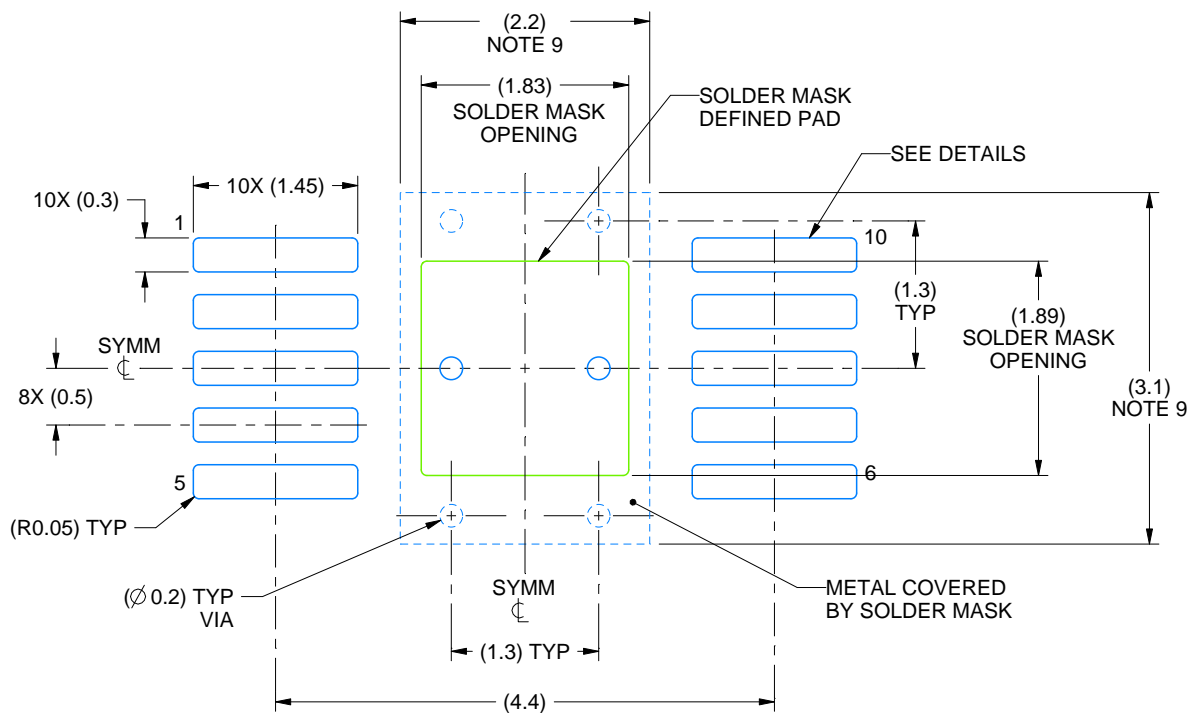


4218842/A 01/2019

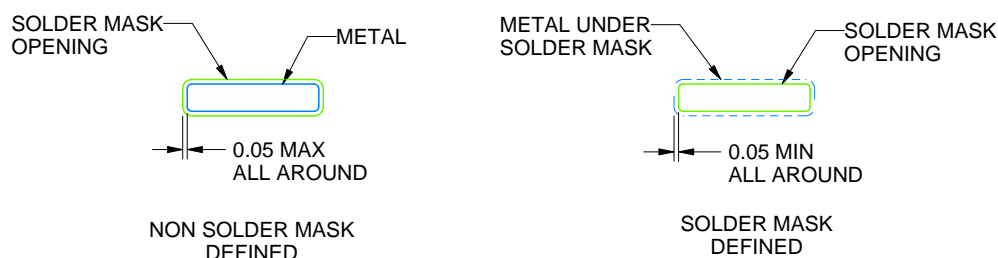
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4218842/A 01/2019

NOTES: (continued)

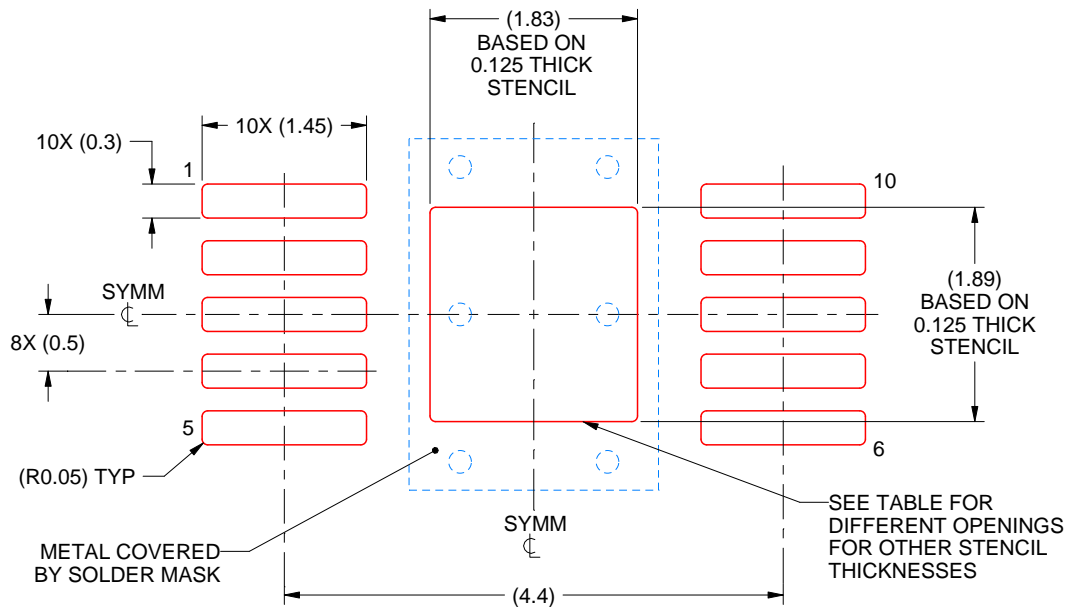
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

4218842/A 01/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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