具有小解决方案尺寸的 TPS6380x 高效率、低 I_Q 降压/升压转换器

1 特性

- 两个引脚对引脚器件选项，TPS63805 和 TPS63806 具有特定的应用重点
- 输入电压范围：1.3V 至 5.5V
  - 器件启动时输入电压大于 1.8V
- 输出电压范围：1.8V 至 5.2V（可调）
- 在整个负载范围内具有高效率
  - 低工作静态电流
  - 具有省电模式和适用于强制 PWM 模式的模式选择
- 峰值电流降压/升压模式架构
  - 可在降压、降压/升压和升压操作模式之间定义切换点
  - 正向和反向电流运行
  - 启动至预偏置输出
- 安全、可靠运行 特性
  - 集成软启动
  - 过热和过压保护
  - 带负载断开功能的真正关断功能
  - 正向和反向电流限制
- TPS63805
  - 经优化可实现 18.5mm^2 的最小解决方案尺寸（与 22µF 最小输出电容器配合使用）
  - $V_I \geq 2.3V$、$V_O = 3.3V$ 时，输出电流为 2A
  - 11µA 运行静态电流
- TPS63806
  - 经优化可实现最佳负载阶跃响应（电流阶跃为 2A 时可实现 180mV 负载阶跃响应）
  - 高达 2.5A 的瞬态输出电流支持
  - 13µA 运行静态电流

删除了射频放大器电源

2 应用

- TPS63805
  - 系统前置稳压器（智能手机、平板电脑、EFT 终端和远程信息处理）
  - 负载点调节（有线传感器、端口/电缆适配器和加密狗）
- TPS63806
  - 飞行时间摄像头传感器（智能手机、电子智能锁和 IP 网络摄像头）
  - 宽带网络无线电或 SoC 电源（物联网、跟踪、家庭自动化和 EPOS）
  - 热电器件电源（TEC、光纤模块）
  - 通用电压稳定器

3 说明

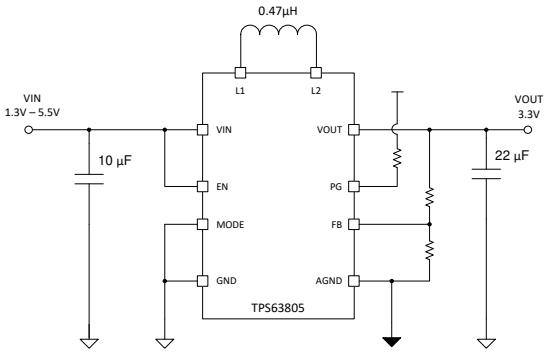
TPS63805 和 TPS63806 是高效率、高输出电流降压/升压转换器。根据输入电压不同，当输入电压近似等于输出电压时，它们会自动以升压、降压或全新的 4 周期降压/升压模式运行。在定义的阈值内进行模式切换，避免不必要的模式内切换，以减少输出电压纹波。这类器件的输出电压可在较宽输出电压范围内通过电阻式分压器进行单独调整。TPS63805 以最少的物料清单实现了最小的解决方案尺寸。 静态电流为 11µA，可在极小直至空载条件下实现最高效率。

器件信息(1)

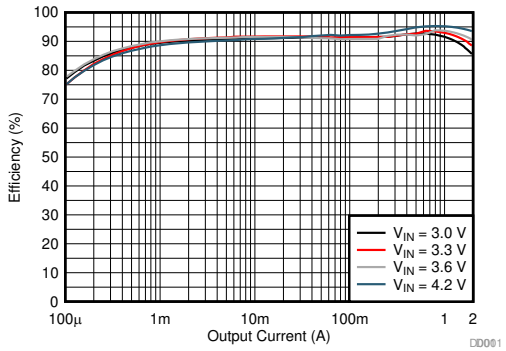
器件型号	封装	封装尺寸（标称值）
TPS63805	3x5 焊球 WCSP（0.4mm 间距）	2.3mm x 1.4mm
TPS63806		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



效率与输出电流间的关系 ($V_O = 3.3V$)



目录

4 修订历史记录

Changes from Revision B (August 2019) to Revision C **Page**

- 从数据表标题中删除了 2A ... 1
- 更改了*特性* 列表以包含引脚对引脚器件 TPS63805 和 TPS63806 ... 1
- 从 *应用* ... 1
- 向*应用* 添加了飞行时间摄像头传感器、宽带网络无线电或 SoC 电源以及通用电压稳压器 ... 1
- 更改了*说明* ... 1
- Changed application information in Table 2 from ≥ 100 µF to 100 µF to be aligned with Table 3 ... 18
- Added 0.8 mm component height capacitors to Table 5 ... 19
- Added comment column for V_O condition of application characteristics ... 20
- Changed Figure 17 image data ... 24

Changes from Revision A (October 2018) to Revision B **Page**

- 更改了*特性* 列表 ... 1
- 向数据表中添加了 TPS63086 ... 1
- 将可调输出电压范围更改为 5.0V 至 5.2V ... 1
- 从特性列表中删除了*使用低输出电容值和高输出电容值* 特性 ... 1
- 删除了 特性 列表中的封装尺寸参数 ... 1
- 更改了*说明* 部分的文本以包含 TPS63805 和 TPS63806 ... 1
- 更改了效率与输出电流之间关系的曲线 ... 1
- Added If not used can be left floating for PG-pin ... 4
- Added V_{IN} = 3.6 V for typical value in condition text ... 5
- Changed V_{OUT} from 5 V to 5.2 V condition text ... 5
- Added PG Pin ... 5
- Changed PFM/PWM pin name to Mode ... 5
- Changed V_O from 5 V to 5.2 V ... 5
- Changed typical effective output capacitance from 10 uF to 8.2 uF ... 5

- Added Vo conditions for C_O range 5
- Changed Soft-start Current limit ramp time test conditions 6
- Changed typical Soft-start Current limit ramp time from 0.6 ms to 224 us 6
- Changed Delay from EN-edge until rising V_{OUT} test conditions 6
- Changed typical Delay from EN-edge until rising V_{OUT} from 100 us to 321 us 6
- Changed typical Overvoltage Protection Threshold from 5.66 V to 5.7 V 6
- Changed maximum Overvoltage Protection Threshold from 5.8 V to 5.9 V 6
- Changd Peak Inductor Current to enter PFM-Mode to 1.06 A typical only 6
- Changed minimum Peak Current Limit Boost Mode from 3.5 A to 4 A 6
- Changed typical Peak Current Limit Boost Mode from 4.8 A to 5 A 6
- Changed maximum Peak Current Limit Boost Mode from 5.8 A to 5.75 A 6
- Changed Peak Current Limit for Reverse Operation to 0.9 A typical only 6
- Changed Inductor Switching Frequency, Buck Mode from 2.7 MHz to 1.6 MHz 7
- Changed typical Line regulation from 0.5% to 0.3 % 7
- Changed typical Load regulation from 0.5% to 0.1% 7
- Changed Quiescent Current vs. Temperature Curve for TPS63805 in Typical Characteristics 8
- Changed Typical Characteristics shutdown current vs. temperature curve for TPS63805 8

Changes from Original (July 2018) to Revision A **Page**

- 将 TPS63805 的文档状态从*预告信息* 更改为*生产数据* 1

5 说明 （续）

TPS63806 针对需要关注重负载曲线下的负载阶跃响应的 应用 进行了优化。

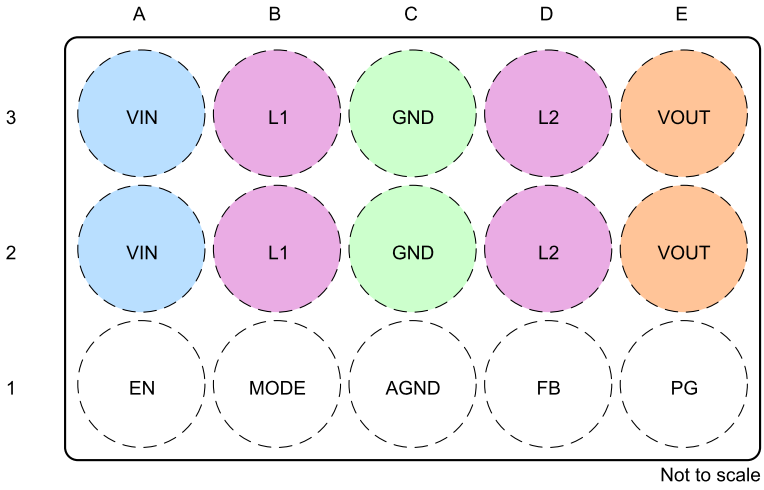
TPS63805 和 TPS63806 采用 1.4mm x 2.3mm 封装。该器件可与微型无源组件配合使用，从而使整体解决方案尺寸保持小巧。

6 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE (V_O)	$I_{(Q;VIN)}$ (TYP.)	$C_{(O,EFF)}$ (MIN.)	V_{PP} LOAD TRANSIENT RESPONDS (TYP.)
TPS63805	Adjustable	11 µA	7 µF	320 mV
TPS63806	Adjustable	13 µA	21 µF	180 mV

7 Pin Configuration and Functions

WCSP Package
Top View



Not to scale

Pin Functions Table

PIN		DESCRIPTION
NO	NAME	
A2, A3	VIN	Supply voltage
B2, B3	L1	Connection for inductor
A1	EN	Device Enable input. Set HIGH to enable and LOW to disable. It must not be left floating.
C2, C3	GND	Power ground
B1	MODE	PFM/PWM mode selection. Set LOW for power safe mode, set HIGH for forced PWM mode. It must not be left floating.
C1	AGND	Analog ground
D2, D3	L2	Connection for inductor
E2, E3	VOUT	Power stage output
D1	FB	Voltage feedback sensing pin
E1	PG	Power good indicator, open drain output. If not used can be left floating.

8 Specifications

8.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, L1, L2, EN, MODE, VOUT, FB, PG	–0.3	6	V
	L1, L2 (AC, less than 10 ns)	–3	9	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_I	Input voltage		1.3 (1)		5.5	V
V_O	Output voltage		1.8		5.2 (2)	V
C_I	Effective capacitance connected to V_{IN}		4	5		µF
L	Effective inductance		0.37	0.47	0.57	µH
C_O	TPS63805 Effective capacitance connected to V_{OUT}	1.8 V ≤ V_O ≤ 2.3 V	10			µF
		V_O > 2.3 V	7	8.2		µF
C_O	TPS63806; Effective capacitance connected to V_{OUT}	1.8 V ≤ V_O < 2.3 V	30			µF
		V_O > 2.3 V	21	27		µF
T_J	Operating junction temperature	Operating junction temperature	–40		125	°C

(1) Minimum startup voltage of V_I > 1.8 V until power good
(2) V_O margin for accuracy and load steps is considerd in absolut maximum ratings

8.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPS63805, TPS63806 3x5 Ball WCSP 15 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	78.8	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	19.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

V_{IN}= 1.8 V to 5.5 V, V_{OUT} = 1.8 V to 5.2 V , T_J= –40°C to +125°C, typical values are at V_{IN}= 3.6 V, V_{OUT} = 3.3 V and T_J= 25°C (unless otherwise noted)

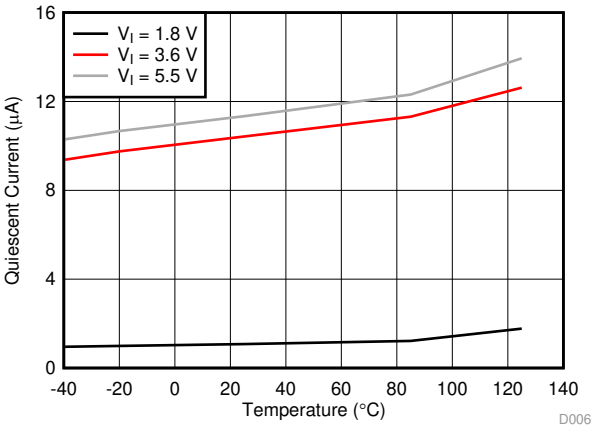
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
$V_{IN;LOAD}$	Minimum input voltage for full load, once started	I_{OUT} = 2 A, VOUT = 3.3 V, T_J = 25°C			2.3		V
$I_{Q;VIN}$	Quiescent current into VIN	TPS63805; T_J = 25°C, EN = V_{IN} = 3.6 V, V_{OUT} = 3.3 V, not switching			11		µA
$I_{Q;VIN}$	Quiescent current into VIN	TPS63806; T_J = 25°C, EN = V_{IN} = 3.6 V, V_{OUT} = 3.3 V, not switching			13		µA
I_{SD}	Shutdown current into VIN	EN = low, -40°C ≤ T_J ≤ 85°C, V_{IN} = 3.6 V, V_{OUT} = 0 V			45	600	nA
UVLO	Undervoltage lockout threshold	V_{IN} falling, VOUT ≥ 1.8 V, once started		1.2	1.25	1.29	V
	Undervoltage lockout threshold	V_{IN} rising		1.6	1.7	1.79	V
T_{SD}	Thermal shutdown	Temperature rising			150		°C
$T_{SD;HYST}$	Thermal shutdown hysteresis				20		°C
SOFT-START, POWER GOOD							
T_{ramp}	Soft-start, Current limit ramp time	T_J = 25°C, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_O = 3.5 A, time from first switching to power good			224		µs
T_{delay}	Delay from EN-edge until rising V_{OUT}	T_J = 25°C, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, Delay from EN-edge until rising first switching			321		µs
LOGIC SIGNALS EN, MODE							
$V_{THR;EN}$	Threshold Voltage rising for EN-Pin			1.07	1.1	1.13	V
$V_{THF;EN}$	Threshold Voltage falling for EN-Pin			0.97	1	1.03	V
V_{IH}	High-level input voltage			1.2			V
V_{IL}	Low-level input voltage					0.4	V
$V_{PG;rising}$	Power Good threshold voltage	VOUT rising, referenced to VOUT nominal			95		%
$V_{PG;falling}$		VOUT falling, referenced to VOUT nominal			90		%
$V_{PG;Low}$	Power Good low-level output voltage	I_{SINK} = 1 mA				0.4	V
$t_{PG;delay}$	Power Good delay time	V_{FB} falling			14		µs
I_{lkg}	Input leakage current				0.01	0.2	µA
OUTPUT							
I_{SD}	Shutdown current into VOUT	EN = low, -40°C ≤ T_J ≤ 85°C, V_{IN} = 3.6 V, V_{OUT} = 3.3 V			±0.5	±600	nA
V_{FB}	Feedback Regulation Voltage				500		mV
V_{FB}	Feedback Voltage accuracy	PWM mode		–1		1	%
	Overvoltage Protection Threshold	V_{OUT} rising		5.5	5.7	5.9	V
		V_{IN} rising		5.5	5.7	5.9	V
$I_{PWM/PFM}$	Peak Inductor Current to enter PFM-Mode	V_{IN} = 3.6 V; V_{OUT} = 3.3 V			1.06		A
I_{FB}	Feedback Input Bias Current	V_{FB} = 500 mV			5	100	nA
I_{PK}	Peak Current Limit, Boost Mode	TPS63805; V_{IN} ≥ 2.5 V		4	5	5.75	A
	Peak Current Limit, Buck-Boost Mode				5		A
	Peak Current Limit, Buck Mode				3.8		A
I_{PK}	Peak Current Limit, Boost Mode	TPS63806; V_{IN} ≥ 2.5V		4.4	5.5	6.25	A
	Peak Current Limit, Buck-Boost Mode				5.5		A
	Peak Current Limit, Buck Mode				4		A
$I_{PK;Reverse}$	Peak Current Limit for Reverse Operation	V_I = 5 V, V_O = 3.3 V			–0.9		A
Buck $R_{DS;ON}$	High-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V; $I_{(L2)}$ = 0.19 A	V_{IN} = 3 V, V_{OUT} = 3.3 V; I_O = 0.5 A		47		mΩ
	Low-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V; $I_{(L2)}$ = 0.19 A	V_{IN} = 3 V, V_{OUT} = 3.3 V; I_O = 0.5 A		30		mΩ

Electrical Characteristics (continued)

V_{IN}= 1.8 V to 5.5 V, V_{OUT} = 1.8 V to 5.2 V , T_J= –40°C to +125°C, typical values are at V_{IN}= 3.6 V, V_{OUT} = 3.3 V and T_J= 25°C (unless otherwise noted)

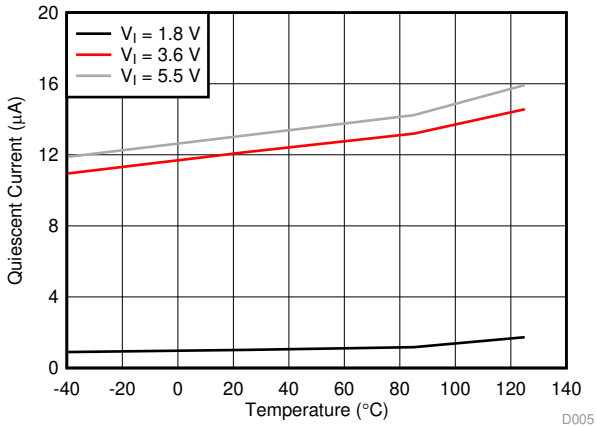
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Boost $R_{DS;ON}$	High-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V; $I_{(L1)}$ = 0.19 A	V_{IN} = 3 V, V_{OUT} = 3.3 V; I_O = 0.5 A		43		mΩ
	Low-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V; $I_{(L1)}$ = 0.19 A	V_{IN} = 3 V, V_{OUT} = 3.3 V; I_O = 0.5 A		18		mΩ
f_{SW}	Inductor Switching Frequency, Boost Mode	V_{IN} = 2.3V, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C			2.1		MHz
	Inductor Switching Frequency, Buck-Boost Mode	V_{IN} = 3.3V, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C			1.4		MHz
	Inductor Switching Frequency, Buck Mode	V_{IN} = 4.3, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C			1.6		MHz
	Line regulation	V_{IN} = 2.4 V to 5.5 V, V_{OUT} = 3.3V, I_{OUT} = 2 A			0.3		%
	Load regulation	V_{IN}= 3.6 V, V_{OUT} = 3.3V, I_{OUT} = 0 A to 2 A, forced-PWM mode			0.1		%

8.6 Typical Characteristics



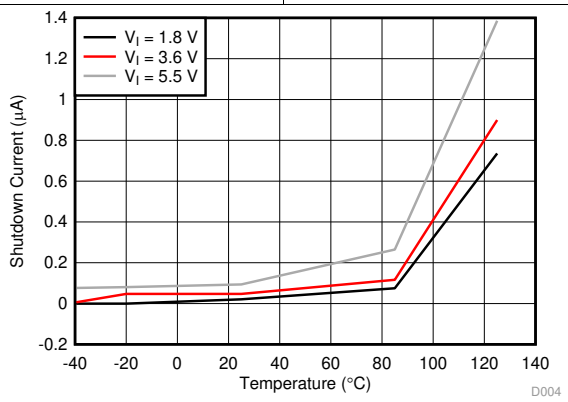
MODE = LOW V_O = 3.3 V I_O = 0 mA, not switching

图 1. TPS63805 Quiescent Current vs. Temperature



MODE = LOW V_O = 3.3 V I_O = 0 mA, not switching

图 2. Quiescent Current vs. Temperature



EN = LOW

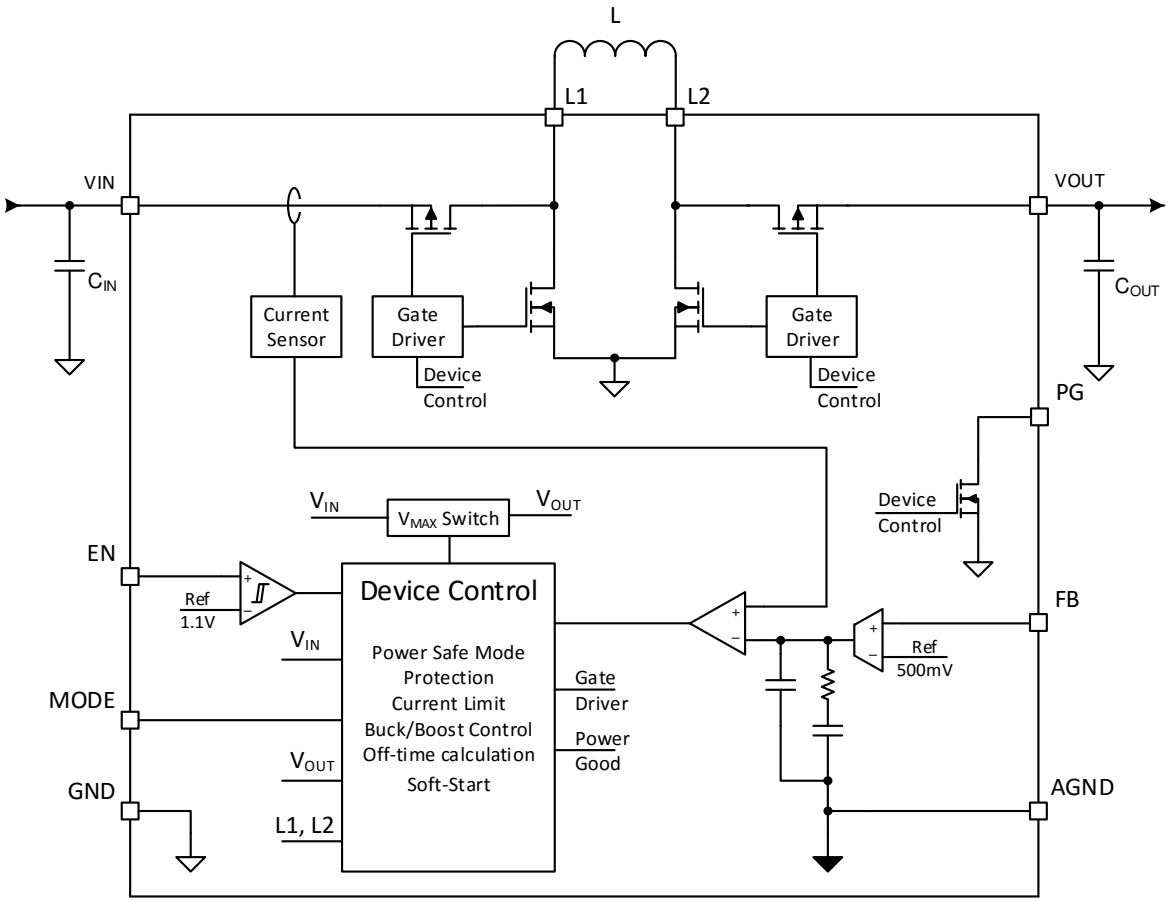
图 3. Shutdown Current vs. Temperature

9 Detailed Description

9.1 Overview

The TPS63805 and TPS63806 buck-boost converter use four internal switches to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output load range. To regulate the output voltage at all possible input voltage conditions, the device automatically transitions between buck, buck-boost, and boost operation as required by the operating conditions. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. When the input voltage is close to the output voltage, it operates in a 3-cycle buck-boost operation. In this mode, all four switches are active (see *Buck-Boost Operation*). The RMS current through the switches and the inductor is kept at a minimum to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep high efficiency over the complete input voltage range. The device provides a seamless transition between all modes.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Control Loop Description

The TPS63805 and TPS63806 use a peak current mode control architecture. It has an inner current loop where it measures the peak current of the boost high-side MOSFET and compares it to a reference current. This current is the output of the outer voltage loop. It measures the output voltage via the FB-pin and compares it with the internal voltage reference. That means, the outer voltage loop measures the voltage error (V_{REF}-V_{FB}), and transforms it into the system current demand (I_{REF}) for the inner current loop.

图 4 shows the simplified schematic of the control loop. The error amplifier and the type-2 compensation represent the voltage loop. The voltage output is converted into the reference current IREF and fed into the current comparator.

The scheme shows the skip-comparator handling the power-save mode (PFM) to achieve high efficiency at light loads. See *Power Save Mode Operation* for further details.

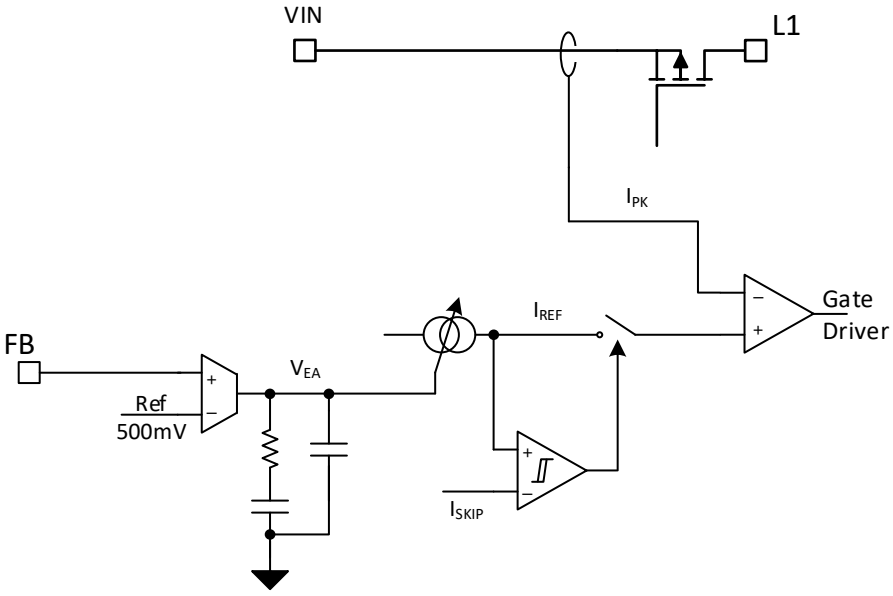


图 4. Control Loop Architecture Scheme

9.3.2 Precise Device Enable: Threshold- or Delayed Enable

The enable-pin is a digital input to enable or disable the device by applying a high or low level. The device enters shutdown when EN is set low. In addition, this input features a precise threshold and can be used as a comparator that enables and disables the part at a defined threshold. This allows you to drive the state by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. The enable pin can also be used with an external voltage divider to set a user-defined minimum supply voltage. For proper operation, the EN pin must be terminated and must not be left floating.

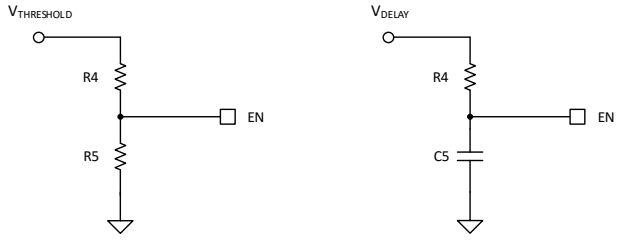


图 5. Circuit Example for How to Use the Precise Device Enable Feature

Feature Description (接下页)

9.3.3 Mode Selection (PFM/PWM)

The mode-pin is a digital input to enable the automatic PWM/PFM mode that features the highest efficiency by allowing pulse-frequency-modulation for lower output currents. This mode is enabled by applying a low level. The device can be forced in PWM operation regardless of the output current to achieve minimum output ripple by applying a high level. This pin must not be left floating.

9.3.4 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. It activates the device once the input voltage (V_I) has increased the $UVLO_{rising}$ value. Once active, the device allows operation down to even smaller input voltages, which is determined by the $UVLO_{falling}$. This behavior requires V_O to be higher than the minimum value of 1.8 V.

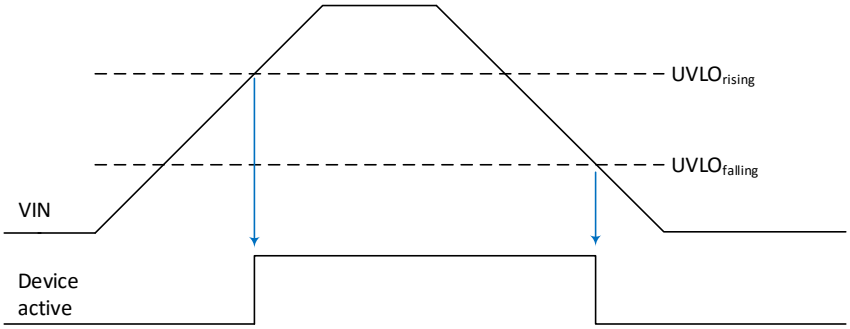


图 6. Rising and Falling Undervoltage Lockout Behavior

9.3.5 Soft-start

To minimize inrush current and output voltage overshoot during start-up, the device features a controlled soft start-up. After the device is enabled, the device starts all internal reference and control circuits within the enable delay time, T_{delay}. After that, the maximum switch current limit rises monotonically from 0 mA to the current limit. The loop stops switching once V_O is reached. This allows a quick output voltage raise for small capacitors at the output. The bigger the output capacitor, the longer it takes to settle V_o. A potential load during start is lengthening the ramp as well. The raise of the current limit allows the smallest inrush current for no-load conditions, as well as the possibility to start into high loads at start-up.

Feature Description (接下页)

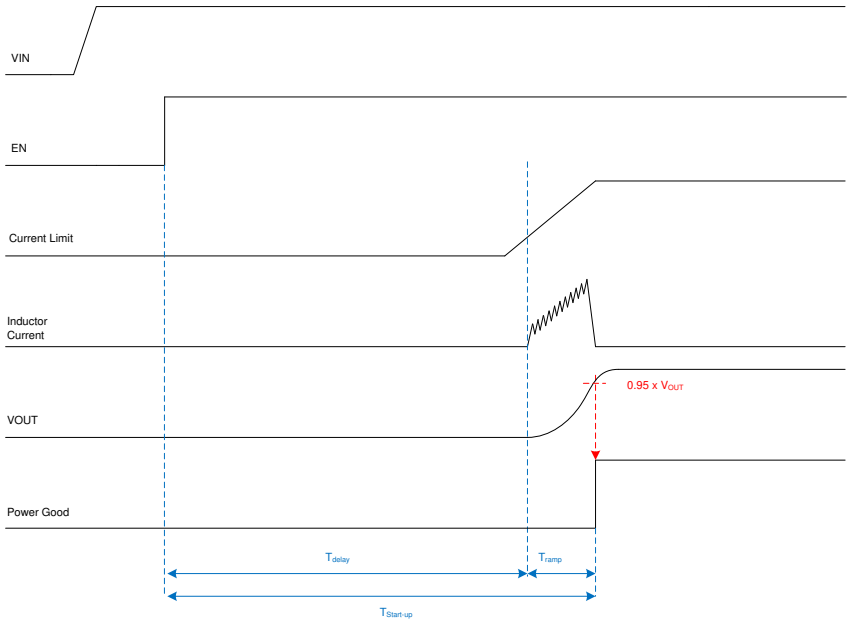


图 7. Device Start-up Scheme

9.3.6 Adjustable Output Voltage

The output voltage of the device is adjusted by applying an external resistive divider between V_O, the FB-pin, and GND. This allows you to program the output voltage in the recommended range. The divider must provide a low-side resistor of less than 100 kΩ. The high-side resistor is chosen accordingly.

9.3.7 Overtemperature Protection - Thermal Shutdown

The device has a built-in temperature sensor which monitors the junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at junction temperatures at the overtemperature threshold.

9.3.8 Input Overvoltage - Reverse-Boost Protection (IVP)

The TPS63805 and TPS63806 can operate in reverse mode where the device transfers energy from the output back to the input. If the source is not able to sink the revers current, the negative current builds up a charge to the input capacitance and V_{IN} rises. To protect the device and other components from that scenario, the device features an input voltage protection (IVP) for reverse boost operation. Once the input voltage is above the threshold, the converter forces PFM mode and the negative current operation is interrupted.

The PG signal goes low to indicate that behavior.

9.3.9 Output Overvoltage Protection (OVP)

In case of a broken feedback-path connection, the device can loose V_O information and is not able to regulate. To avoid an uncontrolled boosting of V_O, the TPS63805 and TPS63806 feature output overvoltage protection. It measures the voltage on the VOUT pin and stops switching when V_O is greater than the threshold to avoid harm to the converter and other components.

Feature Description (接下页)

9.3.10 Power-Good Indicator

The power good goes high-impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. This feature also indicates overvoltage and device shutdown cases as shown in 表 1. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used to sequence multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 1. Power-Good Indicator Truth Table

LOGIC SIGNALS					PG LOGIC STATUS
EN	V_O	V_I	OVP	IVP	
X	< 1.8 V	< UVLO_R	X	X	Undefined
LOW	X	> UVLO_F	X	X	LOW
HIGH	V_O < 0.9 × target-V_O	> 1.3V	X	X	LOW
HIGH	X	> UVLO_F	HIGH	X	LOW
HIGH	X	> UVLO_F	X	HIGH	LOW
HIGH	V_O > 0.95 × target-V_O	> UVLO_F	LOW	LOW	HIGH Z

9.4 Device Functional Modes

9.4.1 Peak-Current Mode Architecture

The TPS63805 and TPS63806 are based on a peak-current mode architecture. The error amplifier provides a peak-current target (voltage that is translated into an equivalent current, see 图 4), based on the current demand from the voltage loop. This target is compared to the actual inductor current during the ON-time. The ON-time is ended once the inductor current is equal to the current target and OFF-time is initiated. The OFF-time is calculated by the control and a function of V_I and V_O.

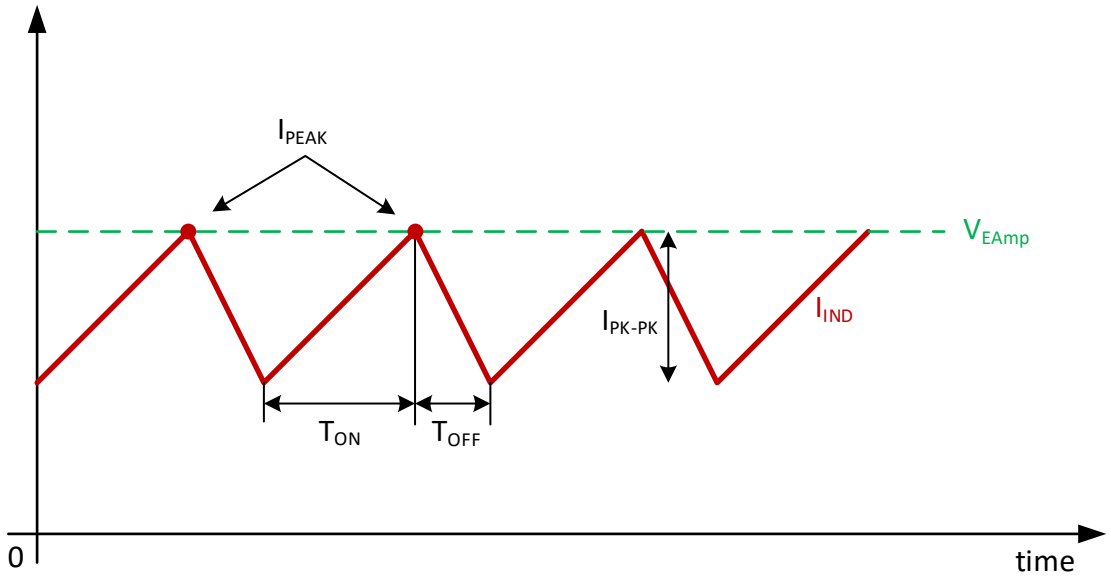


图 8. Peak-Current Architecture Operation

9.4.1.1 Reverse Current Operation, Negative Current

When the TPS63805 and TPS63806 are forced to PWM operation (MODE = HIGH), the device current can flow in reverse direction. This happens by the negative current capability of the TPS63805 and TPS63806. The error amplifier provides a peak-current target (voltage that is translated into an equivalent current, see 图 4), even if the target has a negative value. The maximum average current is even more negative than the peak current.

Device Functional Modes (接下页)

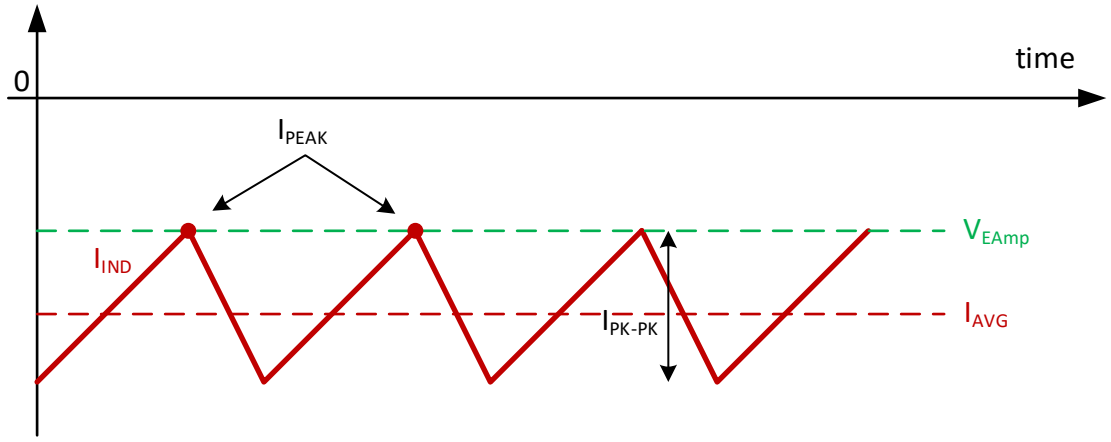


图 9. Peak-Current Operation, Reverse Current

9.4.1.2 Boost Operation

When V_I is smaller than V_O (and the voltages are not close enough to trigger buck-boost operation), the TPS63805 and TPS63806 operate in boost mode where the boost high-side and low-side switches are active. The buck high-side switch is always turned on and the buck low-side switch is always turned off. This lets the TPS63805 and TPS63806 operate as a classical boost converter.

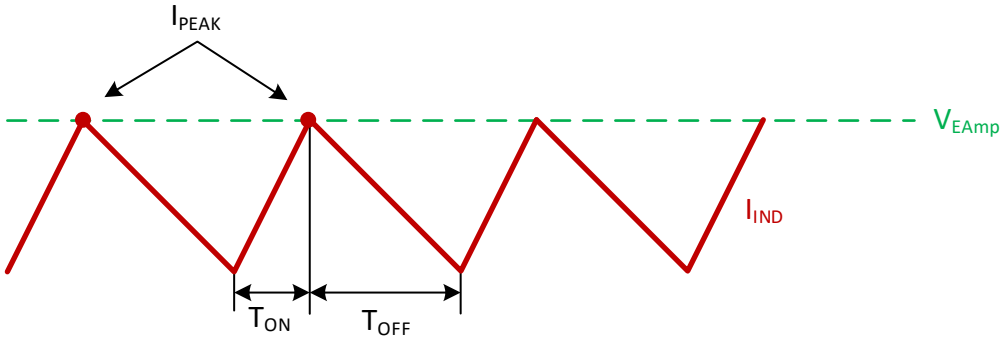


图 10. Peak-Current Boost Operation

9.4.1.3 Buck-Boost Operation

When V_I is close to V_O, the TPS63805 and TPS63806 operate in buck-boost mode where all switches are active and the device repeats 3-cycles:

- T_{ON}: Boost-charge phase where boost low-side and buck high-side are closed and the inductor current is built up
- T_{OFF}: Buck discharge phase where boost high-side and buck low-side are closed and the inductor is discharged
- T_{COM}: V_I connected to V_O where all high-side switches are closed and the input is connected to the output

Device Functional Modes (接下页)

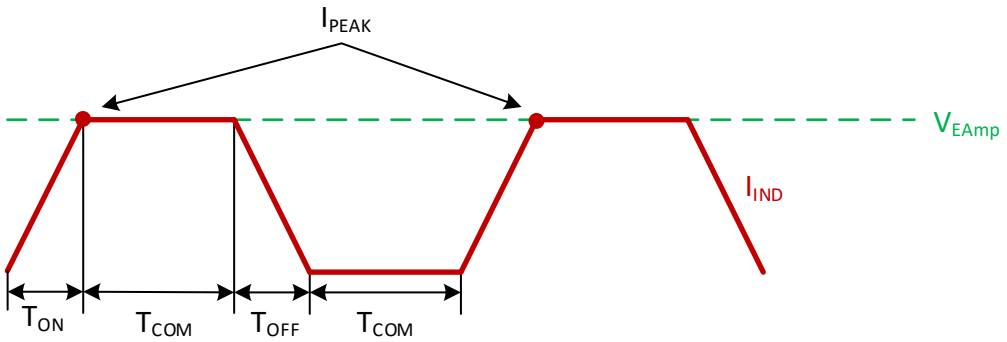


图 11. Peak-Current Buck-Boost Operation

9.4.1.4 Buck Operation

When V_I is greater than V_O (and the voltages are not close enough to trigger buck-boost operation), the TPS63805 and TPS63806 operate in buck mode where the buck high-side and low-side switches are active. The boost high-side switch is always turned on and the boost low-side switch is always turned off. This lets the TPS63805 and TPS63806 operate as a classical buck converter.

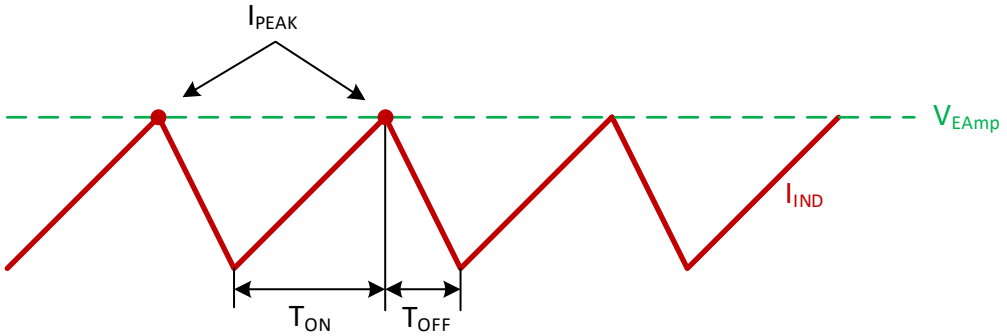


图 12. Peak-Current Buck Operation

9.4.2 Power Save Mode Operation

Besides continuos conduction mode (PWM), the TPS63805 and TPS63806 feature power safe mode (PFM) operation to achieve high efficiency at light load currents. This is implemented by pausing the switching operation, depending on the load current.

The skip comparator manages the switching or pause operation. It compares the current demand signal from the voltage loop, I_{REF}, with the skip threshold, I_{SKIP}, as shown in 图 4. If the current demand is lower than the skip value, the comparator pauses switching operation. If the current demand goes higher (due to falling V_O), the comparator activates the current loop and allows switching according to the loop behavior. Whenever the current loop has risen V_O by bringing charge to the output, the voltage loop output, I_{REF} (respectively V_{EA}), decreases. When I_{REF} falls below I_{SKIP}-hysteresis, it automatically pauses again.

Device Functional Modes (接下页)

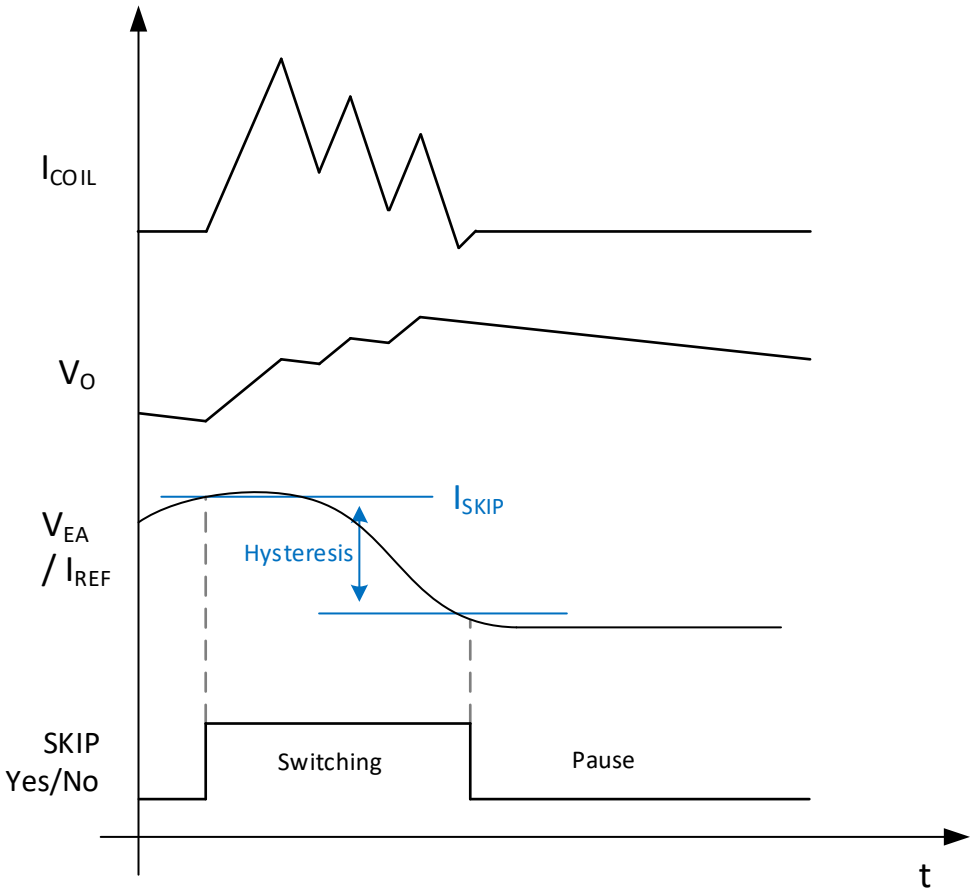


图 13. Power Safe Mode Operation Curves

9.4.2.1 Current Limit Operation

To limit current and protect the device and application, the maximum peak inductor current is limited internally on the IC. It is measured at the buck high-side switch which turns into an input current detection. To provide a certain load current across all operation modes, the boost and buck-boost peak current limit is higher than in buck mode. It limits the input current and allows no further increase of the delivered current. When using the device in this mode, it behaves similar to a current source.

The current limit depends on the operation mode (buck, buck-boost, or boost mode).

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS63805 and TPS63806 are high efficiency, low quiescent current, non-inverting buck-boost converters, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage.

10.2 Typical Application

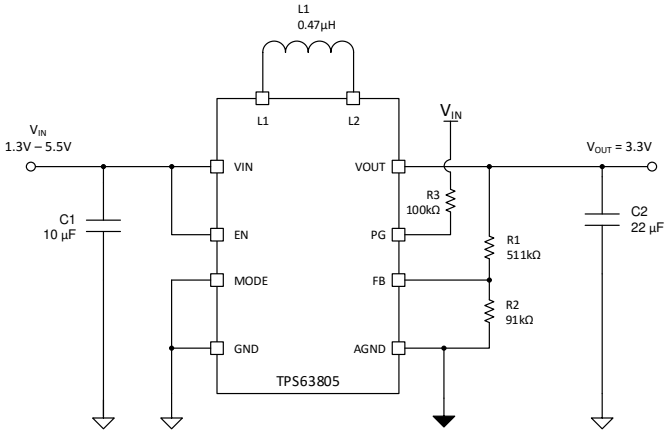


Figure 14. TPS63805 3.3 V_{OUT} Typical Application

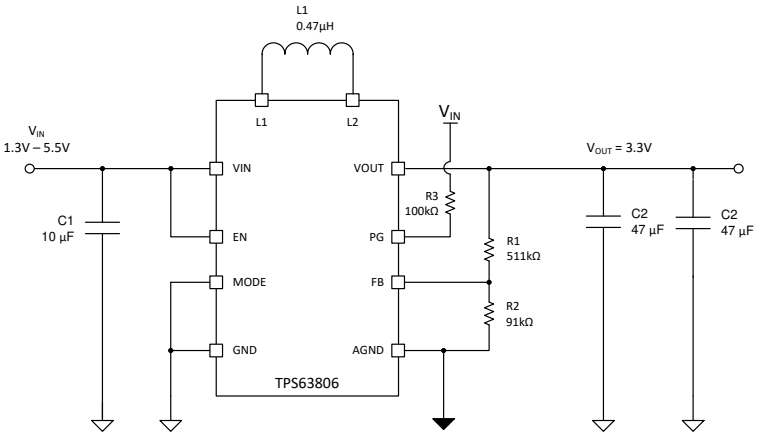


Figure 15. TPS63806 3.3 V_{OUT} Typical Application

10.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the *Table 2*.

Table 2 shows the list of components for the application characteristic curves.

Typical Application (continued)

Table 2. Matrix of Output Capacitor and Inductor Combinations for the TPS63805

NOMINAL INDUCTOR VALUE [µH](1)	NOMINAL OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	66	100
0.47	-	+ (3)	+	+	+

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) TPS63805 typical application. Other check marks indicate possible filter combinations.

Table 3. Matrix of Output Capacitor and Inductor Combinations for TPS63806

NOMINAL INDUCTOR VALUE [µH](1)	NOMINAL OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	66	100
0.47	-	-	+(3)	+	+

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) TPS63806 typical application. Other check marks indicate possible filter combinations.

10.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, the *Absolute Maximum Ratings* outlines minimum and maximum values for inductance and capacitance. Take tolerance and derating into account when selecting nominal inductance and capacitance.

10.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS63805 device with the WEBENCH® Power Designer. Click here to create a custom design using the TPS63806 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.2.2 Inductor Selection

The inductor selection is affected by several parameters such as the following:

- Inductor ripple current
- Output voltage ripple
- Transition point into power save mode
- Efficiency

See Table 4 for typical inductors.

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced, mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady-state operation is calculated using Equation 2. Only the equation which defines the switch current in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{2}$$

where

- D = Duty Cycle in Boost mode
- f = Converter switching frequency
- L = Inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption)

NOTE

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated using Equation 2. Table 4 lists the possible inductors.

Table 4. List of Recommended Inductors (1)

INDUCTOR VALUE [µH]	SATURATION CURRENT [A]	DCR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (LxWxH mm)
0.47	5.4	7.6	XFL4015-471ME	Coilcraft	4 x 4 x 2
0.47	5.5	26	DFE201612E	Toko	2.0 x 1.6 x 1.2

(1) See *Third-party Products Disclaimer*.

10.2.2.3 Output Capacitor Selection

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. The recommended nominal output capacitor value is a single 22 µF for the TPS63805 and 2x47 µF for the TPS63806 for all programmed output voltages ≤ 3.6 V. Above that voltage, 2x22 µF for the TPS63805 and 3x47 µF for the TPS63806 capacitors are recommended.

It is important that the effective capacitance is given according to the recommended value in *Recommended Operating Conditions*. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior since higher capacitance reduces transient response overshoot and undershoot and increases transient response time. Table 5 lists possible output capacitors.

There is no upper limit for the output capacitance value.

Table 5. List of Recommended Capacitors (1)

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
22	6.3	10	GRM188R60J226MEA0	Murata	0603 (1608)
22	6.3	10	GRM187R61A226ME15	Murata	0603 (1608)
22	10	40	GRM188R61A226ME15	Murata	0603 (1608)

(1) See *Third-party Products Disclaimer*.

Table 5. List of Recommended Capacitors() (continued)

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
22	10	10	GRM187R60J226ME15	Murata	0603 (1608)
47	6.3	43	GRM188R60J476ME15	Murata	0603 (1608)
47	6.3	43	GRM219R60J476ME44	Murata	0805 (2012)

10.2.2.4 Input Capacitor Selection

A 10 µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS63805 and TPS63806 converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

Table 6. List of Recommended Capacitors(1)

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
10	6.3	10	GRM188R60J106ME84	Murata	0603 (1608)
10	10	40	GRM188R61A106ME69	Murata	0603 (1608)
22	6.3	10	GRM188R60J226MEA0	Murata	0603 (1608)

(1) See *Third-party Products Disclaimer*.

10.2.2.5 Setting The Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is 500 mV nominal. The low-side resistor R2 (between FB and GND) must not exceed 100 kΩ. The high-side resistor (between FB and VOUT) R1 is calculated by Equation 3.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (3)$$

where

- V_{FB} = 500 mV

Table 7. Resistor Selection for Typ. Voltages

V_O [V]	R1 [kΩ]	R2 [kΩ]
2.5	365	91
3.3	511	91
3.6	562	91
5	806	91

10.2.3 Application Curves

Table 8. Components for Application Characteristic Curves (1)

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER	COMMENT
L1	0.47µH, 4 mm x 4 mm x 1.5 mm, 5.4 A, 7.6 mΩ	XFL4015-471ME	Coilcraft	
C1	10 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J106ME84	Murata	
C2	TPS63805 1x 22 µF, 0603, Ceramic Capacitor, ±20%, 10 V	GRM188R61A226ME15	Murata	TPS63805, $V_O \le 3.6$ V
C2	TPS63806 2x 47 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J476ME15	Murata	TPS63806, $V_O \le 3.6$ V

(1) See *Third-party Products Disclaimer*.

Table 8. Components for Application Characteristic Curves (1) (continued)

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER	COMMENT
C2	TPS63805 2x 22 µF, 0603, Ceramic Capacitor, ±20%, 10 V	GRM188R61A226ME15	Murata	TPS63805, V_O > 3.6 V
C2	TPS63806 3x 47 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J476ME15	Murata	TPS63806, V_O > 3.6 V
R1	511 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	V_O = 3.3 V
R1	562 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	V_O = 3.6 V
R1	806 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	V_O = 5 V
R2	91 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	
R3	100 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	

Table 9. Typical Characteristics Curves

PARAMETER	CONDITIONS	FIGURE
Output Current Capability		
Typical Output Current Capability versus Input Voltage	V_O = 3.3 V, TPS63805	Figure 16
Typical Output Current Capability versus Input Voltage	V_O = 3.3 V, TPS63806	Figure 17
Switching Frequency (TPS63805, TPS63806)		
Typical Inductor Switching Frequency versus Input Voltage	I_O = 0 A, MODE = High	Figure 18
Typical Inductor Burst Frequency versus Output Current	V_O = 3.3 V	Figure 19
Efficiency (TPS63805)		
Efficiency versus Output Current (PFM/PWM)	V_I = 2.5 V to 4.2 V, V_O = 3.3 V, MODE = Low	Figure 20
Efficiency versus Output Current (PWM only)	V_I = 2.5 V to 4.2 V, V_O = 3.3 V, MODE = High	Figure 21
Efficiency versus Output Current (PFM/PWM)	V_I = 1.8 V to 5 V, V_O = 3.3 V, MODE = Low	Figure 22
Efficiency versus Output Current (PWM only)	V_I = 1.8 V to 5 V, V_O = 3.3 V, MODE = High	Figure 23
Efficiency versus. Input Voltage (PFM/PWM)	V_O = 3.3 V, MODE = Low	Figure 24
Efficiency versus Input Voltage (PWM only)	I_O = 1 A, MODE = High	Figure 25
Efficiency (TPS63806)		
Efficiency versus Output Current (PFM/PWM)	V_I = 2.5 V to 4.2, V_O = 3.3 V, MODE = Low	Figure 26
Efficiency versus Output Current (PWM only)	V_I = 2.5 V to 4.2 , V_O = 3.3 V, MODE = High	Figure 27
Efficiency versus Output Current (PFM/PWM)	V_I = 1.8 V to 5, V_O = 3.3 V, MODE = Low	Figure 28
Efficiency versus Output Current (PWM only)	V_I = 2.5 V to 5, V_O = 3.3 V, MODE = High	Figure 31
Efficiency versus Input Voltage (PFM/PWM)	V_O = 3.3 V, MODE = Low	Figure 30
Efficiency versus Input Voltage (PWM only)	I_O = 1 A, MODE = High	Figure 31
Regulation Accuracy (TPS63805)		
Load Regulation, PWM Operation	V_O = 3.3 V, MODE = High	Figure 32
Load Regulation, PFM/PWM Operation	V_O = 3.3 V, MODE = Low	Figure 33
Line Regulation, PWM Operation	I_O = 1 A, MODE = High	Figure 34
Line Regulation, PFM/PWM Operation	I_O = 1 A, MODE = Low	Figure 35
Regulation Accuracy (TPS63806)		
Load Regulation, PWM Operation	V_O = 3.3 V, MODE = High	Figure 36
Load Regulation, PFM/PWM Operation	V_O = 3.3 V, MODE = Low	Figure 37
Line Regulation, PWM Operation	I_O = 1 A, MODE = High	Figure 38
Line Regulation, PFM/PWM Operation	I_O = 1 A, MODE = Low	Figure 39
Switching Waveforms (TPS63805, TPS63806)		
Switching Waveforms, PFM Boost Operation	V_I = 2.3 V, V_O = 3.3 V, MODE = Low	Figure 40
Switching Waveforms, PFM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, MODE = Low	Figure 41
Switching Waveforms, PFM Buck Operation	V_I = 4.3 V, V_O = 3.3 V, MODE = Low	Figure 42
Switching Waveforms, PWM Boost Operation	V_I = 2.3 V, V_O = 3.3 V, MODE = High	Figure 43
Switching Waveforms, PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, MODE = High	Figure 44
Switching Waveforms, PWM Buck Operation	V_I = 4.3 V, V_O = 3.3 V, MODE = High	Figure 45
Transient Performance (TPS63805)		
Load Transient, PFM/PWM Boost Operation	V_I = 2.5 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = Low	Figure 46
Load Transient, PFM/PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = Low	Figure 47
Load Transient, PFM/PWM Buck Operation	V_I = 4.2 V, V_O = 3.3V, Load = 100 mA to 1A, MODE = Low	Figure 48
Load Transient, PWM Boost Operation	V_I = 2.5 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = High	Figure 49

Table 9. Typical Characteristics Curves (continued)

PARAMETER	CONDITIONS	FIGURE
Load Transient, PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = High	Figure 50
Load Transient, PWM Buck Operation	V_I = 4.2 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = High	Figure 51
Line Transient, PWM Operation	V_I = 2.3 V to 4.3 V, V_O = 3.3 V, Load = 0.5 A , MODE = Low	Figure 52
Line Transient, PWM Operation	V_I = 2.3 V to 4.3 V, V_O = 3.3 V, Load = 1 A , MODE = Low	Figure 53
Line Transient, PWM Operation	V_I = 3 V to 3.6 V, V_O = 3.3 V, Load = 0.5 A , MODE = Low	Figure 54
Transient Performance (TPS63806)		
Load Transient, PFM/PWM Boost Operation	V_I = 2.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = Low	Figure 55
Load Transient, PFM/PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = Low	Figure 56
Load Transient, PFM/PWM Buck Operation	V_I = 4.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = Low	Figure 57
Load Transient, PWM Boost Operation	V_I = 2.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = High	Figure 58
Load Transient, PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = High	Figure 59
Load Transient, PWM Buck Operation	V_I = 4.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = High	Figure 60
Line Transient, PWM Operation	V_I = 2.3 V to 4.3 V, V_O = 3.3 V, Load = 0.5 A , MODE = Low	Figure 61
Line Transient, PWM Operation	V_I = 2.3 V to 4.3 V, V_O = 3.3 V, Load = 1 A , MODE = Low	Figure 62
Line Transient, PWM Operation	V_I = 3 V to 3.6 V, V_O = 3.3 V, Load = 0.5 A , MODE = Low	Figure 63
Pulsed load, PWM Operation	V_I = 2.8 V, V_O = 3.3 V, Load = 50 mA to 5 A, with 1 MHz and 50% duty cycle, t_r = 120 ns, t_f = 60 ns, MODE = High	Figure 64
Pulsed load, PWM Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 50 mA to 5 A, with 1 MHz and 50% duty cycle, t_r = 120 ns, t_f = 60 ns, MODE = High	Figure 65
Pulsed load, PWM Operation	V_I = 4.2 V, V_O = 3.3 V, Load = 50 mA to 5 A, with 1 MHz and 50% duty cycle, t_r = 120 ns t_f = 60 ns, MODE = High	Figure 66
Start-up (TPS63805, TPS63806)		
Start-up Behavior from Rising Enable, PFM Operation	V_I = 2.2 V, V_O = 3.3 V, Load = 10 mA, MODE = Low	Figure 67
Start-up Behavior from Rising Enable, PWM Operation	V_I = 2.2 V, V_O = 3.3 V, Load = 10 mA, MODE = High	Figure 68

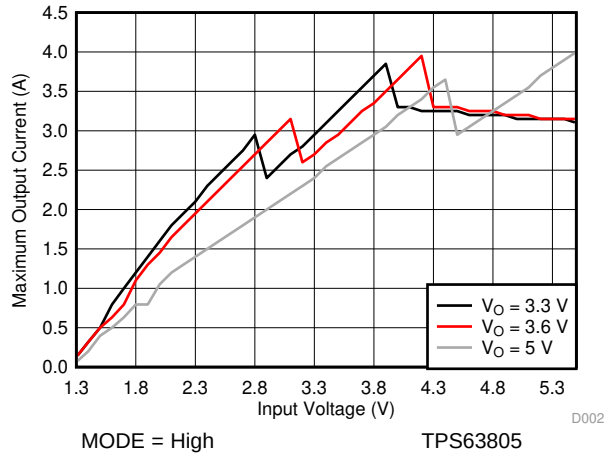


Figure 16. Typical Output Current Capability versus Input Voltage

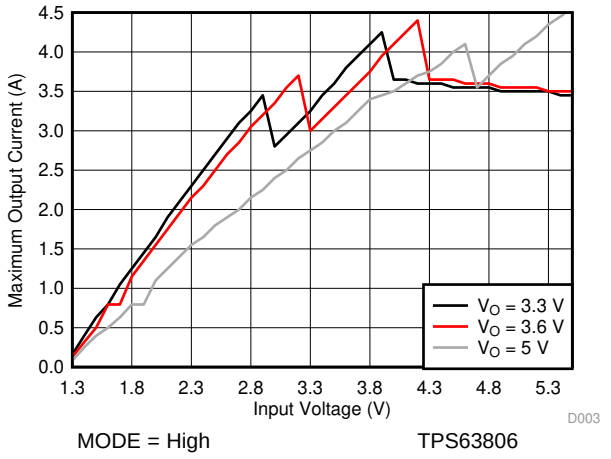


Figure 17. Typical Output Current Capability versus Input Voltage

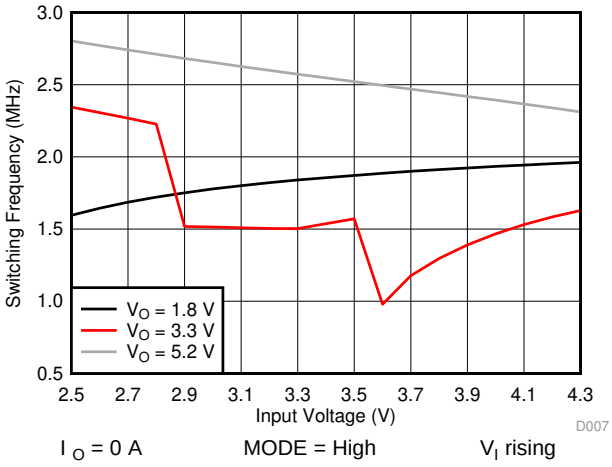


Figure 18. Typical Inductor Switching Frequency versus Input Voltage

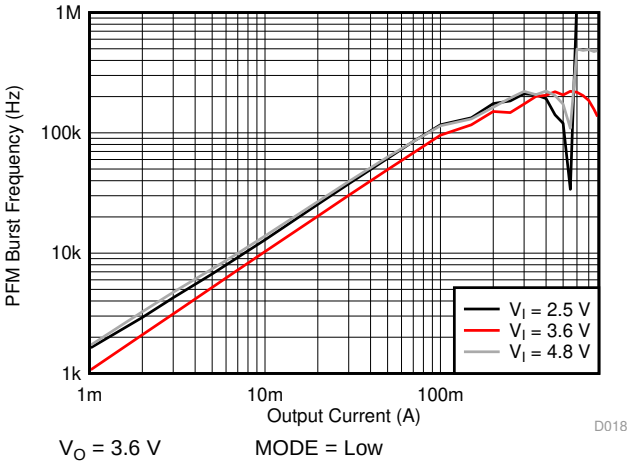


Figure 19. Typical Inductor Burst Frequency versus Output Current

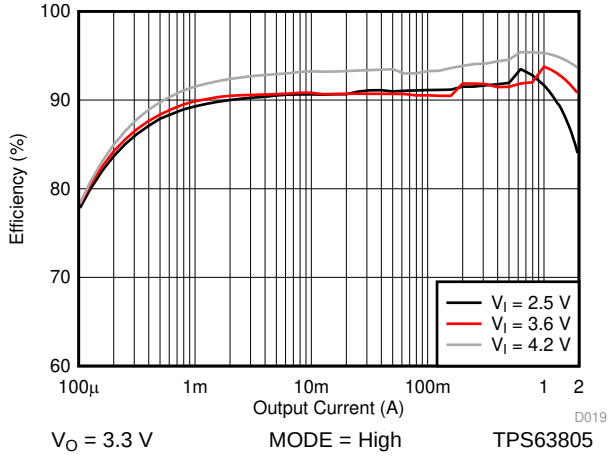


Figure 20. Efficiency versus Output Current (PFM/PWM)

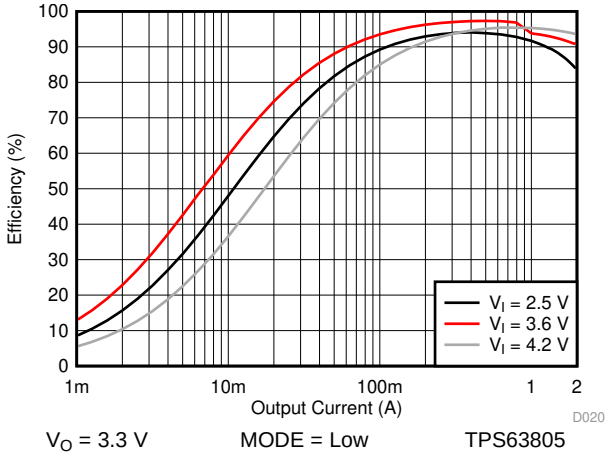
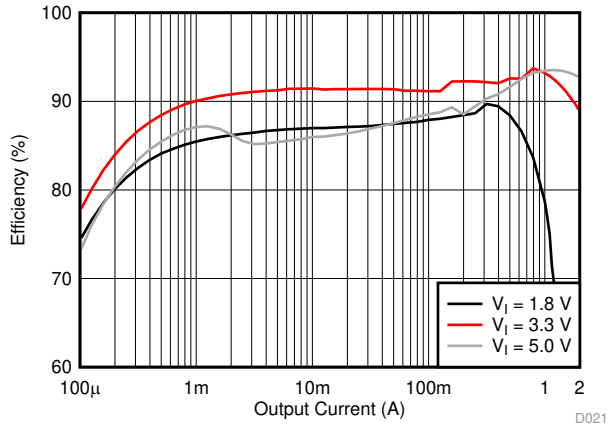
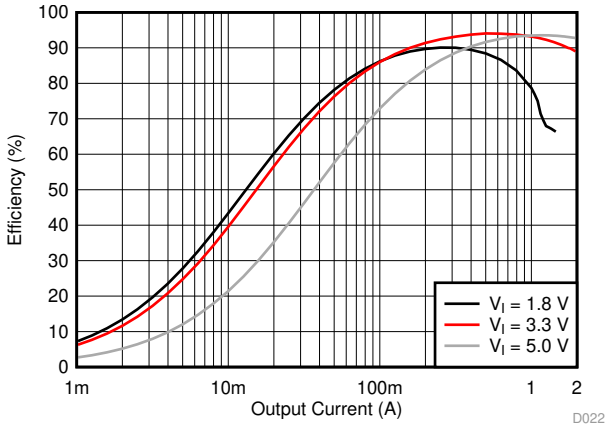


Figure 21. Efficiency versus Output Current (PWM Only)



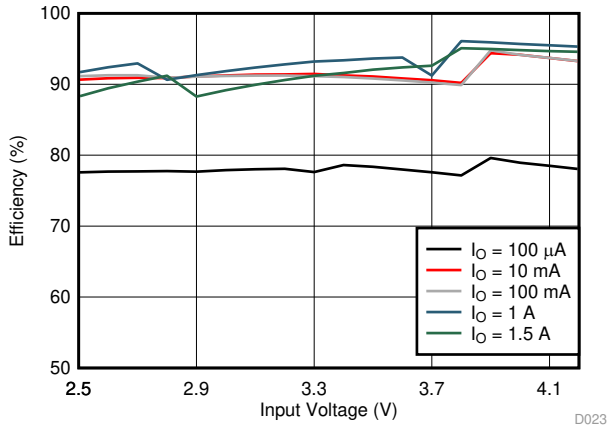
V_O = 3.3 V MODE = High TPS63805

Figure 22. Efficiency versus Output Current (PFM/PWM)



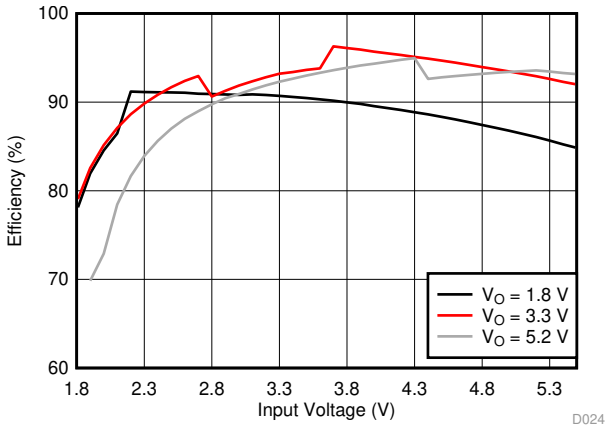
V_O = 3.3 V MODE = Low TPS63805

Figure 23. Efficiency versus Input Voltage (PWM Only)



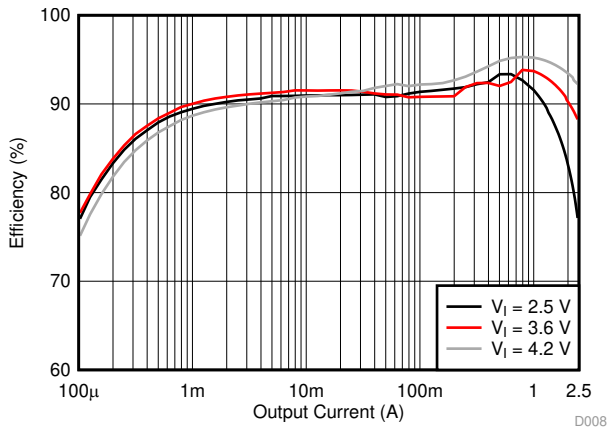
V_O = 3.3 V MODE = High TPS63805

Figure 24. Efficiency versus Input Voltage (PFM/PWM)



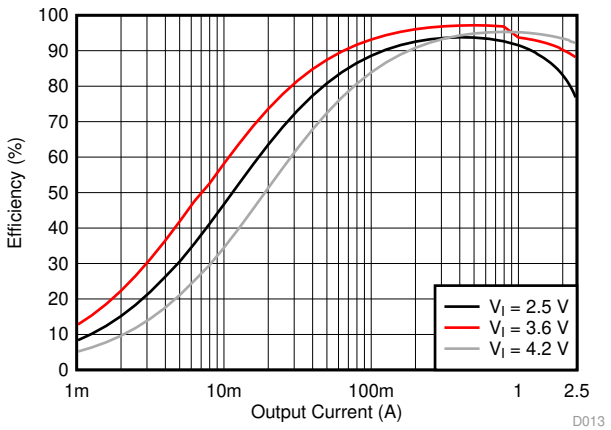
I_O = 1 A MODE = Low TPS63805

Figure 25. Efficiency versus Input Voltage (PWM Only)



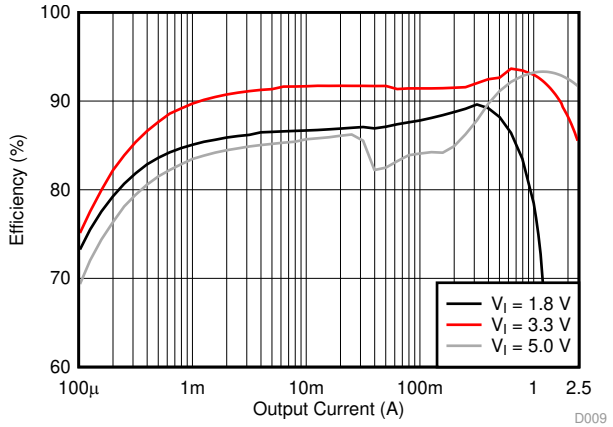
V_O = 3.3 V MODE = High TPS63806

Figure 26. Efficiency versus Output Current (PFM/PWM)



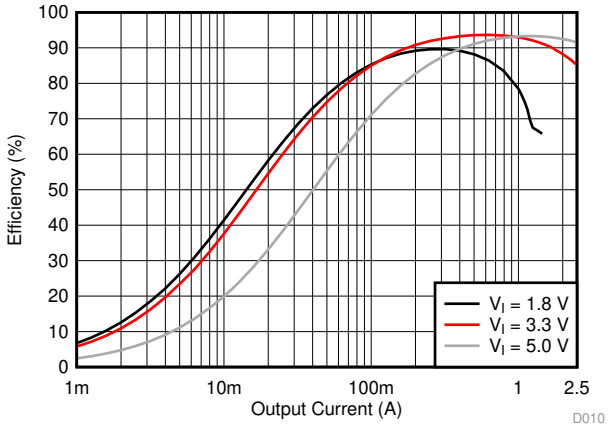
V_O = 3.3 V MODE = Low TPS63806

Figure 27. Efficiency versus Output Current (PWM Only)



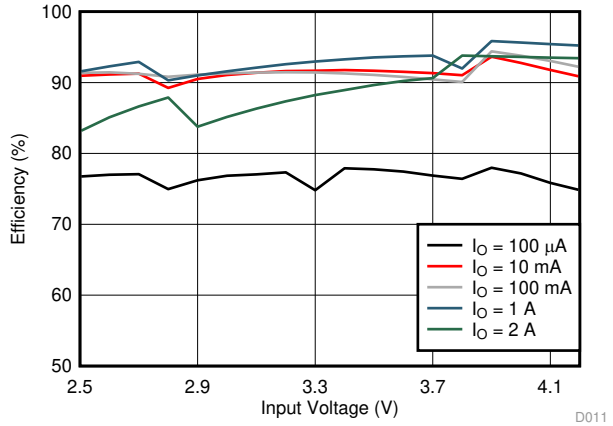
V_O = 3.3 V MODE = High TPS63806

Figure 28. Efficiency versus Output Current (PFM/PWM)



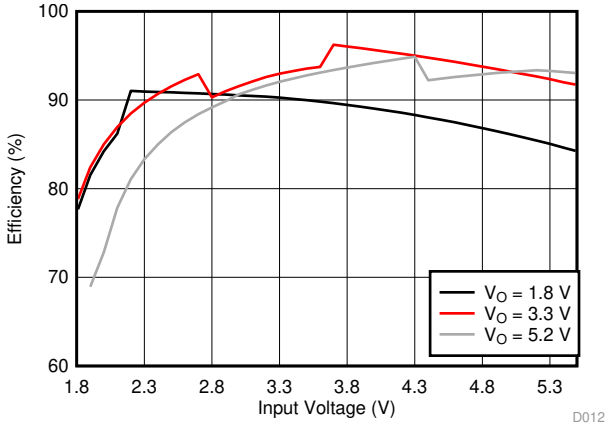
V_O = 3.3 V MODE = Low TPS63806

Figure 29. Efficiency versus Input Voltage (PWM Only)



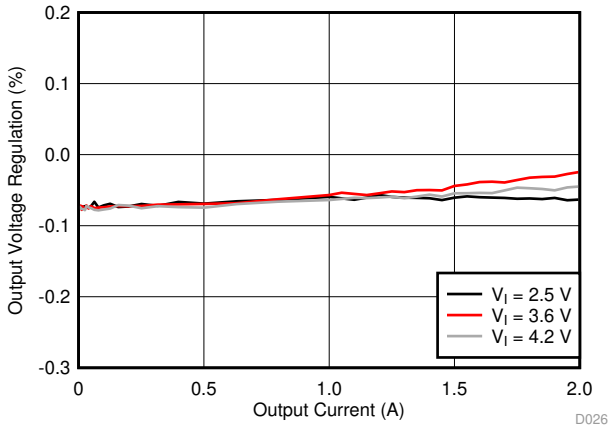
V_O = 3.3 V MODE = High TPS63806

Figure 30. Efficiency versus Input Voltage (PFM/PWM)



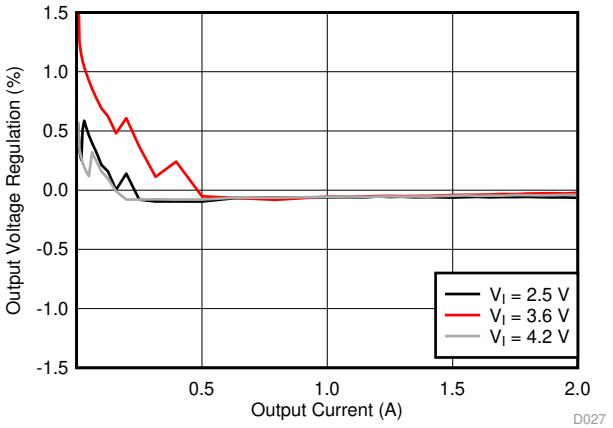
I_O = 1 A MODE = Low TPS63806

Figure 31. Efficiency versus Input Voltage (PWM Only)



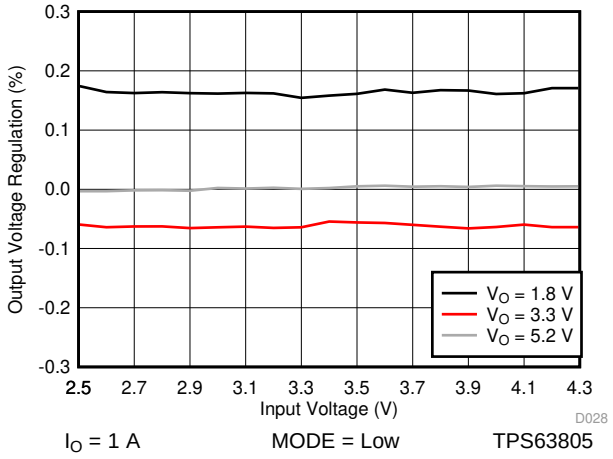
V_O = 3.3 V MODE = High TPS63805

Figure 32. Load Regulation (PWM Only)



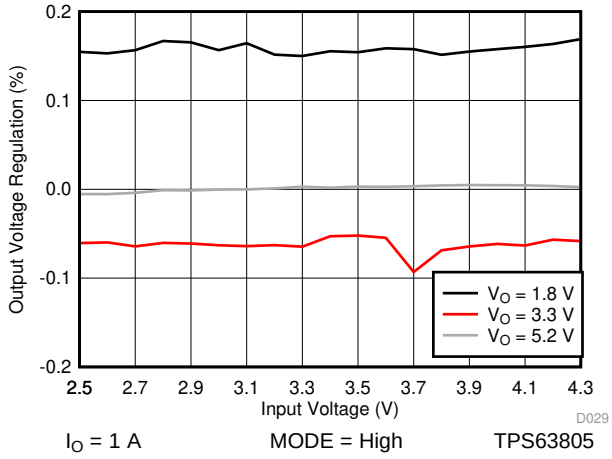
V_O = 3.3 V MODE = Low TPS63805

Figure 33. Load Regulation (PFM/PWM)



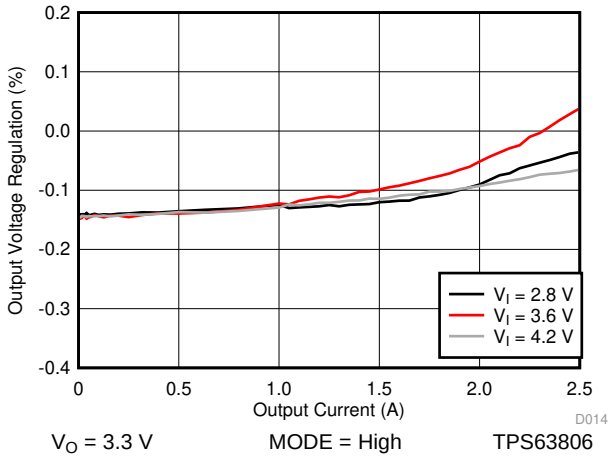
I_O = 1 A MODE = Low TPS63805

Figure 34. Line Regulation (PWM Only)



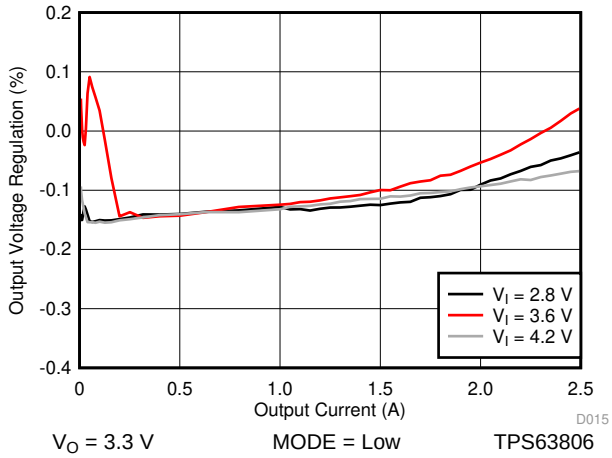
I_O = 1 A MODE = High TPS63805

Figure 35. Line Regulation (PFM/PWM)



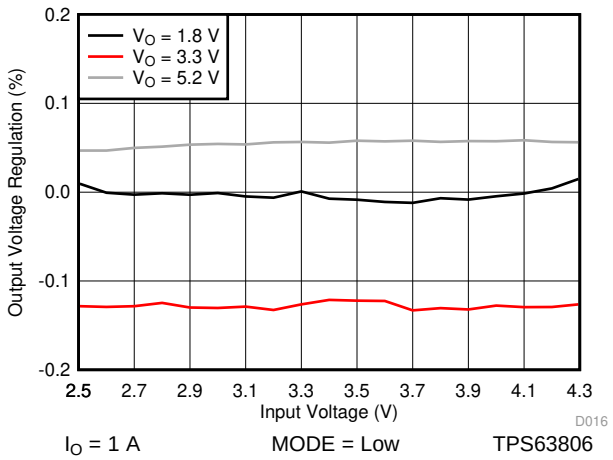
V_O = 3.3 V MODE = High TPS63806

Figure 36. Load Regulation (PWM Only)



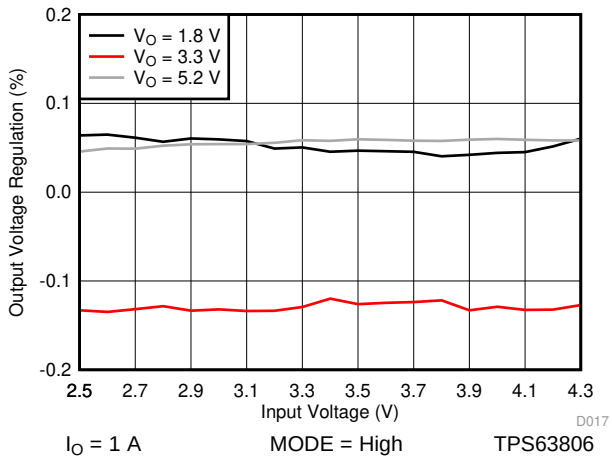
V_O = 3.3 V MODE = Low TPS63806

Figure 37. Load Regulation (PFM/PWM)



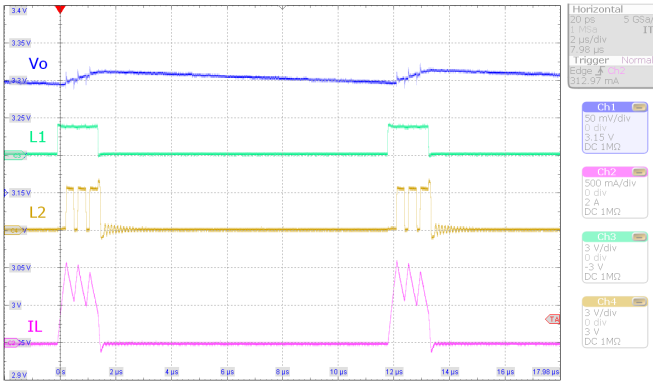
I_O = 1 A MODE = Low TPS63806

Figure 38. Line Regulation (PWM Only)



I_O = 1 A MODE = High TPS63806

Figure 39. Line Regulation (PFM/PWM)

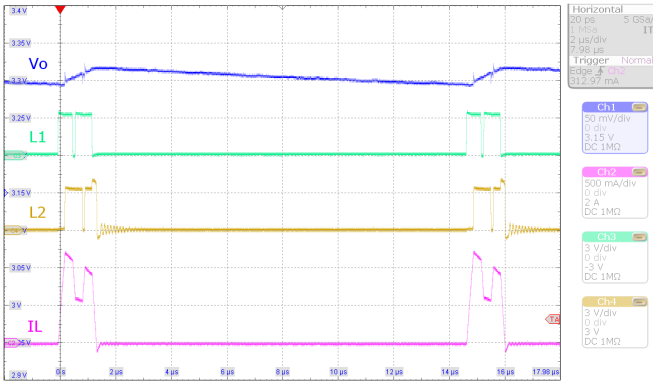


V_I = 2.3 V,
V_O = 3.3 V

MODE = Low

I_O = 40 mA

Figure 40. Switching Waveforms, PFM Boost Operation

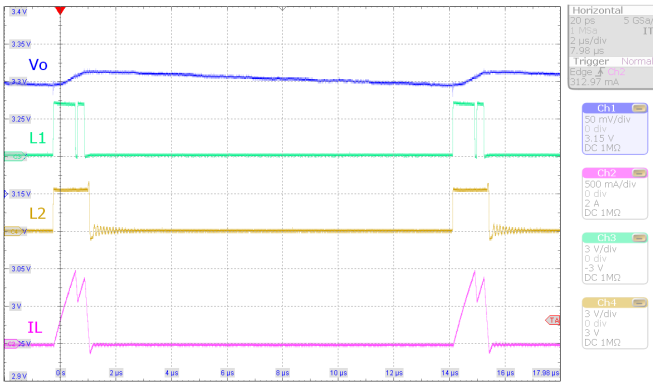


V_I = 3.3 V,
V_O = 3.3 V

MODE = Low

I_O = 40 mA

Figure 41. Switching Waveforms, PFM Buck-Boost Operation

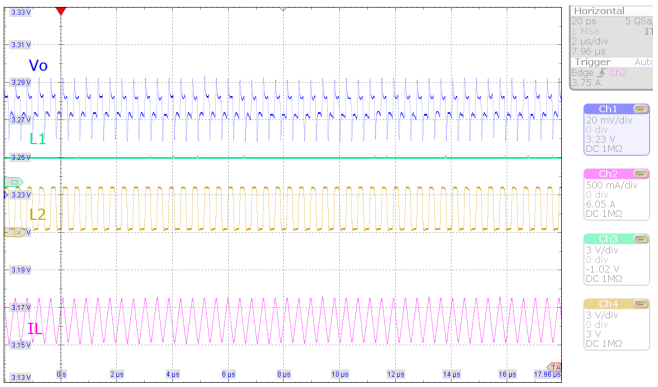


V_I = 4.2 V,
V_O = 3.3 V

MODE = Low

I_O = 40 mA

Figure 42. Switching Waveforms, PFM Buck Operation

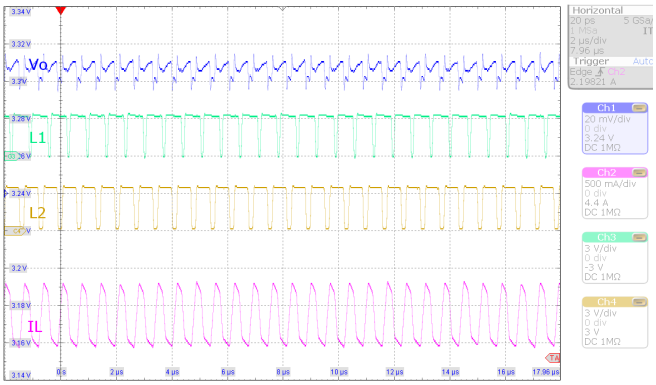


V_I = 2.3 V,
V_O = 3.3 V

MODE = Low

I_O = 2 A

Figure 43. Switching Waveforms, PWM Boost Operation

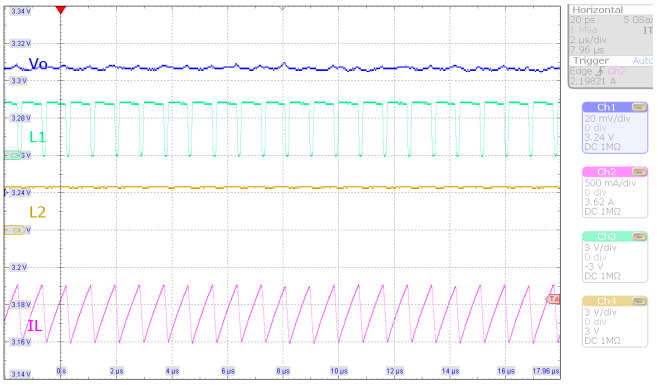


V_I = 3.3 V,
V_O = 3.3 V

MODE = Low

I_O = 2 A

Figure 44. Switching Waveforms, PWM Buck-Boost Operation

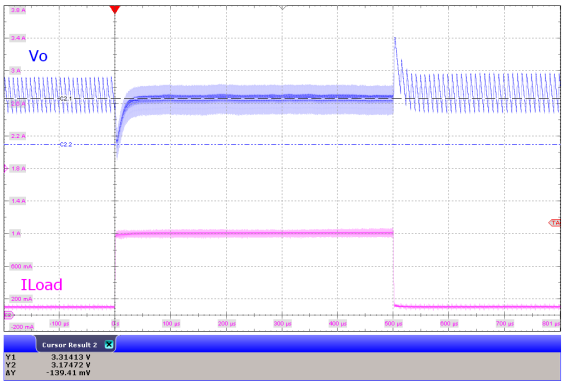


V_I = 4.2 V,
V_O = 3.3 V

MODE = Low

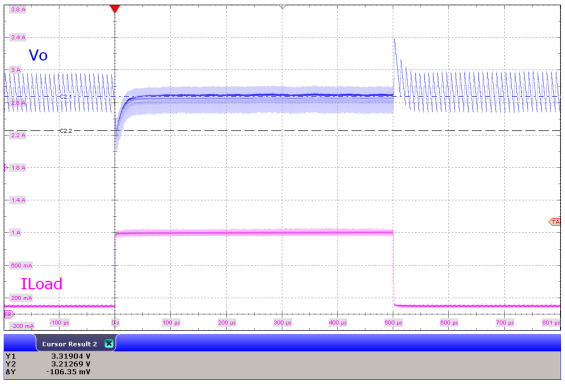
I_O = 2 A

Figure 45. Switching Waveforms, PWM Buck Operation



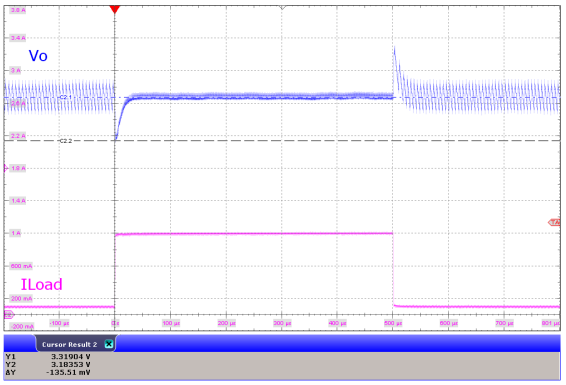
V_I = 2.5 V, V_O = 3.3 V | I_O from 100 mA to 1 A, t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = Low

Figure 46. Load Transient, PFM/PWM Boost Operation



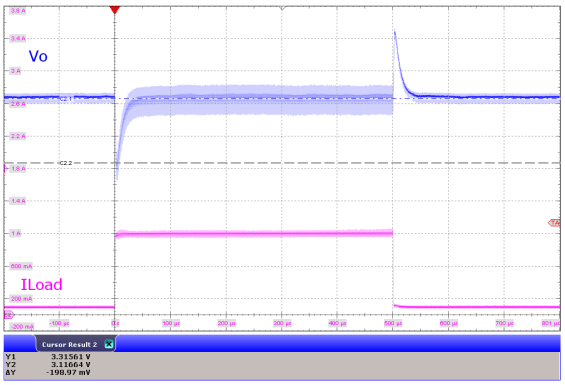
V_I = 3.3 V, V_O = 3.3 V | I_O from 100 mA to 1 A, t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = Low

Figure 47. Load Transient, PFM/PWM Buck-Boost Operation



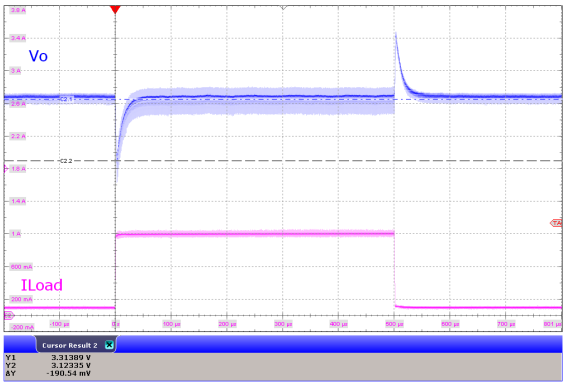
V_I = 5 V, V_O = 3.3 V | I_O from 100 mA to 1 A, t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = Low

Figure 48. Load Transient, PFM/PWM Buck Operation



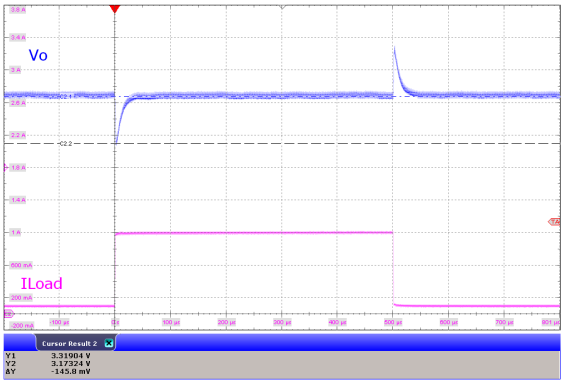
V_I = 2.5 V, V_O = 3.3 V | I_O from 100 mA to 1 A, t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

Figure 49. Load Transient, PWM Boost Operation



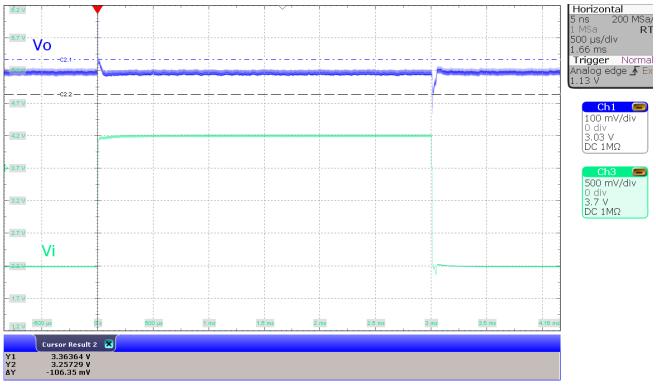
V_I = 3.3 V, V_O = 3.3 V | I_O from 100 mA to 1 A, t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

Figure 50. Load Transient, PWM Buck-Boost Operation



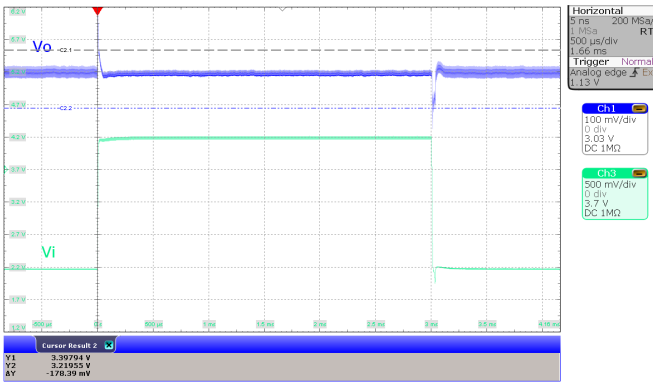
V_I = 5 V, V_O = 3.3 V | I_O from 100 mA to 1 A, t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

Figure 51. Load Transient, PWM Buck Operation



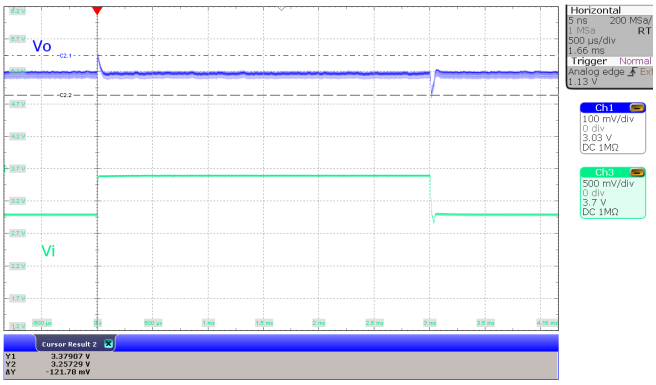
I_O = 0.5 A | V_I from 2.2 V to 4.2 V t_r =1 µs, t_f = 1 µs | TPS63805 MODE = High

Figure 52. Line Transient, PWM Operation



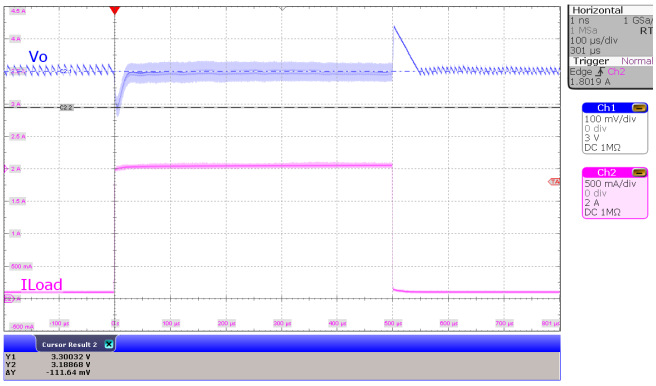
I_O = 1 A | V_I from 2.2 V to 4.2 V t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

Figure 53. Line Transient, PWM Operation



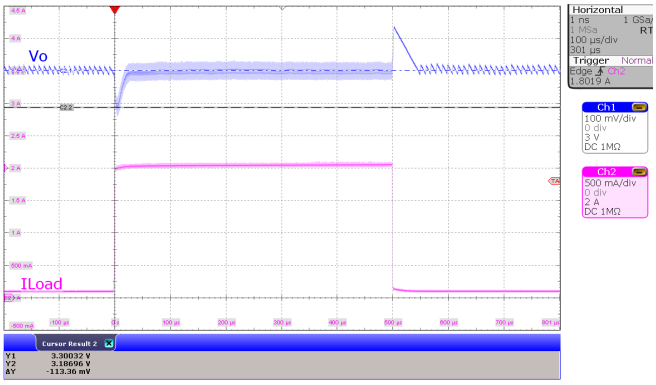
I_O = 0.5 A | V_I from 3 V to 3.6 V t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

Figure 54. Line Transient, PWM Operation



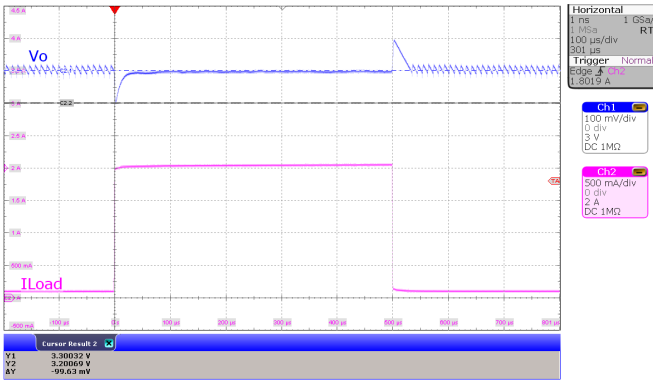
V_I = 2.8 V, V_O = 3.3 V | I_O from 100 mA to 2 A t_r = 1 µs, t_f = 1 µs | TPS63806 MODE = Low

Figure 55. Load Transient, PFM/PWM Boost Operation



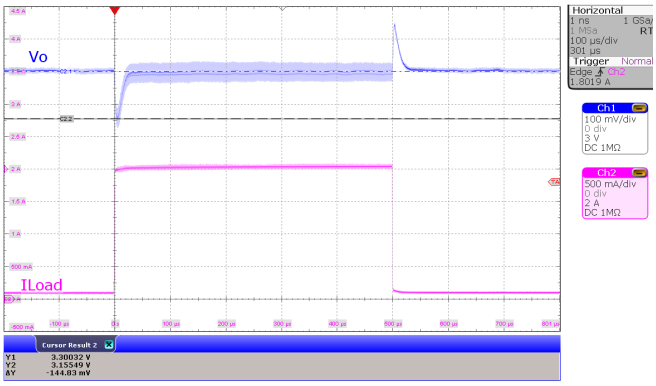
V_I = 3.3 V, V_O = 3.3 V | I_O from 100 mA to 2 A t_r = 1 µs, t_f = 1 µs | TPS63806 MODE = Low

Figure 56. Load Transient, PFM/PWM Buck-Boost Operation



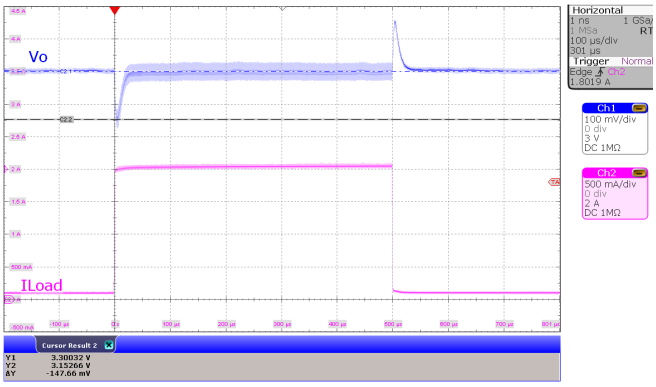
V_I = 4.2 V, V_O = 3.3 V | I_O from 100 mA to 2 A t_r = 1 µs, t_f = 1 µs | TPS63806 MODE = Low

Figure 57. Load Transient, PFM/PWM Buck Operation



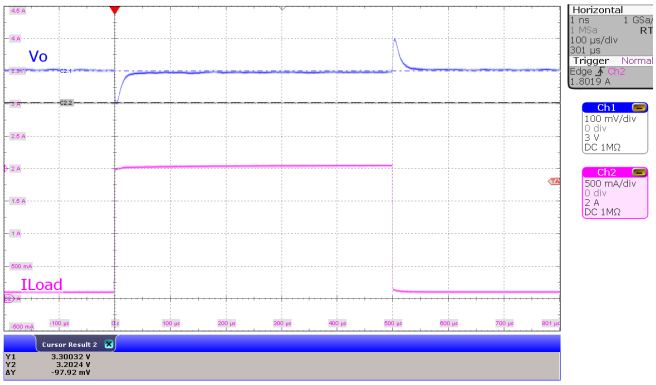
V_I = 2.8 V, V_O = 3.3 V	I_O from 100 mA to 2 A t_r = 1 µs, t_f = 1 µs	TPS63806 MODE = High

Figure 58. Load Transient, PWM Boost Operation



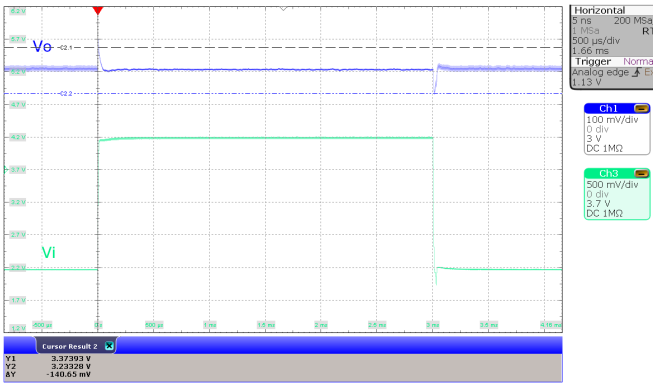
V_I = 3.3 V, V_O = 3.3 V	I_O 100 mA to 2 A t_r = t_f = 1 µs	TPS63806 MODE = High

Figure 59. Load Transient, PWM Buck-Boost Operation



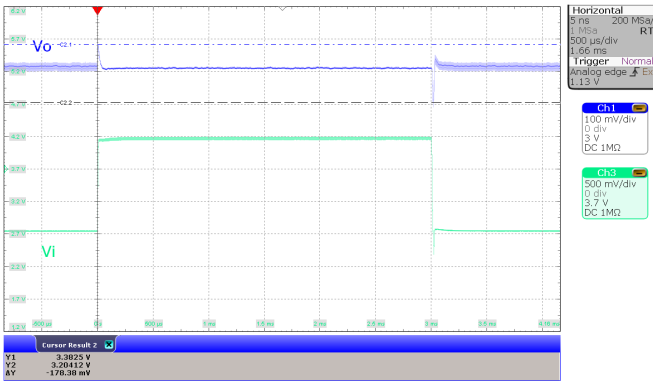
V_I = 4.2 V, V_O = 3.3 V	I_O 100 mA to 2 A t_r = t_f = 1 µs	TPS63806 MODE = High

Figure 60. Load Transient, PWM Buck Operation



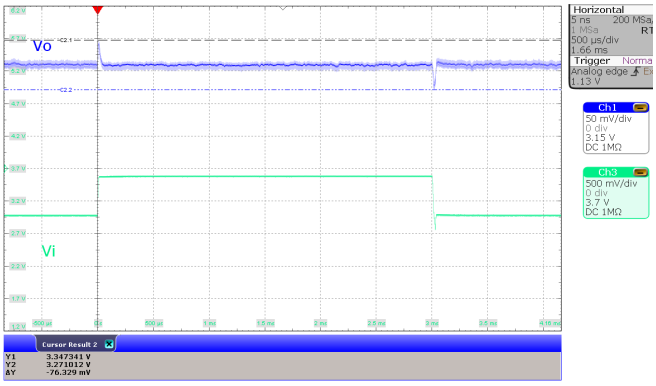
I_O = 1 A	V_I 2.2 V to 4.2 V t_r = t_f = 1 µs	TPS63806 MODE = High

Figure 61. Line Transient, PWM Operation



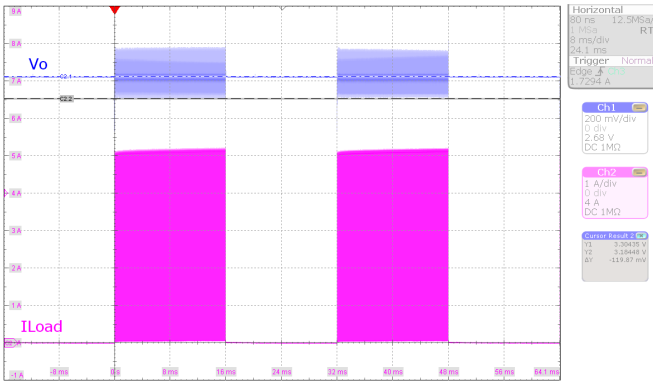
I_O = 2 A	V_I 2.2 V to 4.2 V t_r = t_f = 1 µs	TPS63806 MODE = High

Figure 62. Line Transient, PWM Operation



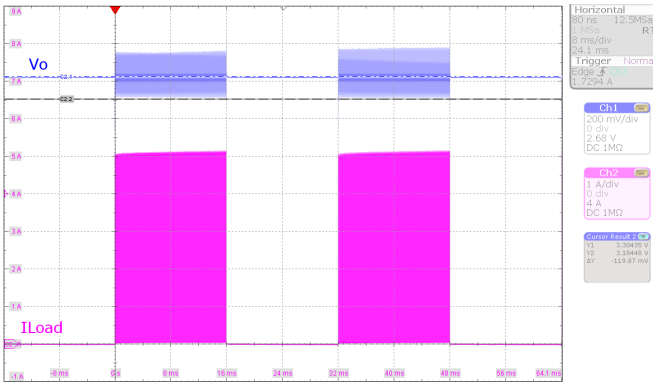
I_O = 1 A	V_I 3.0 V to 3.6 V t_r = t_f = 1 µs	TPS63806 MODE = High

Figure 63. Line Transient, PWM Operation



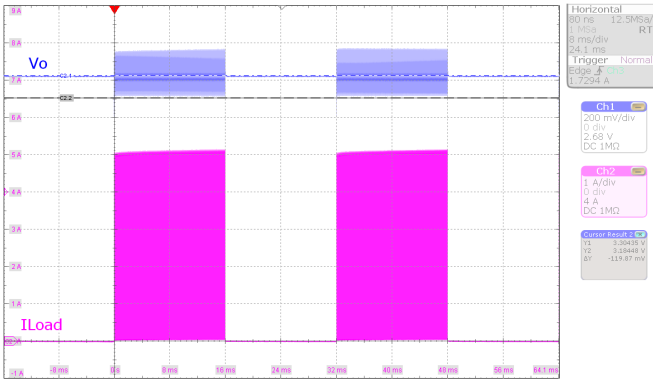
V_I = 2.8 V, V_O = 3.3 V | I_O 50 mA to 5 A with 1 MHz and 50% duty cycle t_r = 120 ns, t_f = 60 ns | TPS63806 MODE = High

Figure 64. Pulsed Load, PWM Operation



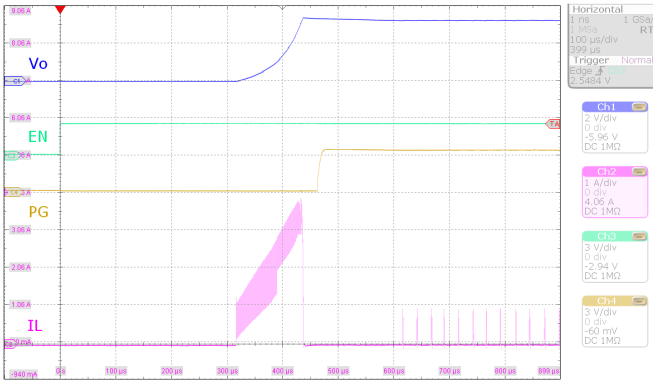
V_I = 3.3 V, V_O = 3.3 V | I_O 50 mA to 5 A with 1 MHz and 50% duty cycle t_r = 120 ns, t_f = 60 ns | TPS63806 MODE = High

Figure 65. Pulsed Load, PWM Operation



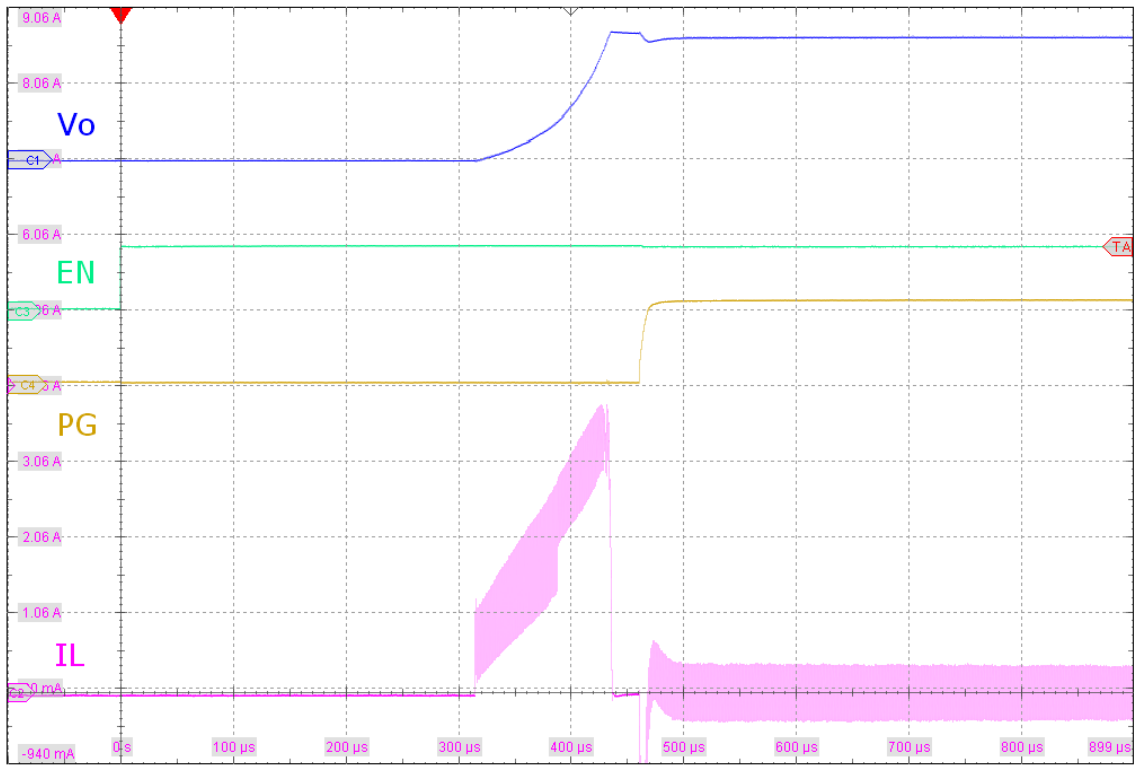
V_I = 4.2 V, V_O = 3.3 V | I_O 50 mA to 5 A with 1 MHz and 50% duty cycle t_r = 120 ns, t_f = 60 ns | TPS63806 MODE = High

Figure 66. Pulsed Load, PWM Operation



V_I = 4.2 V, V_O = 3.3 V | MODE = Low | 100 mΩ resistive load

Figure 67. Start-up Behavior from Rising Enable, PFM Operation



V_I = 4.2 V,
V_O = 3.3 V

MODE = High

100 mΩ resistive load

Figure 68. Start-up Behavior from Rising Enable, PWM Operation

11 Power Supply Recommendations

The TPS63805 and TPS63806 device families have no special requirements for its input power supply. The input power supply output current needs to be rated according to the supply voltage, output voltage, and output current of the TPS63805 and TPS63806.

12 Layout

12.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS63805 and TPS63806 device.

1. Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Route wide and direct traces to the input and output capacitor results in low trace resistance and low parasitic inductance.
2. Separate AGND and PGND. Do not connect AGND and PGND directly at the IC. See 图 69 as an example.
3. Use a common-power GND, but connect AGND and PGND through a via at a different layer.
4. Use separate traces for the supply voltage of the power stage and the supply voltage of the analog stage.
5. The sense trace connected to FB is signal trace. Keep these traces away from L1 and L2 nodes.

12.2 Layout Example

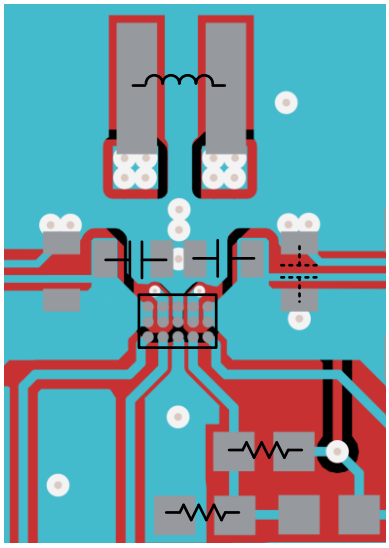


图 69. TPS63805 and TPS63806 Layout

13 器件和文档支持

13.1 器件支持

13.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

13.1.2 使用 WEBENCH® 工具创建定制设计方案

单击此处，使用 TPS63805 器件并借助 WEBENCH® 电源设计器创建定制设计方案。单击此处，使用 TPS63806 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

13.1.3 开发支持

QFN/SON 封装常见问题解答

13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **10.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TPS63805	单击此处	单击此处	单击此处	单击此处	单击此处
TPS63806	单击此处	单击此处	单击此处	单击此处	单击此处

13.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63805YFFR	ACTIVE	DSBGA	YFF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63805	Samples
TPS63805YFFT	ACTIVE	DSBGA	YFF	15	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63805	Samples
TPS63806YFFR	ACTIVE	DSBGA	YFF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63806	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

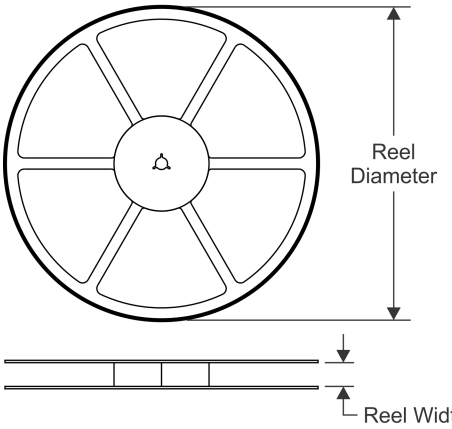
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

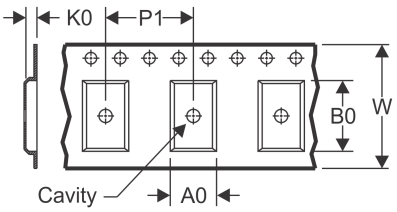
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

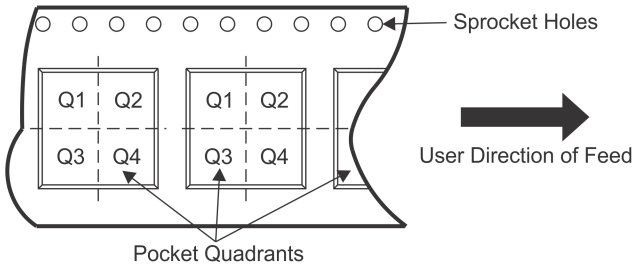


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

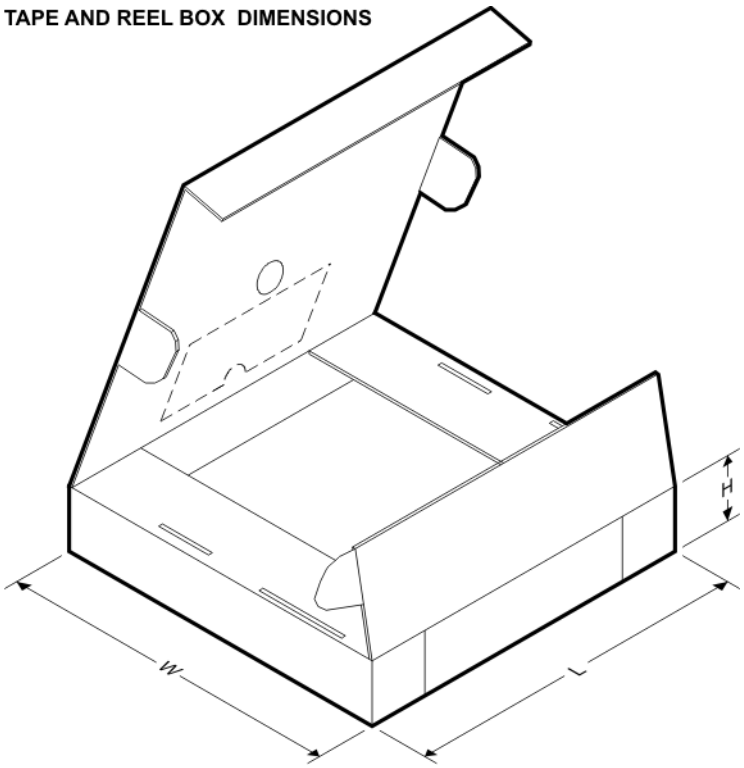
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63805YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1
TPS63805YFFT	DSBGA	YFF	15	250	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1
TPS63806YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

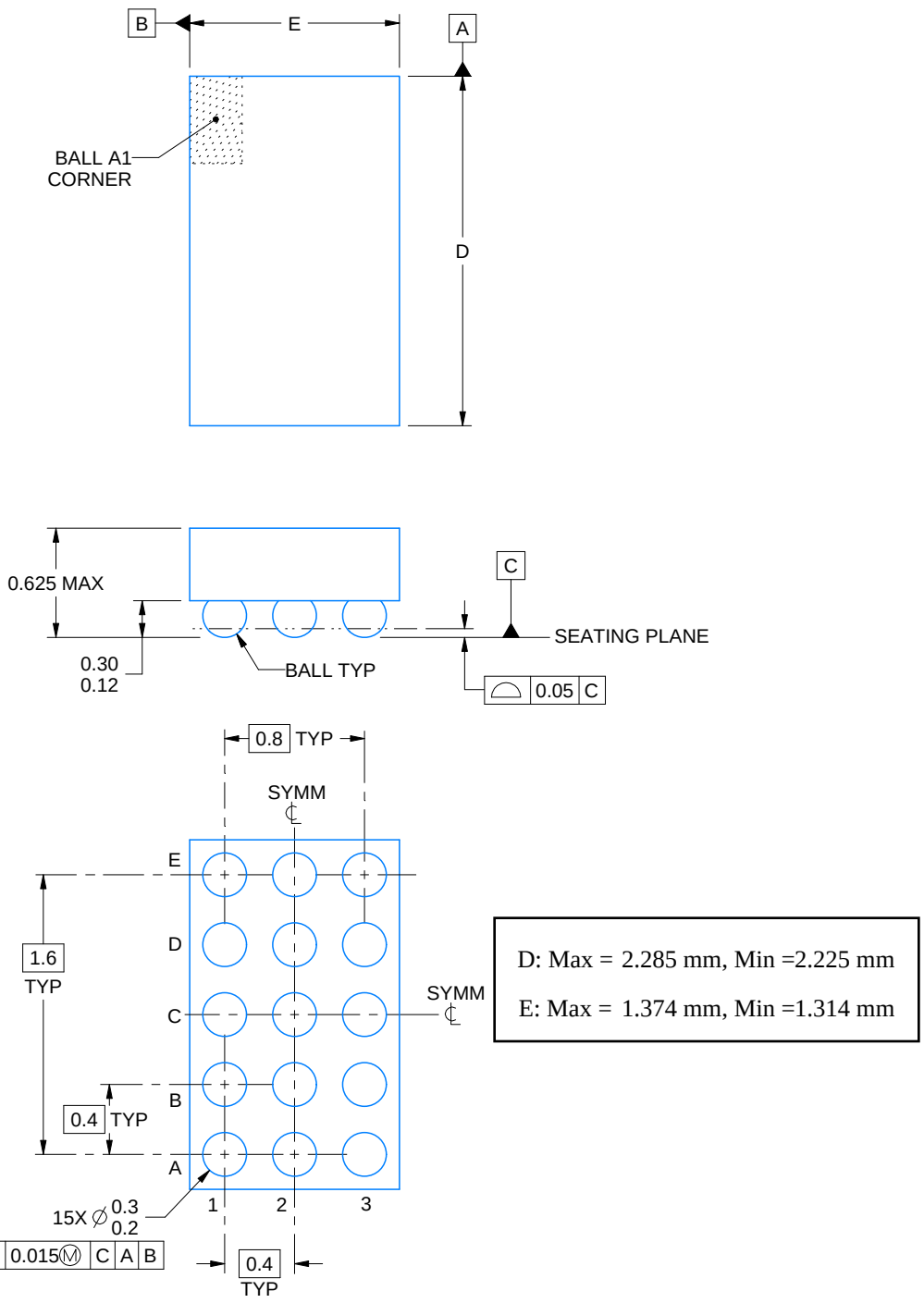
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63805YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS63805YFFT	DSBGA	YFF	15	250	182.0	182.0	20.0
TPS63806YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0015

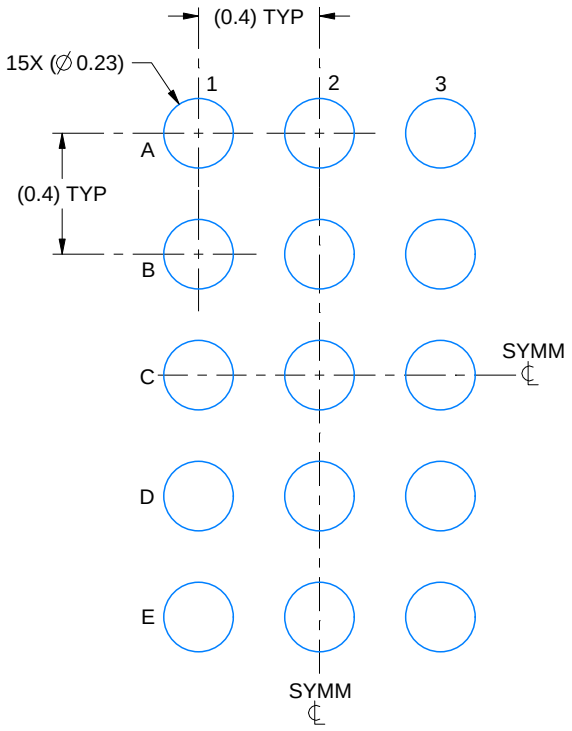
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

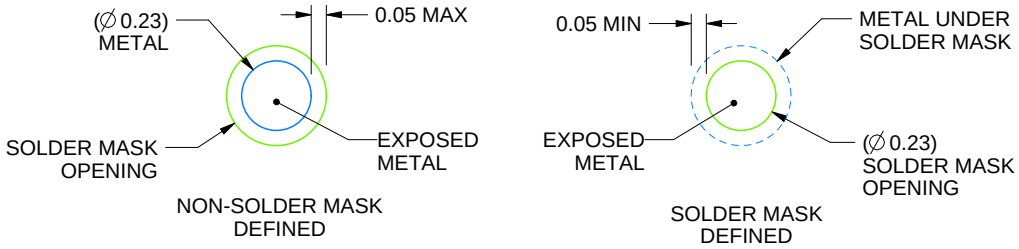


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219378/B 05/2020

NOTES: (continued)

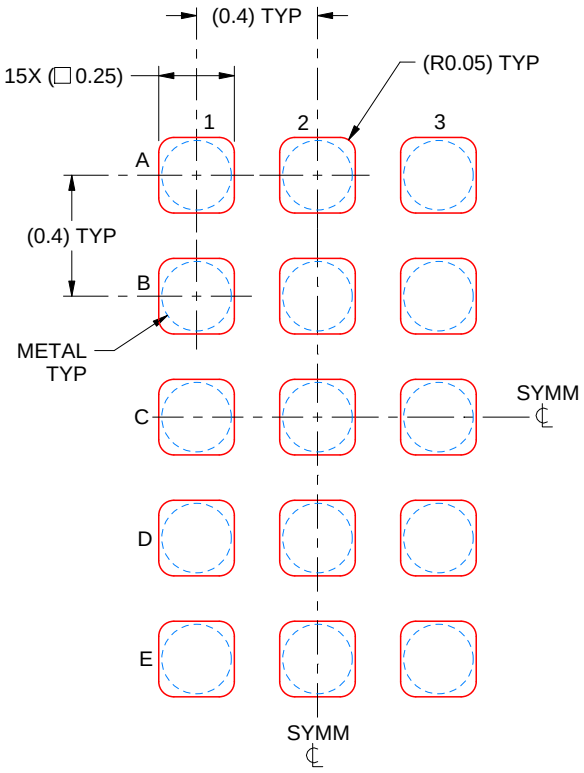
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0015

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219378/B 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122