DAC0800/DAC0802 8-Bit Digital-to-Analog Converters

Check for Samples: DAC0800, DAC0802

FEATURES

- **Fast Settling Output Current: 100 ns**
- **Full Scale Error: ±1 LSB**
- **Nonlinearity Over Temperature: ±0.1%**
- **Full Scale Current Drift: ±10 ppm/°C**
- **High Output Compliance: −10V to +18V**
- **Complementary Current Outputs**
- **Interface Directly with TTL, CMOS, PMOS and Others**
- **2 Quadrant Wide Range Multiplying Capability**
- **Wide Power Supply Range: ±4.5V to ±18V**
- **Low Power Consumption: 33 mW at ±5V**
- **Low Cost**

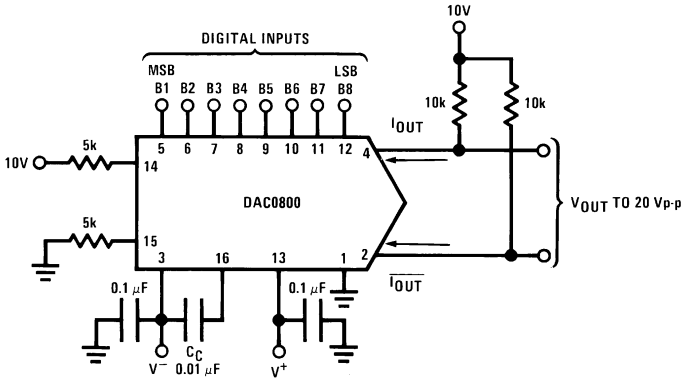
DESCRIPTION

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications, while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs will accept a variety of logic levels. The performance and characteristics of the device are essentially unchanged over the ±4.5V to ±18V power supply range and power consumption at only 33 mW with ±5V supplies is independent of logic input levels.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively. For single supply operation, refer to AN-1525.

Typical Application



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 1. ±20 V_{P-P} Output Digital-to-Analog Converter

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage ($V^+ - V^-$)	±18V or 36V
Power Dissipation (2)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs (V_S- = −15V)	4.25 mA
ESD Susceptibility (3)	TBD V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
PDIP Package (plastic)	260°C
CDIP Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(2) The maximum junction temperature of the DAC0800 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the CDIP package must be derated based on a thermal resistance of 100°C/W, junction-to-ambient, 175°C/W for the molded PDIP package and 100°C/W for the SOIC package.
(3) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Conditions(1)

	Min	Max	Units
Temperature (T_A)			
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0802LC	0	+70	°C
V^+	(V^-) + 10	(V^-) + 30	V
V−	−15	−5	V
I_{REF} (V^- = −5V)	1	2	mA
I_{REF} (V^- = −15V)	1	4	mA

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Electrical Characteristics

The following specifications apply for V_S = ±15V, I_{REF} = 2 mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Parameter		Test Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19	%FS
t_S	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", T_A=25°C		100	135				ns
		DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
t_{PLH}, t_{PHL}	Propagation Delay	T_A=25°C							
	Each Bit			35	60		35	60	ns
	All Bits Switched			35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change <½ LSB, R_{OUT}>20 MΩ, Typical	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000V, R14 = R15 = 5.000 kΩ, T_A=25°C	1.984	1.992	2.00	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4}-I_{FS2}$		±0.5	±4.0		±1	±8.0	µA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0	µA
I_{FSR}	Output Current Range	V^- = −5V V^- = −8V to −18V	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
	Logic Input Levels	V_{LC} = 0V							
V_{IL}	Logic "0"				0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			V
	Logic Input Current	V_{LC} = 0V							
I_{IL}	Logic "0"	−10V ≤ V_{IN} ≤ +0.8V		−2.0	−10		−2.0	−10	µA
I_{IH}	Logic "1"	2V ≤ V_{IN} ≤ +18V		0.002	10		0.002	10	µA
V_{IS}	Logic Input Swing	V^- = −15V	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S = ±15V	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0	µA
dI/dt	Reference Input Slew Rate	(Figure 26)	4.0	8.0		4.0	8.0		mA/µs
$PSSI_{FS+}$	Positive Power Supply Sensitivity	4.5V ≤ V^+ ≤ 18V		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$	Negative Power Supply Sensitivity	−4.5V ≤ V^- ≤ 18V, I_{REF} = 1mA		0.0001	0.01		0.0001	0.01	%/%
I+	Power Supply Current	V_S = ±5V, I_{REF} = 1 mA		2.3	3.8		2.3	3.8	mA
I−				−4.3	−5.8		−4.3	−5.8	mA
I+	Power Supply Current	V_S = +5V, −15V, I_{REF} = 2 mA		2.4	3.8		2.4	3.8	mA
I−				−6.4	−7.8		−6.4	−7.8	mA
I+	Power Supply Current	V_S = ±15V, I_{REF} = 2 mA		2.5	3.8		2.5	3.8	mA
I−				−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Consumption	±5V, I_{REF} = 1 mA		33	48		33	48	mW
		+5V, −15V, I_{REF} = 2 mA		108	136		108	136	mW
		±15V, I_{REF} = 2 mA		135	174		135	174	mW

Connection Diagrams

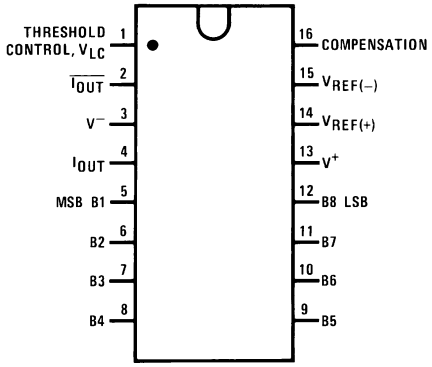


Figure 2. PDIP, CDIP Packages - Top View
(See Package Number NFG0016E or NFE0016A)

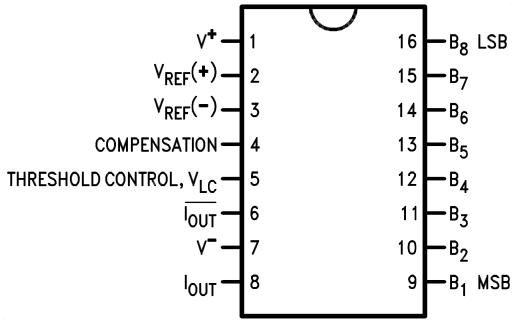
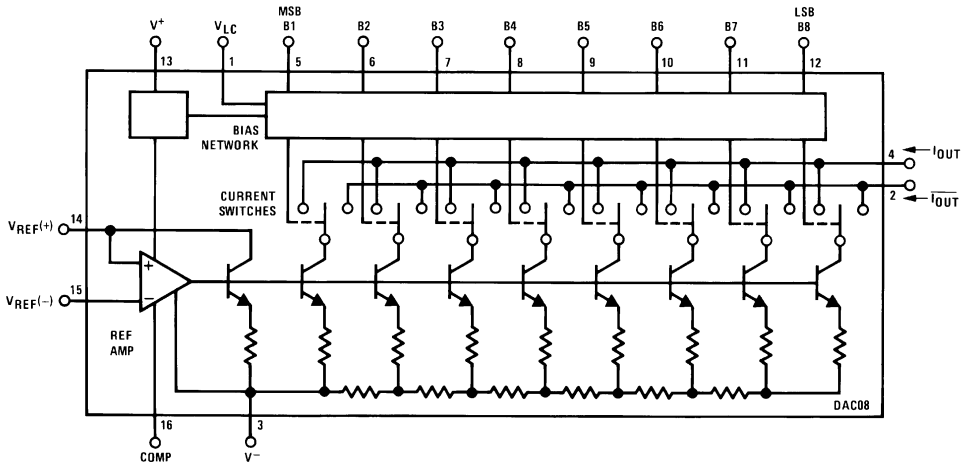


Figure 3. SOIC Package - Top View
(See Package Number D0016A)

Block Diagram



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 4.

Typical Performance Characteristics

Full Scale Current vs. Reference Current

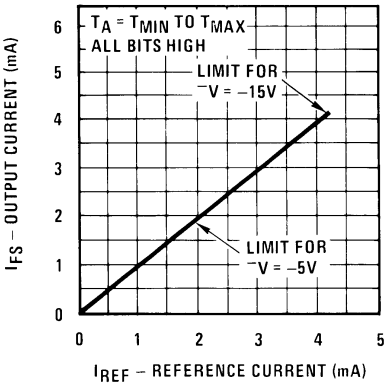


Figure 5.

LSB Propagation Delay vs. I_{FS}

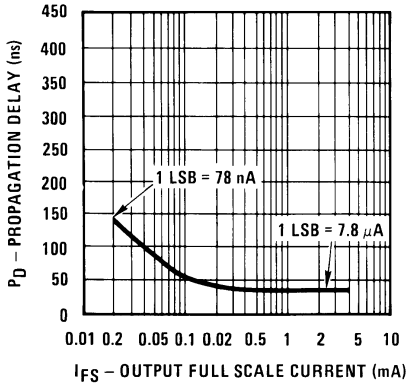
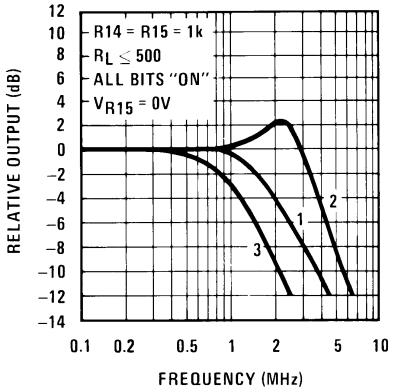


Figure 6.

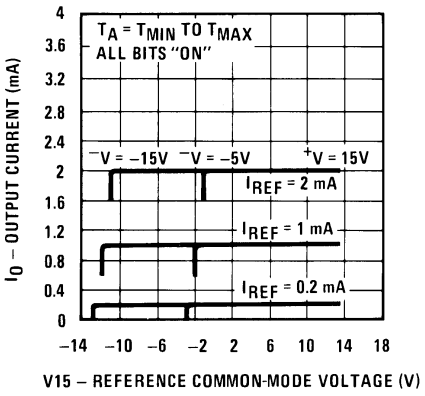
Reference Input Frequency Response



Curve 1: C_C=15 pF, V_{IN}=2 Vp-p centered at 1V.
Curve 2: C_C=15 pF, V_{IN}=50 mVp-p centered at 200 mV.
Curve 3: C_C=0 pF, V_{IN}=100 mVp-p centered at 0V and applied through 50Ω connected to pin 14.2V applied to R14.

Figure 7.

Reference Amp Common-Mode Range



Note. Positive common-mode range is always (V+) − 1.5V.

Figure 8.

Logic Input Current vs. Input Voltage

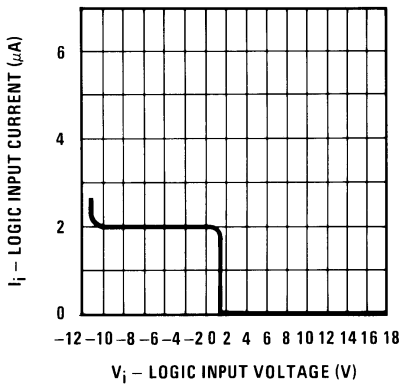


Figure 9.

V_{TH} — V_{LC} vs. Temperature

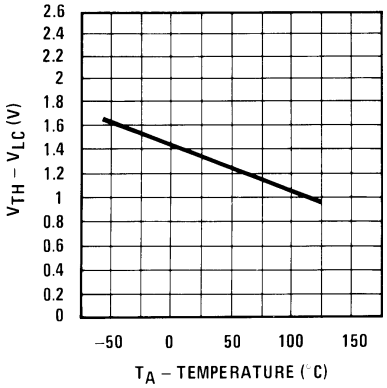


Figure 10.

Typical Performance Characteristics (continued)

Output Current vs. Output Voltage (Output Voltage Compliance)

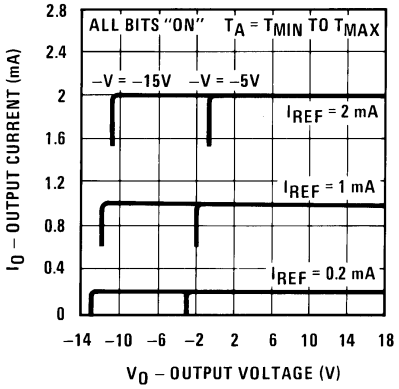


Figure 11.

Output Voltage Compliance vs. Temperature

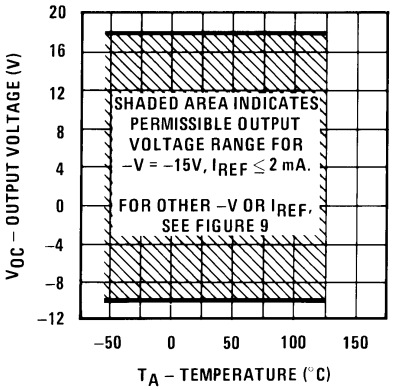
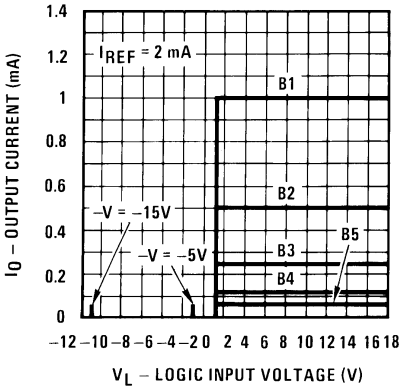


Figure 12.

Bit Transfer Characteristics



Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

Figure 13.

Power Supply Current vs. +V

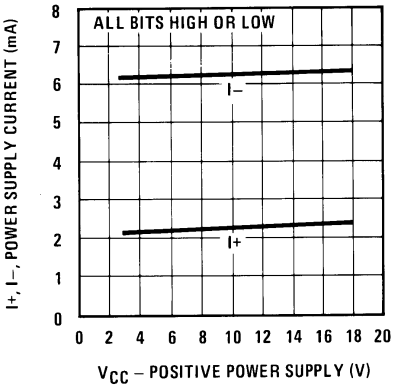


Figure 14.

Power Supply Current vs. –V

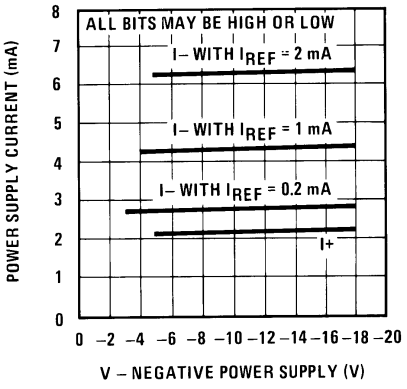


Figure 15.

Power Supply Current vs. Temperature

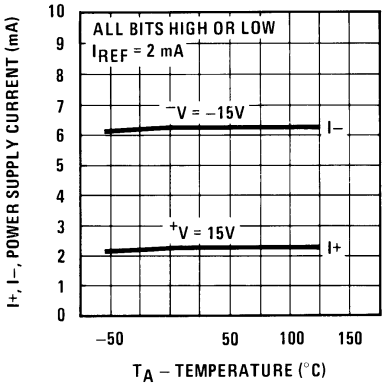


Figure 16.

EQUIVALENT CIRCUIT

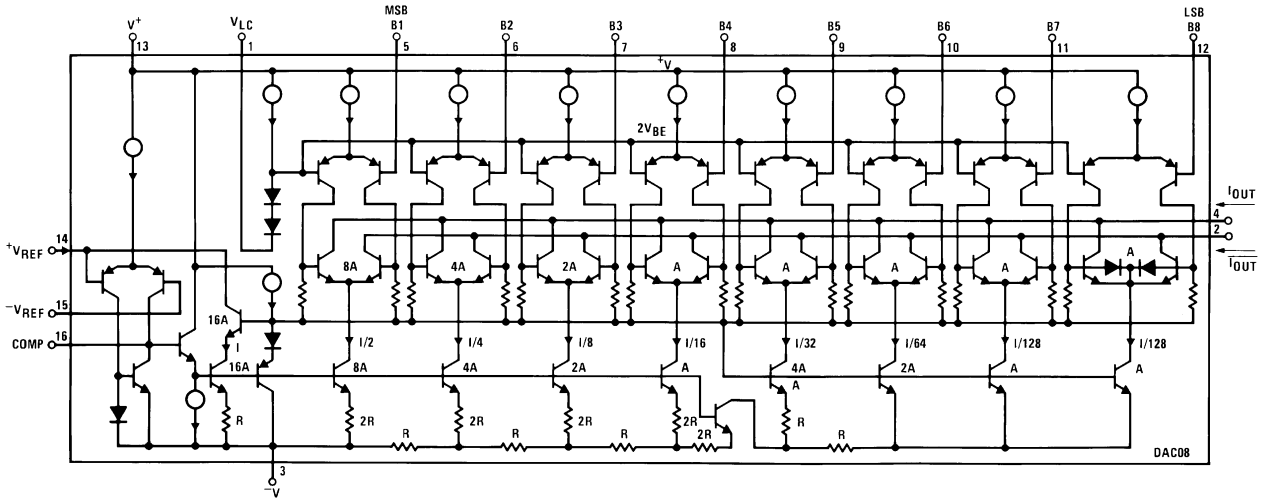
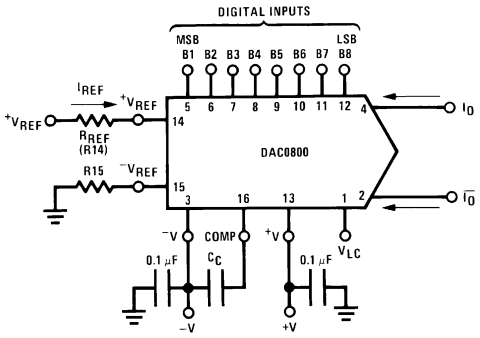


Figure 17. Equivalent Circuit

TYPICAL APPLICATIONS



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \bar{I}_O = I_{FS}$ for all logic states
For fixed reference, TTL operation, typical values are:
V_{REF} = 10.000V
R_{REF} = 5.000k
R15 ≈ R_{REF}
C_C = 0.01 µF
V_{LC} = 0V (Ground)

Figure 18. Basic Positive Reference Operation

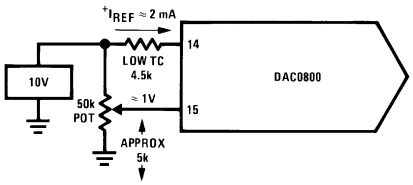


Figure 19. Recommended Full Scale Adjustment Circuit

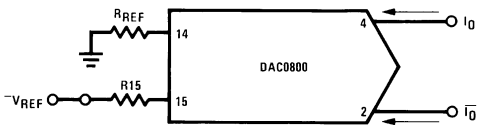
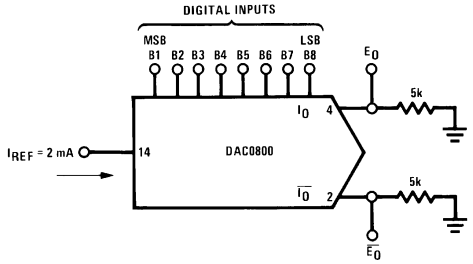


Figure 20. Basic Negative Reference Operation

Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

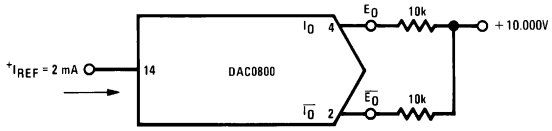


Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 21. Basic Unipolar Negative Operation

Table 1. Basic Unipolar Negative Operation

	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

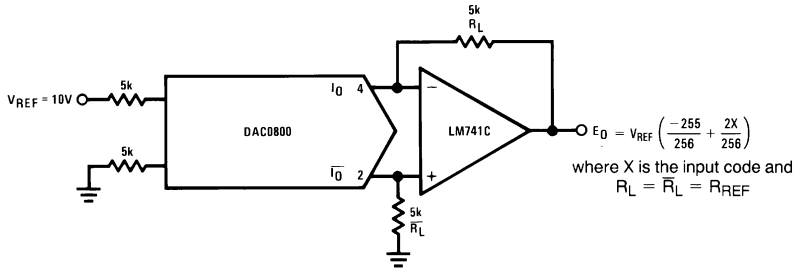


Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 22. Basic Bipolar Output Operation

Table 2. Basic Bipolar Output Operation

	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920



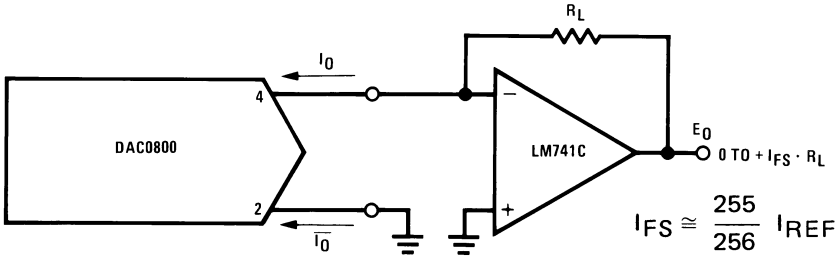
(1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

(2) If $R_L = \overline{R}_L$ within ±0.05%, output is symmetrical about ground.

Figure 23. Symmetrical Offset Binary Operation

Table 3. Symmetrical Offset Binary Operation

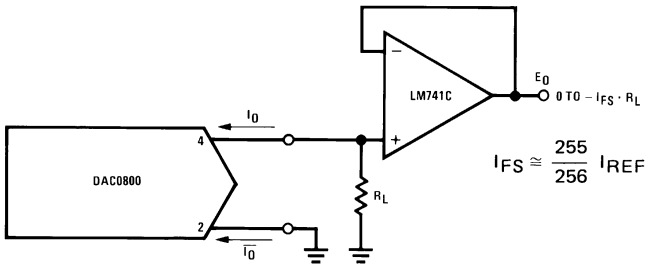
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−)Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	−9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.960



(1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

(2) For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I}_O$ (pin 2), connect I_O (pin 4) to ground.

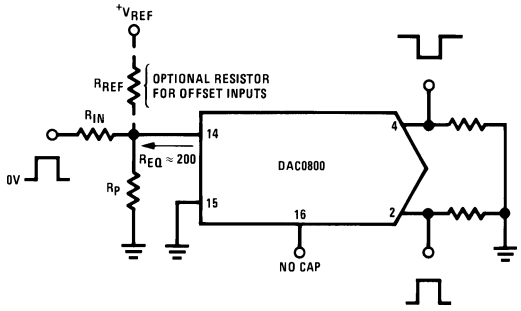
Figure 24. Positive Low Impedance Output Operation



(1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

(2) For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to $\overline{I}_O$ (pin 2); connect I_O (pin 4) to ground.

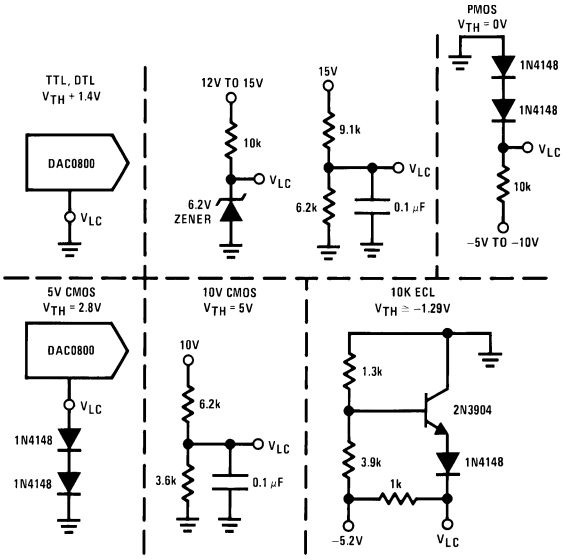
Figure 25. Negative Low Impedance Output Operation



Typical values: R_{IN}=5k,+V_{IN}=10V

Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

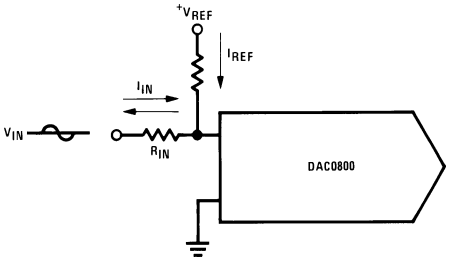
Figure 26. Pulsed Reference Operation



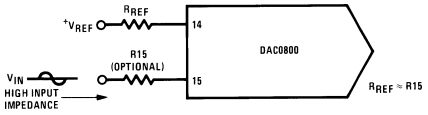
$V_{TH} = V_{LC} + 1.4V$
15V CMOS, HTL, HNIL
V_{TH} = 7.6V
Note. Do not exceed negative logic input range of DAC.

Figure 27. Interfacing with Various Logic Families

(a) I_{REF} ≥ peak negative swing of I_{IN}

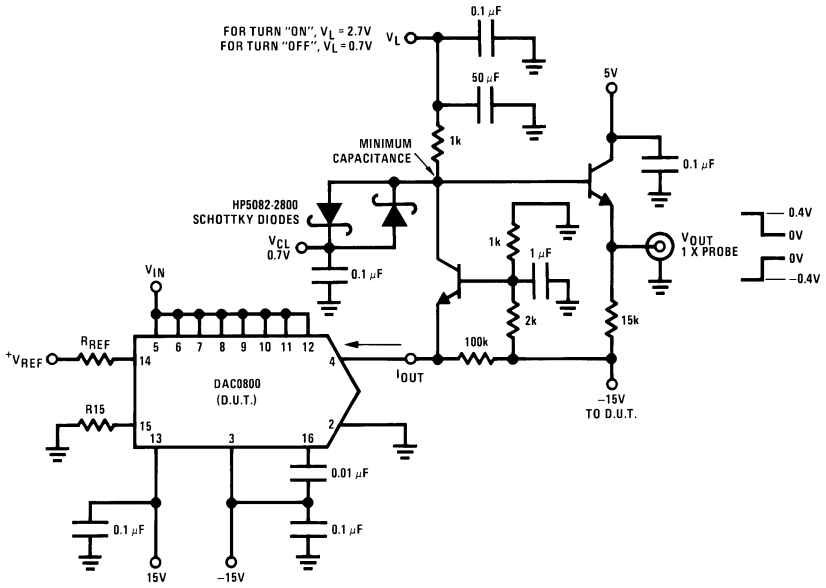


(b) +V_{REF} must be above peak positive swing of V_{IN}



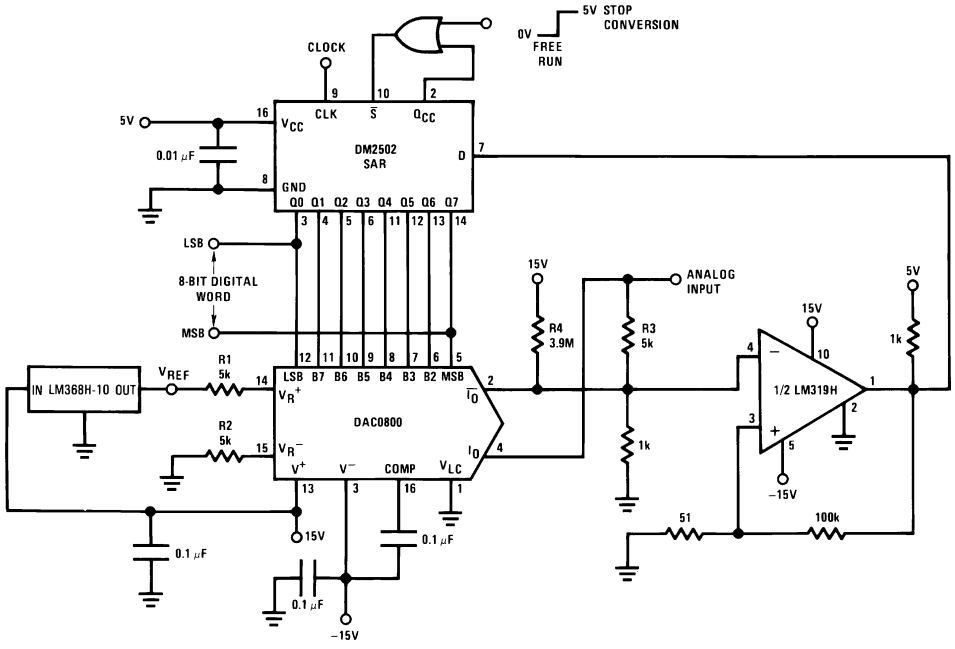
Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 28. Accommodating Bipolar References



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 29. Settling Time Measurement



(1) For 1 µs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

(2) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 30. A Complete 2 µs Conversion Time, 8-Bit A/D Converter

REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC0800LCM	NRND	SOIC	D	16	48	Non-RoHS & Green	Call TI	Call TI	0 to 70	DAC0800LCM	
DAC0800LCM/NOPB	ACTIVE	SOIC	D	16	48	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM	Samples
DAC0800LCMX/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM	Samples
DAC0800LCN/NOPB	ACTIVE	PDIP	NFG	16	25	RoHS & Non-Green	SN	Level-1-NA-UNLIM	0 to 70	DAC0800LCN DAC-08EP	Samples
DAC0802LCMX	NRND	SOIC	D	16	2500	Non-RoHS & Green	Call TI	Call TI	0 to 70	DAC0802LCM	
DAC0802LCMX/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	DAC0802LCM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

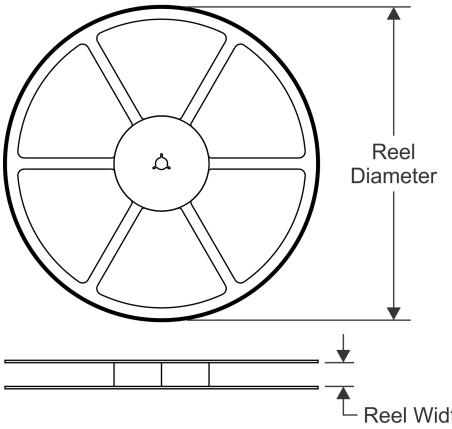
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

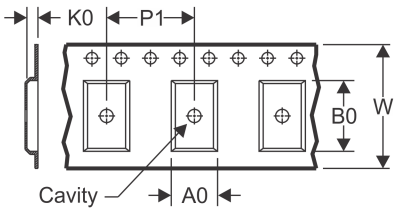
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

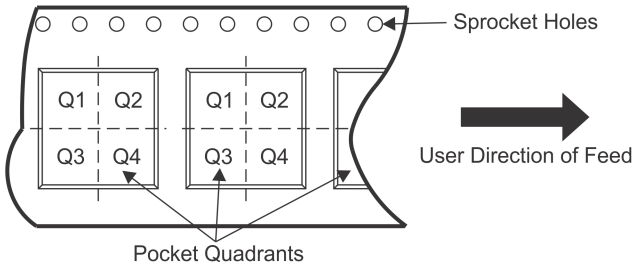


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

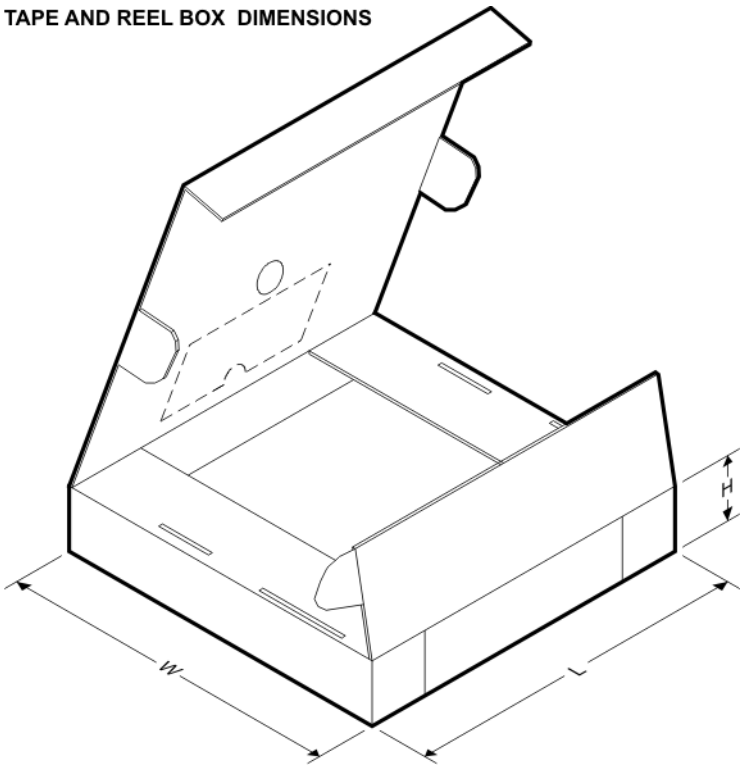
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC0800LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DAC0802LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

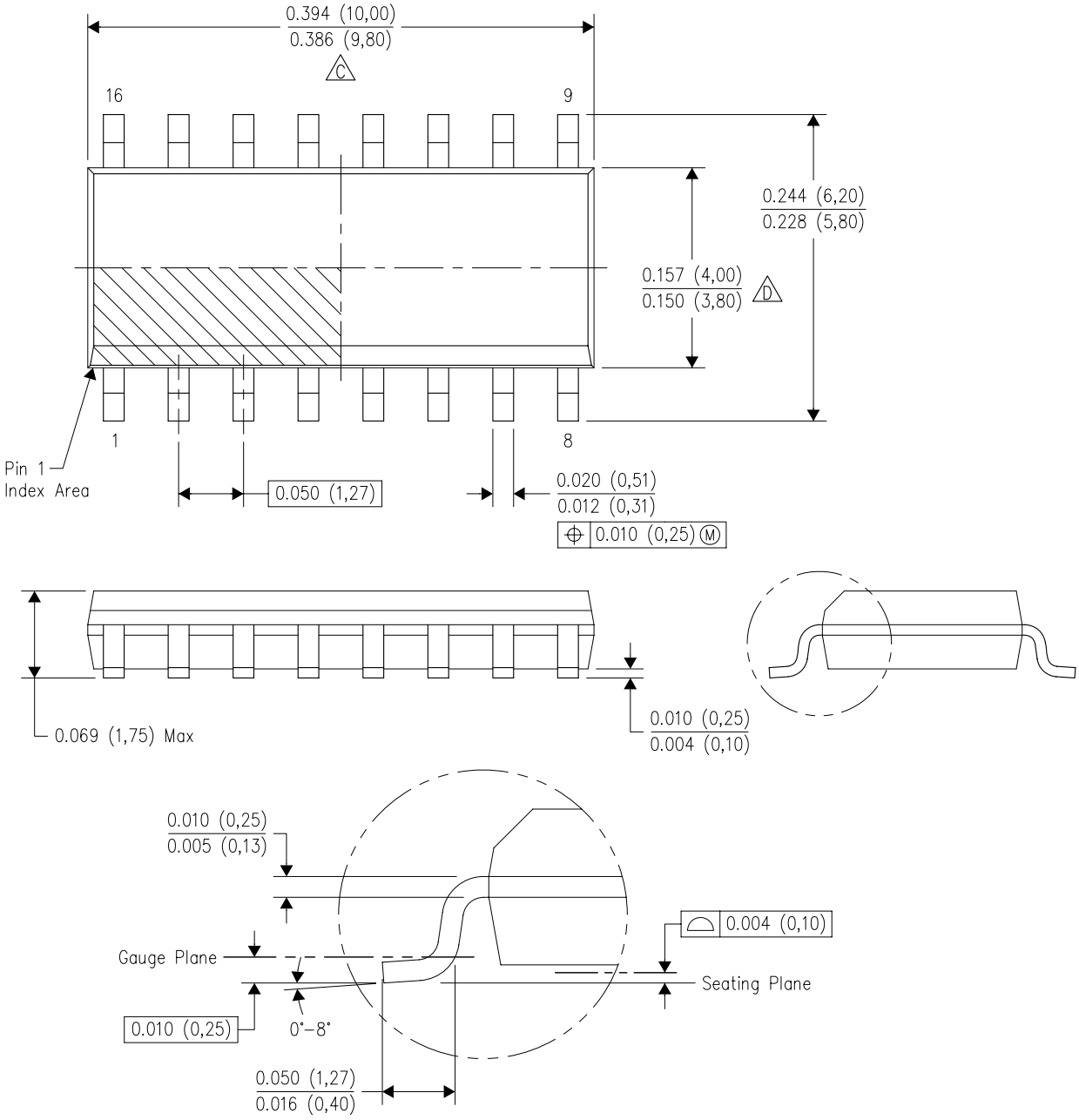
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

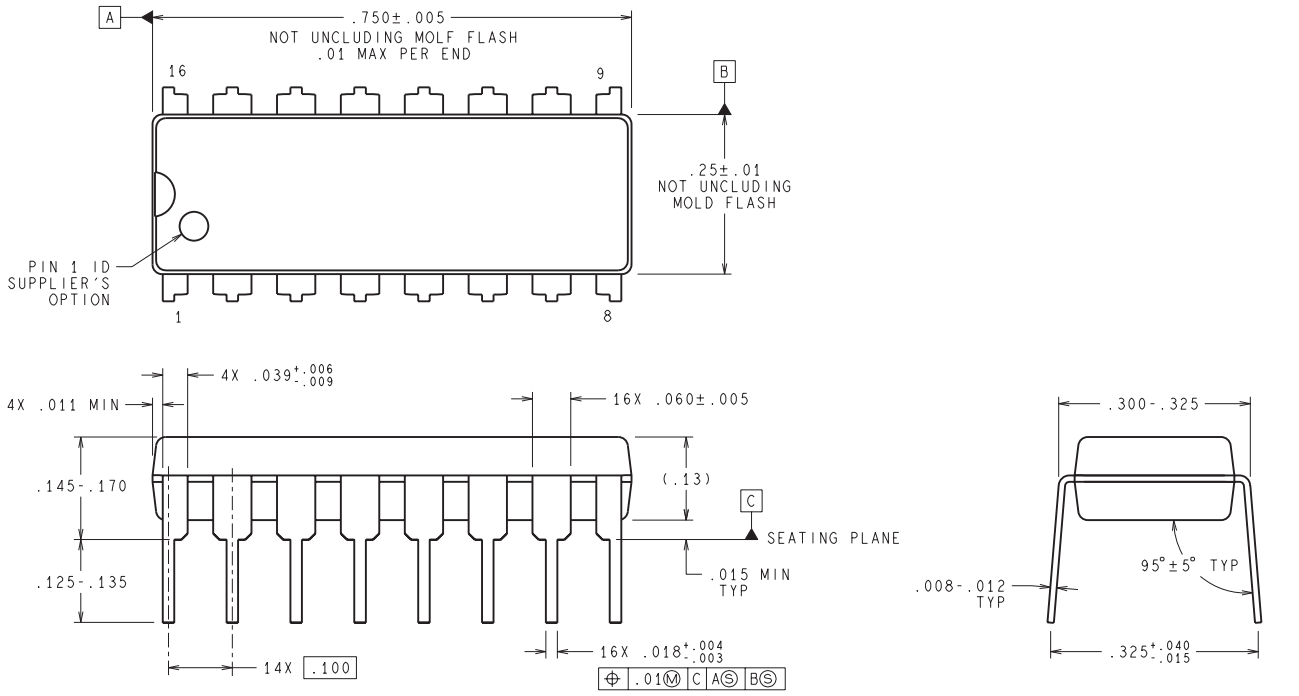
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC0800LCMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
DAC0802LCMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

NFG0016E



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

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