ADS8355
双路、16 位、1MSPS、同步采样，模数转换器

1 特性

- 1MSPS 吞吐量、无延迟输出
- 两个通道同步采样
- 支持单端和伪差分输入
- 出色的直流和交流性能：
  - 16 位 NMC DNL，±1LSB INL
  - 88dB SNR，–97dB THD
- 双路、可编程
  2.5V 内部基准电压
- 完整的扩展工业温度范围：–40°C 至 +125°C
- 小型封装：
  WQFN-16 (3mm × 3mm)

2 应用

- 伺服驱动器位置反馈
- 光学模块
- 多功能继电器
- 电能质量分析仪
- 三相 UPS
- 模拟输入模块

3 说明

ADS8355 是一款双路高速同步采样模数转换器 (ADC)，可支持单端和伪差分模拟输入。

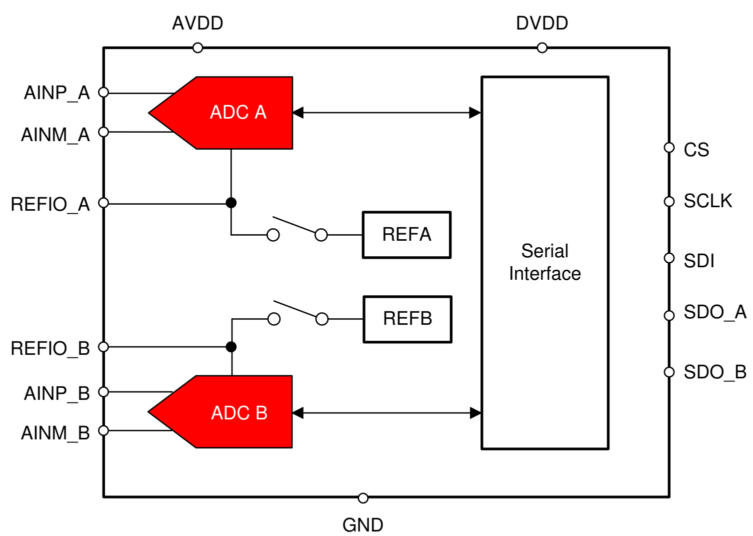
该器件支持灵活的串行接口，可以在宽电源电压范围内正常工作。通过灵活的接口可以方便地与各种主机控制器通信。该系列器件支持两种低功耗模式，可针对给定输出优化功耗。该器件可在完整的扩展工业温度范围（–40°C 至 +125°C）内正常工作，并采用 16 引脚 WQFN（3mm × 3mm）封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS8355	WQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型方框图



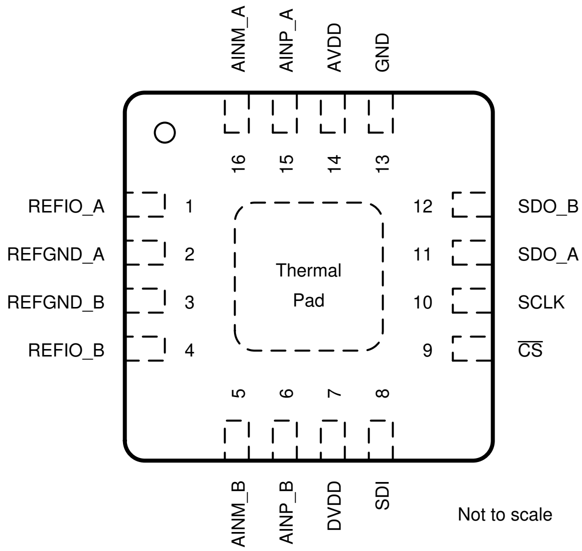
目录

4 修订历史记录

Changes from Original (February 2020) to Revision A	**Page**
• Deleted AVDD supply condition and MIN MAX specification for internal reference.	6
• Deleted AVDD supply condition and MIN MAX specification for internal reference.	6

5 Pin Configuration and Functions

**RTE Package
16-Pin WQFN
Top View**



Pin Functions

NAME	NO.	TYPE	DESCRIPTION
AINM_A	16	Analog input	Negative analog input, channel A
AINM_B	5	Analog input	Negative analog input, channel B
AINP_A	15	Analog input	Positive analog input, channel A
AINP_B	6	Analog input	Positive analog input, channel B
AVDD	14	Power supply	Supply voltage for ADC operation
$\overline{CS}$	9	Digital input	Chip-select signal; active low
DVDD	7	Digital I/O supply	Digital I/O supply
GND	13	Power supply	Device ground
REFGND_A	2	Power supply	Reference A ground
REFGND_B	3	Power supply	Reference B ground
REFIO_A	1	Analog input/output	Reference voltage input/output, channel A
REFIO_B	4	Analog input/output	Reference voltage input/output, channel B
SCLK	10	Digital input	Clock for serial communication
SDI	8	Digital input	Data input for serial communication
SDO_A	11	Digital output	Data output A for serial communication, channel A and channel B
SDO_B	12	Digital output	Data output B for serial communication, channel B
Thermal pad		Power supply	Exposed thermal pad. TI recommends connecting this pin to the printed circuit board (PCB) ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
AVDD to REFGND_x[2] or GND	–0.3	6	V
DVDD to GND	–0.3	6	V
Analog (AINP_x and AINM_x)[3] and reference input (REFIO_x) voltage with respect to REFGND_x	REFGND_x – 0.3	AVDD + 0.3	V
Digital input voltage with respect to GND	GND – 0.3	DVDD + 0.3	V
REFGND_x	GND – 0.3	GND + 0.3	V
Input current to any pin except supply pins	–10	10	mA
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) REFGND_x refers to REFGND_A and REFGND_B. REFIO_x refers to REFIO_A and REFIO_B.
(3) AINP_x refers AINP_A and AINP_B. AINM_x refers to AINM_A and AINM_B.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage (AVDD to AGND)	V_{REF} range, internal reference	4.5	5	5.5	V
		V_{REF} range, external reference V_{REF} < 4.5 V	4.5	5	5.5	
		V_{REF} range, external reference V_{REF} > 4.5 V	V_{REF}	5	5.5	
		2 x V_{REF} range, internal reference	5	5	5.5	
		2 x V_{REF} range, external reference	2 x V_{REF}	5	5.5	
DVDD	Digital supply voltage		1.65	3.3	5.5	V
ANALOG INPUTS (Single-Ended Configuration)						
FSR	Full-scale input range (AINP_x to AINM_x)(1)	V_{REF} range	0		V_{REF}	V
		2 x V_{REF} range	0		2 x V_{REF}	
V_{INP}	Absolute input voltage (AINP_x to REFGND_x)(2)	V_{REF} range	0		V_{REF}	V
		2 x V_{REF} range, AVDD ≥ 2 x V_{REF}	0		2 x V_{REF}	
V_{INM}	Absolute input voltage (AINM_x to REFGND_x)		–0.1		0.1	V
ANALOG INPUTS (Pseudo-Differential Configuration)						
FSR	Full-scale input range (AINP_x to AINM_x)(1)	V_{REF} range	–V_{REF} / 2		V_{REF} / 2	V
		2 x V_{REF} range	–V_{REF}		V_{REF}	
V_{INP}	Absolute input voltage (AINP_x to REFGND_x)	V_{REF} range	0		V_{REF}	V
		2 x V_{REF} range	0		2 x V_{REF}	
V_{INM}	Absolute input voltage (AINM_x -REFGND_x)	V_{REF} range	V_{REF} / 2 – 0.1	V_{REF} / 2	V_{REF} / 2 + 0.1	V
		2 x V_{REF} range	V_{REF} – 0.1	V_{REF}	V_{REF} + 0.1	
EXTERNAL REFERENCE INPUT						
V_{REFIO}	REFIO_x(3) input voltage	V_{REF} range	2.4	2.5	AVDD	V
		2 x V_{REF} range	2.4	2.5	AVDD / 2	
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) AINP_x refers to analog input pins AINP_A and AINP_B. AINM_x refers to analog input pins AINM_A and AINM_B.
(2) REFGND_x refers to reference ground pins REFGND_A and REFGND_B.
(3) REFIO_x refers to voltage reference inputs REFIO_A and REFIO_B.

6.4 Thermal Information

THERMAL METRIC(1)		ADS8355 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at AVDD = 5 V, DVDD = 2.35 V to 5.5 V, V_{REFIO_A} = V_{REFIO_B} = 5 V (external) and f_{SAMPLE} = 1 MSPS (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY						
NMC	No missing codes		16			Bits
INL	Integral nonlinearity		–3	±1	3	LSB
		V_{REF} input range, internal V_{REF} = 2.5 V		±1		
DNL	Differential nonlinearity		–0.99	±0.5	0.99	LSB
		V_{REF} input range, internal V_{REF} = 2.5 V		±0.5		
E_{IO}	Input offset error		–1	±0.5	1	mV
	E_{IO} match	ADC_A to ADC_B	–1	±0.5	1	
dE_{IO}/dT	Input offset thermal drift			1		µV/°C
E_G	Gain error	Referenced to the voltage at REFIO_x	–0.1	±0.05	0.1	%FS
	E_G match	ADC_A to ADC_B	–0.1	±0.05	0.1	
dE_G/dT	Gain error thermal drift	Referenced to the voltage at REFIO_x		±1		ppm/°C
AC ACCURACY						
SNR	Signal-to-noise ratio	V_{REF} input range	86	88		dB
		AVDD = 3.3 V, V_{REF} input range, internal V_{REF} = 2.5 V		84		
		V_{REF} = 2.5 V internal / external, 2 x V_{REF} input range		84		
THD	Total harmonic distortion	V_{REF} input range		–97		dB
		AVDD = 3.3 V, V_{REF} input range, internal V_{REF} = 2.5 V		–97		
		V_{REF} = 2.5 V internal/external, 2 x V_{REF} input range		–97		

Electrical Characteristics (continued)

at AVDD = 5 V, DVDD = 2.35 V to 5.5 V, V_{REFIO_A} = V_{REFIO_B} = 5 V (external) and f_{SAMPLE} = 1 MSPS (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion	V_{REF} input range		87.5		dB
		AVDD = 3.3 V, V_{REF} input range, internal V_{REF} = 2.5 V		83		
		V_{REF} = 2.5 V internal / external, 2 x V_{REF} input range		83		
SFDR	Spurious-free dynamic range	V_{REF} input range		100		dB
		AVDD = 3.3 V, V_{REF} input range, internal V_{REF} = 2.5 V		100		
		V_{REF} = 2.5 V internal/external, 2 x V_{REF} input range		100		
ANALOG INPUTS						
C_i	Input capacitance	In sample mode		40		pF
		In hold mode		4		
I_{lkg}	Input leakage current			0.1		µA
INTERNAL VOLTAGE REFERENCE						
V_{REFIO_x}	Reference output voltage	REFDAC_x = 1FFh at 25°C		2.5		V
$V_{REF\text{-}match}$	VREF_A to VREF_B matching	REFDAC_x = 1FFh at 25°C		±3		mV
C_{REFIO}	Reference output capacitor			10		µF
t_{REFON}	Reference output settling time			8		ms
VOLTAGE REFERENCE INPUT						
I_{REF}	Average reference input current	Per ADC		300		µA
C_{REF}	External reference capacitor			10		µF
$I_{lkg(dc)}$	DC leakage current			±0.1		µA
SAMPLING DYNAMICS						
t_A	Aperture delay			8		ns
	t_A match	ADC_A to ADC_B		40		ps
t_{AJIT}	Aperture jitter			50		ps
DIGITAL INPUTS						
V_{IH} (1)	High-level input voltage	DVDD ≥ 2.35 V	0.7 x DVDD		DVDD + 0.3	V
		DVDD < 2.35 V	0.8 x DVDD		DVDD + 0.3	
V_{IL} (1)	Low-level input voltage	DVDD ≥ 2.35 V	–0.3		0.3 x DVDD	V
		DVDD < 2.35 V	–0.3		0.2 x DVDD	
	Input current			±10		nA
DIGITAL OUTPUTS						
V_{OH} (1)	High-level output voltage	I_{OH} = 500-µA source	0.8 x DVDD		DVDD	V
V_{OL} (1)	Low-level output voltage	I_{OL} = 500-µA sink	0		0.2 x DVDD	V

(1) Specified by design.

Electrical Characteristics (continued)

at AVDD = 5 V, DVDD = 2.35 V to 5.5 V, V_{REFIO_A} = V_{REFIO_B} = 5 V (external) and f_{SAMPLE} = 1 MSPS (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AIDD	Analog supply current			11	13	mA
		AVDD = 5 V, internal reference		12		mA
		AVDD = 5V, no conversion internal reference		8		mA
		AVDD = 5 V, no conversion external reference(2)		7		mA
		AVDD = 5 V, STANDBY mode internal reference		2.5		mA
		AVDD = 5 V, STANDBY mode external reference(2)		1		mA
		Power-down mode		10	50	µA
DIDD	Digital supply current	DVDD = 3.3 V, C_{load} = 10 pF		0.5		mA
		DVDD = 5 V, C_{load} = 10 pF		1		mA

(2) With internal reference powered down, REF_SEL = 1.

6.6 Timing Requirements

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

			MIN	NOM	MAX	UNIT
t_{CYCLE}	Cycle time	DVDD ≥ 2.35 V	1			µs
		1.65 V < DVDD < 2.35 V	1.5			µs
f_{CLK}	Serial clock frequency	DVDD ≥ 2.35 V			50	MHz
		1.65 V < DVDD < 2.35 V			24	MHz
t_{CLK}	Serial clock time period	DVDD ≥ 2.35 V	20			ns
		1.65 V < DVDD < 2.35 V	42			ns
t_{PH_CK}	Clock high time		0.45		0.55	t_{CLK}
t_{PL_CK}	Clock low time		0.45		0.55	t_{CLK}
t_{ACQ}	Acquisition time		350			ns
t_{PH_CS}	$\overline{CS}$ high time, NOP		40			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling edge to SCLK falling edge	DVDD ≥ 2.35 V	12			ns
		1.65 V < DVDD < 2.35 V	20			ns
t_{D_CKCS}	Delay time: Last SCLK falling edge to $\overline{CS}$ rising edge		12			ns
t_{SU_CKDI}	Setup time: DIN data valid to SCLK falling edge		2			ns
t_{HT_CKDI}	Hold time: SCLK falling edge to (previous) data valid on DIN		2			ns

6.7 Switching Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time				650	ns
t_{DEN_CSDO}	Delay time: $\overline{CS}$ falling edge to data enable	DVDD ≥ 2.35 V			14.5	ns
	Delay time: $\overline{CS}$ falling edge to data enable	1.65 V < DVDD < 2.35 V			14.5	
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising edge to data going to 3-state	DVDD ≥ 2.35 V			31	ns
	Delay time: $\overline{CS}$ rising edge to data going to 3-state	1.65 V < DVDD < 2.35 V			37	
t_{D_CKDO}	Delay time: SCLK falling edge to next data valid	DVDD ≥ 2.35 V			19.5	ns
	Delay time: SCLK falling edge to next data valid	1.65 V < DVDD < 2.35 V			19.5	

图 1 shows the details of the serial interface between the device and the digital host controller.

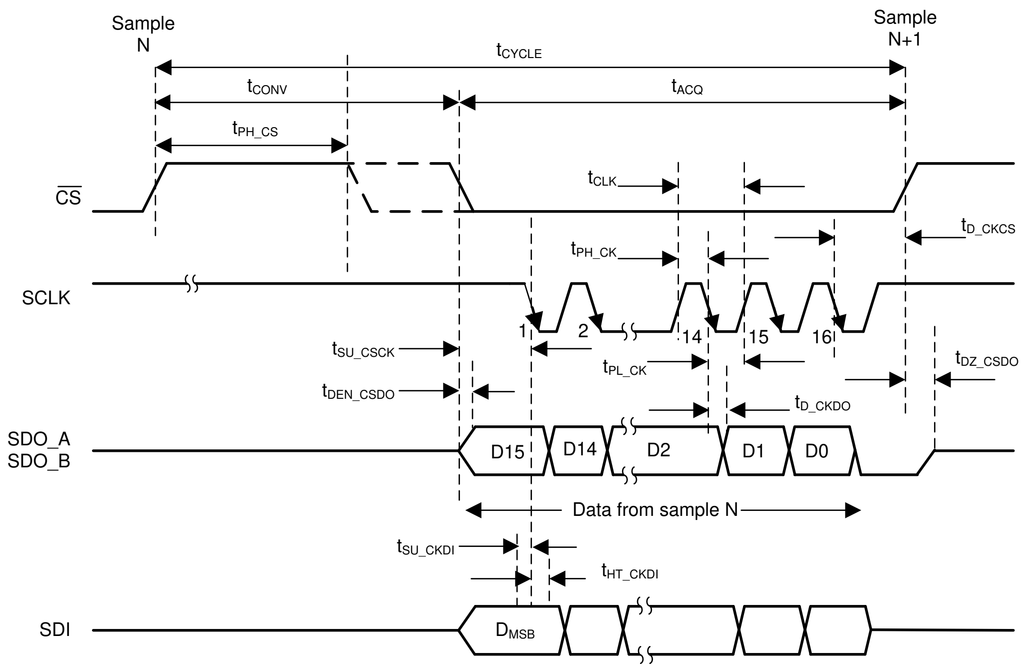
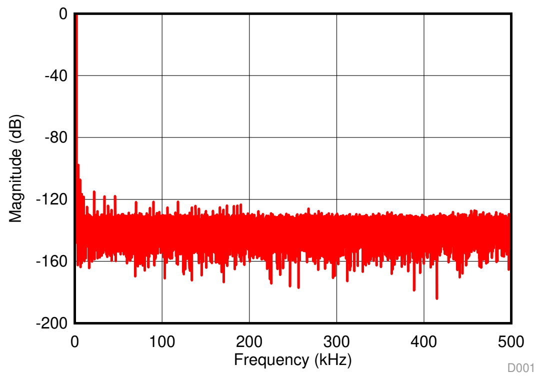


图 1. Serial interface Timing Diagram

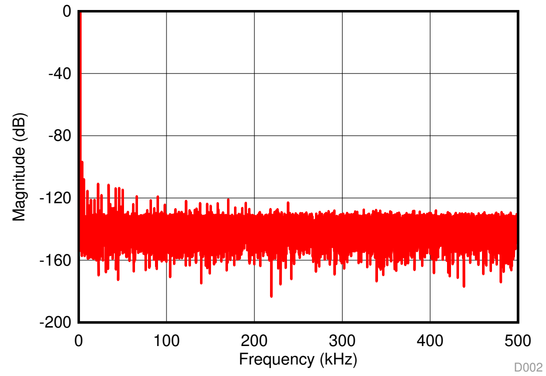
6.8 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (external), and f_{DATA} = 1 MSPS (unless otherwise noted)



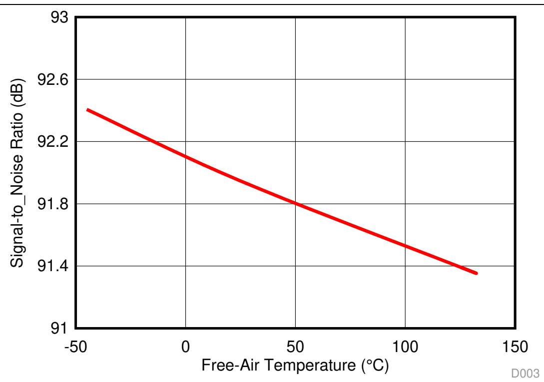
f_{IN} = 2 kHz, SNR = 91.27 dB, THD = –96.78 dB

图 2. Typical FFT ADC A



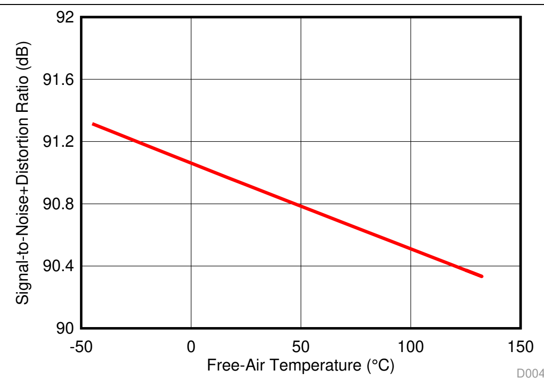
f_{IN} = 2 kHz, SNR = 91.31 dB, THD = –96.04 dB

图 3. Typical FFT ADC B



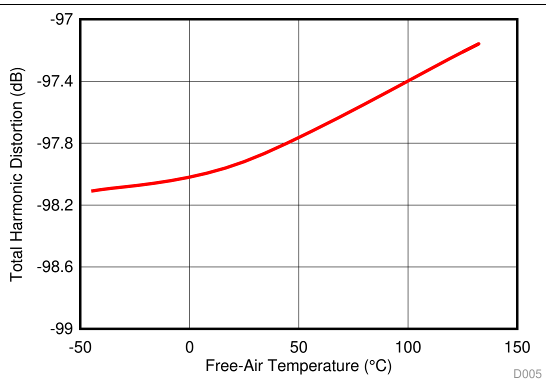
f_{IN} = 2 kHz

图 4. SNR vs Free-Air Temperature



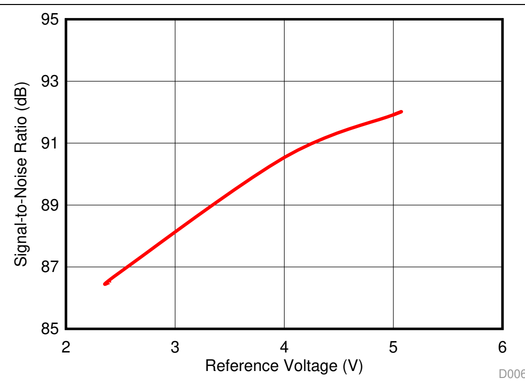
f_{IN} = 2 kHz

图 5. SINAD vs Free-Air Temperature



f_{IN} = 2 kHz

图 6. THD vs Free-Air Temperature

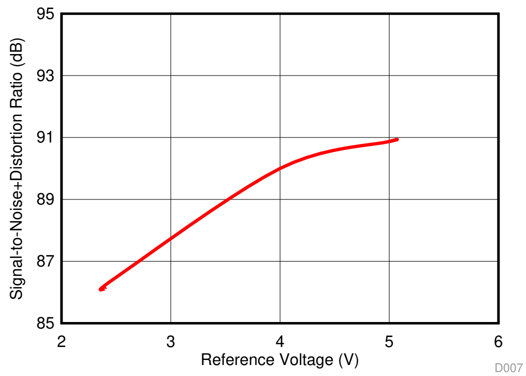


f_{IN} = 2 kHz

图 7. SNR vs Reference Voltage

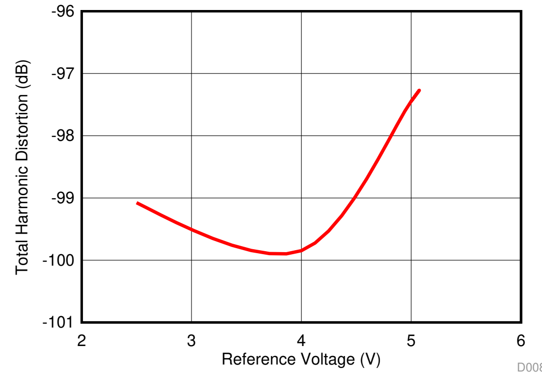
Typical Characteristics (接下页)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (external), and f_{DATA} = 1 MSPS (unless otherwise noted)



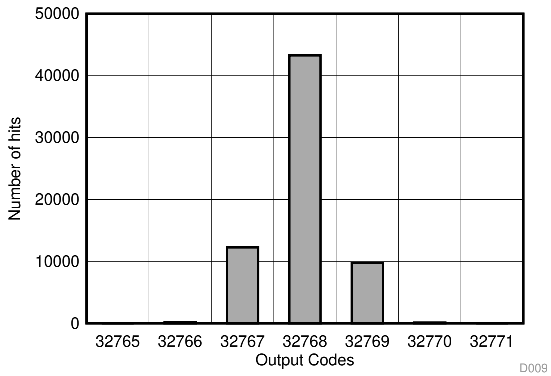
f_{IN} = 2 kHz

图 8. SINAD vs Reference Voltage



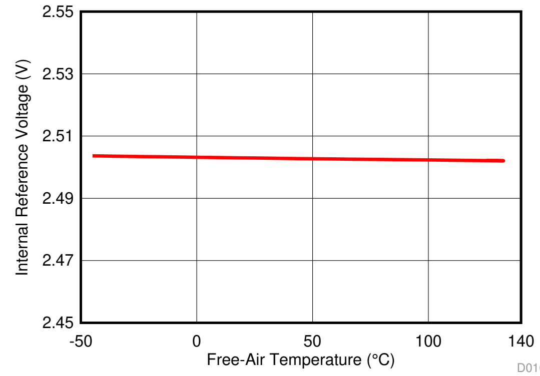
f_{IN} = 2 kHz

图 9. THD vs Reference Voltage



Number of samples = 65536, standard deviation = 0.59

图 10. DC Histogram



V_{REFIO_x} = 2.5 V

图 11. Internal Reference vs Free-Air Temperature

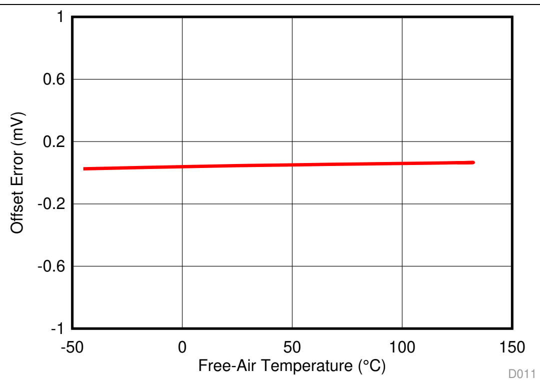


图 12. Offset Error vs Free-Air Temperature

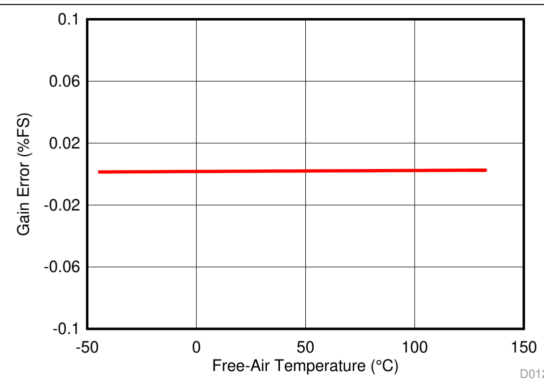


图 13. Gain Error vs Free-Air Temperature

Typical Characteristics (接下页)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (external), and f_{DATA} = 1 MSPS (unless otherwise noted)

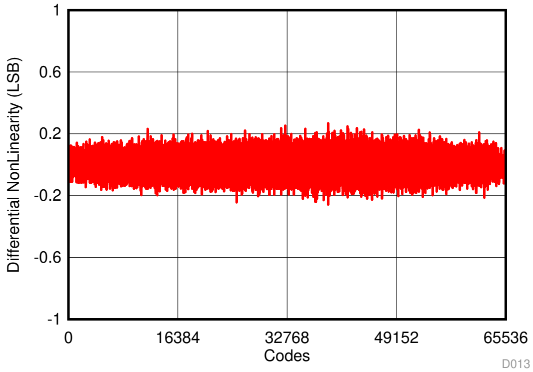


图 14. Differential Nonlinearity ADC A

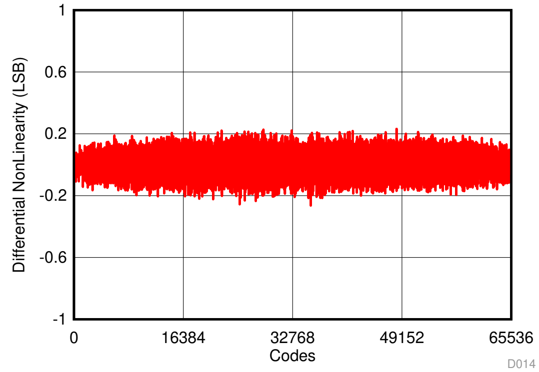


图 15. Differential Nonlinearity ADC B

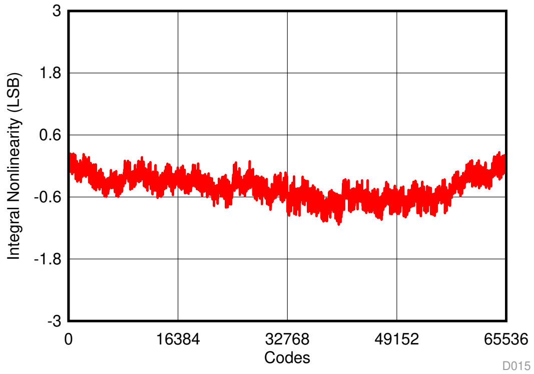


图 16. Integral Nonlinearity ADC A

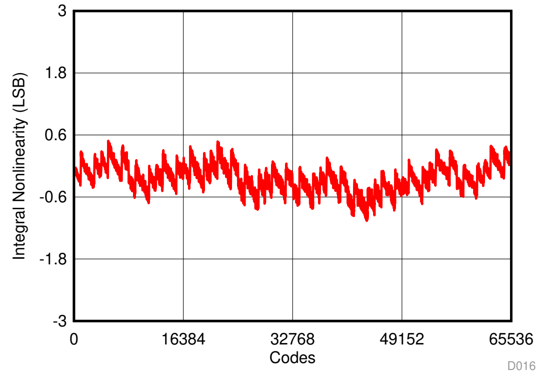


图 17. Integral Nonlinearity ADC B

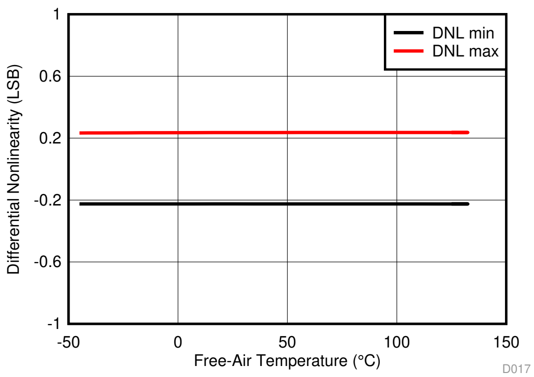


图 18. Differential Nonlinearity vs Free-Air Temperature

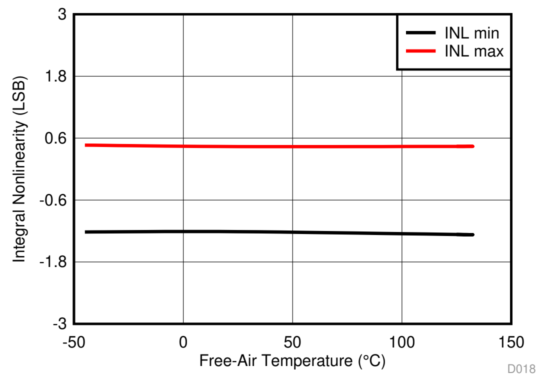


图 19. Integral Nonlinearity vs Free-Air Temperature

Typical Characteristics (接下页)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (external), and f_{DATA} = 1 MSPS (unless otherwise noted)

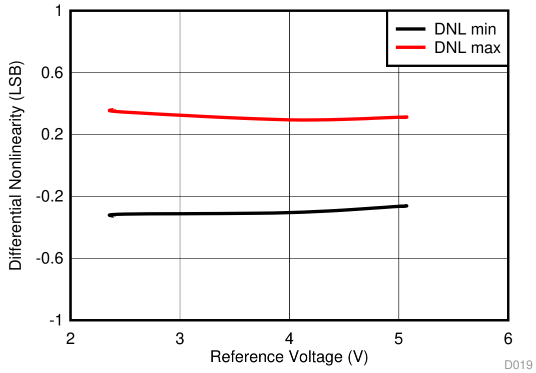


图 20. Differential Nonlinearity vs Reference Voltage

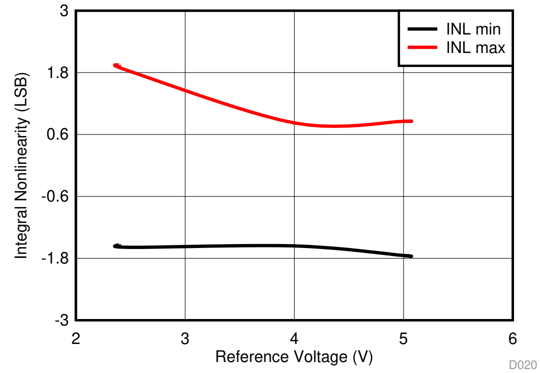


图 21. Integral Nonlinearity vs Reference Voltage

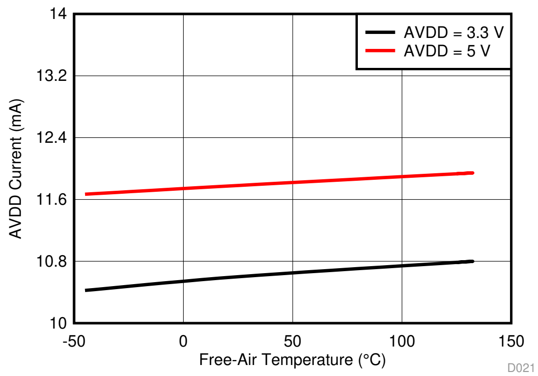


图 22. Analog Supply Current vs Free-Air Temperature

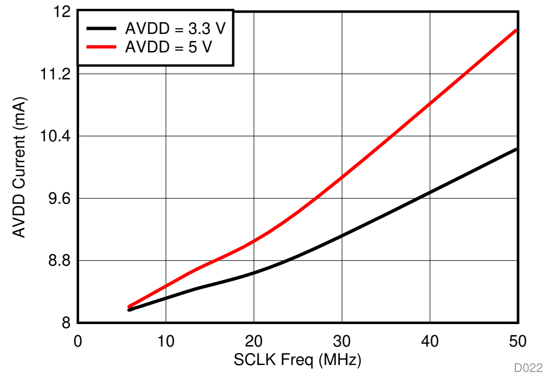


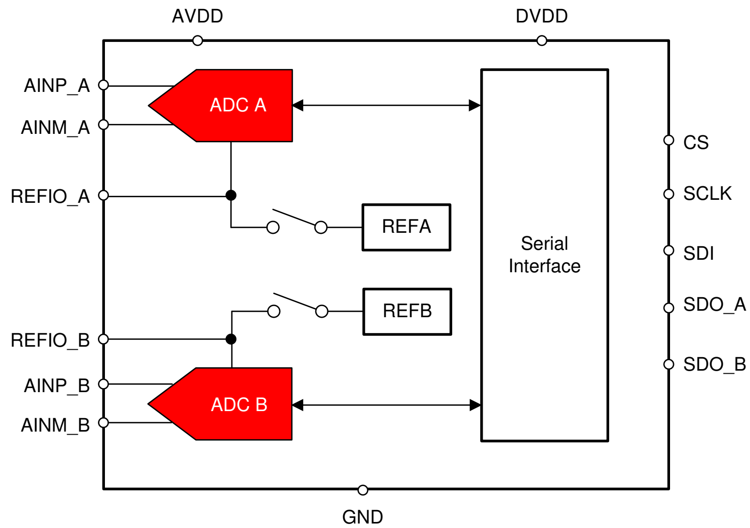
图 23. Analog Supply Current vs SCLK Frequency

7 Detailed Description

7.1 Overview

The ADS8355 is a 16-bit, 1-MSPS, dual, simultaneous-sampling, analog-to-digital converter (ADC) with an integrated programmable reference. The ADS8355 supports single-ended and pseudo-differential input signals. The device provides a simple, serial interface to the host controller and operates over a wide range of analog and digital power supplies.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference

The device has two simultaneous sampling ADCs: ADC_A and ADC_B. ADC_A and ADC_B operate with reference voltages V_{REF_A} and V_{REF_B} present on the REFIO_A and REFIO_B pins, respectively. Decouple the REFIO_A and REFIO_B pins with the REFGND_A and REFGND_B pins, respectively, with 10-µF decoupling capacitors.

As illustrated in 图 24, the device supports operation either with an internal or external reference source. The reference voltage source is determined by programming the INT_EXT bit of the REF_SEL register. This bit is common to ADC_A and ADC_B.

Feature Description (接下页)

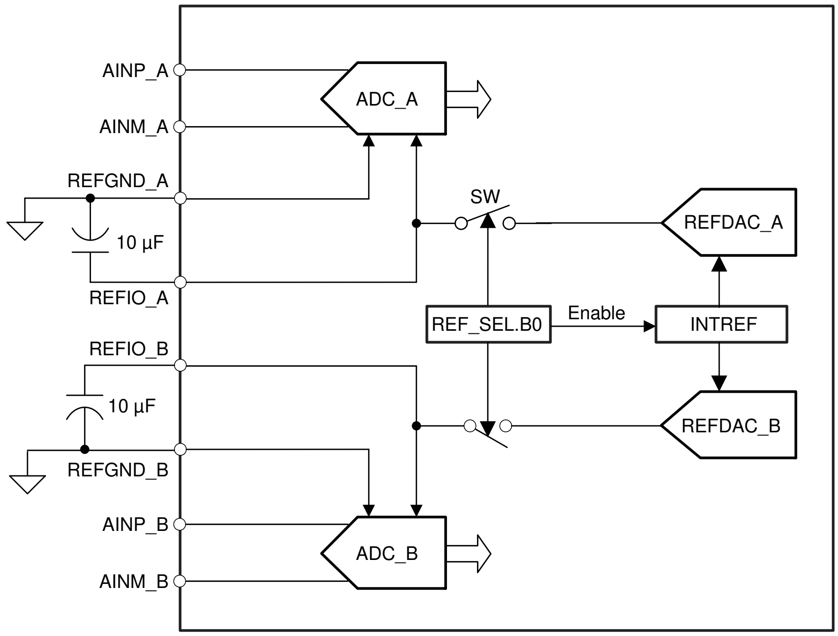


图 24. Reference Configurations and Connections

The default value of the REF_SEL register bit INT_EXT is set to 0. The device ADC_A and ADC_B operate with the external reference voltages provided on the REFIO_A and REFIO_B pins, respectively.

When the REF_SEL register bit INT_EXT is set to 1, the device operates with the internal reference source connected to REFIO_A and REFIO_B. The individual reference voltages can be set independently by programming the REFDAC_A and REFDAC_B values, respectively. For a 2.5-V internal reference, program REFDAC_x with a 0x1FF value..

图 25 shows a typical transfer function for the internal REFDAC when the internal reference is enabled.

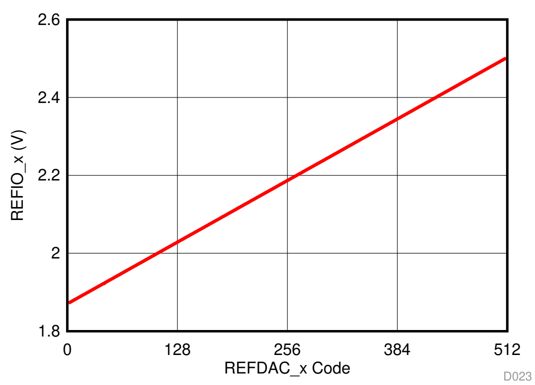


图 25. REFDAC Transfer Function

7.3.2 Analog Inputs

The ADS8355 supports single-ended or pseudo-differential analog input signals on both ADC channels. These inputs are sampled and converted simultaneously by the two ADCs, ADC_A and ADC_B. ADC_A samples and converts ($V_{AINP\_A} – V_{AINM\_A}$), and ADC_B samples and converts ($V_{AINP\_B} – V_{AINM\_B}$).

图 26 depicts equivalent circuits for the ADC_A and ADC_B analog input pins. Series resistance, R_S, represents the on-state sampling switch resistance (typically 50 Ω) and C_{SAMPLE} is the device sampling capacitor (typically 40 pF).

Feature Description (接下页)

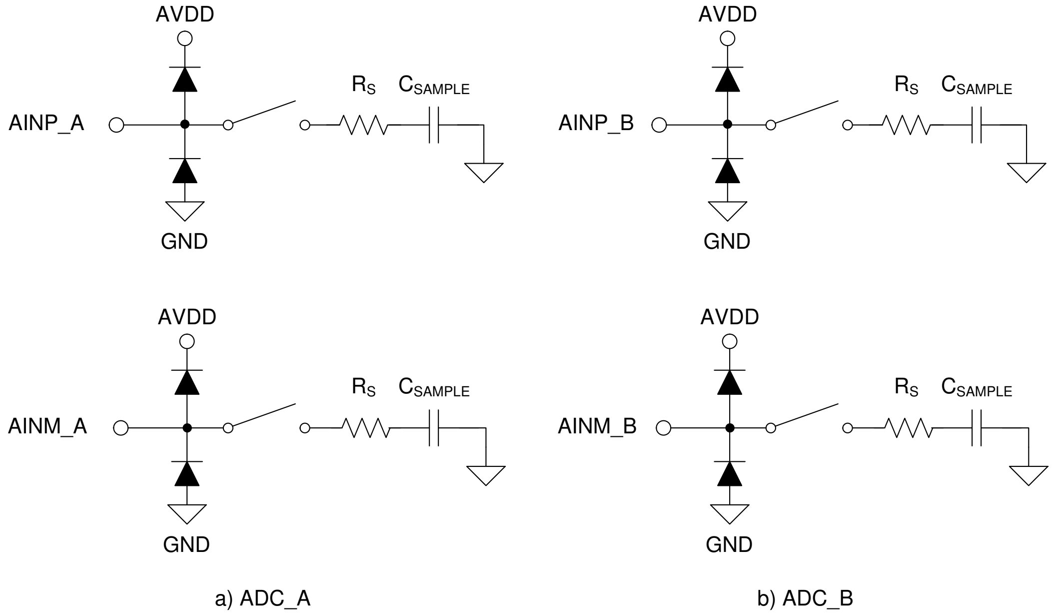


图 26. Equivalent Circuit for the Analog Input Pins

7.3.2.1 Analog Input: Full-Scale Range Selection

The full-scale range (FSR) supported at the analog inputs of the device is programmable with the RANGE_SEL bit of the INPUT_CONFIG register. The RANGE_SEL bit has a default value of low. This bit is common for both ADCs (ADC_A and ADC_B). 公式 1 and 公式 2 give the FSR.

$$\text{RANGE\_SEL} = 0, \text{FSR\_ADC\_A} = 0 \text{ to } V_{REF\_A} \text{ and FSR\_ADC\_B} = 0 \text{ to } V_{REF\_B} \quad (1)$$

$$\text{For RANGE\_SEL} = 1, \text{FSR\_ADC\_A} = 0 \text{ to } 2 \times V_{REF\_A} \text{ and FSR\_ADC\_B} = 0 \text{ to } 2 \times V_{REF\_B} \quad (2)$$

V_{REF_A} and V_{REF_B} are the reference voltages going to ADC_A and ADC_B, respectively (as described in the *Reference* section).

When operating with internal reference mode, the maximum dynamic range of the ADC can be used by programming the appropriate setting for the INPUT_CONFIG and REFDAC_x registers.

Ensure that the ADC analog supply (AVDD) meets the criteria defined in 公式 3 and 公式 4 when the RANGE_SEL bit is set to 1.

$$2 \times V_{REF\_A} \le \text{AVDD} \le \text{AVDD(max)} \quad (3)$$

$$2 \times V_{REF\_B} \le \text{AVDD} \le \text{AVDD(max)} \quad (4)$$

7.3.2.2 Analog Input: Single-Ended and Pseudo-Differential Configurations

The ADS8355 can support single-ended or pseudo-differential input configuration. The device operates in single-ended configuration by default.

The AINM_SEL bit in the INPUT_CONFIG register determines the input configuration used for the input pins. The selection is common for both input channels.

Program the AINM_SEL pin to logic low to operate the device in single-ended input configuration. Connect the AINM_A and AINM_B inputs to GND.

Program the AINM_SEL pin to logic high to operate the device in pseudo-differential input configuration. Connect the AINM_A and AINM_B inputs to a voltage equivalent to FSR_ADC_A / 2 and FSR_ADC_B / 2, respectively.

表 1 summarizes the analog input pin connections based on the various user settings.

Feature Description (接下页)

表 1. Input Configurations and Connections

INPUT RANGE SELECTION RANGE_SEL	INPUT CONFIGURATION SELECTION AINM_SEL	AINP_X	AINM_X
0	0	Input signal range 0 to V_{REF_X}	Connect to GND
1	0	Input signal range 0 to 2 X V_{REF_X}	Connect to GND
0	1	Input signal range 0 to V_{REF_X}	Connect to V_{REF_X} / 2
1	1	Input signal range 0 to 2 X V_{REF_X}	Connect to V_{REF_X}

7.3.3 Transfer Function

The device supports two input configurations:

1. Default, single-ended inputs, INPUT_CONFIG register bit 0 = 0
2. Pseudo-differential inputs, INPUT_CONFIG register bit 0 = 1

The device supports two output data formats:

1. Default, straight binary output, DATA_OUT_CTRL register bit 0 = 0
2. Two's compliment output, DATA_OUT_CTRL register bit 0 = 1

公式 5 calculates the device resolution:

$$1\ LSB = (FSR\_ADC\_x) / (2^N) \tag{5}$$

where:

- N = 16 and
- FSR_ADC_x is the full-scale input range of the ADC

表 2 and 表 3 show the different input voltages and the corresponding output codes from the device.

表 2. Transfer Characteristics for Straight Binary Output (Default)

INPUT CONFIGURATION	INPUT VOLTAGE			OUTPUT CODE (Hex) STRAIGHT BINARY	
	AINP_x	AINM_x	AINP_x - AINM_x	CODE	ADS8355
Single-ended	≤ 1 LSB	0	≤ 1 LSB	ZC	0000
	FSR_ADC_x / 2		FSR_ADC_x / 2	MC	7FFF
	≥ FSR_ADC_x – 1 LSB		≥ FSR_ADC_x – 1 LSB	FSC	FFFF
Pseudo-differential	≤ 1 LSB	FSR_ADC_x / 2	≤ –FSR_ADC_x / 2 + 1 LSB	ZC	0000
	FSR_ADC_x / 2		0	MC	7FFF
	≥ FSR_ADC_x – 1 LSB		≥ FSR_ADC_x / 2 – 1 LSB	FSC	FFFF

表 3. Transfer Characteristics for Twos Compliment Output

INPUT CONFIGURATION	INPUT VOLTAGE			OUTPUT CODE (Hex) TWO'S COMPLIMENT	
	AINP_x	AINM_x	AINP_x - AINM_x	CODE	ADS8355
Single-ended	≤ 1 LSB	0	≤ 1 LSB	NFSC	8000
	FSR_ADC_x / 2		FSR_ADC_x / 2	MC	0000
	≥ FSR_ADC_x – 1 LSB		≥ FSR_ADC_x – 1 LSB	PFSC	7FFF
Pseudo-differential	≤ 1 LSB	FSR_ADC_x / 2	≤ –FSR_ADC_x / 2 + 1 LSB	NFSC	8000
	FSR_ADC_x / 2		0	MC	0000
	≥ FSR_ADC_x – 1 LSB		≥ FSR_ADC_x / 2 – 1 LSB	PFSC	7FFF

图 27 shows the ideal device transfer characteristics for the single-ended analog input.

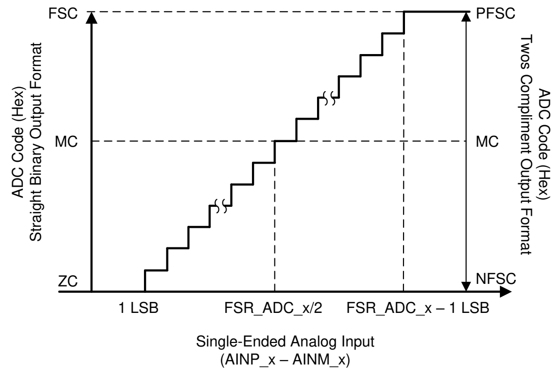


图 27. Ideal Transfer Characteristics for a Single-Ended Analog Input

图 28 shows the ideal device transfer characteristics for the pseudo-differential analog input.

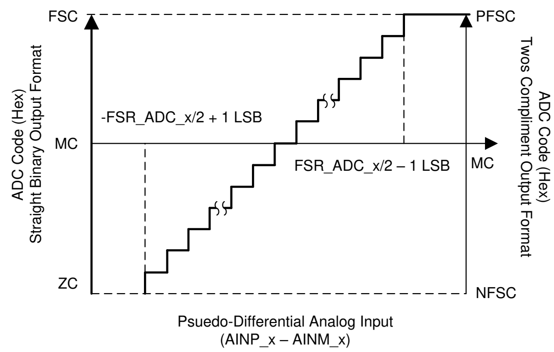


图 28. Ideal Transfer Characteristics for a Pseudo-Differential Analog Input

7.4 Device Functional Modes

7.4.1 Conversion Data Read: Dual-SDO Mode (Default)

The dual-SDO mode is designed to support the maximum throughput at lower SCLK frequencies.

The single-SDO mode is enabled by programming the SDO_MODE bit in the SDO_CTRL register to logic low. In this mode, the SDO_A pin outputs the ADC_A conversion result and the SDO_B pin outputs the ADC_B conversion result. 图 29 shows a detailed timing diagram for this mode.

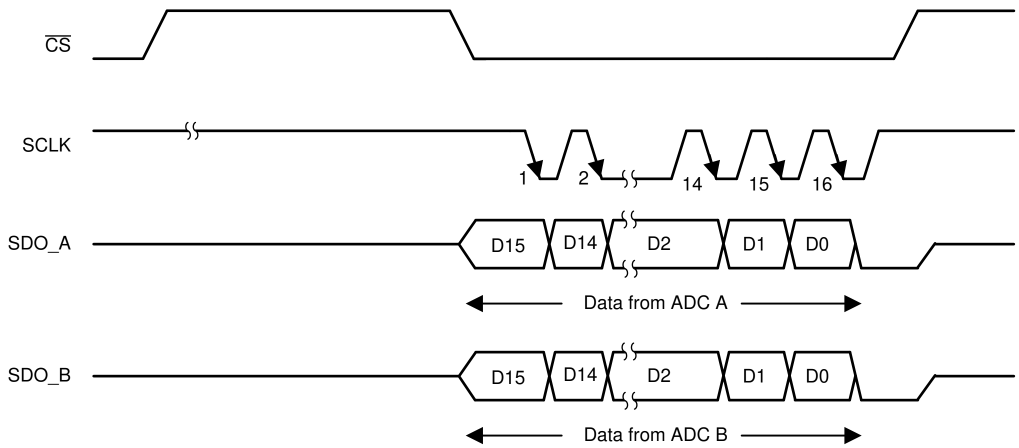


图 29. Dual-SDO Mode Timing Diagram

A CS rising edge forces SDO_x to tri-state. CS also samples the input signal and causes the device to enter conversion phase. Conversion is done with the internal clock. CS and SCLK must remain high for a minimum time of t_{CONV}. A CS falling edge brings the serial data bus out of tri-state and the device outputs the MSB of the data. The lower data bits are output on the subsequent SCLK falling edges. SDO_A and SDO_B go low after the 16th SCLK falling edge. The SDO_x signals remain low until the CS signal is pulled high.

Device Functional Modes (接下页)

7.4.2 Conversion Data Read: Single-SDO Mode

The single-SDO mode is designed to support operation with a wide variety of hosts that can support only one master in, slave out (MISO) signal for the SPI interface. The maximum throughput is limited based on the SCLK frequency supported by the host.

The single-SDO mode is enabled by programming the SDO_MODE bit in the SDO_CTRL register to logic high. In this mode, the SDO_A pin outputs the conversion results for ADC_A followed by ADC_B. 图 30 shows a detailed timing diagram for this mode.

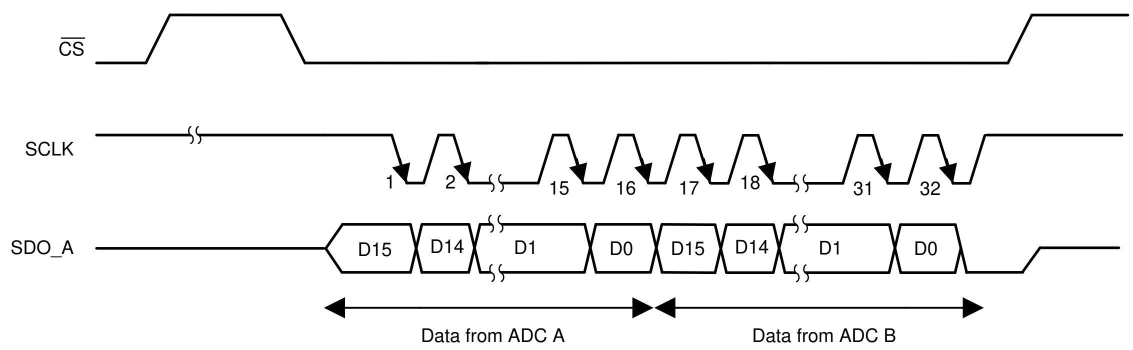


图 30. Single-SDO Mode Timing Diagram

A $\overline{CS}$ rising edge forces SDO_x to tri-state. $\overline{CS}$ also samples the input signal and causes the device to enter conversion phase. Conversion is done with the internal clock. $\overline{CS}$ and SCLK must remain high for a minimum time of t_{CONV}. A $\overline{CS}$ falling edge brings the serial data bus out of tri-state and the device outputs the MSB of the ADC_A conversion result. The lower data bits are output on the subsequent SCLK falling edges. After ADC_A, the device outputs the ADC_B conversion result starting from 17th falling edge of SCLK. SDO_A drives the output line to a zero logic level after 32nd falling edge of SCLK. SDO_A remains low until the $\overline{CS}$ signal is pulled high. SDO_B is driven low when the SPI interface is active in single-SDO mode.

7.4.3 Low-Power Modes

In normal mode of operation, all internal circuits of the device are always powered up and the device is ready to commence a new conversion when $\overline{CS}$ is pulled high. The device also supports two low-power modes to optimize the power consumption at lower throughput or when the device is not expected to perform conversions.

7.4.3.1 STANDBY Mode

The device supports a standby mode of operation where the ADCs and the internal oscillator are powered down to save power. The internal reference, if already enabled, stays enabled and the contents of the REFDAC_A and REFDAC_B registers are retained to enable faster power-up to a normal mode of operation.

Standby mode is enabled by programming the PD_KEY register with 0x09h followed by setting the STANDBY bit in the PD_STANDBY register with logic high. See the *Register Map* section for the register setting information. See the *Register Read/Write Operation* section for timing information for register access.

Standby mode is disabled by programming the PD_KEY register with 0x09h followed by setting the STANDBY bit in the PD_STANDBY register with logic low. After existing standby mode, a delay of 10 µs must elapse for the internal circuits to power up and resume normal operation.

7.4.3.2 PD (Power-Down) Mode

The device supports a PD (power-down) mode of operation where all internal blocks except the interface and I/O are powered down to save power.

PD mode is enabled by programming the PD_KEY register with 0x09h followed by setting the PD_EN bit in the PD_STANDBY register with logic high. See the *Register Map* section for the register setting information. See the *Register Read/Write Operation* section for timing information for register access.

Device Functional Modes (接下页)

PD mode is disabled by programming the PD_KEY register with 0x09h followed by setting the PD_EN bit in the PD_STANDBY register with logic low. After exiting PD mode, a delay of 1 ms must elapse with the external reference mode and 3 ms must elapse with the internal reference mode for the internal circuits to power up and resume normal operation.

7.5 Programming

7.5.1 Register Read/Write Operation

This device features configuration registers and supports the commands listed in 表 4 to access the internal configuration registers.

表 4. Supported Commands

B[19:16]	B[15:8]	B[7:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
0000	00000000000	00000000	NOP	No operation. Next frame provides the ADC conversion result output on the SDO_X lines.
0001	<8-bit address>	<8-bit data>	WR_REG	Write <8-bit data> to the <8-bit address>
0010	<8-bit address>	00000000	RD_REG	Read contents from the <8-bit address>
0011	<8-bit address>	<8-bit unmasked bits>	SET_BITS	Set <8-bit unmasked bits> from <8-bit address>
0100	<8-bit address>	<8-bit unmasked bits>	CLR_BITS	Clear <8-bit unmasked bits> from <8-bit address>
Remaining combinations	xxxxxxxxx	xxxxxxxx	Reserved	These commands are reserved and treated by the device as no operation.

The ADS8355 supports two types of data transfer operations: *data write* (the host controller configures the device), and *data read* (the host controller reads data from the device).

Any data write to the device is always synchronous to the external clock provided on the SCLK pin. The WR_REG command writes the 8-bit data into the 8-bit address specified in the command string. The CLR_BITS command clears the specified bits (identified by 1) at the 8-bit address (without affecting the other bits), and the SET_BITS command sets the specified bits (identified by 1) at the 8-bit address (without affecting the other bits).

图 31 shows the digital waveform for a register read operation. A register read operation consists of two frames: one frame to initiate a register read and a second frame to read data from the register address provided in the first frame. As shown in 图 31, the 8-bit register address and the 8-bit dummy data are sent over the SDI pin during the first 20-bit frame with the read command (0010b). The 20-bit command information is right-aligned with the frame. If a command frame is smaller than 20 bits, the contents of the command are discarded. If a frame has more than 20 bits, the last 20 bits are used to decode the operation. When $\overline{CS}$ goes from low to high, this read command is decoded and the requested register data are available for reading during the next frame. During the second frame, the first eight bits on SDO_A correspond to the requested register read. During the second frame, SDI can be used to initiate another operation or can be set to 0.

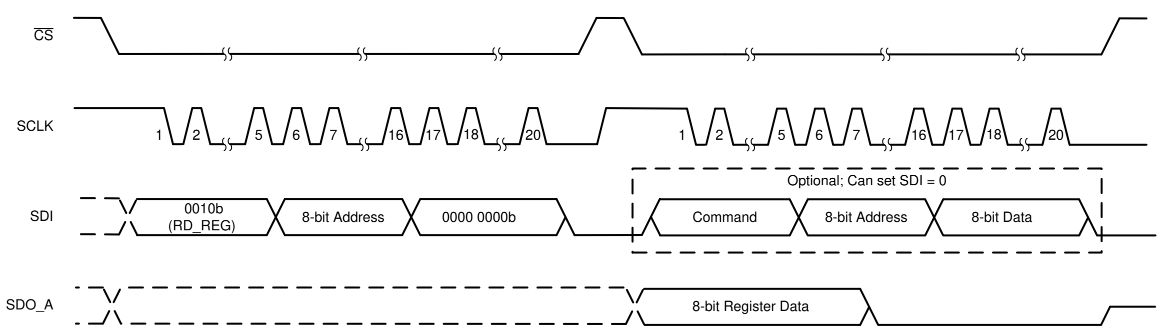


图 31. Register Read Operation

图 32 shows that for writing data to the register, one 20-bit frame is required. The frame contents are right-aligned. If a command frame is smaller than 20 bits, the contents of the command are discarded. If a frame has more than 20 bits, the last 20 bits are used to decode the operation. The 20-bit data on SDI consists of a 4-bit write command (0001b), set bit command (0011b), or clear bit command (0100b), an 8-bit register address, and 8-bit data. The write command is decoded on the $\overline{CS}$ rising edge and the specified register is updated with the 8-bit data specified during the register write operation.

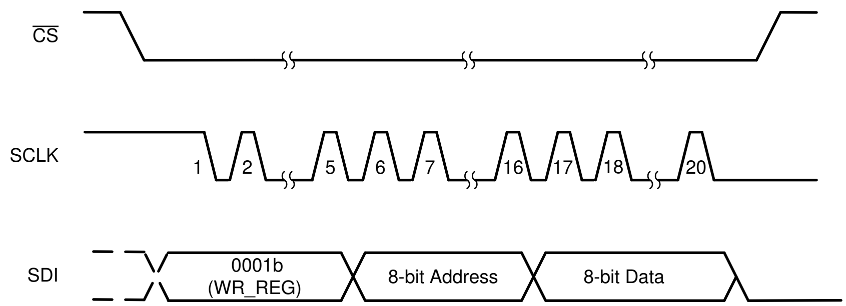


图 32. Register Write Operation

7.6 Register Map

7.6.1 ADS8355 Registers

Table 5 lists the ADS8355 registers. All register offset addresses not listed in Table 5 should be considered as reserved locations and the register contents should not be modified.

Table 5. ADS8355 Registers

Offset	Acronym	Register Name	Section
4h	PD_STANDBY	Power down configuration register	PD_STANDBY Register (Offset = 4h) [reset = 0h]
5h	PD_KEY	Power down key register	PD_KEY Register (Offset = 5h) [reset = 0h]
Dh	SDO_CTRL	SDO mode selection register	SDO_CTRL Register (Offset = Dh) [reset = 0h]
11h	DATA_OUT_CTRL	Output data format register	DATA_OUT_CTRL Register (Offset = 11h) [reset = 0h]
20h	REF_SEL	ADC reference selection register	REF_SEL Register (Offset = 20h) [reset = 0h]
24h	REFDAC_A_LSB	REFDACA configuration register (LSB)	REFDAC_A_LSB Register (Offset = 24h) [reset = 0h]
25h	REFDAC_A_MSB	REFDACA configuration register (MSB)	REFDAC_A_MSB Register (Offset = 25h) [reset = 0h]
26h	REFDAC_B_LSB	REFDACB configuration register (LSB)	REFDAC_B_LSB Register (Offset = 26h) [reset = 0h]
27h	REFDAC_B_MSB	REFDACB configuration register (MSB)	REFDAC_B_MSB Register (Offset = 27h) [reset = 0h]
28h	INPUT_CONFIG	Analog input configuration register	INPUT_CONFIG Register (Offset = 28h) [reset = 0h]

Complex bit access types are encoded to fit into small table cells. Table 6 shows the codes that are used for access types in this section.

Table 6. ADS8355 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		

Table 6. ADS8355 Access Type Codes (continued)

Access Type	Code	Description
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

7.6.1.1 PD_STANDBY Register (Offset = 4h) [reset = 0h]

PD_STANDBY is shown in Figure 33 and described in Table 7.

Return to the Summary Table.

Power down configuration register

Figure 33. PD_STANDBY Register

7	6	5	4	3	2	1	0
RESERVED					STANDBY	PD_EN	RESERVED
R-00000b					R/W-0b	R/W-0b	R-0b

Table 7. PD_STANDBY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	
2	STANDBY	R/W	0b	This bit enables partial powerdown of ADCs and internal oscillator , all other blocks are active 0b = Disable partial power down 1b = Enable partial power down
1	PD_EN	R/W	0b	This bit enables all blocks to powerdown except the interface and IO 0b = Disable power down 1b = Enable power down
0	RESERVED	R	0b	

7.6.1.2 PD_KEY Register (Offset = 5h) [reset = 0h]

PD_KEY is shown in Figure 34 and described in Table 8.

Return to the Summary Table.

Power down key register

Figure 34. PD_KEY Register

7	6	5	4	3	2	1	0
RESERVED				PD_WKEY[3:0]			
R-0000b				R/W-0000b			

Table 8. PD_KEY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	
3-0	PD_WKEY[3:0]	R/W	0000b	Writing 1001 to these bits enable register write operation to PD_STANDBY register.

7.6.1.3 SDO_CTRL Register (Offset = Dh) [reset = 0h]

SDO_CTRL is shown in Figure 35 and described in Table 9.

Return to the Summary Table.

SDO mode selection register

Figure 35. SDO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							SDO_MODE
R-0000000b							R/W-0b

Table 9. SDO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	
0	SDO_MODE	R/W	0b	This bit selects ADC to output data in either single SDO or Dual SDO mode. 0b = data out on both SDO_A and SDO_B 1b = data out on SDO_A only

7.6.1.4 DATA_OUT_CTRL Register (Offset = 11h) [reset = 0h]

DATA_OUT_CTRL is shown in Figure 36 and described in Table 10.

Return to the Summary Table.

Output data format register

Figure 36. DATA_OUT_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							OP_DATA_FORMAT
R-0000000b							R/W-0b

Table 10. DATA_OUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	
0	OP_DATA_FORMAT	R/W	0b	This bit selects ADC output data format. 0b = Straight Binary format 1b = 2's complements format

7.6.1.5 REF_SEL Register (Offset = 20h) [reset = 0h]

REF_SEL is shown in Figure 37 and described in Table 11.

Return to the Summary Table.

ADC reference selection register

Figure 37. REF_SEL Register

7	6	5	4	3	2	1	0
RESERVED							INT_EXT
R-0000000b							R/W-0b

Table 11. REF_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	
0	INT_EXT	R/W	0b	This bit selects ADC reference source. 0b = Device uses external reference for ADC conversion 1b = Device uses internal reference for ADC conversion

7.6.1.6 REFDAC_A_LSB Register (Offset = 24h) [reset = 0h]

REFDAC_A_LSB is shown in Figure 38 and described in Table 12.

Return to the Summary Table.

REFDACA configuration register (LSB)

Figure 38. REFDAC_A_LSB Register

7	6	5	4	3	2	1	0
REFDAC_A_LSB[7:0]							
R/W-00000000b							

Table 12. REFDAC_A_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REFDAC_A_LSB[7:0]	R/W	00000000b	Least significant byte to program the REFDAC_A. REFDAC_A _MSB and REFDAC_A_LSB in combination are used to set the internal reference for ADC_A. For 2.5V internal reference, program 0x1FF to REFDAC_A.

7.6.1.7 REFDAC_A_MSB Register (Offset = 25h) [reset = 0h]

REFDAC_A_MSB is shown in Figure 39 and described in Table 13.

Return to the Summary Table.

REFDACA configuration register (MSB)

Figure 39. REFDAC_A_MSB Register

7	6	5	4	3	2	1	0
RESERVED							REFDAC_A_MSB
R/W-00000000b							

Table 13. REFDAC_A_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	
0	REFDAC_A_MSB	R/W	0b	Most significant bit to program the REFDAC_A. REFDAC_A _MSB and REFDAC_A_LSB in combination are used to set the internal reference for ADC_A. For 2.5V internal reference, program 0x1FF to REFDAC_A.

7.6.1.8 REFDAC_B_LSB Register (Offset = 26h) [reset = 0h]

REFDAC_B_LSB is shown in Figure 40 and described in Table 14.

Return to the Summary Table.

REFDACB configuration register (LSB)

Figure 40. REFDAC_B_LSB Register

7	6	5	4	3	2	1	0
REFDAC_B_LSB[7:0]							
R/W-00000000b							

Table 14. REFDAC_B_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REFDAC_B_LSB[7:0]	R/W	00000000b	Least significant byte to program the REFDAC_B. REFDAC_B_MSB and REFDAC_B_LSB in combination are used to set the internal reference for ADC_B. For 2.5V internal reference, program 0x1FF to REFDAC_B.

7.6.1.9 REFDAC_B_MSB Register (Offset = 27h) [reset = 0h]

REFDAC_B_MSB is shown in Figure 41 and described in Table 15.

Return to the Summary Table.

REFDACB configuration register (MSB)

Figure 41. REFDAC_B_MSB Register

7	6	5	4	3	2	1	0
RESERVED							REFDAC_B_MSB
R/W-00000000b							

Table 15. REFDAC_B_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	
0	REFDAC_B_MSB	R/W	0b	Most significant bit to program the REFDAC_B. REFDAC_B _MSB and REFDAC_B_LSB in combination are used to set the internal reference for ADC_B. For 2.5V internal reference, program 0x1FF to REFDAC_B.

7.6.1.10 INPUT_CONFIG Register (Offset = 28h) [reset = 0h]

INPUT_CONFIG is shown in Figure 42 and described in Table 16.

Return to the Summary Table.

Analog input configuration register

Figure 42. INPUT_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED						RANGE_SEL	AINM_SEL
R-000000b						R/W-0b	R/W-0b

Table 16. INPUT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	
1	RANGE_SEL	R/W	0b	This bit selects ADC input full scale range 0b = ADC operates with full scale range of 0 to V_{REF} 1b = ADC operates with full scale range of 0 to 2 X V_{REF}

Table 16. INPUT_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AINM_SEL	R/W	0b	This bit selects ADC input configuration 0b = ADC operates in single-ended configuration. AINM pin must be connected to GND potential. 1b = ADC operates in pseudo-differential configuration. AINM pin must be connected to FSR / 2 potential.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, and some application circuits designed using these devices.

The device supports operation either with an internal or external reference source. See the *Reference* section for details about the decoupling requirements.

The reference source to the ADC must provide low-drift and very accurate DC voltage and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise (typically in the order of a few 100 μV_{RMS}) of the reference source must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred hertz. After band-limiting the noise from the reference source, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. At the start of each conversion, the reference buffer must regulate the voltage of the reference pin within 1 LSB of the intended value. This condition necessitates the use of a large filter capacitor at the reference pin of the ADC. The amplifier selected to drive the reference input pin must be stable while driving this large capacitor and must have low output impedance, low offset, and temperature drift specifications. To reduce the dynamic current requirements and crosstalk between the channels, a separate reference buffer is recommended for driving the reference input of each ADC channel.

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an charge kickback filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

8.1.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. Select the amplifier bandwidth as described in 公式 6 to maintain the overall stability of the input driver circuit:

$$Unity-Gain\ Bandwidth \geq 4 \times \left(\frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (6)$$

Application Information (接下页)

- *Noise.* Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, keep the total noise contribution from the front-end circuit below 20% of the input-referred noise of the ADC. 公式 7 calculates noise from the input driver circuit. This noise is band-limited by designing a low cutoff frequency RC filter:

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e^2_{n\_RMS} \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)}$$

where:

- V_{1/f_AMP_PP} = the peak-to-peak flicker noise in µV
- e_{n_RMS} = the amplifier broadband noise density in nV/√Hz
- f_{-3dB} = the 3-dB bandwidth of the RC filter
- N_G = the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration (7)

- *Distortion.* Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, the distortion of the input driver must be at least 10 dB lower than the distortion of the ADC, as shown in 公式 8, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit.

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \quad (8)$$

- *Settling Time.* For DC signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, always verify the settling behavior of the input driver with TINA™-SPICE simulations before selecting the amplifier.

8.1.2 Charge Kickback Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, charge kickback filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. A charge kickback filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For DC signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For AC signals, keep the filter bandwidth low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system.

A filter capacitor, C_{FLT}, connected across the ADC inputs (see 图 43), filters the noise from the front-end drive circuitry, reduces the sampling charge injection, and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor must be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of C_{FLT} must be greater than 400 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Application Information (接下页)

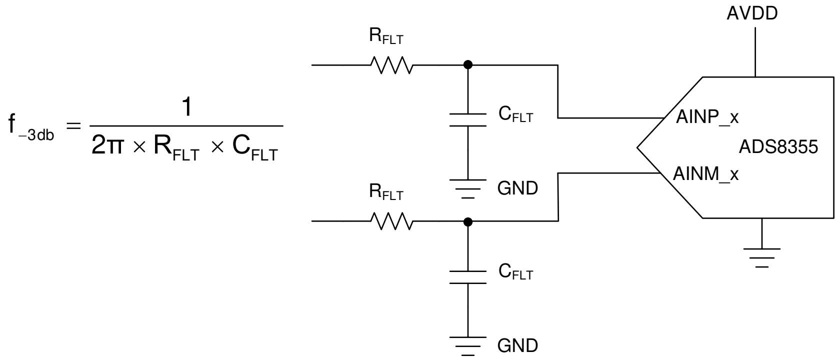
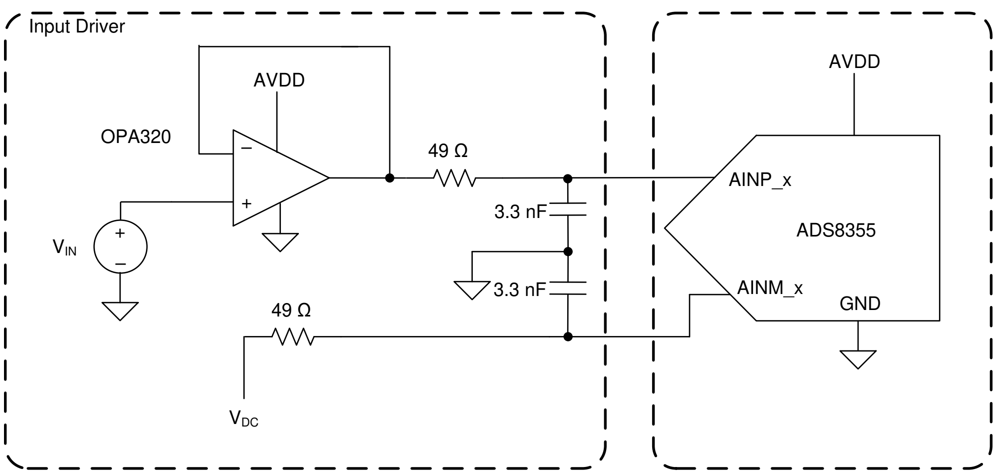


图 43. Charge Kickback Filter

Driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For more information on ADC input R-C filter component selection, see the TI Precision Labs on ti.com.

8.2 Typical Application



NOTE: Only one ADC channel is shown in this diagram. Replicate the same circuit for the other ADC channel.

图 44. DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at Full Throughput

Typical Application (接下页)

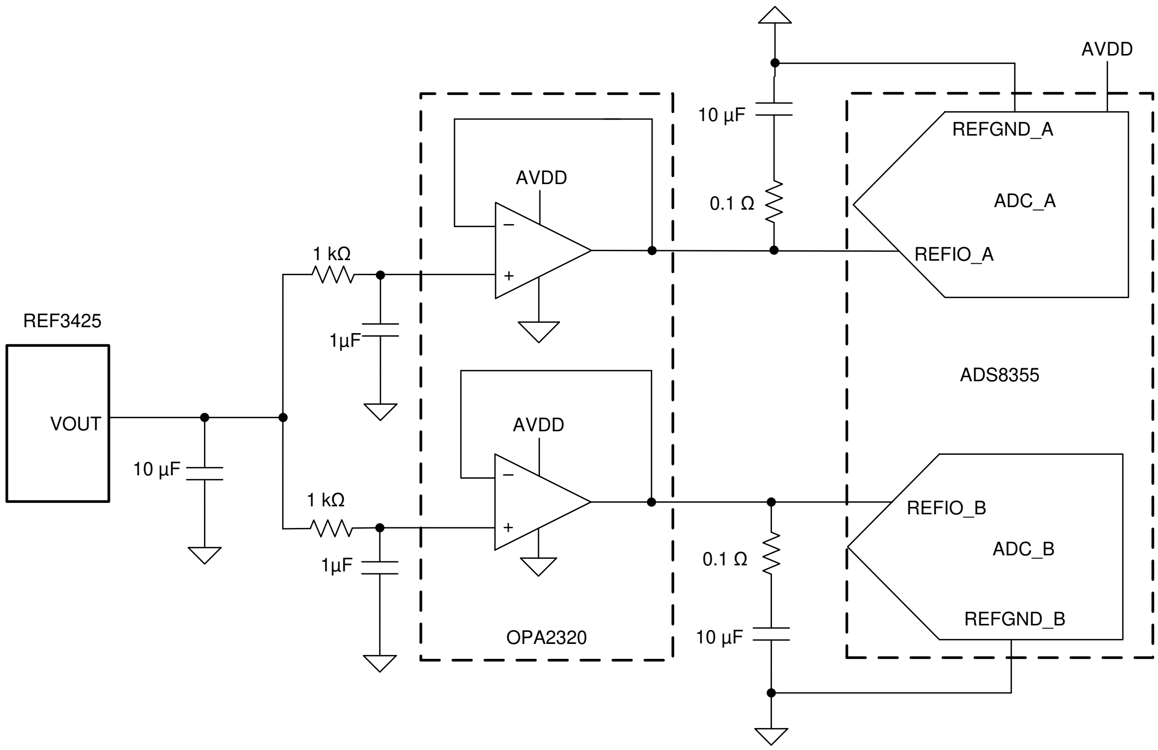


图 45. Reference Drive Circuit

8.2.1 Design Requirements

表 17 lists the target specifications for this application.

表 17. Target Specifications

TARGET SPECIFICATIONS	TEST CONDITIONS
> 83-dB SNR, < –95-dB THD	10-kHz input signal frequency, 1-MSPS throughput

8.2.2 Detailed Design Procedure

Best practice is for the distortion from the input driver to be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of rail-to-rail swing at the amplifier input. The low-power OPA320, used as an input driver, provides exceptional AC performance because of its extremely low-distortion and high-bandwidth specifications. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

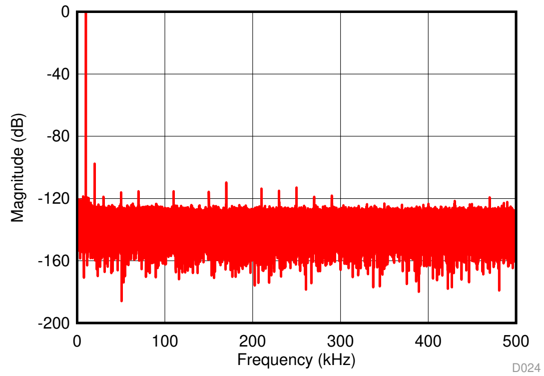
The application circuit illustrated in 图 44 is optimized to achieve the lowest distortion and lowest noise for a 10-kHz input signal fed to the ADS8355 operating at full throughput with the default dual-SDO interface mode. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the device.

图 45 illustrates the reference driver circuit when operation with an external reference is desired. The reference voltage is generated by the high-precision, low-noise REF3425 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10 µF. The low output impedance, low noise, and fast settling time make the OPA2320 a good choice for driving this high capacitive load.

8.2.3 Application Curve

To minimize external components and to maximize the dynamic range of the ADC, the device is configured to operate with an internal reference (REF_SEL register, INT_EXT bit = 1) and a 2 × V_{REF_x} input full-scale range (INPUT_CONFIG register, RANGE_SEL bit = 1). The REFDAC_x registers are programmed to 0x1FFh to program the internal reference to 2.5 V.

图 46 shows the FFT plot and test result obtained with the ADS8355 operating at full throughput with a dual-SDO interface and the circuit configuration of 图 44.



SNR = 86.38 dB, THD = –97.24 dB, f_{IN} = 10 kHz

图 46. The ADS8355 in Dual-SDO Interface Mode

9 Power Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges.

When using the device with the 2 × V_{REF} input range (INPUT_CONFIG register, RANGE_SEL bit = 1), the AVDD supply voltage value defines the permissible voltage swing on the analog input pins. AVDD must be set as described in 公式 3 and 公式 4 to avoid saturation of output codes and to use the full dynamic range on the analog input pins.

Decouple the AVDD and DVDD pins, as shown in 图 47, with the GND pin using individual 10-µF decoupling capacitors.

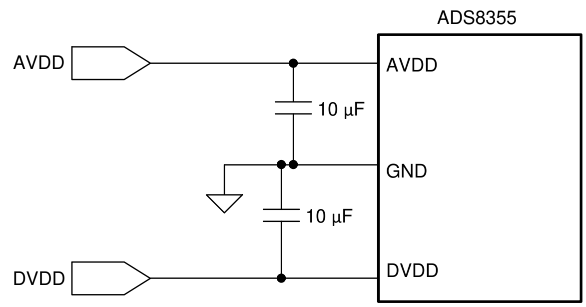


图 47. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

图 48 provides a board layout example for the device WQFN package. Partition the printed circuit board (PCB) into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As illustrated in 图 48, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the device must be clean and well-bypassed. Use 10-µF, ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low impedance paths.

The REFIO_A and REFIO_B reference inputs and outputs are bypassed with 10-µF, X7R-grade, 0805-size, 16-V rated ceramic capacitors (C_{REF_x}). Place the reference bypass capacitors as close as possible to the reference REFIO_x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIO_x pins and the bypass capacitors.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

10.2 Layout Example

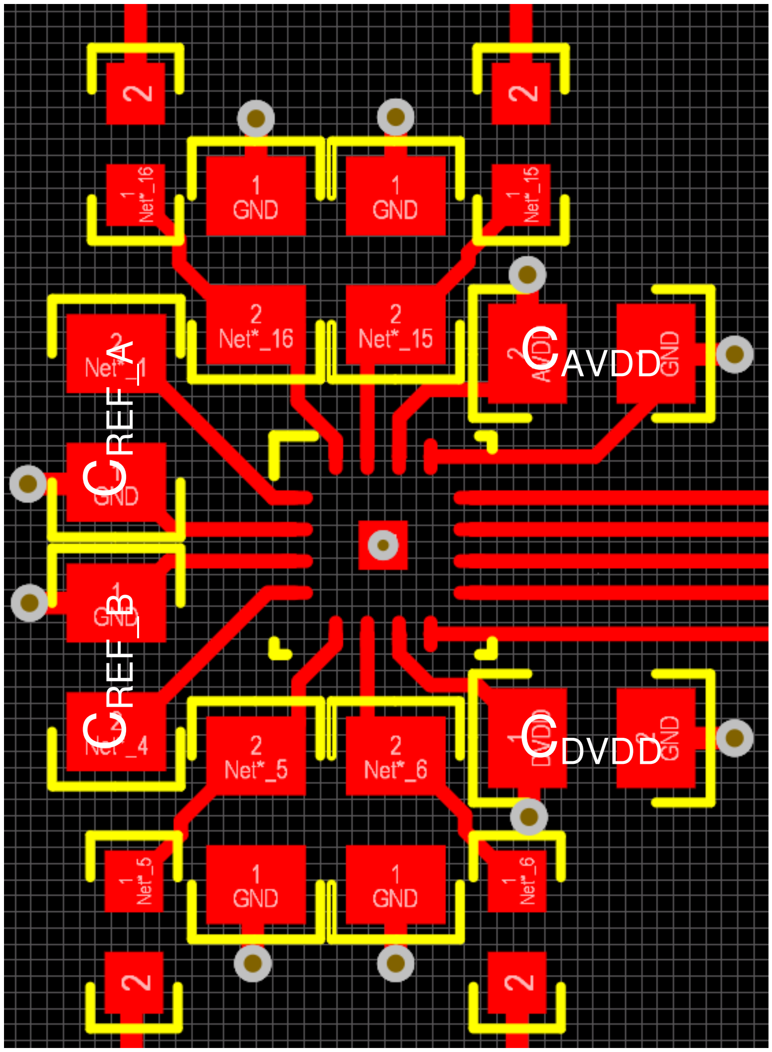


图 48. Recommended Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

德州仪器 (TI)，TI 高精度实验室

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《具有关断功能的 OPAx320x 高精度 20MHz、0.9pA、低噪声 RRIO CMOS 运算放大器》* 数据表
- 德州仪器 (TI)，*《REF34xx 低漂移、低功耗、小封装串联电压基准》* 数据表

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 商标

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11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8355IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8355	Samples
ADS8355IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8355	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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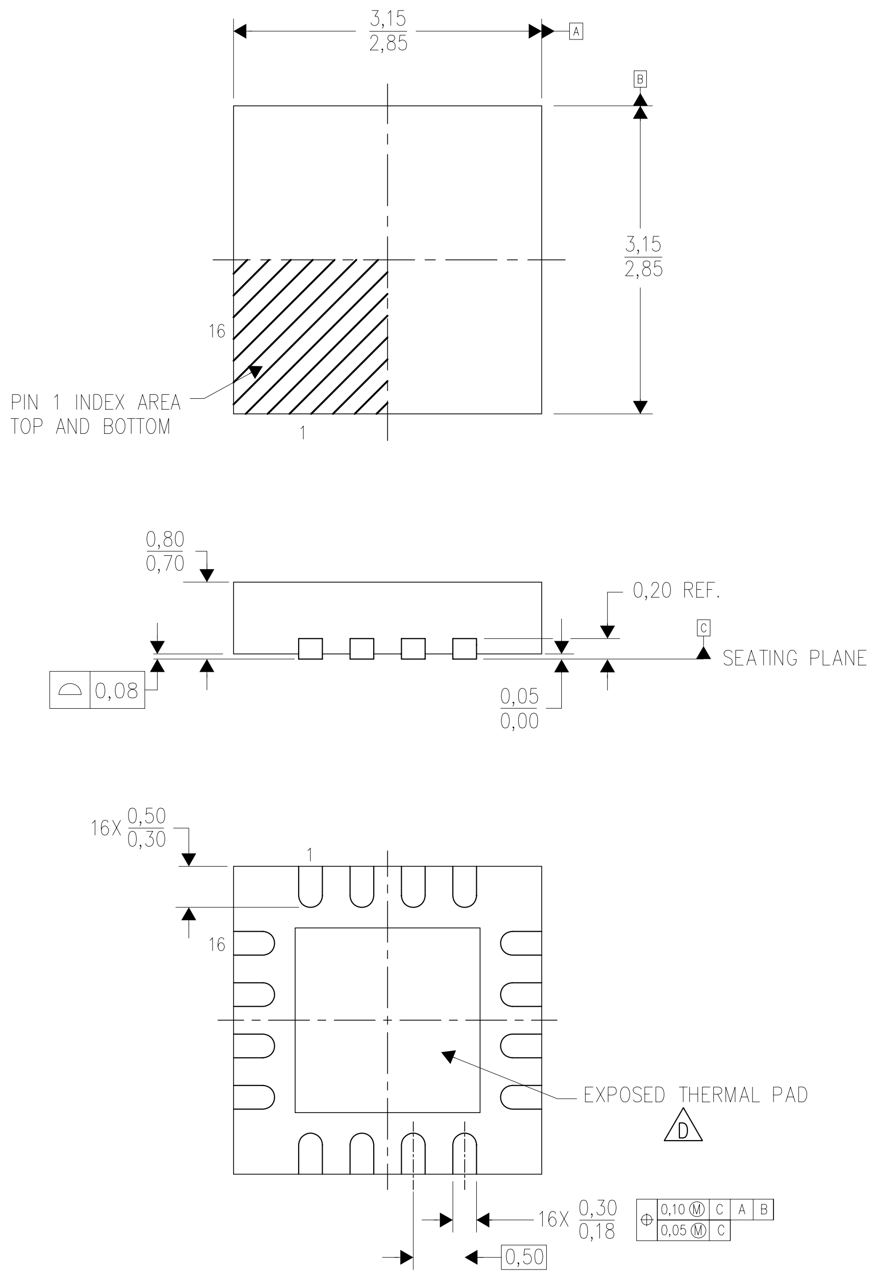
RTE (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



4205254/D 01/11

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-220.

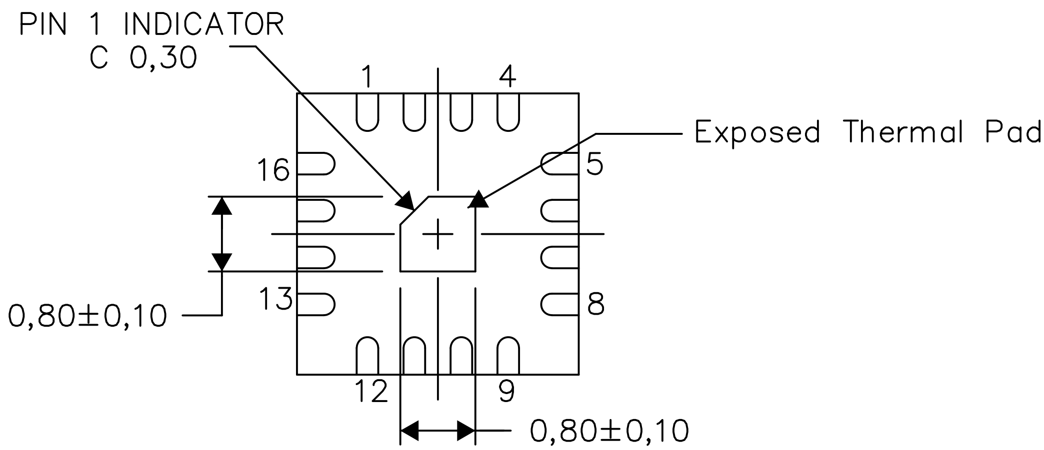
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



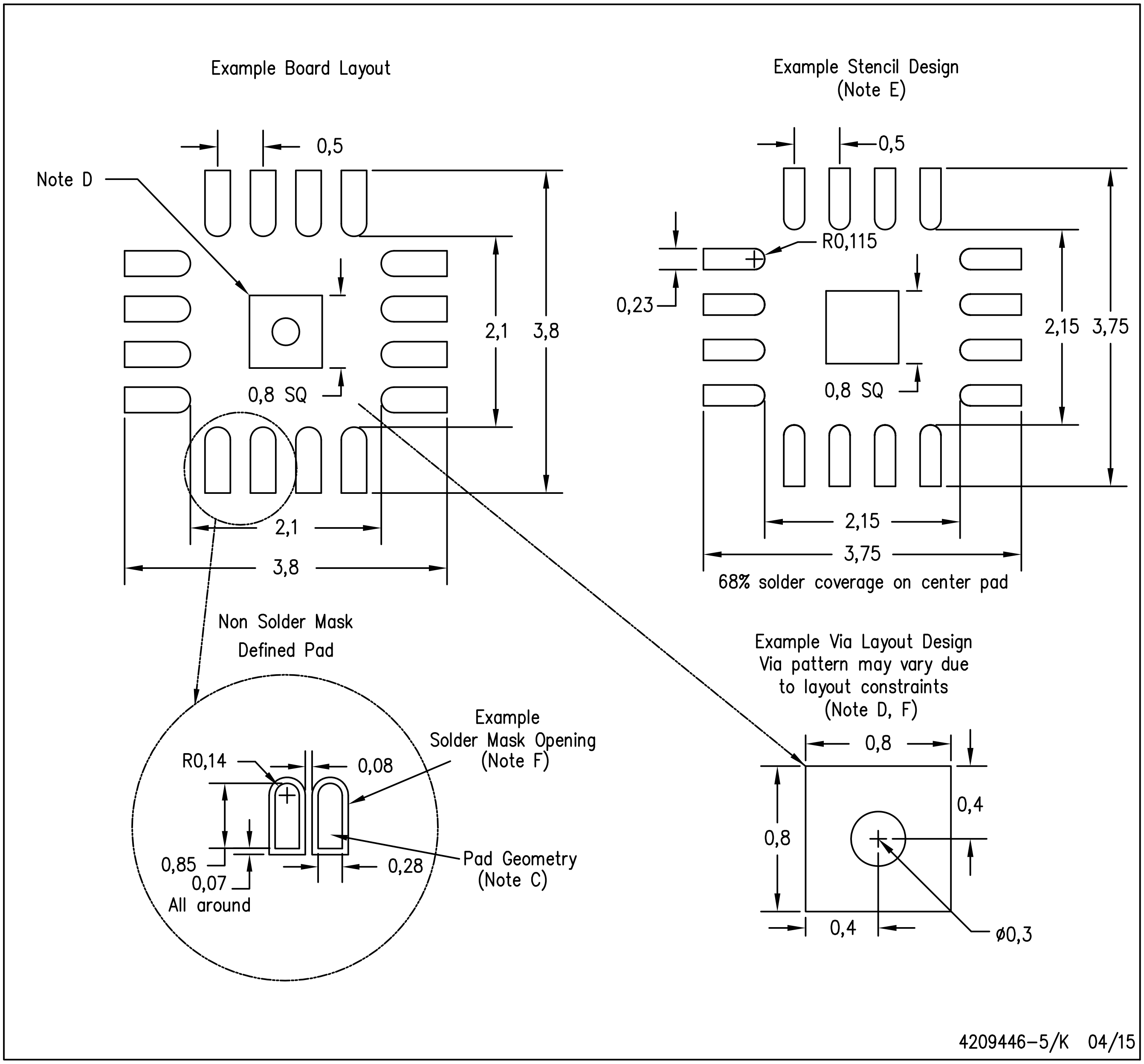
Bottom View

Exposed Thermal Pad Dimensions

4206446–5/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

重要声明和免责声明

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