

ADS41xx 14、12 位、65MSPS 或 125MSPS 超低功耗 ADC

1 特性

- 超低功耗，采用 1.8V 单电源：
 - 65MSPS 时的总功耗为 103mW
 - 125MSPS 时的总功耗为 153mW
- 高动态性能：
 - 信噪比 (SNR): 170MHz 时为 72.2dBFS
 - 无杂散动态范围 (SFDR): 170MHz 时为 81dBc
- 随采样速率动态地进行功率调节
- 空闲通道 SNR 74.8 dBFS (ADS414x)
- 输出接口：
 - 支持可编程摆幅和强度的双倍数据速率 (DDR) LVDS:
 - 标准摆幅: 350mV
 - 低摆幅: 200mV
 - 默认信号强度: 100Ω 端接
 - 2x 强度: 50Ω 端接
 - 还支持 1.8V 平行 CMOS 接口
- 用于 SNR、SFDR 权衡的最高 6dB 可编程增益
- 直流偏移校正
- 支持低至 200mV_{pp} 的输入时钟幅度

2 应用

- 无线通信基础设施
- 软件定义的无线电
- 功率放大器线性化
- 成像系统

3 说明

ADS412x 和 ADS414x 器件是 ADS41xx 系列模数转换器 (ADC) 中采样速度较低的型号。该器件凭借创新设计技术实现了高动态性能，并且采用 1.8V 电源供电运行，功耗极低。它们非常适合于多载波、高带宽通信应用。

ADS412x 和 ADS414x 器件具有精细增益选项，可用于提升在较小满量程输入范围内的 SFDR 性能，特别是高输入频率条件下。这些器件包括一个 DC 偏移校正环路，可以用来消除 ADC 偏移。在较低的采样速率条件下，ADC 自动以低功耗运行，且没有性能损失。

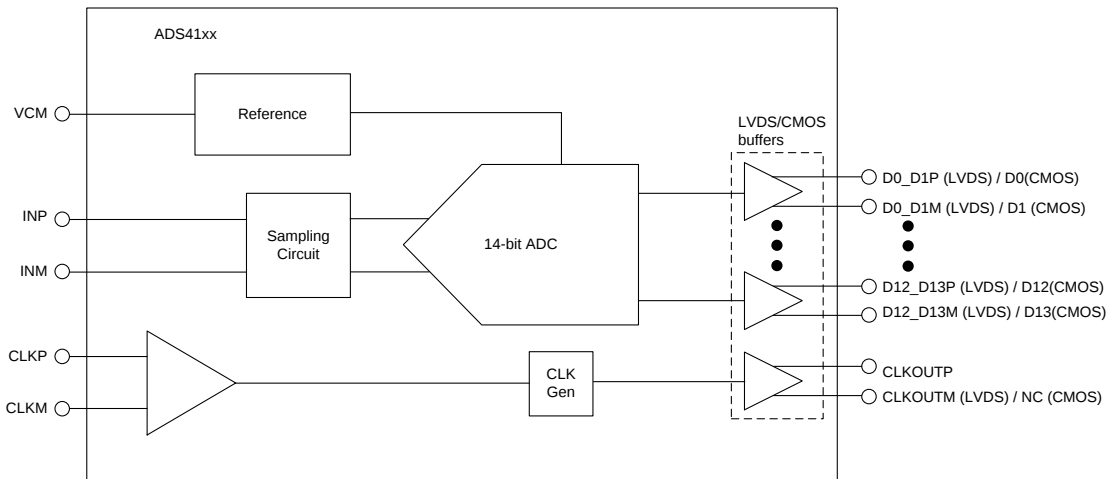
ADS412x 和 ADS414x 器件采用紧凑型 VQFN-48 封装，额定温度涵盖了工业温度范围（-40°C 至 +85°C）。

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
ADS4122	VQFN (48)	7.00mm x 7.00mm
ADS4125		
ADS4142		
ADS4145		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

ADS41xx 方框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (January 2016) to Revision C	Page
• 已添加 在 特性 部分中添加了新特性空闲通道 SNR 74.8 dBFS (ADS414x)	1
• 已添加 在 应用 部分中添加了 成像系统 应用	1
• 已更改 将 ADS412x/4x 更改为 ADS412x 和 ADS414x （在 说明 部分中）	1
• 已更改 更改了第一页中的 ADS41xx 方框图 。	1
• Changed input clock sample rate minimum for the ADS4122/ADS4142, low-speed mode enabled by default from: 20 MSPS to: 3 MSPS	8
• Changed input clock sample rate minimum for the ADS4122/ADS4142, low-speed mode enabled from: 20 MSPS to: 3 MSPS	8
• Deleted <i>High Performance Modes</i> section from <i>Recommended Operating Conditions</i> table, moved to <i>Programming</i> section	8
• Added <i>order</i> to HD2 and HD3 parameter names in <i>Electrical Characteristics</i> tables	10
• Added test conditions header to <i>Electrical Characteristics: General</i> table	13
• Added <i>Using the ADS41xx at Low Sampling Rates</i> subsection in <i>Application and Implementation</i> section	62
• Added Figure 114 to Figure 124 in ADS412x (12-Bit Device) section	62
• Changed the order of figures in ADS412x (12-Bit Device) section.	62
• Added the device name ADS412x to the conditions of ADS412x (12-Bit Device) section.	62
• Changed the unit of f_s from MHz to MSPS in the specifications of Figure 115	62
• Added new subsection ADS412x (12-Bit Device) in <i>Application Information</i> section.	62

修订历史记录 (接下页)

• Changed the unit of f_s from MHz to MSPS in the specifications of Figure 116	62
• Changed the unit of f_s from MHz to MSPS in the specifications of Figure 119	63
• Changed the unit of f_s from MHz to MSPS in the specifications of Figure 120	63
• Changed the unit of f_s from MHz to MSPS in the specifications of Figure 121	63
• Changed the unit of f_s from MHz to MSPS in the specifications of Figure 122	63
• Added Figure 125 through Figure 128 in typical performance at lower sampling rate for ADS412x (12-bit devices) in CMOS interface mode.	64
• Added Figure 129 through Figure 130 in typical performance at lower sampling rate for ADS412x (12-bit devices) in CMOS interface mode.	64
• Added Figure 131 through Figure 132 in typical performance at lower sampling rate for ADS412x (12-bit devices) in CMOS interface mode.	65
• Added Figure 136 to Figure 146 in ADS414x (14-Bit Device) section	66
• Changed the order of figures in ADS414x (14-Bit Device) section.	66
• Added the device name ADS414x to the conditions of ADS414x (14-Bit Device) section.	66
• Changed the unit of f_s from MHz to MSPS in the specifications of Figure 137 and Figure 138	66
• Added new subsection ADS414x (14-Bit Device) in <i>Application Information</i> section.	66
• Changed the SNR and SINAD values of Figure 138	66
• Changed the unit of f_s from MHz to MSPS in the specifications of Figure 141 through Figure 144	66
• Added Figure 147 through Figure 157 in typical performance at lower sampling rate for ADS414x (14-bit devices) in CMOS interface mode.	67
• Added Figure 151 through Figure 158 in typical performance at lower sampling rate for ADS414x (14-bit devices) in CMOS interface mode.	68
• Added Figure 153 through Figure 155 in typical performance at lower sampling rate for ADS414x (14-bit devices) in CMOS interface mode.	68
• Added <i>Output Timing at Low Sampling Rates</i> subsection in <i>Application and Implementation</i> section	71
• Changed the name of the header from ADS4128 CAPABILITY to ADS4125 CAPABILITY in the last column of Table 25	72
• 已添加 接收文档更新通知部分	78

Changes from Revision A (March 2011) to Revision B

Page

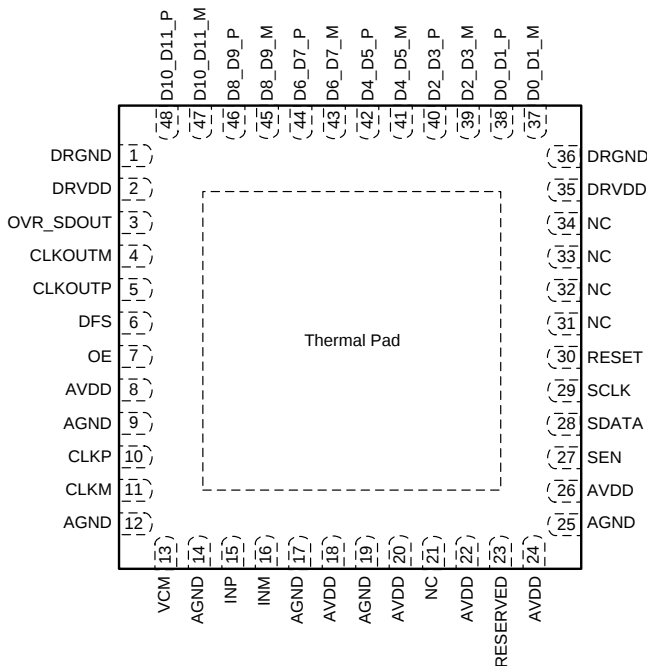
• 已添加 引脚配置和功能部分, 处理额定值表, 特性 描述部分, 器件功能模式, 应用和实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分	1
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5 Device Family Comparison

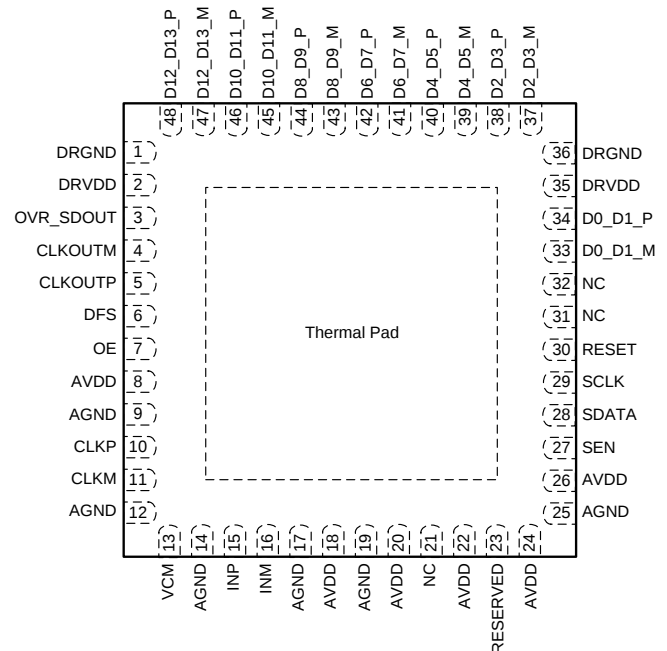
FAMILY	65 MSPS	125 MSPS	160 MSPS	250 MSPS	WITH ANALOG INPUT BUFFERS	
					200 MSPS	250 MSPS
ADS412x, 12-bit family	ADS4122	ADS4125	ADS4126	ADS4129	—	ADS41B29
ADS414x, 14-bit family	ADS4142	ADS4145	ADS4146	ADS4149	—	ADS41B49
9-Bit	—	—	—	—	—	ADS58B19
11-Bit	—	—	—	—	ADS58B18	—

6 Pin Configuration and Functions

ADS412x RGZ Package
48-Pin VQFN With Exposed Thermal Pad
LVDS Mode - Top View



ADS414x RGZ Package
48-Pin VQFN With Exposed Thermal Pad
LVDS Mode - Top View



The thermal pad is connected to DRGND.

Pin Functions: LVDS Mode

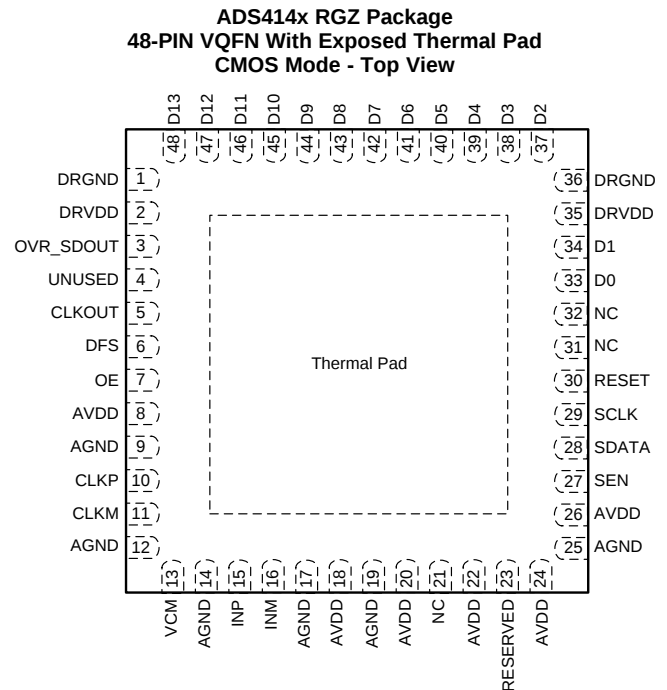
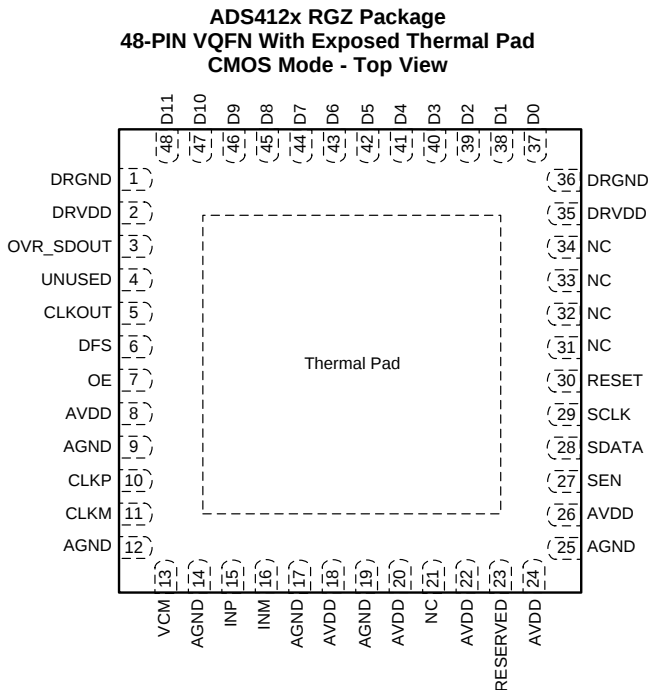
NAME	PIN		I/O	DESCRIPTION
	ADS412x	ADS414x		
AGND	9, 12, 14, 17, 19, 25	9, 12, 14, 17, 19, 25	I	Analog ground
AVDD	8, 18, 20, 22, 24, 26	8, 18, 20, 22, 24, 26	I	1.8-V analog power supply
CLKM	11	11	I	Differential clock input, complement
CLKP	10	10	I	Differential clock input, true
CLKOUTM	4	4	O	Differential output clock, complement
CLKOUTP	5	5	O	Differential output clock, true
D0_D1_M	37	33	O	Differential output data D0 and D1 multiplexed, complement
D0_D1_P	38	34	O	Differential output data D0 and D1 multiplexed, true
D2_D3_M	39	37	O	Differential output data D2 and D3 multiplexed, complement
D2_D3_P	40	38	O	Differential output data D2 and D3 multiplexed, true
D4_D5_M	41	39	O	Differential output data D4 and D5 multiplexed, complement
D4_D5_P	42	40	O	Differential output data D4 and D5 multiplexed, true

Pin Functions: LVDS Mode (continued)

NAME	PIN		I/O	DESCRIPTION
	ADS412x	ADS414x		
D6_D7_M	43	41	O	Differential output data D6 and D7 multiplexed, complement
D6_D7_P	44	42	O	Differential output data D6 and D7 multiplexed, true
D8_D9_M	45	43	O	Differential output data D8 and D9 multiplexed, complement
D8_D9_P	46	44	O	Differential output data D8 and D9 multiplexed, true
D10_D11_M	47	45	O	Differential output data D10 and D11 multiplexed, complement
D10_D11_P	48	46	O	Differential output data D10 and D11 multiplexed, true
D12_D13_M	—	47	O	Differential output data D12 and D13 multiplexed, complement
D12_D13_P	—	48	O	Differential output data D12 and D13 multiplexed, true
DFS	6	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS, CMOS output interface type. See Table 5 for detailed information.
DRGND	1, 36, PAD	1, 36, PAD	I	Digital and output buffer ground
DRVDD	2, 35	2, 35	I	1.8-V digital and output buffer supply
INM	16	16	I	Differential analog input, negative
INP	15	15	I	Differential analog input, positive
NC	21, 31, 32, 33, 34	21, 31, 32	—	Do not connect
OE	7	7	I	Output buffer enable input, active high; this pin has an internal 180-k Ω pullup resistor to DRVDD.
OVR_SDOUT	3	3	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1.
RESERVED	23	23	I	Digital control pin, reserved for future use
RESET	30	30	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; see the Serial Interface section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180-k Ω pulldown resistor.
SCLK	29	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180-k Ω pulldown resistor.
SDATA	28	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 7). This pin has an internal 180-k Ω pulldown resistor.
SEN	27	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and must be tied to AVDD. This pin has an internal 180-k Ω pullup resistor to AVDD.
VCM	13	13	O	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.

ADS4122, ADS4125, ADS4142, ADS4145

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The thermal pad is connected to DRGND.

Pin Functions: CMOS Mode

NAME	PIN		I/O	DESCRIPTION
	ADS412x	ADS414x		
AVDD	8, 18, 20, 22, 24, 26	8, 18, 20, 22, 24, 26	I	1.8-V analog power supply
AGND	9, 12, 14, 17, 19, 25	9, 12, 14, 17, 19, 25	I	Analog ground
CLKM	11	11	I	Differential clock input, complement
CLKP	10	10	I	Differential clock input, true
CLKOUT	5	5	O	CMOS output clock
D0	37	33	O	12-bit, 14-bit CMOS output data
D1	38	34	O	12-bit, 14-bit CMOS output data
D2	39	37	O	12-bit, 14-bit CMOS output data
D3	40	38	O	12-bit, 14-bit CMOS output data
D4	41	39	O	12-bit, 14-bit CMOS output data
D5	42	40	O	12-bit, 14-bit CMOS output data
D6	43	41	O	12-bit, 14-bit CMOS output data
D7	44	42	O	12-bit, 14-bit CMOS output data
D8	45	43	O	12-bit, 14-bit CMOS output data
D9	46	44	O	12-bit, 14-bit CMOS output data
D10	47	45	O	12-bit, 14-bit CMOS output data
D11	48	46	O	12-bit, 14-bit CMOS output data
D12	—	47	O	12-bit, 14-bit CMOS output data
D13	—	48	O	12-bit, 14-bit CMOS output data
DFS	6	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS, CMOS output interface type. See Table 5 for detailed information.
DRGND	1, 36, PAD	1, 36, PAD	I	Digital and output buffer ground
DRVDD	2, 35	2, 35	I	1.8-V digital and output buffer supply
INM	16	16	I	Differential analog input, negative
INP	15	15	I	Differential analog input, positive
NC	21, 31, 32, 33, 34	21, 31, 32	—	Do not connect

Pin Functions: CMOS Mode (continued)

PIN			I/O	DESCRIPTION
NAME	ADS412x	ADS414x		
OE	7	7	I	Output buffer enable input, active high; this pin has an internal 180-k Ω pullup resistor to DRVDD.
OVR_SDOUT	3	3	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1.
RESERVED	23	23	I	Digital control pin, reserved for future use
RESET	30	30	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; see the Serial Interface section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180-k Ω pulldown resistor.
SCLK	29	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and must be tied to ground. This pin has an internal 180-k Ω pulldown resistor.
SDATA	28	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 7). This pin has an internal 180-k Ω pulldown resistor.
SEN	27	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and must be tied to AVDD. This pin has an internal 180-k Ω pullup resistor to AVDD.
UNUSED	4	4	–	Unused pin in CMOS mode
VCM	13	13	O	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, AVDD		–0.3	2.1	V
Supply voltage, DRVDD		–0.3	2.1	V
Voltage between AGND and DRGND		–0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		0	2.1	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		0	2.1	V
Voltage applied to input pins	INP, INM	–0.3	minimum (1.9, AVDD + 0.3)	V
	CLKP, CLKM ⁽²⁾ , DFS, OE	–0.3	AVDD + 0.3	
	RESET, SCLK, SDATA, SEN	–0.3	3.9	
Operating free-air temperature, T _A		–40	85	°C
Operating junction temperature, T _J			125	°C
Storage temperature, T _{stg}		–65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3 V|. This prevents the ESD protection diodes at the clock input pins from turning on.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	NOM	MAX	UNIT
SUPPLIES					
AVDD	Analog supply voltage	1.7	1.8	1.9	V
DRVDD	Digital supply voltage	1.7	1.8	1.9	V
ANALOG INPUTS					
Differential input voltage ⁽¹⁾		2			V _{PP}
Input common-mode voltage		V _{CM} ± 0.05			V
Maximum analog input frequency with 2-V _{PP} input amplitude ⁽²⁾		400			MHz
Maximum analog input frequency with 1-V _{PP} input amplitude ⁽²⁾		800			MHz
CLOCK INPUT					
Input clock sample rate	ADS4122, ADS4142, low-speed mode enabled by default	3	65		MSPS
	ADS4125, ADS4145, low-speed mode enabled	3	80		
	ADS4125, ADS4145, low-speed mode disabled	> 80	125		
Input clock amplitude differential (V _{CLKP} – V _{CLKM})	Sine wave, ac-coupled	0.2	1.5		V _{PP}
	LVPECL, ac-coupled		1.6		
	LVDS, ac-coupled		0.7		
	LVC MOS, single-ended, ac-coupled		1.8		V
Input clock duty cycle	Low-speed enabled	40%	50%	60%	
	Low-speed disabled	35%	50%	65%	
DIGITAL OUTPUTS					
C _{LOAD}	Maximum external load capacitance from each output pin to DRGND	5			pF
R _{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)	100			Ω
T _A	Operating free-air temperature	–40			85 °C

- (1) With 0-dB gain. See the [Gain for SFDR, SNR Trade-Off](#) section in the [Application Information](#) for the relationship between input voltage range and gain.
- (2) See the [Application Information](#) section.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ADS412x, ADS414x	UNIT
		RGZ (VQFN)	
		48 PIN	
R _{θJA}	Junction-to-ambient thermal resistance	29	°C/W
R _{θJTop}	Junction-to-case (top) thermal resistance	N/A	°C/W
R _{θJB}	Junction-to-board thermal resistance	10	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	9	°C/W
R _{θJBot}	Junction-to-case (bottom) thermal resistance	1.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics: ADS412x

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution						12	Bits
SNR	Signal-to-noise ratio, LVDS	f _{IN} = 10 MHz	ADS4122 (65 MSPS)		71.1		dBFS
			ADS4125 (125 MSPS)		71		
		f _{IN} = 70 MHz	ADS4122 (65 MSPS)		70.9		
			ADS4125 (125 MSPS)		70.8		
		f _{IN} = 100 MHz	ADS4122 (65 MSPS)		70.7		
			ADS4125 (125 MSPS)		70.6		
		f _{IN} = 170 MHz	ADS4122 (65 MSPS)	67	70.2		
			ADS4125 (125 MSPS)	68	70.1		
		f _{IN} = 300 MHz	ADS4122 (65 MSPS)		68.8		
			ADS4125 (125 MSPS)		69.6		
SINAD	Signal-to-noise and distortion ratio, LVDS	f _{IN} = 10 MHz	ADS4122 (65 MSPS)		70.8		dBFS
			ADS4125 (125 MSPS)		70.7		
		f _{IN} = 70 MHz	ADS4122 (65 MSPS)		70.8		
			ADS4125 (125 MSPS)		70.7		
		f _{IN} = 100 MHz	ADS4122 (65 MSPS)		70.6		
			ADS4125 (125 MSPS)		70.3		
		f _{IN} = 170 MHz	ADS4122 (65 MSPS)	66	70.1		
			ADS4125 (125 MSPS)	67	69.8		
		f _{IN} = 300 MHz	ADS4122 (65 MSPS)		68		
			ADS4125 (125 MSPS)		69		
SFDR	Spurious-free dynamic range	f _{IN} = 10 MHz	ADS4122 (65 MSPS)		86.5		dBc
			ADS4125 (125 MSPS)		86		
		f _{IN} = 70 MHz			86		
					86		
		f _{IN} = 100 MHz	ADS4122 (65 MSPS)		87		
			ADS4125 (125 MSPS)		82		
		f _{IN} = 170 MHz	ADS4122 (65 MSPS)	70	85		
			ADS4125 (125 MSPS)	71	81		
		f _{IN} = 300 MHz	ADS4122 (65 MSPS)		72.5		
			ADS4125 (125 MSPS)		77		
THD	Total harmonic distortion	f _{IN} = 10 MHz	ADS4122 (65 MSPS)		82.5		dBc
			ADS4125 (125 MSPS)		82		
		f _{IN} = 70 MHz	ADS4122 (65 MSPS)		84		
			ADS4125 (125 MSPS)		83.5		
		f _{IN} = 100 MHz	ADS4122 (65 MSPS)		84		
			ADS4125 (125 MSPS)		80.5		
		f _{IN} = 170 MHz	ADS4122 (65 MSPS)	69.5	81		
			ADS4125 (125 MSPS)	69.5	79.5		
		f _{IN} = 300 MHz	ADS4122 (65 MSPS)		72		
			ADS4125 (125 MSPS)		75.5		

Electrical Characteristics: ADS412x (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD2	Second-order harmonic distortion	f _{IN} = 10 MHz			87		dBc
		f _{IN} = 70 MHz	ADS4122 (65 MSPS)		88		
			ADS4125 (125 MSPS)		86		
		f _{IN} = 100 MHz	ADS4122 (65 MSPS)		88		
			ADS4125 (125 MSPS)		82		
		f _{IN} = 170 MHz	ADS4122 (65 MSPS)	70	86		
			ADS4125 (125 MSPS)	71	83		
		f _{IN} = 300 MHz	ADS4122 (65 MSPS)		72.5		
			ADS4125 (125 MSPS)		77		
HD3	Third-order harmonic distortion	f _{IN} = 10 MHz	ADS4122 (65 MSPS)		86.5		dBc
			ADS4125 (125 MSPS)		86		
		f _{IN} = 70 MHz	ADS4122 (65 MSPS)		86		
			ADS4125 (125 MSPS)		88		
		f _{IN} = 100 MHz	ADS4122 (65 MSPS)		87		
			ADS4125 (125 MSPS)		85		
		f _{IN} = 170 MHz	ADS4122 (65 MSPS)	70	85		
			ADS4125 (125 MSPS)	71	81		
	Worst spur (other than second and third harmonics)	f _{IN} = 10 MHz	ADS4122 (65 MSPS)		96		dBc
			ADS4125 (125 MSPS)		95		
		f _{IN} = 70 MHz	ADS4122 (65 MSPS)		96		
			ADS4125 (125 MSPS)		95		
		f _{IN} = 100 MHz	ADS4122 (65 MSPS)		94		
			ADS4125 (125 MSPS)		95		
		f _{IN} = 170 MHz	ADS4122 (65 MSPS)	76.5	92		
			ADS4125 (125 MSPS)	76.5	91		
IMD	Two-tone intermodulation distortion	f ₁ = 100 MHz, f ₂ = 105 MHz, each tone at –7 dBFS			90		dBFS
					87.5		
	Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine-wave input			1		Clock cycles
PSRR	AC power-supply rejection ratio	For 100-mV _{PP} signal on AVDD supply, up to 10 MHz			> 30		dB
ENOB	Effective number of bits	f _{IN} = 170 MHz			11.2		LSBs
DNL	Differential nonlinearity	f _{IN} = 170 MHz			–0.85	±0.2	1.5
INL	Integrated nonlinearity	f _{IN} = 170 MHz	ADS4122 (65 MSPS)		±0.3	3.5	LSBs
			ADS4125 (125 MSPS)		±0.35	3.5	

7.6 Electrical Characteristics: ADS414x

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution						14	Bits
SNR	Signal-to-noise ratio, LVDS	f _{IN} = 10 MHz	ADS4142 (65 MSPS)		73.9		dBFS
			ADS4145 (125 MSPS)		73.7		
		f _{IN} = 70 MHz	ADS4142 (65 MSPS)		73.5		
			ADS4145 (125 MSPS)		73.4		
		f _{IN} = 100 MHz	ADS4142 (65 MSPS)		73.2		
			ADS4145 (125 MSPS)		73.1		
		f _{IN} = 170 MHz	ADS4142 (65 MSPS)	69	72.4		
			ADS4145 (125 MSPS)	70	72.2		
		f _{IN} = 300 MHz	ADS4142 (65 MSPS)		70.5		
			ADS4145 (125 MSPS)		71.3		
SINAD	Signal-to-noise and distortion ratio, LVDS	f _{IN} = 10 MHz	ADS4142 (65 MSPS)		73.5		dBFS
			ADS4145 (125 MSPS)		73.2		
		f _{IN} = 70 MHz	ADS4142 (65 MSPS)		73.3		
			ADS4145 (125 MSPS)		73		
		f _{IN} = 100 MHz	ADS4142 (65 MSPS)		73		
			ADS4145 (125 MSPS)		72.6		
		f _{IN} = 170 MHz	ADS4142 (65 MSPS)	68	72.3		
			ADS4145 (125 MSPS)	69	71.8		
		f _{IN} = 300 MHz	ADS4142 (65 MSPS)		69.2		
			ADS4145 (125 MSPS)		70.6		
SFDR	Spurious-free dynamic range	f _{IN} = 10 MHz	ADS4142 (65 MSPS)		87		dBc
			ADS4145 (125 MSPS)		86		
		f _{IN} = 70 MHz	ADS4142 (65 MSPS)		86.5		
			ADS4145 (125 MSPS)		85.5		
		f _{IN} = 100 MHz	ADS4142 (65 MSPS)		87		
			ADS4145 (125 MSPS)		82		
		f _{IN} = 170 MHz	ADS4142 (65 MSPS)	71	85		
			ADS4145 (125 MSPS)	72.5	81.5		
		f _{IN} = 300 MHz	ADS4142 (65 MSPS)		72.5		
			ADS4145 (125 MSPS)		77		
THD	Total harmonic distortion	f _{IN} = 10 MHz	ADS4142 (65 MSPS)		84		dBc
			ADS4145 (125 MSPS)		83		
		f _{IN} = 70 MHz	ADS4142 (65 MSPS)		84		
			ADS4145 (125 MSPS)		83.5		
		f _{IN} = 100 MHz	ADS4142 (65 MSPS)		84		
			ADS4145 (125 MSPS)		81		
		f _{IN} = 170 MHz	ADS4142 (65 MSPS)	69.5	82.5		
			ADS4145 (125 MSPS)	70.5	80		
		f _{IN} = 300 MHz	ADS4142 (65 MSPS)		72.5		
			ADS4145 (125 MSPS)		75.5		

Electrical Characteristics: ADS414x (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD2	Second-order harmonic distortion	f _{IN} = 10 MHz	ADS4142 (65 MSPS)		88		dBc
			ADS4145 (125 MSPS)		87		
		f _{IN} = 70 MHz	ADS4142 (65 MSPS)		87		
			ADS4145 (125 MSPS)		85.5		
		f _{IN} = 100 MHz	ADS4142 (65 MSPS)		88		
			ADS4145 (125 MSPS)		82		
		f _{IN} = 170 MHz	ADS4142 (65 MSPS)	71	87		
			ADS4145 (125 MSPS)	72.5	84		
		f _{IN} = 300 MHz	ADS4142 (65 MSPS)		72.5		
			ADS4145 (125 MSPS)		77		
	Third-order harmonic distortion	f _{IN} = 10 MHz	ADS4142 (65 MSPS)		87		
			ADS4145 (125 MSPS)		86		
		f _{IN} = 70 MHz	ADS4142 (65 MSPS)		86.5		
			ADS4145 (125 MSPS)		87		
		f _{IN} = 100 MHz	ADS4142 (65 MSPS)		87		
			ADS4145 (125 MSPS)		85		
		f _{IN} = 170 MHz	ADS4142 (65 MSPS)	71	85		
			ADS4145 (125 MSPS)	72.5	81.5		
		f _{IN} = 300 MHz	ADS4142 (65 MSPS)		85		
			ADS4145 (125 MSPS)		84		
	Worst spur (other than second and third harmonics)	f _{IN} = 10 MHz	ADS4142 (65 MSPS)		96		
			ADS4145 (125 MSPS)		95		
		f _{IN} = 70 MHz			95		
		f _{IN} = 100 MHz	ADS4142 (65 MSPS)		94		
			ADS4145 (125 MSPS)		95		
		f _{IN} = 170 MHz	ADS4142 (65 MSPS)	77.5	92		
			ADS4145 (125 MSPS)	78.5	91		
IMD	Two-tone intermodulation distortion	f ₁ = 100 MHz, f ₂ = 105 MHz, each tone at –7 dBFS	ADS4142 (65 MSPS)		88.5		dBFS
			ADS4145 (125 MSPS)		87.5		
	Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine-wave input			1		Clock cycles
PSRR	AC power-supply rejection ratio	For 100-mV _{PP} signal on AVDD supply, up to 10 MHz			> 30		dB
ENOB	Effective number of bits	f _{IN} = 170 MHz	ADS4142 (65 MSPS)		11.5		LSBs
			ADS4145 (125 MSPS)		11.3		
DNL	Differential nonlinearity	f _{IN} = 170 MHz		–0.95	±0.5	1.7	LSBs
INL	Integrated nonlinearity	f _{IN} = 170 MHz			±1.5	±4.5	LSBs

7.7 Electrical Characteristics: General

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Differential input voltage			2		V _{PP}
	Differential input resistance	At dc, see Figure 106		> 1		MΩ
	Differential input capacitance	See Figure 107		4		pF
	Analog input bandwidth			550		MHz
	Analog input common-mode current (per input pin)			0.6		μA/MSPS
VCM	Common-mode output voltage			0.95		V
	VCM output current capability			4		mA
DC ACCURACY						
	Offset error		–15	2.5	15	mV
	Temperature coefficient of offset error			0.003		mV/°C
E _{GREF}	Gain error as a result of internal reference inaccuracy alone		–2		2	%FS
E _{GCHAN}	Gain error of channel alone			–0.2		%FS
	Temperature coefficient of E _{GCHAN}			0.001		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current	ADS4122, ADS4142 (65 MSPS)		42	55	mA
		ADS4125, ADS4145 (125 MSPS)		62	75	
IDRVDD ⁽¹⁾	Output buffer supply current, LVDS interface with 100-Ω external termination, low LVDS swing (200 mV)	ADS4122, ADS4142 (65 MSPS)		28.5		mA
		ADS4125, ADS4145 (125 MSPS)		35.5		
	Output buffer supply current, LVDS interface with 100-Ω external termination, standard LVDS swing (350 mV)	ADS4122, ADS4142 (65 MSPS)		40	53	
		ADS4125, ADS4145 (125 MSPS)		48	57	
	Output buffer supply current ⁽¹⁾⁽²⁾ , CMOS interface ⁽²⁾ , 8-pF external load capacitance, f _{IN} = 2.5 MHz	ADS4122, ADS4142 (65 MSPS)		15		
		ADS4125, ADS4145 (125 MSPS)		23		
	Analog power	ADS4122, ADS4142 (65 MSPS)		76		mW
		ADS4122, ADS4142 (125 MSPS)		112		
	Digital power, LVDS interface, low LVDS swing	ADS4122, ADS4142 (65 MSPS)		52		mW
		ADS4122, ADS4142 (125 MSPS)		66.5		
	Digital power, CMOS interface ⁽²⁾ , 8-pF external load capacitance, f _{IN} = 2.5 MHz	ADS4122, ADS4142 (65 MSPS)		27		mW
		ADS4122, ADS4142 (125 MSPS)		41.5		
	Global power-down			10	15	mW
	Standby	ADS4122, ADS4142 (65 MSPS)		105		mW
		ADS4122, ADS4142 (125 MSPS)		130		

- (1) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10 pF.
- (2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the [CMOS Interface Power Dissipation](#) section in the [Application Information](#)).

7.8 Digital Characteristics

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, and 50% clock duty cycle for the ADS4122, ADS4125, ADS4142, and ADS4145, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, OE)						
High-level input voltage		RESET, SCLK, SDATA, and SEN support 1.8-V and 3.3-V CMOS logic levels	1.3		0.4	V
Low-level input voltage				V		
High-level input voltage		OE only supports 1.8-V CMOS logic levels	1.3		0.4	V
Low-level input voltage				V		
High-level input current: SDATA, SCLK ⁽¹⁾	V _{HIGH} = 1.8 V			10		μA
High-level input current: SEN	V _{HIGH} = 1.8 V			0		μA
Low-level input current: SDATA, SCLK	V _{LOW} = 0 V			0		μA
Low-level input current: SEN	V _{LOW} = 0 V			–10		μA
DIGITAL OUTPUTS (CMOS INTERFACE: D0 TO D13, OVR_SDOUT)						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS (LVDS INTERFACE: DA0P/M TO DA13P/M, DB0P/M TO DB13P/M, CLKOUTP/M)						
High-level output voltage ⁽²⁾	V _{ODH}	Standard swing LVDS	270	350	430	mV
Low-level output voltage ⁽²⁾	V _{ODL}	Standard swing LVDS	–430	–350	–270	mV
High-level output voltage ⁽²⁾	V _{ODH}	Low swing LVDS		200		mV
Low-level output voltage ⁽²⁾	V _{ODL}	Low swing LVDS		–200		mV
Output common-mode voltage	V _{OCM}		0.85	1.05	1.25	V

(1) SDATA and SCLK have an internal 180-kΩ pull-down resistor.

(2) With an external 100-Ω termination.

7.9 Timing Requirements: LVDS and CMOS Modes⁽¹⁾

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 125 MSPS, sine wave input clock, C_{LOAD} = 5 pF⁽²⁾, and R_{LOAD} = 100 Ω⁽³⁾, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

		MIN	TYP	MAX	UNIT
GENERAL					
t _A	Aperture delay	0.6	0.8	1.2	ns
	Variation of aperture delay between two devices at the same temperature and DRVDD supply		±100		ps
t _J	Aperture jitter		100		f _S rms
Wakeup time:	Time to valid data after coming out of STANDBY mode		5	25	μs
	Time to valid data after coming out of PDN GLOBAL mode		100	500	μs
ADC latency ⁽⁴⁾ :	Low-latency mode (default after reset)		10		Clock cycles
	Low-latency mode disabled (gain enabled, offset correction disabled)		16		Clock cycles
	Low-latency mode disabled (gain and offset correction enabled)		17		Clock cycles

(1) Timing parameters are ensured by design and characterization but are not production tested.

(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.

(3) R_{LOAD} is the differential load resistance between the LVDS output pair.

(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.

Timing Requirements: LVDS and CMOS Modes⁽¹⁾ (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 125 MSPS, sine wave input clock, C_{LOAD} = 5 pF⁽²⁾, and R_{LOAD} = 100 Ω⁽³⁾, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

		MIN	TYP	MAX	UNIT
DDR LVDS MODE⁽⁵⁾⁽⁶⁾					
t _{SU}	Data setup time ⁽³⁾ : data valid ⁽⁷⁾ to zero-crossing of CLKOUTP	2.3	3		ns
t _H	Data hold time ⁽³⁾ : zero-crossing of CLKOUTP to data becoming invalid ⁽⁷⁾	0.35	0.6		ns
t _{PDI}	Clock propagation delay: input clock rising edge cross-over to output clock rising edge cross-over, <i>sampling frequency ≤ 125 MSPS</i>	3	4.2	5.4	ns
	Variation of t _{PDI} between two devices at the same temperature and DRVDD supply		±0.6		ns
	LVDS bit clock duty cycle of differential clock, (CLKOUTP – CLKOUTM), <i>sampling frequency ≤ 125 MSPS</i>		48%		
t _{RISE} , t _{FALL}	Data rise time, data fall time: rise time measured from –100 mV to 100 mV, fall time measured from 100 mV to –100 mV, <i>sampling frequency ≤ 125 MSPS</i>		0.14		ns
t _{CLKRISE} , t _{CLKFALL}	Output clock rise time, output clock fall time: rise time measured from –100 mV to 100 mV, fall time measured from 100 mV to –100 mV, <i>sampling frequency ≤ 125 MSPS</i>		0.14		ns
t _{OE}	Output enable (OE) to data delay: time to valid data after OE becomes active		50	100	ns
PARALLEL CMOS MODE⁽⁸⁾					
t _{SETUP}	Data setup time: data valid ⁽⁹⁾ to 50% of CLKOUT rising edge	3.1	3.7		ns
t _{HOLD}	Data hold time: 50% of CLKOUT rising edge to data becoming invalid ⁽⁹⁾	3.2	4		ns
t _{PDI}	Clock propagation delay: input clock rising edge cross-over to 50% of output clock rising edge, <i>sampling frequency ≤ 125 MSPS</i>	4	5.5	7	ns
	Output clock duty cycle of output clock, CLKOUT, <i>sampling frequency ≤ 125 MSPS</i>		47%		
t _{RISE} , t _{FALL}	Data rise time, data fall time: rise time measured from 20% to 80% of DRVDD, fall time measured from 80% to 20% of DRVDD, <i>sampling frequency ≤ 125 MSPS</i>		0.35		ns
t _{CLKRISE} , t _{CLKFALL}	Output clock rise time, output clock fall time: rise time measured from 20% to 80% of DRVDD, fall time measured from 80% to 20% of DRVDD, <i>sampling frequency ≤ 125 MSPS</i>		0.35		ns
t _{OE}	Output enable (OE) to data delay: time to valid data after OE becomes active		20	40	ns

(5) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.

(6) The LVDS timings are unchanged for low latency disabled and enabled.

(7) Data valid refers to a logic high of 100 mV and a logic low of –100 mV.

(8) Low latency mode enabled.

(9) Data valid refers to a logic high of 1.25 V and a logic low of 0.54 V.

7.10 Serial Interface Timing Characteristics

Typical values at 25°C, minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V, unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNIT
f _{SCLK}	SCLK frequency (equal to 1/t _{SCLK})	> dc	20	MHz
t _{SLOADS}	SEN to SCLK setup time	25		ns
t _{SLOADH}	SCLK to SEN hold time	25		ns
t _{DSU}	SDATA setup time	25		ns
t _{DH}	SDATA hold time	25		ns

7.11 Reset Timing Requirements

Typical values at 25°C and minimum and maximum values across the full temperature range: $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = 85^{\circ}\text{C}$, unless otherwise noted.

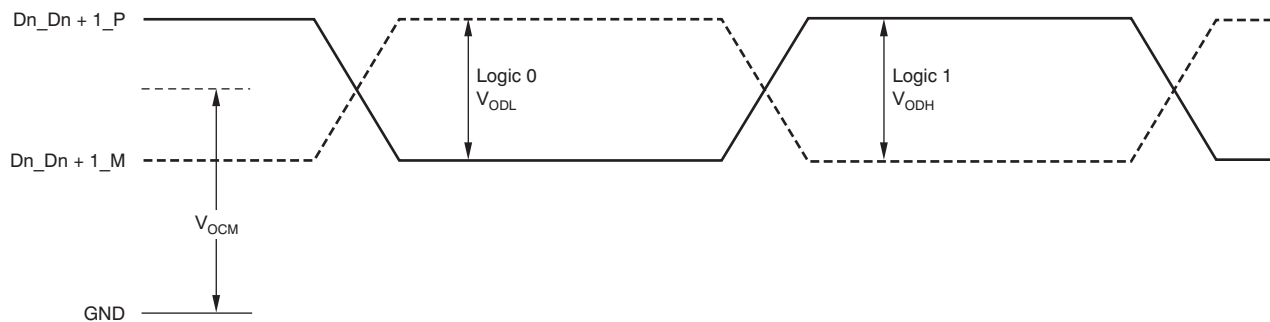
		MIN	TYP	MAX	UNIT
t_1	Power-on delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse duration of active RESET signal that resets the serial registers	10			ns
				1 ⁽¹⁾	μs
t_3	Delay from RESET disable to SEN active	100			ns

- (1) The reset pulse is needed only when using the serial interface configuration. If the pulse width is greater than 1μs, the device could enter the parallel configuration mode briefly and then return back to serial interface mode.

7.12 Timing Characteristics at Lower Sampling Frequencies

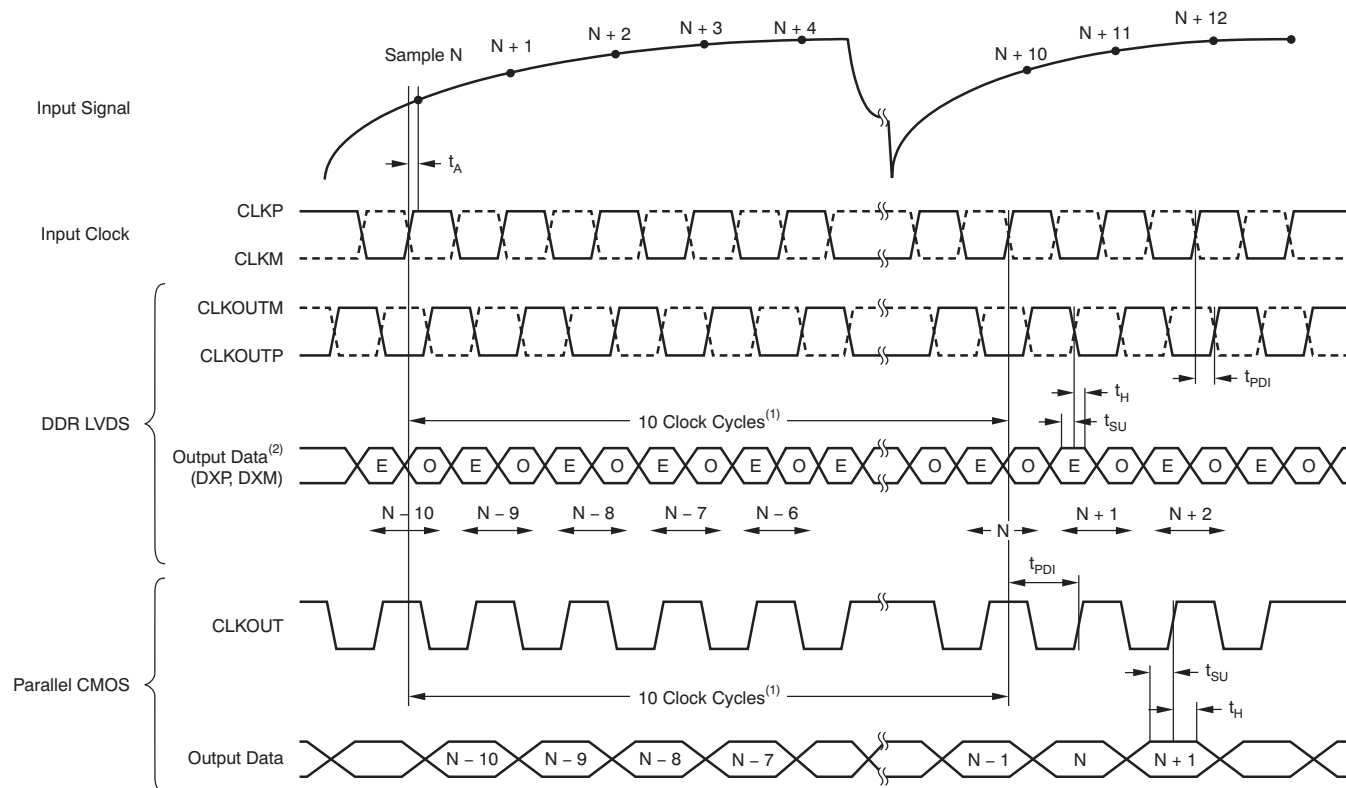
SAMPLING FREQUENCY (MSPS)	t_{su} , SETUP TIME			t_h , HOLD TIME			t_{PD} , CLOCK PROPAGATION DELAY			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DDR LVDS										ns
65	5.5	6.5		0.35	0.6					ns
80	4.5	5.2		0.35	0.6					ns
CMOS (LOW LATENCY ENABLED)⁽¹⁾										ns
65	6.5	7.5		6.5	7.5		4	5.5	7	ns
80	5.4	6		5.4	6		4	5.5	7	ns
CMOS (LOW LATENCY DISABLED)⁽¹⁾										ns
65	6	7		7	8		4	5.5	7	ns
80	4.8	5.5		5.7	6.5		4	5.5	7	ns
125	2.5	3.2		3.5	4.3		4	5.5	7	ns

- (1) Timing specified with respect to output clock



With external 100-Ω termination.

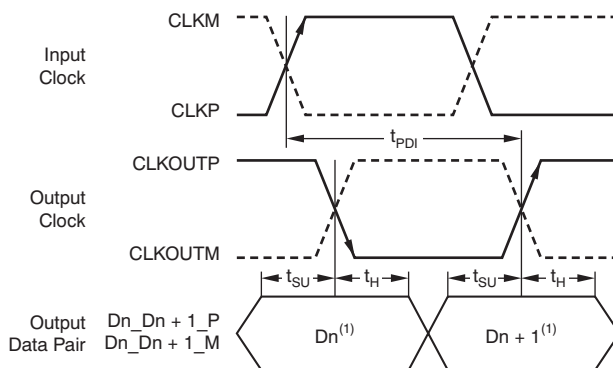
Figure 1. LVDS Output Voltage Levels



ADC latency in low-latency mode. At higher sampling frequencies, t_{PDI} is greater than one clock cycle which then makes the overall latency = ADC latency + 1.

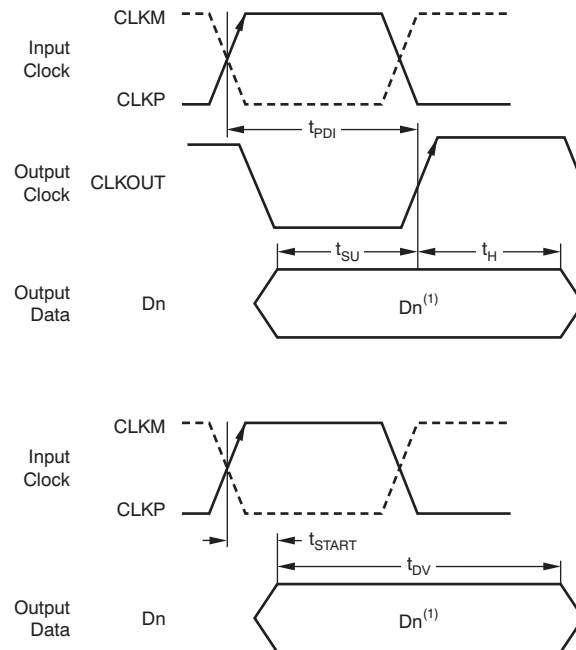
E = Even bits (D0, D2, D4, and so forth). O = Odd bits (D1, D3, D5, and so forth).

Figure 2. Latency Diagram



D_n = bits D0, D2, D4, and so forth. $D_n + 1$ = Bits D1, D3, D5, and so forth.

Figure 3. LVDS Mode Timing



Dn = bits D0, D1, D2, and so forth.

Figure 4. CMOS Mode Timing

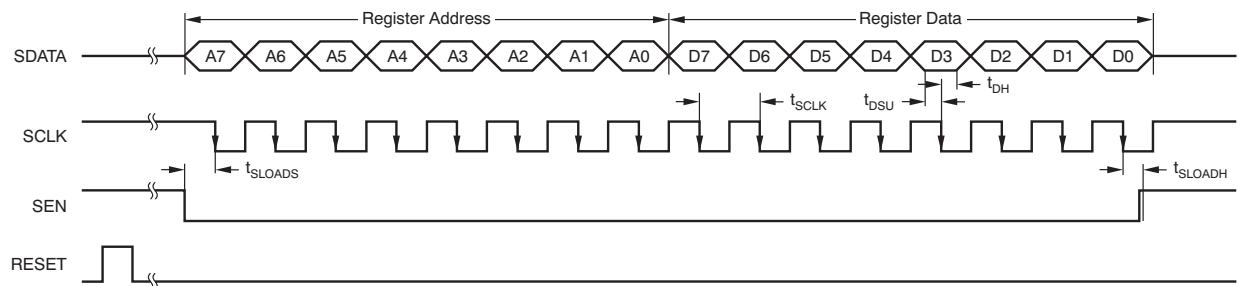
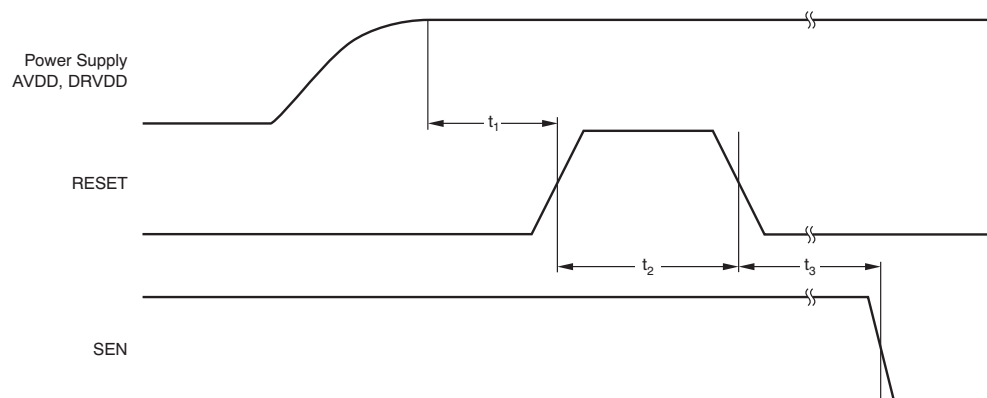


Figure 5. Serial Interface Timing



A high pulse on the RESET pin is required in the serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 6. Reset Timing Diagram

7.13 Typical Characteristics: ADS4122

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

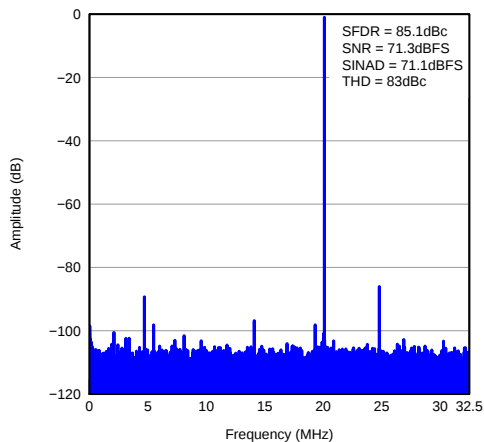


Figure 7. FFT for 20-MHz Input Signal

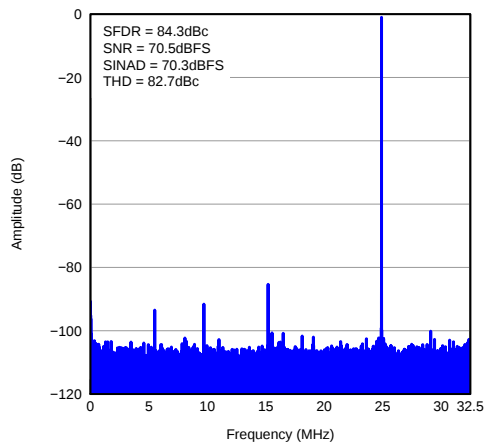


Figure 8. FFT for 170-MHz Input Signal

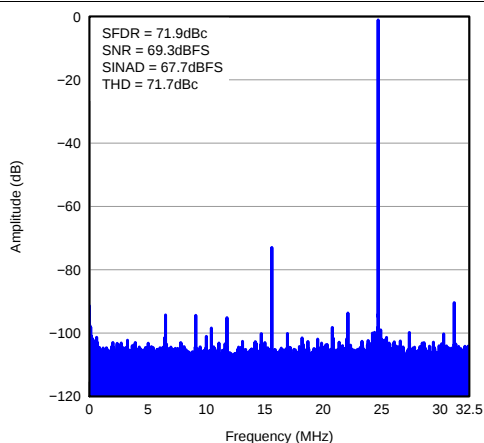


Figure 9. FFT for 300-MHz Input Signal

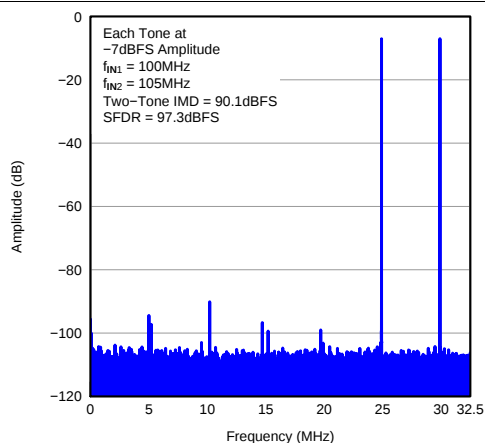


Figure 10. FFT for Two-Tone Input Signal

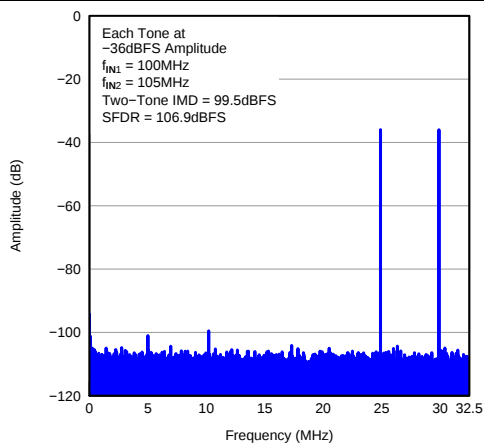


Figure 11. FFT for Two-Tone Input Signal

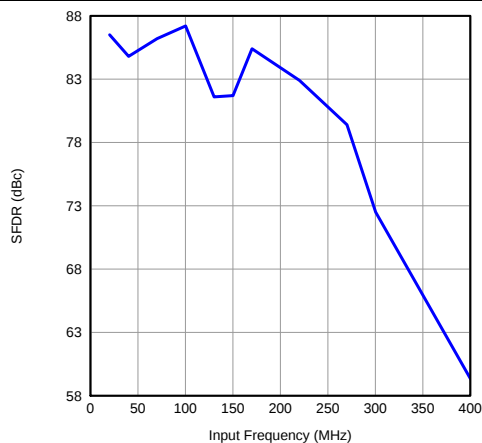


Figure 12. SFDR vs Input Frequency

Typical Characteristics: ADS4122 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

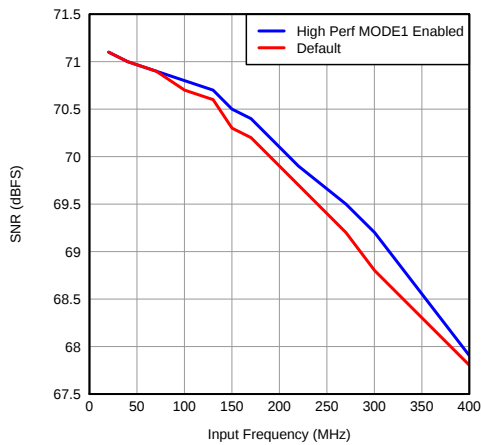


Figure 13. SNR vs Input Frequency

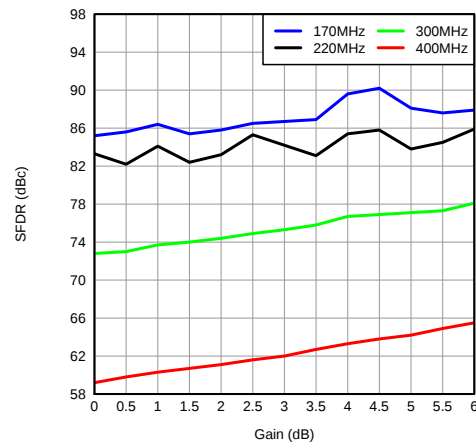


Figure 14. SFDR Across Gain and Input Frequency

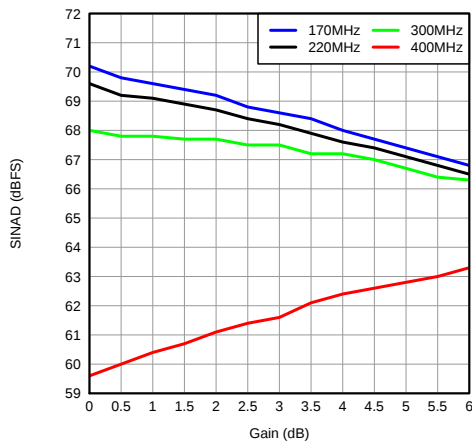


Figure 15. SINAD Across Gain and Input Frequency

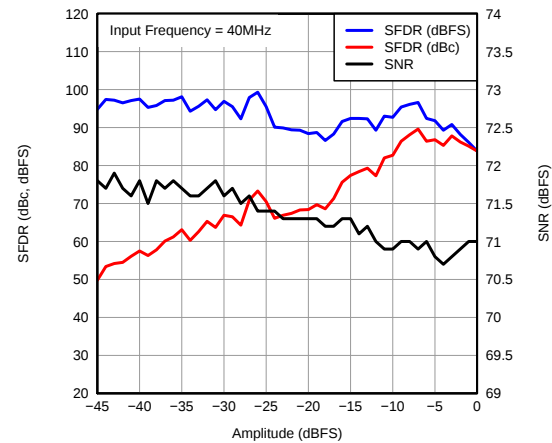


Figure 16. Performance Across Input Amplitude (Single Tone)

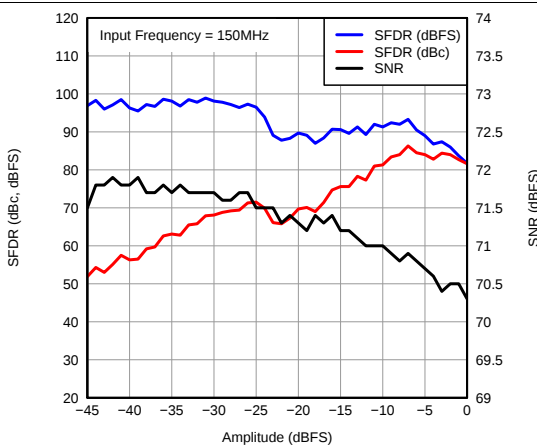


Figure 17. Performance Across Input Amplitude (Single Tone)

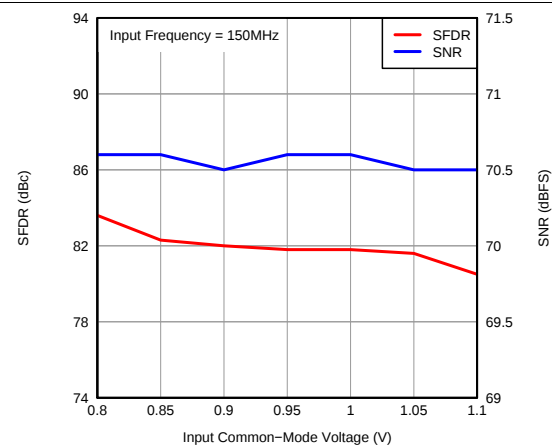


Figure 18. Performance vs Input Common-Mode Voltage

Typical Characteristics: ADS4122 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

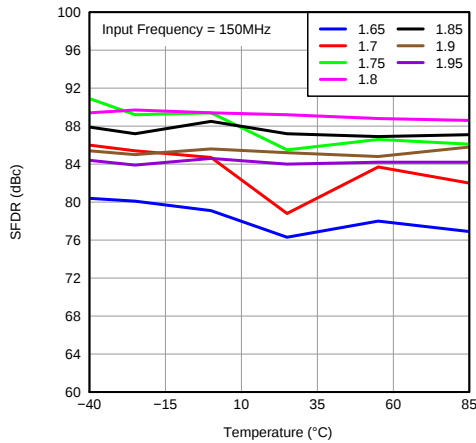


Figure 19. SFDR Across Temperature vs AVDD Supply

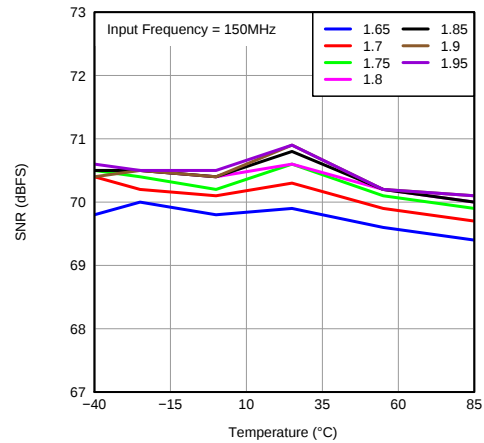


Figure 20. SNR Across Temperature vs AVDD Supply

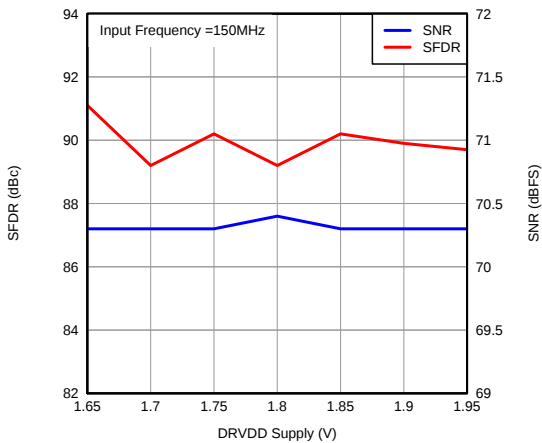


Figure 21. Performance Across DRVDD Supply Voltage

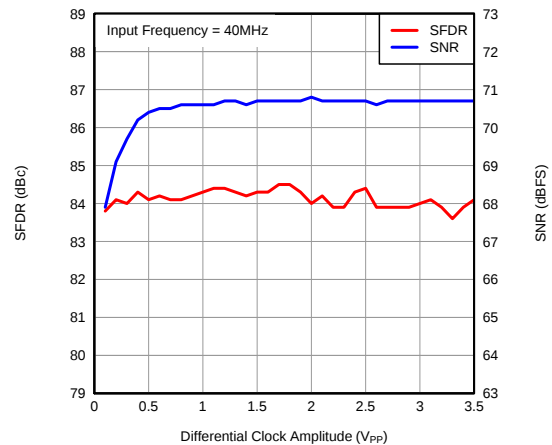


Figure 22. Performance Across Input Clock Amplitude

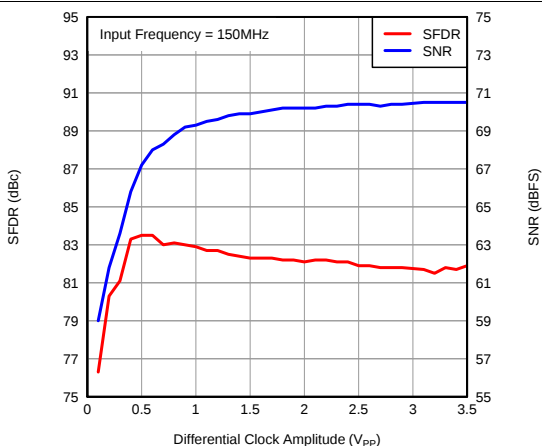


Figure 23. Performance Across Input Clock Amplitude

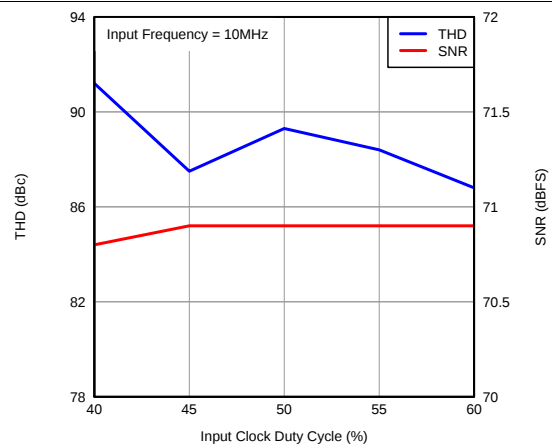


Figure 24. Performance Across Input Clock Duty Cycle

7.14 Typical Characteristics: ADS4125

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

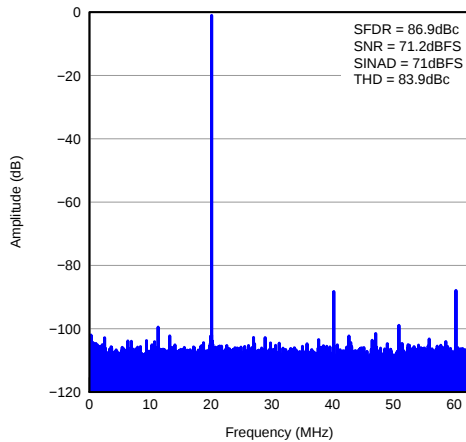


Figure 25. FFT for 20-MHz Input Signal

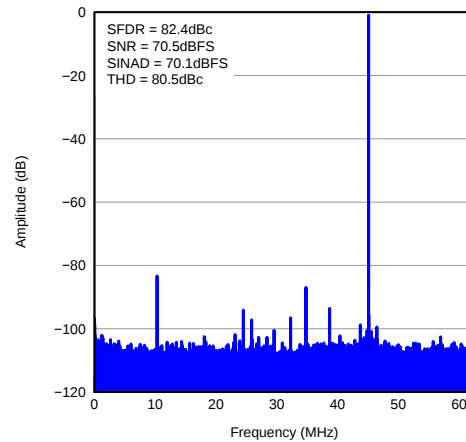


Figure 26. FFT for 170-MHz Input Signal

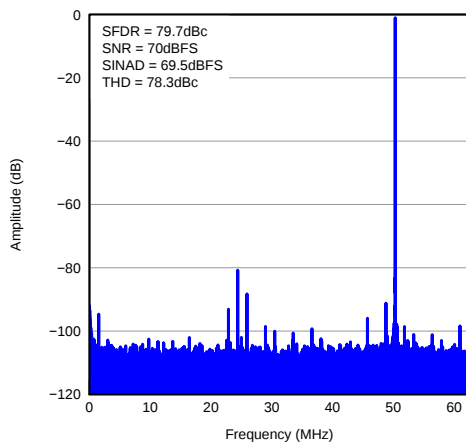


Figure 27. FFT for 300-MHz Input Signal

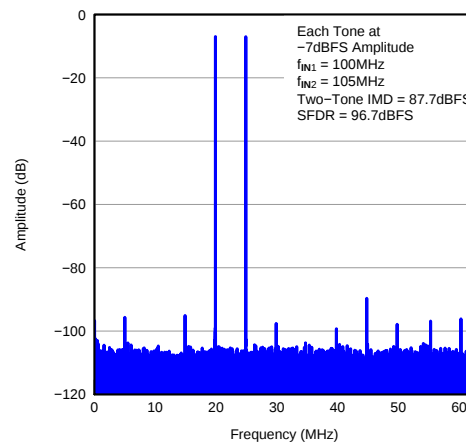


Figure 28. FFT for Two-Tone Input Signal

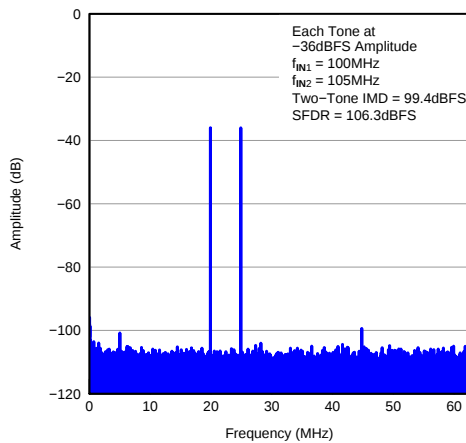


Figure 29. FFT for Two-Tone Input Signal

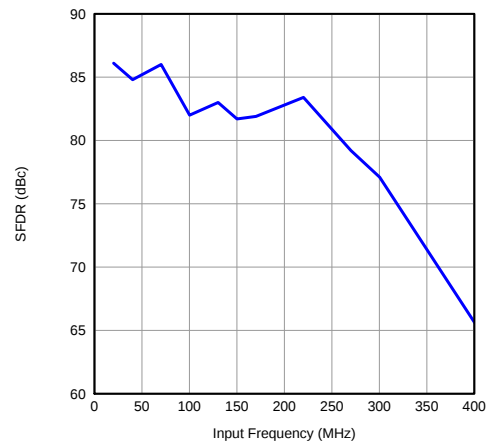


Figure 30. SFDR vs Input Frequency

Typical Characteristics: ADS4125 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

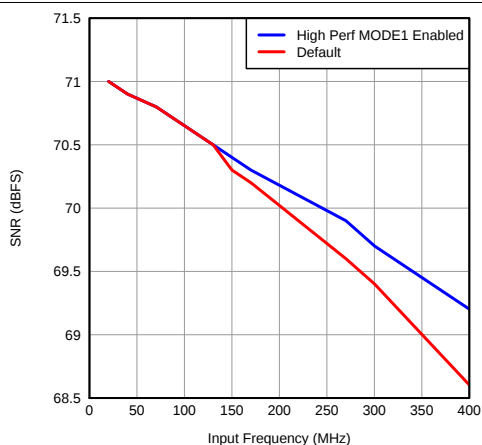


Figure 31. SNR vs Input Frequency

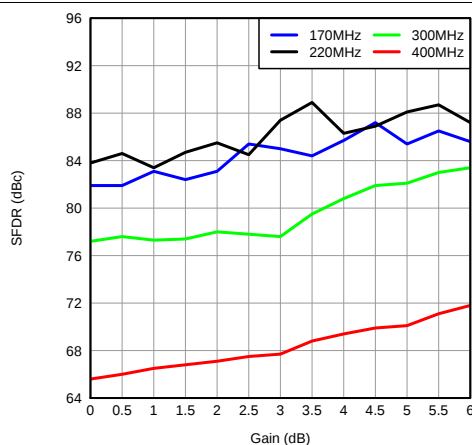


Figure 32. SFDR Across Gain and Input Frequency

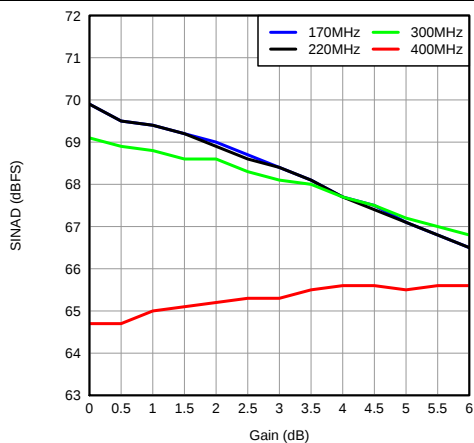


Figure 33. SINAD Across Gain and Input Frequency

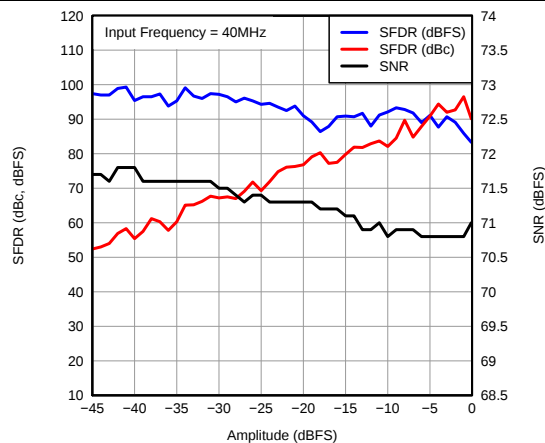


Figure 34. Performance Across Input Amplitude (Single Tone)

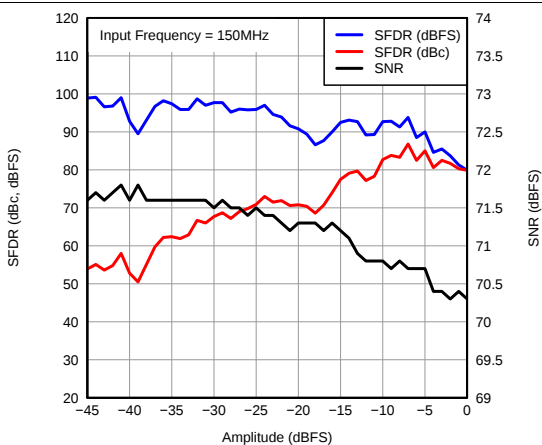


Figure 35. Performance Across Input Amplitude (Single Tone)

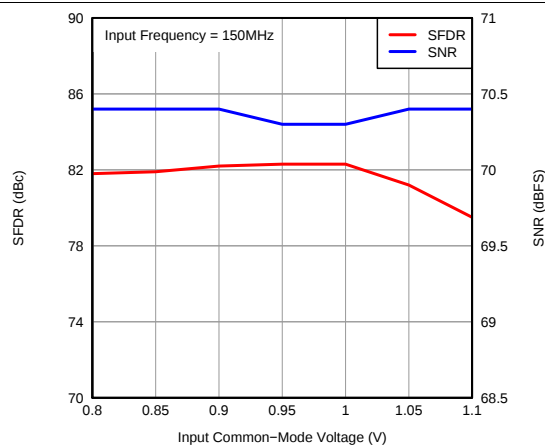


Figure 36. Performance vs Input Common-Mode Voltage

Typical Characteristics: ADS4125 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

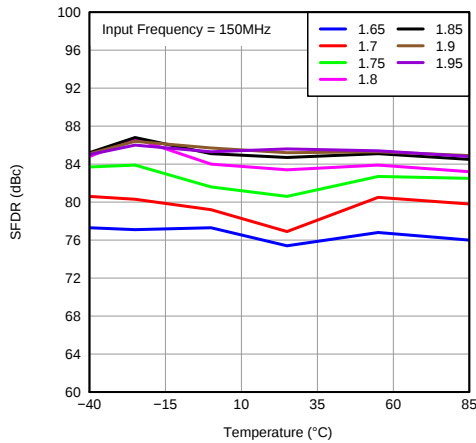


Figure 37. SFDR Across Temperature vs AVDD Supply

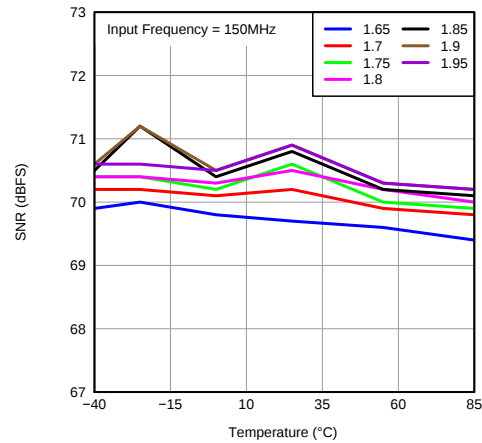


Figure 38. SNR Across Temperature vs AVDD Supply

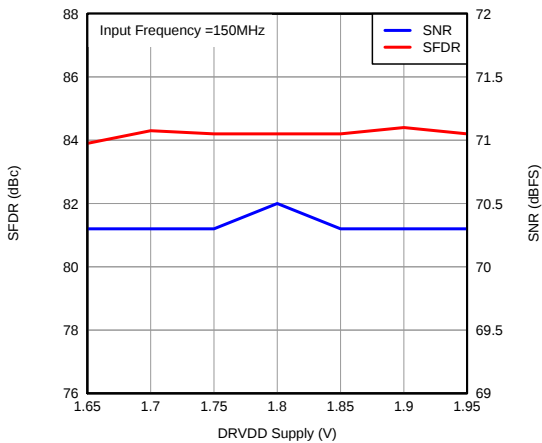


Figure 39. Performance Across DRVDD Supply Voltage

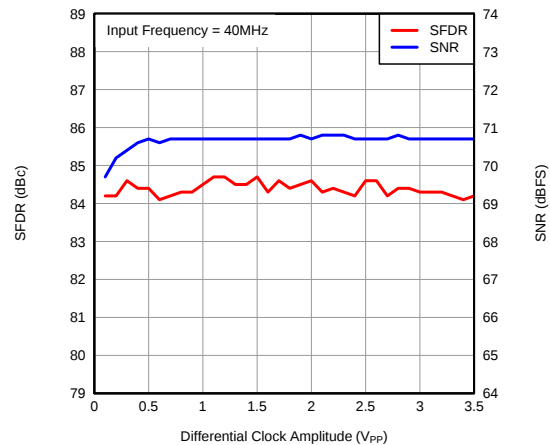


Figure 40. Performance Across Input Clock Amplitude

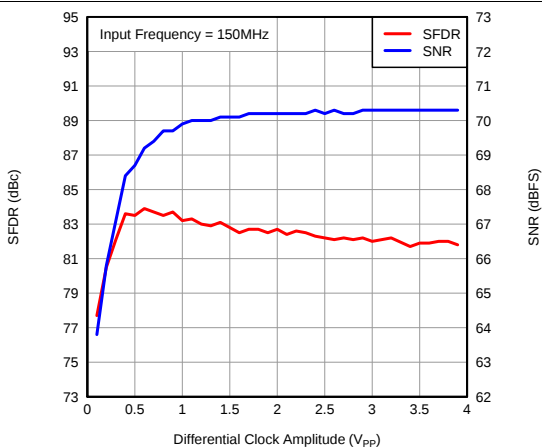


Figure 41. Performance Across Input Clock Amplitude

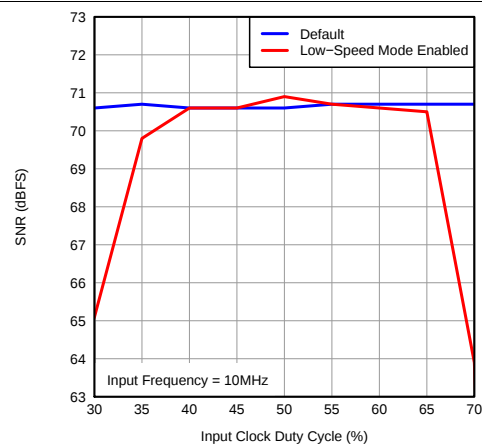


Figure 42. SNR Across Input Clock Duty Cycle

7.15 Typical Characteristics: ADS4142

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

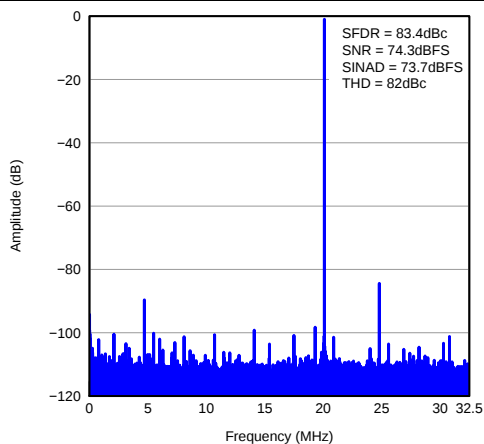


Figure 43. FFT for 20-MHz Input Signal

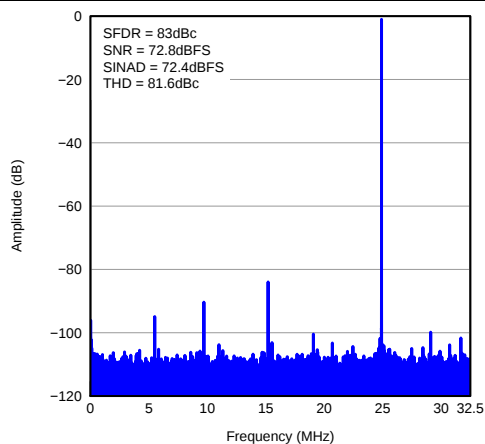


Figure 44. FFT for 170-MHz Input Signal

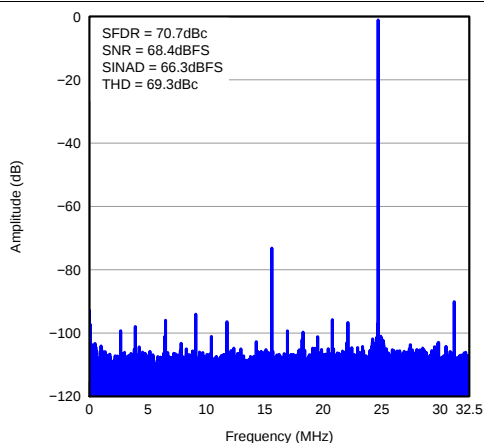


Figure 45. FFT for 300-MHz Input Signal

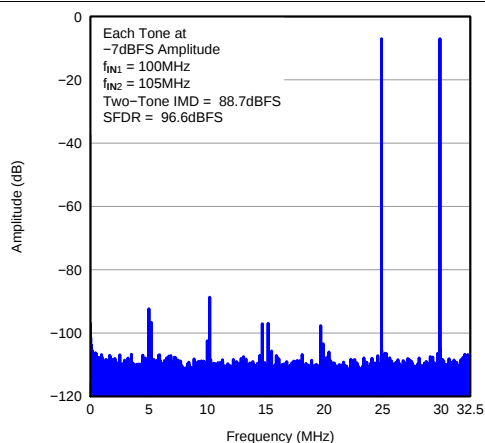


Figure 46. FFT for Two-Tone Input Signal

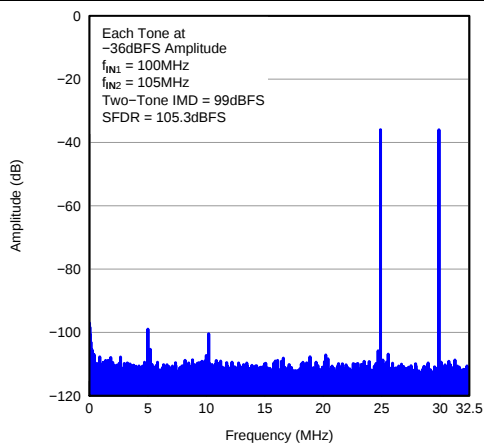


Figure 47. FFT for Two-Tone Input Signal

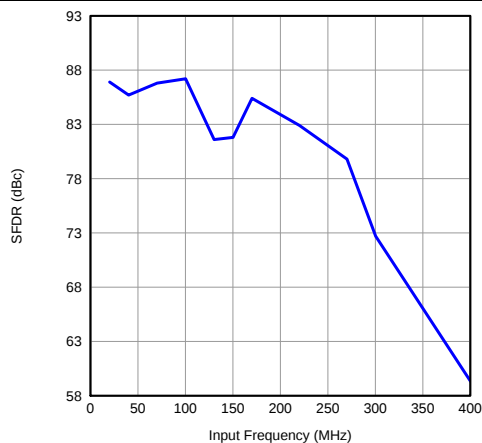


Figure 48. SFDR vs Input Frequency

Typical Characteristics: ADS4142 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

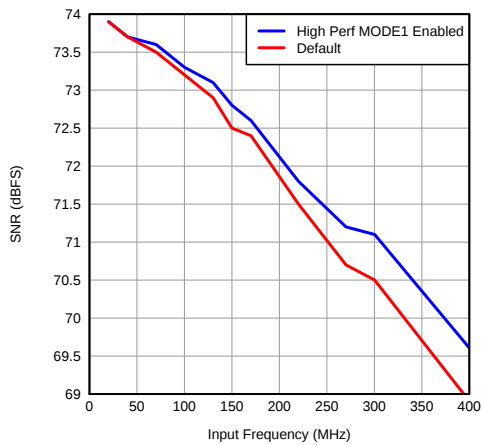


Figure 49. SNR vs Input Frequency

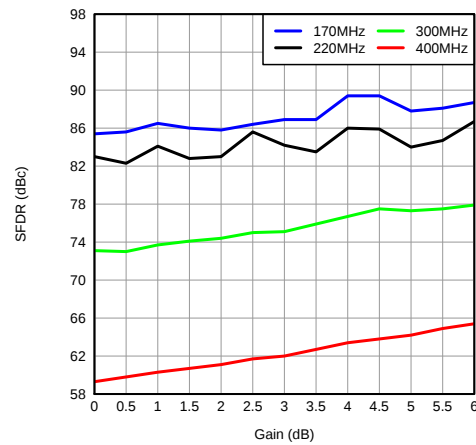


Figure 50. SFDR Across Gain and Input Frequency

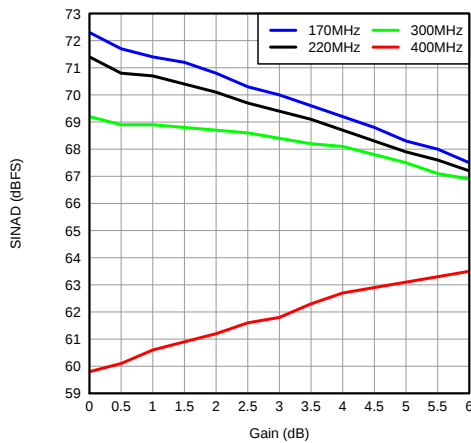


Figure 51. SINAD Across Gain and Input Frequency

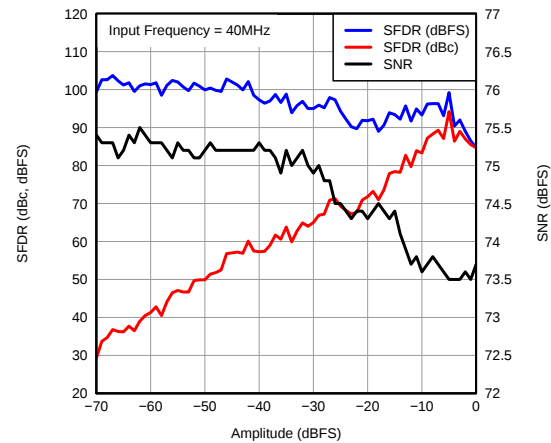


Figure 52. Performance Across Input Amplitude (Single Tone)

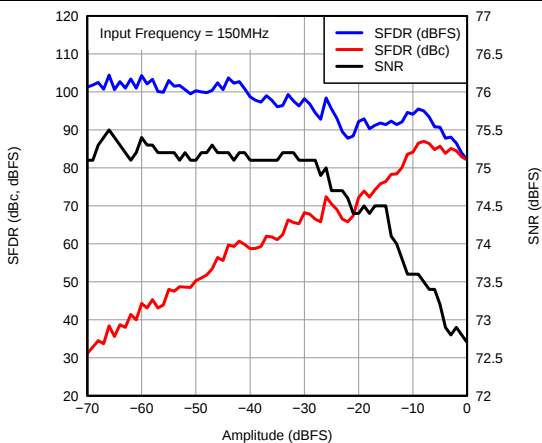


Figure 53. Performance Across Input Amplitude (Single Tone)

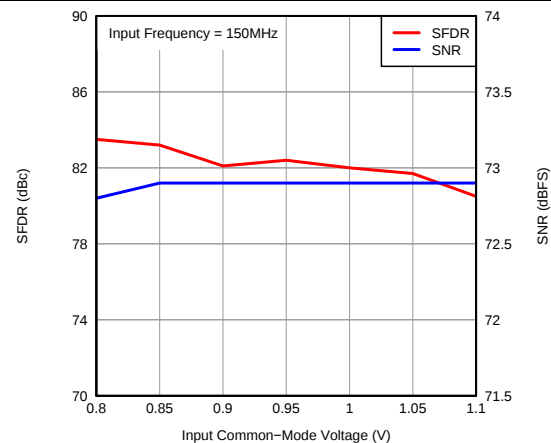


Figure 54. Performance vs Input Common-Mode Voltage

Typical Characteristics: ADS4142 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

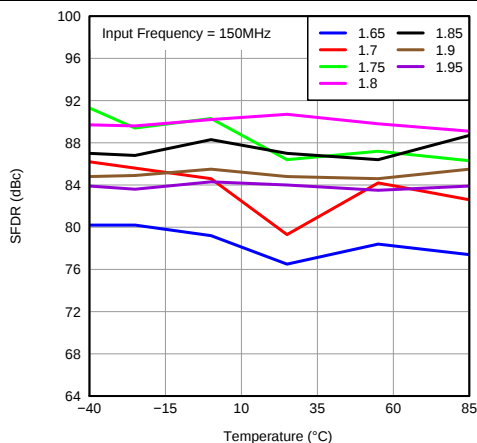


Figure 55. SFDR Across Temperature vs AVDD Supply

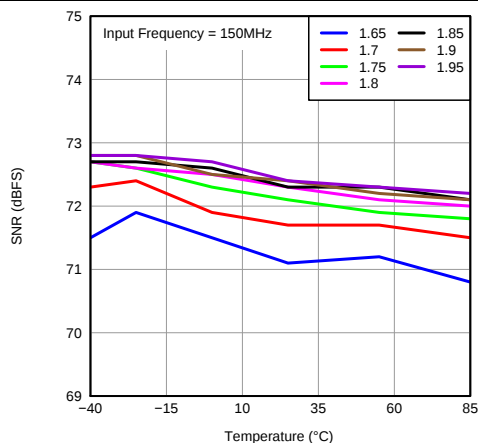


Figure 56. SNR Across Temperature vs AVDD Supply

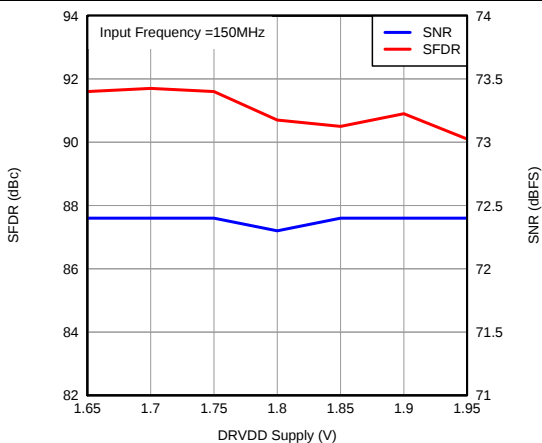


Figure 57. Performance Across DRVDD Supply Voltage

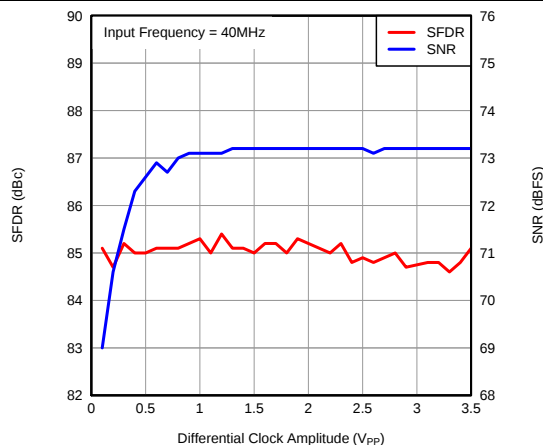


Figure 58. Performance Across Input Clock Amplitude

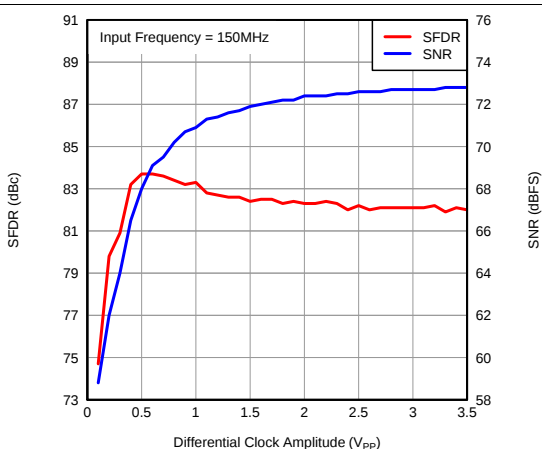


Figure 59. Performance Across Input Clock Amplitude

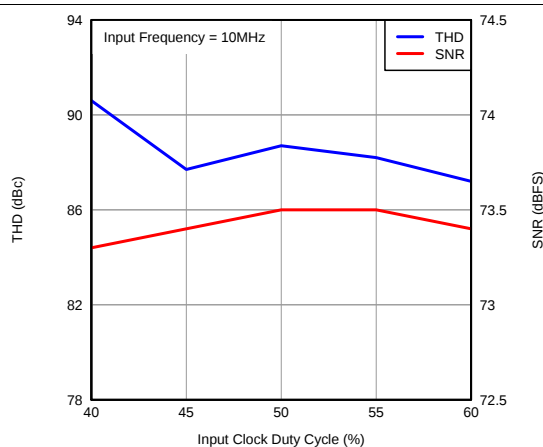


Figure 60. Performance Across Input Clock Duty Cycle

Typical Characteristics: ADS4142 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

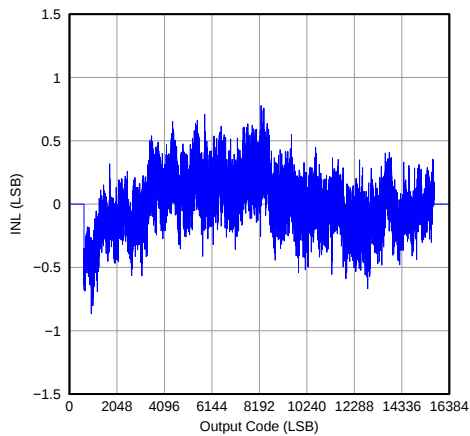


Figure 61. Integral Nonlinearity

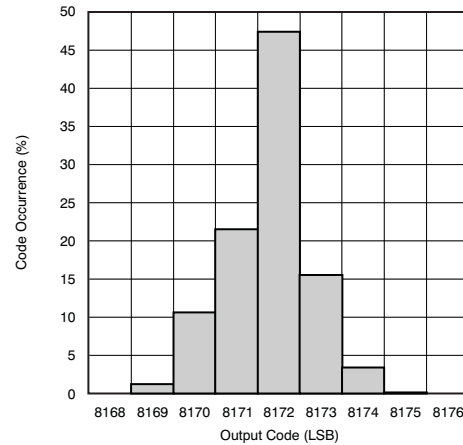


Figure 62. Output Noise Histogram
(With Inputs Shorted to VCM)

7.16 Typical Characteristics: ADS4145

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

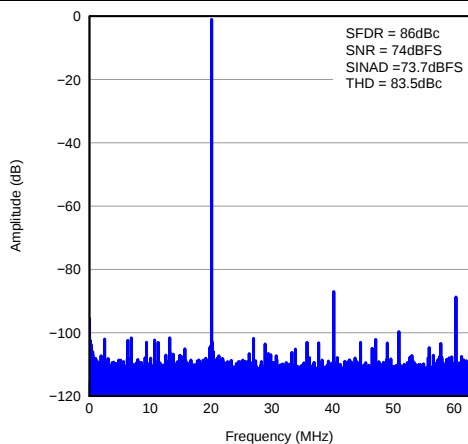


Figure 63. FFT for 20-MHz Input Signal

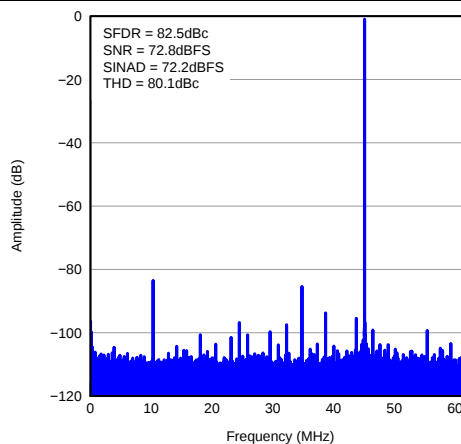


Figure 64. FFT for 170-MHz Input Signal

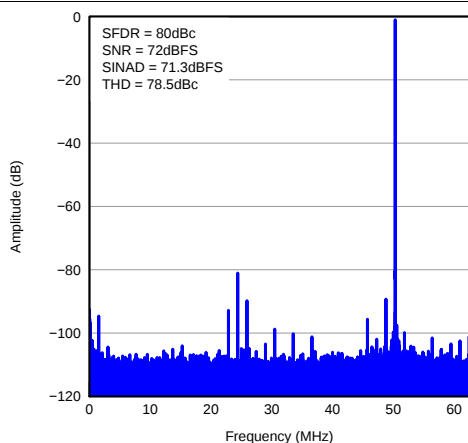


Figure 65. FFT for 300-MHz Input Signal

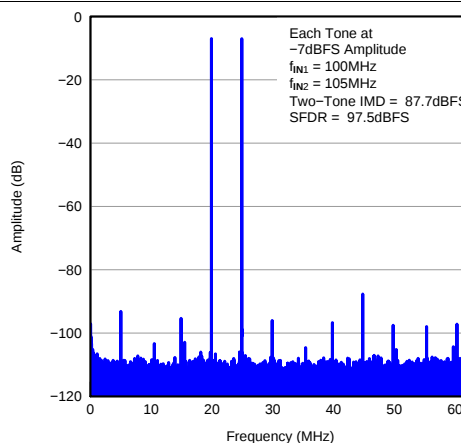


Figure 66. FFT for Two-Tone Input Signal

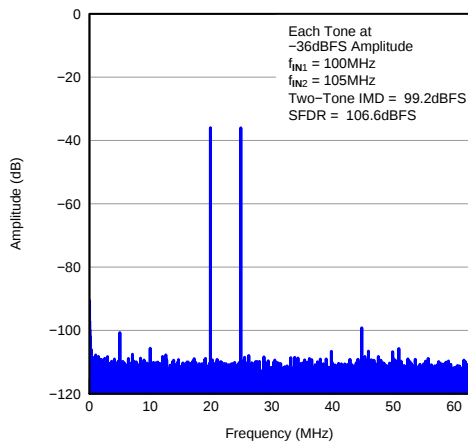


Figure 67. FFT for Two-Tone Input Signal

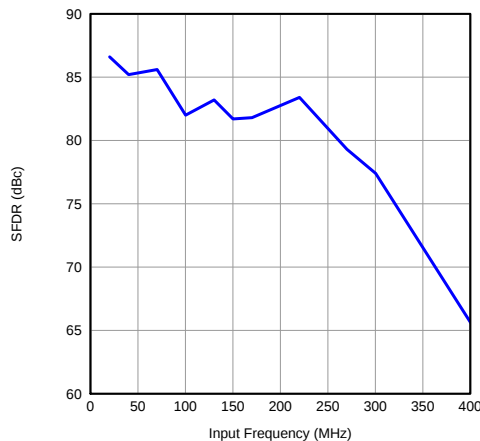


Figure 68. SFDR vs Input Frequency

Typical Characteristics: ADS4145 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

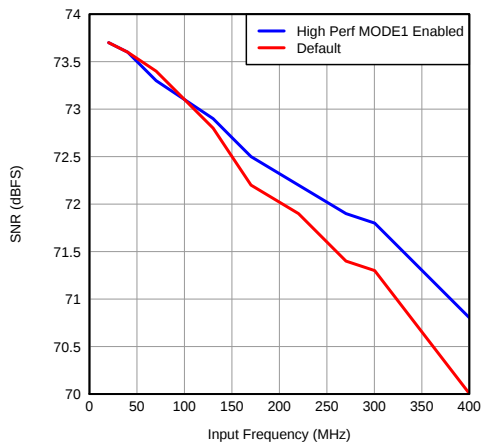


Figure 69. SNR vs Input Frequency

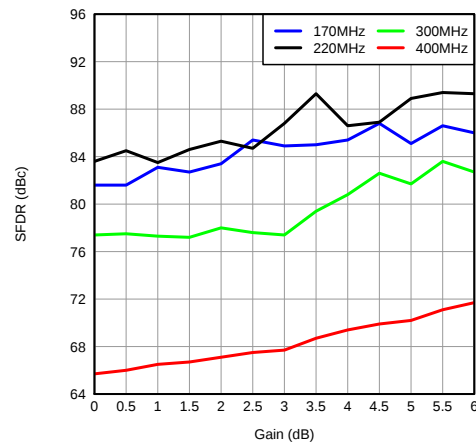


Figure 70. SFDR Across Gain and Input Frequency

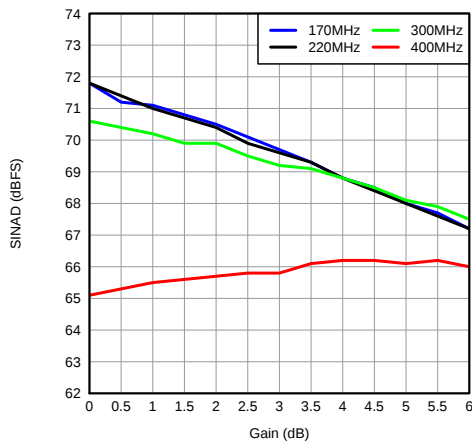


Figure 71. SINAD Across Gain and Input Frequency

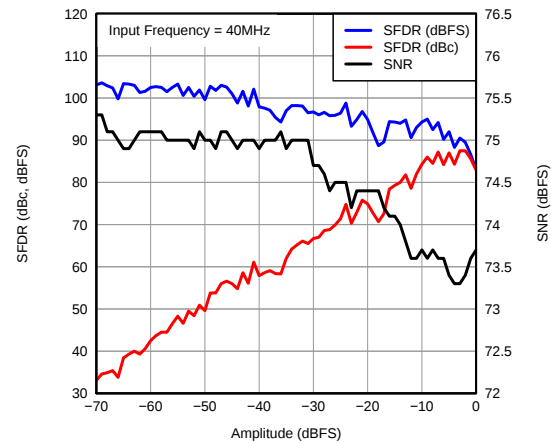


Figure 72. Performance Across Input Amplitude (Single Tone)

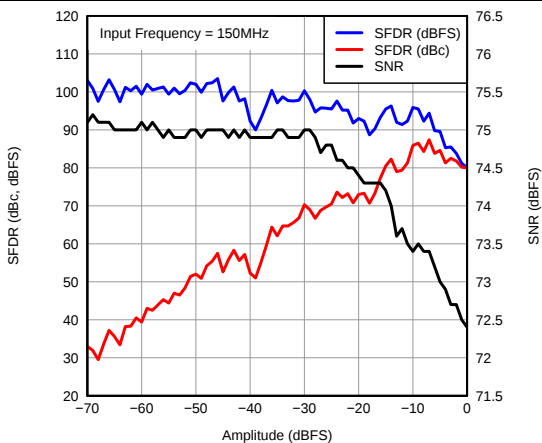


Figure 73. Performance Across Input Amplitude (Single Tone)

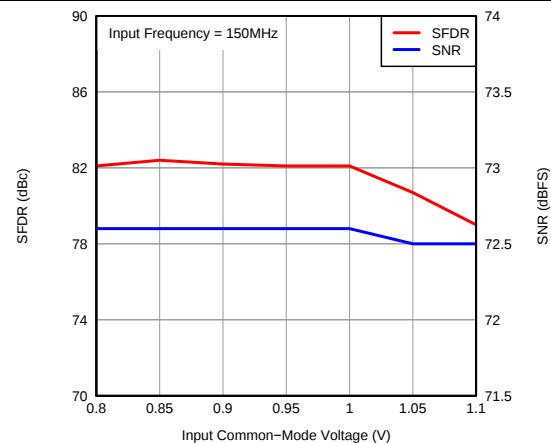


Figure 74. Performance vs Input Common-Mode Voltage

Typical Characteristics: ADS4145 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

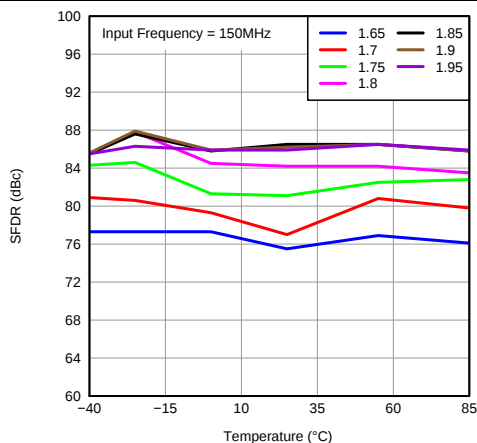


Figure 75. SFDR Across Temperature vs AVDD Supply

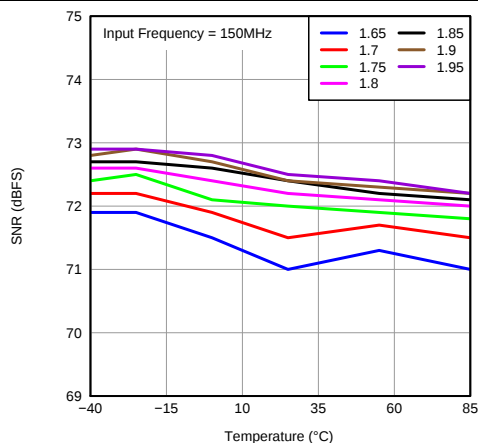


Figure 76. SNR Across Temperature vs AVDD Supply

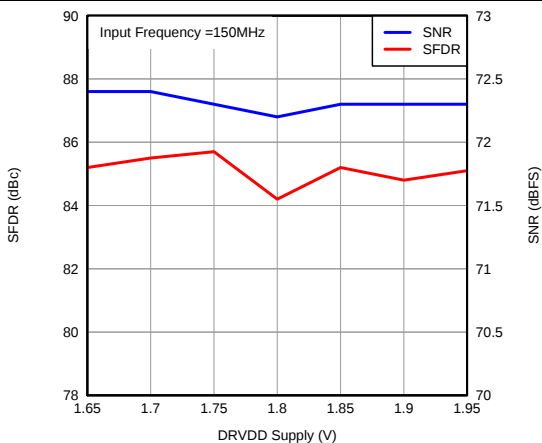


Figure 77. Performance Across DRVDD Supply Voltage

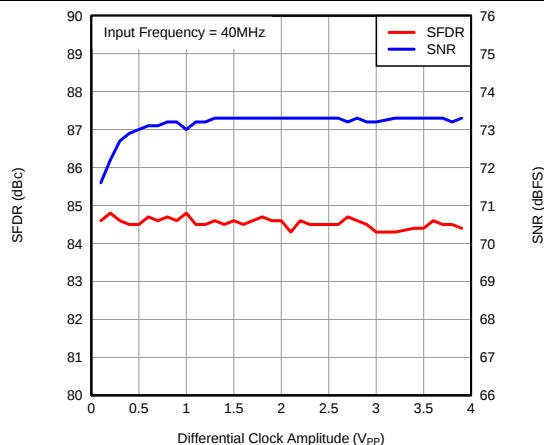


Figure 78. Performance Across Input Clock Amplitude

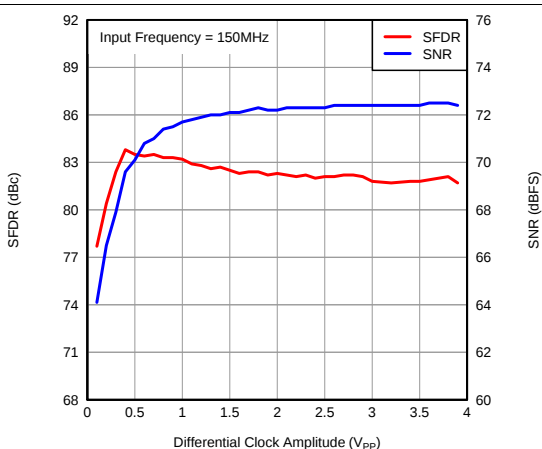


Figure 79. Performance Across Input Clock Amplitude

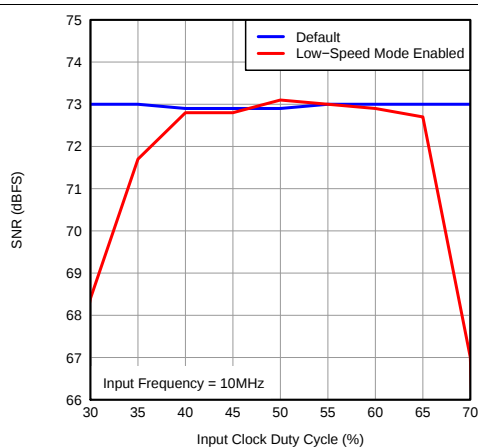


Figure 80. SNR Across Input Clock Duty Cycle

Typical Characteristics: ADS4145 (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

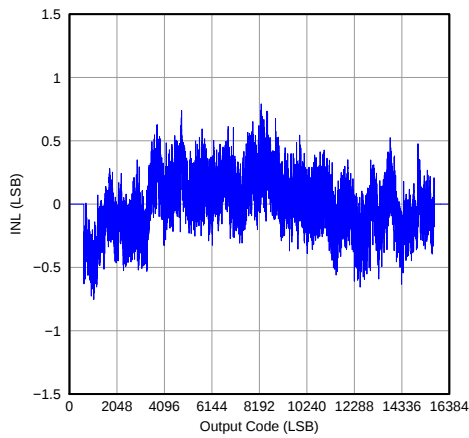


Figure 81. Integral Nonlinearity

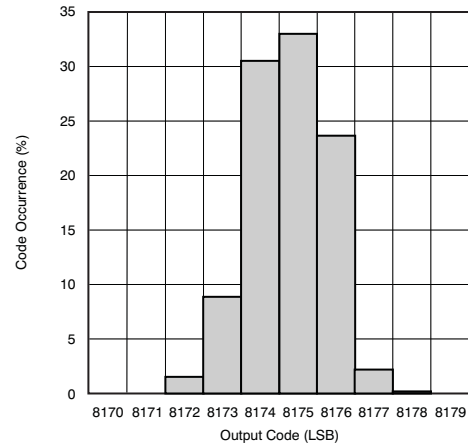


Figure 82. Output Noise Histogram
(With Inputs Shorted to VCM)

7.17 Typical Characteristics: Common

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

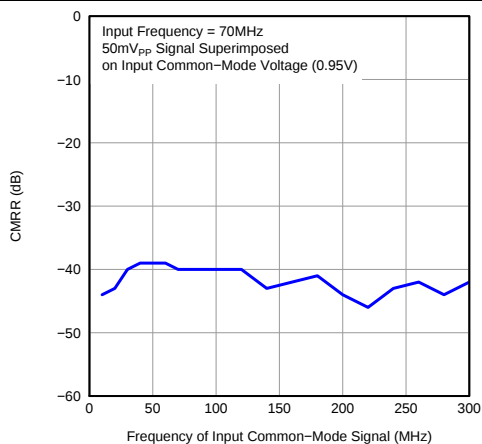


Figure 83. CMRR vs Frequency

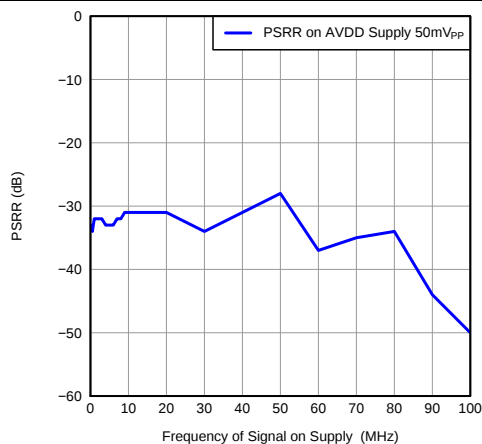


Figure 84. PSRR vs Frequency

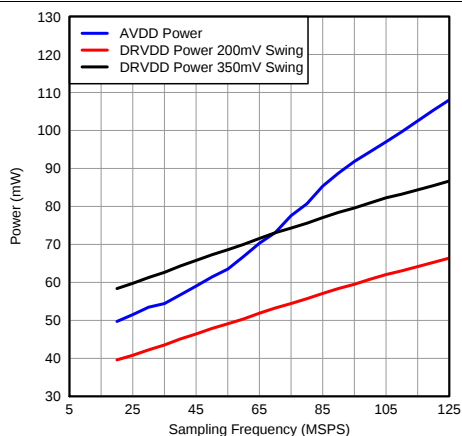


Figure 85. Power vs Sample Rate

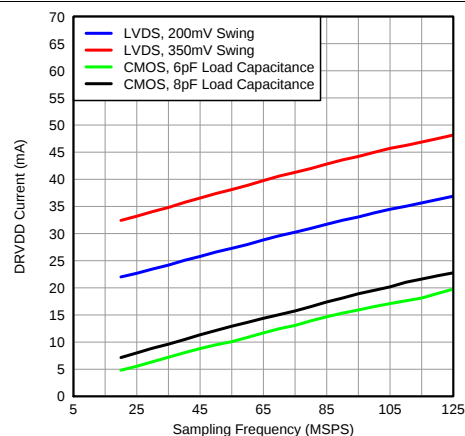


Figure 86. DRVDD Current vs Sample Rate

7.18 Typical Characteristics: Contour

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

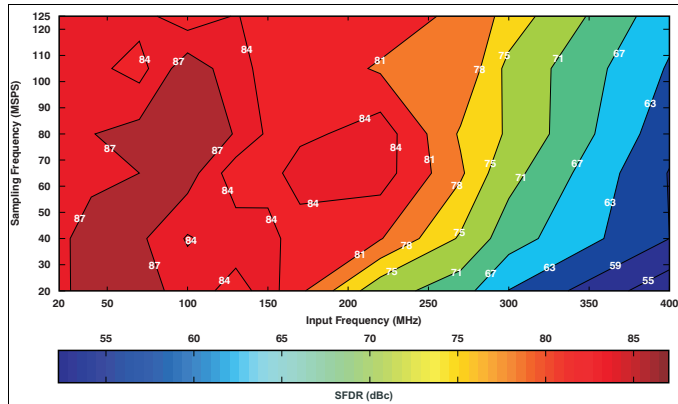


Figure 87. SFDR Across Input and Sampling Frequencies (0-dB Gain)

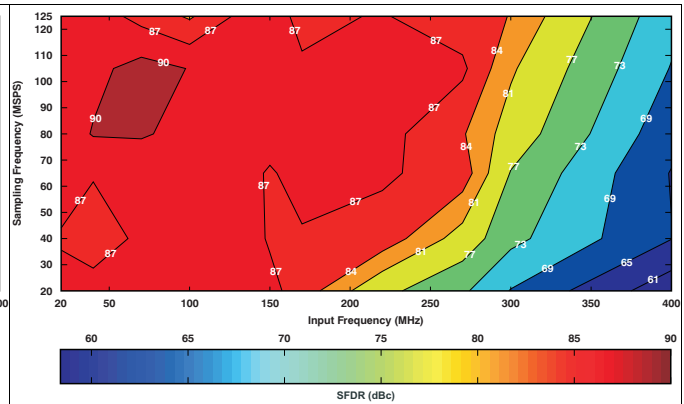


Figure 88. SFDR Across Input and Sampling Frequencies (6-dB Gain)

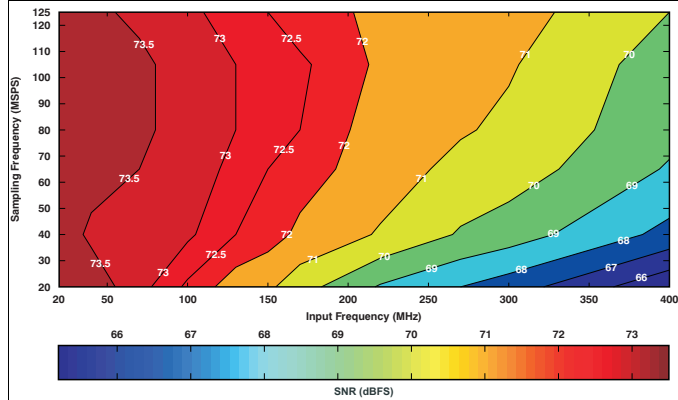


Figure 89. ADS414x: SNR Across Input and Sampling Frequencies (0-dB Gain)

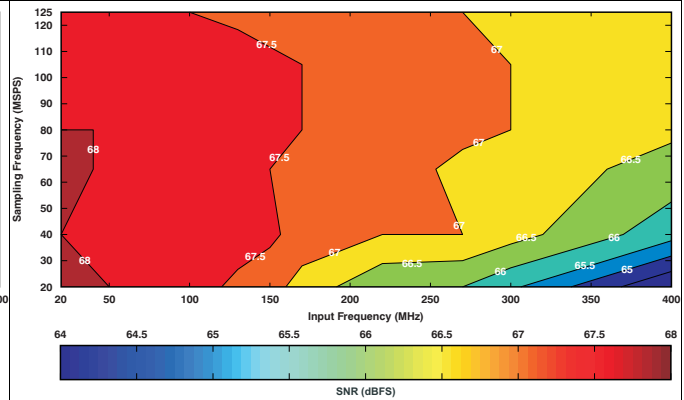


Figure 90. ADS414x: SNR Across Input and Sampling Frequencies (6-dB Gain)

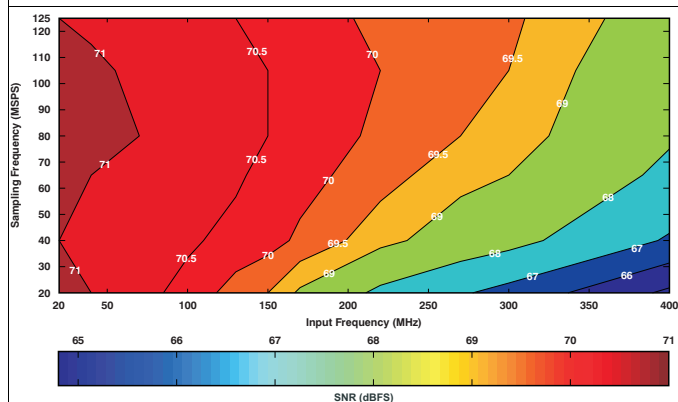


Figure 91. ADS412x SNR Across Input and Sampling Frequencies (0-dB Gain)

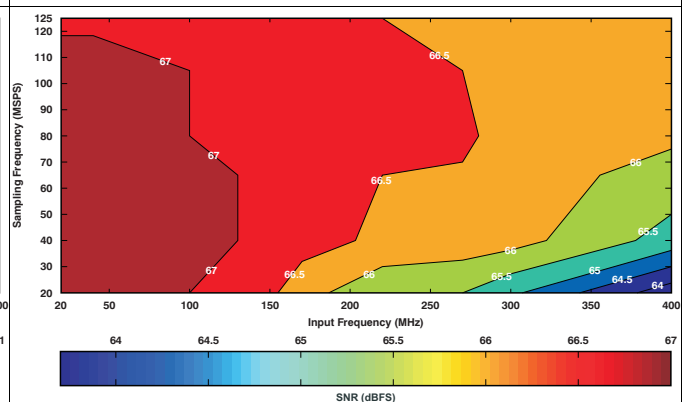


Figure 92. ADS412x SNR Across Input and Sampling Frequencies (6-dB Gain)

8 Detailed Description

8.1 Overview

The ADS412x and ADS414x devices are high-performance, low-power, 12-bit and 14-bit analog-to-digital converters (ADCs) with maximum sampling rates up to 65 MSPS and 125 MSPS. The conversion process is initiated by a rising edge of the external input clock when the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline, resulting in a data latency of 10 clock cycles. The output is available as 12-bit and 14-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

The ADS412x and ADS414x family is pin-compatible to the previous generation [ADS6149](#) family; this architecture enables easy migration. However, there are some important differences between the generations, summarized in [Table 1](#).

Table 1. Migrating from the ADS6149 Family

ADS6149 FAMILY	ADS4145 FAMILY
PINS	
Pin 21 is NC (not connected)	Pin 21 is NC (not connected)
Pin 23 is MODE	Pin 23 is RESERVED in the ADS4145 family. It is reserved as a digital control pin for an (as yet) undefined function in the next-generation ADC series.
SUPPLY	
AVDD is 3.3 V	AVDD is 1.8 V
DRVDD is 1.8 V	No change
INPUT COMMON-MODE VOLTAGE	
VCM is 1.5 V	VCM is 0.95 V
SERIAL INTERFACE	
Protocol: 8-bit register address and 8-bit register data	No change in protocol
	New serial register map
EXTERNAL REFERENCE MODE	
Supported	Not supported
ADS61B49 FAMILY	ADS41B29, ADS41B49, ADS58B18 FAMILY
PINS	
Pin 21 is NC (not connected)	Pin 21 is 3.3 V AVDD_BUF (supply for the analog input buffers)
Pin 23 is MODE	Pin 23 is a digital control pin for the RESERVED function. Pin 23 functions as SNR Boost enable (B18 only).
SUPPLY	
AVDD is 3.3 V	AVDD is 1.8 V, AVDD_BUF is 3.3 V
DRVDD is 1.8 V	No change
INPUT COMMON-MODE VOLTAGE	
VCM is 1.5 V	VCM is 1.7 V
SERIAL INTERFACE	
Protocol: 8-bit register address and 8-bit register data	No change in protocol New serial register map
EXTERNAL REFERENCE MODE	
Supported	Not supported

8.2 Functional Block Diagrams

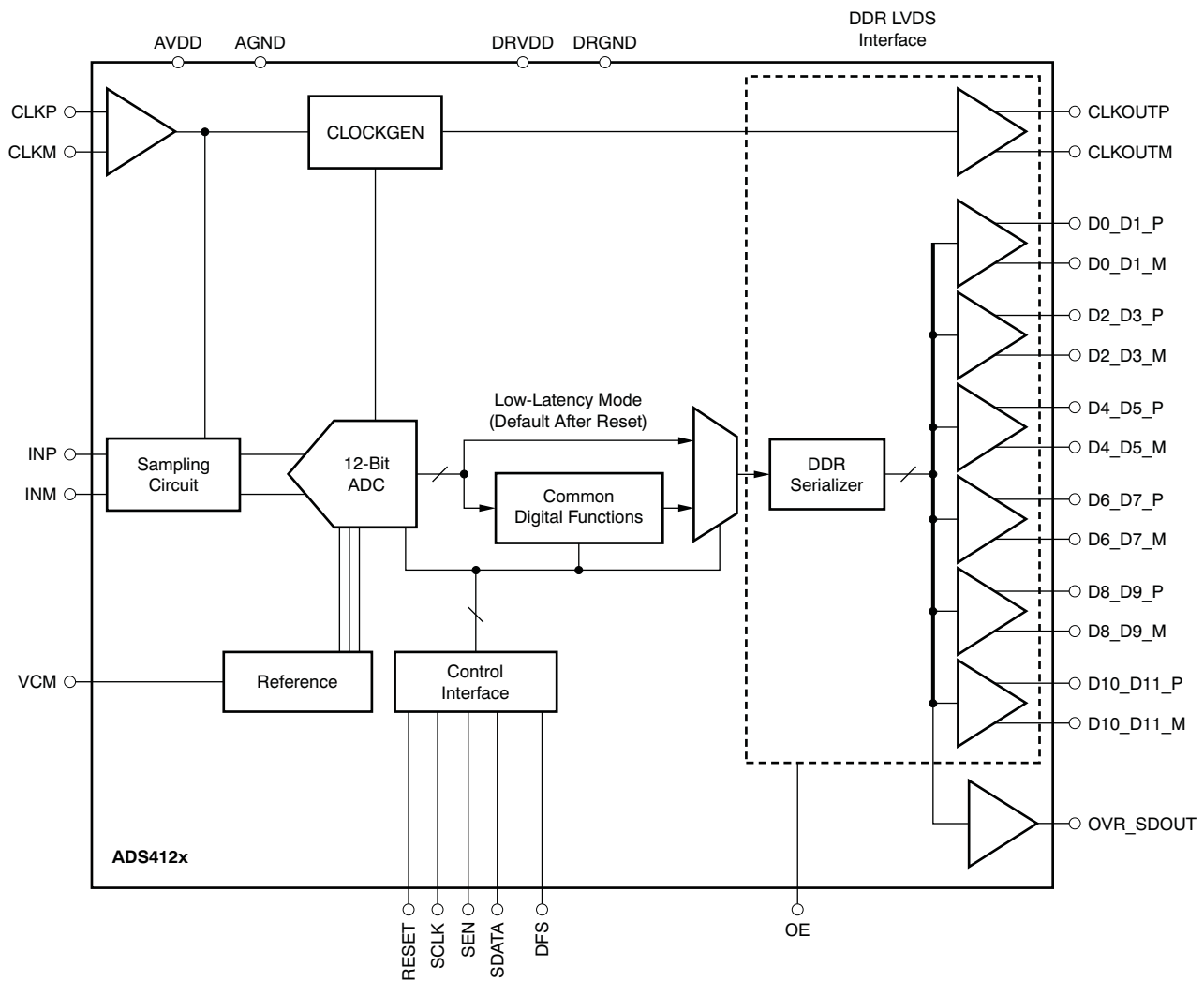


Figure 93. ADS412x Block Diagram

Functional Block Diagrams (continued)

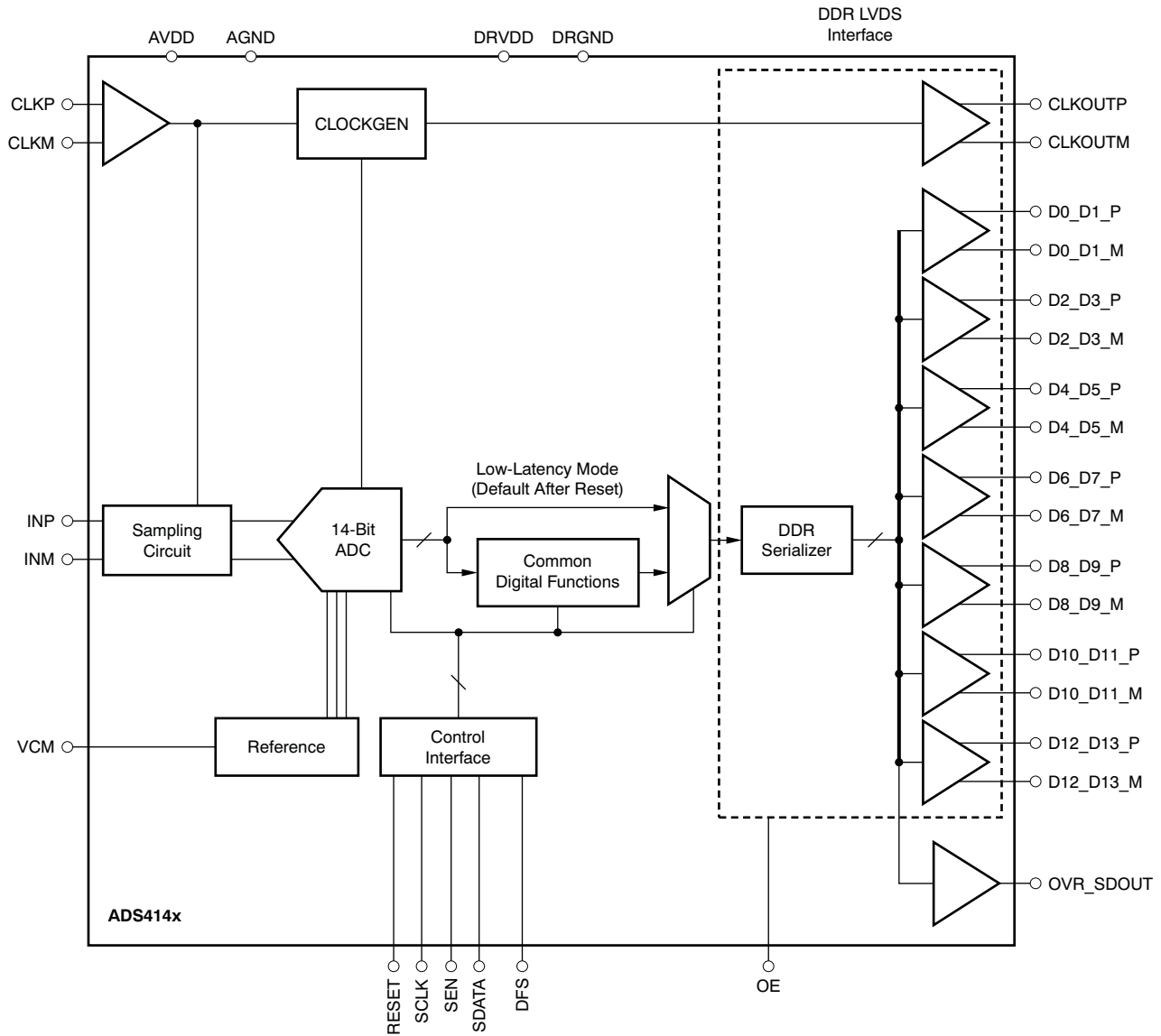


Figure 94. ADS414x Block Diagram

8.3 Feature Description

8.3.1 Digital Functions and Low-Latency Mode

The device has several useful digital functions such as test patterns, gain, and offset correction. All of these functions require extra clock cycles for operation and increase the overall latency and power of the device. Alternately, the device has a low-latency mode in which the raw ADC output is routed to the output data pins with a latency of 10 clock cycles. In this mode, the digital functions are bypassed. [Figure 95](#) shows more details of the processing after the ADC.

The device is in low-latency mode after reset. In order to use any of the digital functions, the low-latency mode must first be disabled by setting the DIS LOW LATENCY register bit to 1. After this process, the respective register bits must be programmed as described in the following sections and in the [Serial Register Map](#) section.

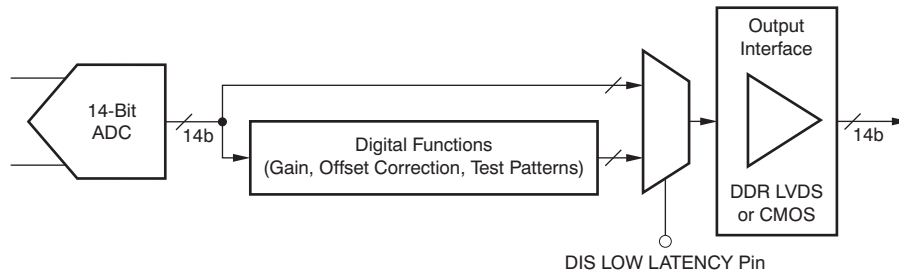


Figure 95. Digital Processing Block Diagram

8.3.2 Gain for SFDR, SNR Trade-Off

The ADS412x and ADS414x include gain settings that can be used to improve SFDR performance. The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in [Table 2](#).

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used to trade-off between SFDR and SNR.

After a reset, the device is in low-latency mode and gain function is disabled. To use gain:

- First, disable the low-latency mode (DIS LOW LATENCY = 1).
- This setting enables the gain and puts the device in a 0-dB gain mode.
- For other gain settings, program the GAIN bits.

Table 2. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V _{PP})
0	Default after reset	2
1	Programmable	1.78
2	Programmable	1.59
3	Programmable	1.42
4	Programmable	1.26
5	Programmable	1.12
6	Programmable	1

8.3.3 Offset Correction

The ADS412x and ADS414x have an internal offset correction algorithm that estimates and corrects dc offset up to ± 10 mV. The correction can be enabled using the EN OFFSET CORR serial register bit. When enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in [Table 3](#).

Table 3. Time Constant of Offset Correction Loop

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_s$ (sec) ⁽¹⁾
0000	1M	8 ms
0001	2M	16 ms
0010	4M	33.4 ms
0011	8M	67 ms
0100	16M	134 ms
0101	32M	268 ms
0110	64M	537 ms
0111	128M	1.08 s
1000	256M	2.15 s
1001	512M	4.3 s
1010	1G	8.6 s
1011	2G	17.2 s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, $f_s = 125$ MSPS.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. When frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by a default after reset.

After a reset, the device is in low-latency mode and offset correction is disabled. To use offset correction:

- First, disable the low-latency mode (DIS LOW LATENCY = 1).
- Then set EN OFFSET CORR to 1 and program the required time constant.

[Figure 96](#) shows the time response of the offset correction algorithm after being enabled.

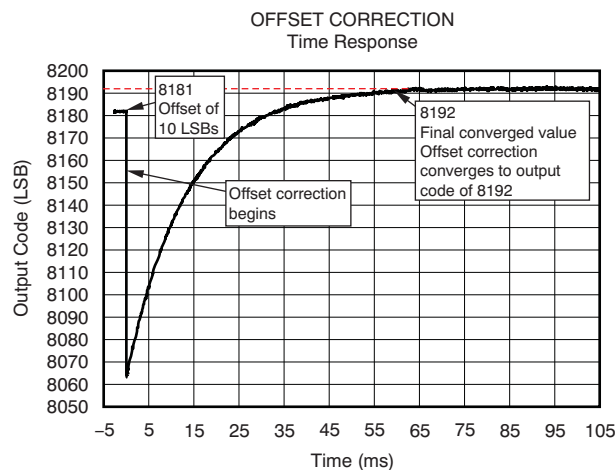


Figure 96. Time Response of Offset Correction

8.3.4 Power-Down

The ADS412x and ADS414x have three power-down modes: power-down global, standby, and output buffer disable.

8.3.4.1 Power-Down Global

In this mode, the entire device (including the ADC, internal reference, and the output buffers) is powered down, resulting in reduced total power dissipation of approximately 10 mW. The output buffers are in a high-impedance state. The wake-up time from the global power-down to data becoming valid in normal mode is typically 100 μ s. To enter the global power-down mode, set the PDN GLOBAL register bit.

8.3.4.2 Standby

In this mode, only the ADC is powered down and the internal references are active, resulting in a fast wake-up time of 5 μ s. The total power dissipation in standby mode is approximately 130 mW at 125 MSPS. To enter the standby mode, set the STBY register bit.

8.3.4.3 Output Buffer Disable

The output buffers can be disabled and put in a high-impedance state; wake-up time from this mode is fast, approximately 100 ns. Disabling the output buffers can be controlled using the PDN OBUF register bit or using the OE pin.

8.3.4.4 Input Clock Stop

In addition, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is approximately 80 mW.

8.3.5 Output Data Format

Two output data formats are supported: twos complement and offset binary. Each mode can be selected using the DATA FORMAT serial interface register bit or controlling the DFS pin in parallel configuration mode. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level.

8.4 Device Functional Modes

8.4.1 Digital Output Information

The ADS412x and ADS414x provide either 14-bit data or 12-bit data, respectively, and an output clock synchronized with the data.

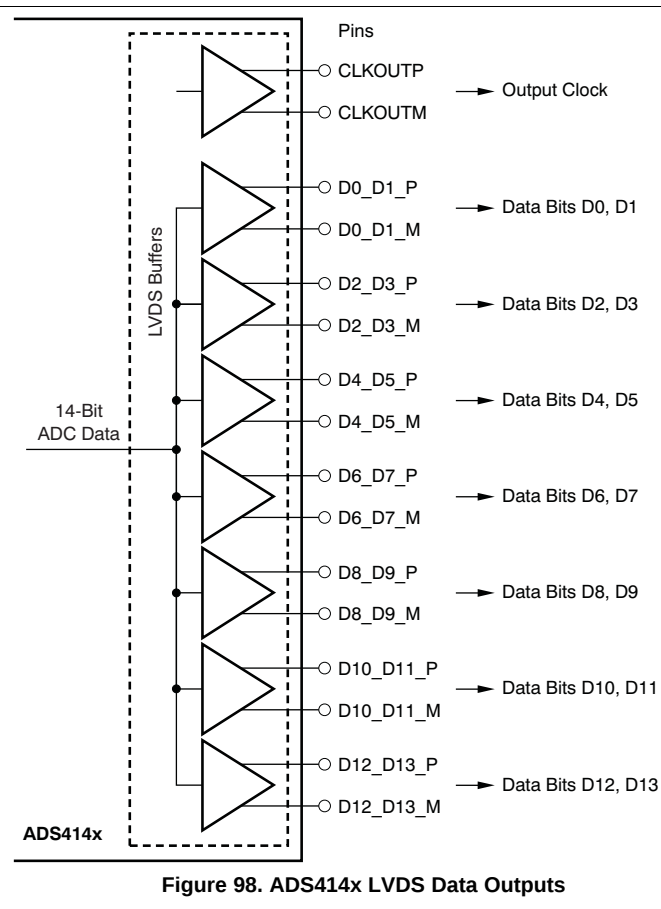
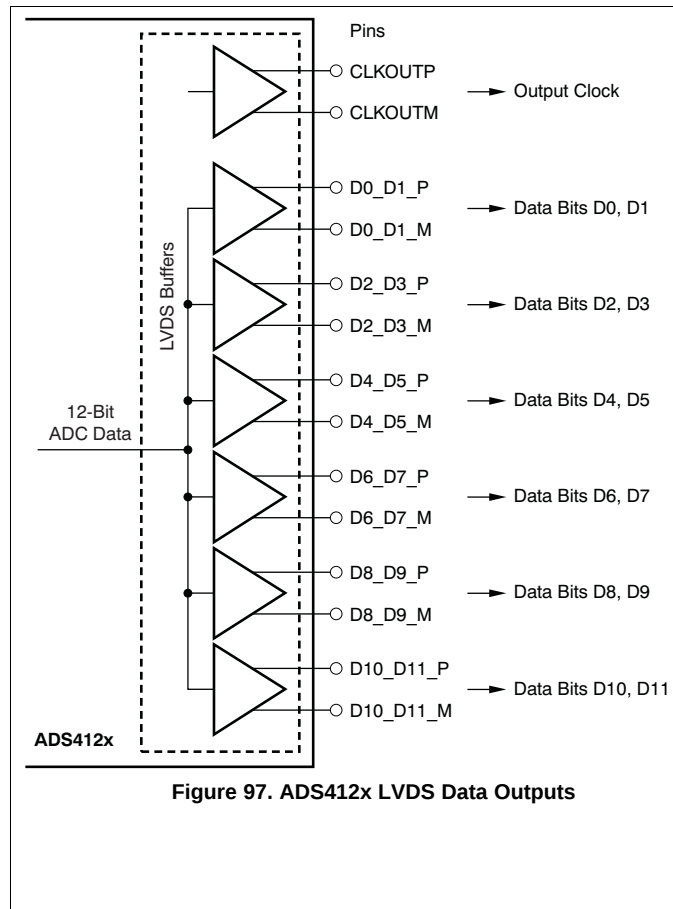
8.4.1.1 Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. These options can be selected using the LVDS CMOS serial interface register bit or using the DFS pin.

Device Functional Modes (continued)

8.4.1.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in [Figure 97](#) and [Figure 98](#).



Device Functional Modes (continued)

Even data bits (D0, D2, D4, and so forth) are output at the falling edge of CLKOUTP and the odd data bits (D1, D3, D5, and so forth) are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all 14 data bits, as shown in [Figure 99](#).

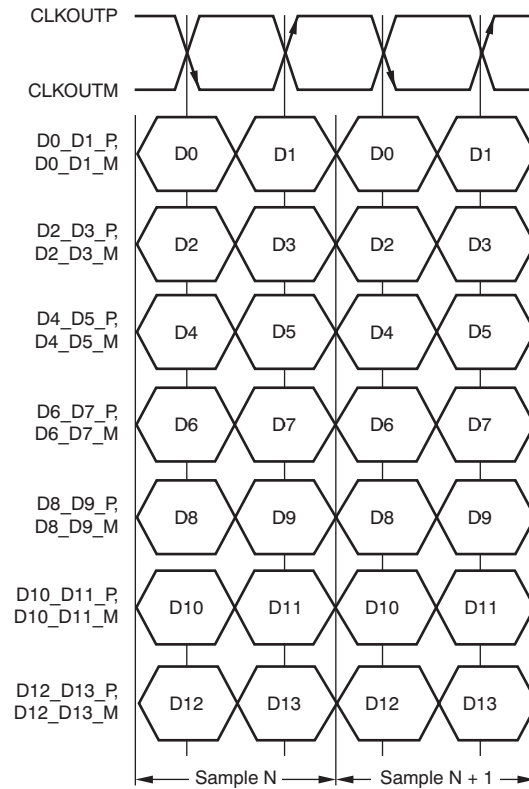


Figure 99. DDR LVDS Interface

Device Functional Modes (continued)

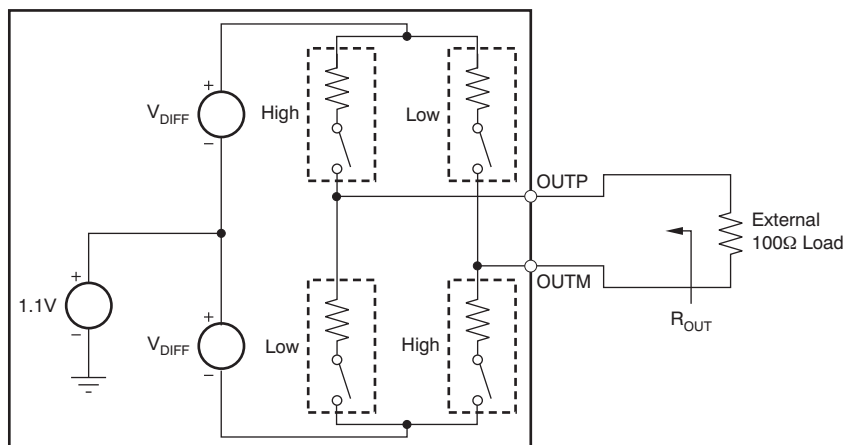
8.4.1.3 LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in [Figure 100](#). After reset, the buffer presents an output impedance of 100 Ω to match with the external 100- Ω termination.

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ± 350 mV with 100- Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ± 125 mV to ± 570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50- Ω differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100- Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, the output impedance of buffer helps improve signal integrity.



Use the default buffer strength to match 100- Ω external termination ($R_{OUT} = 100 \Omega$). To match with a 50- Ω external termination, set the LVDS STRENGTH bit ($R_{OUT} = 50 \Omega$).

Figure 100. LVDS Buffer Equivalent Circuit

Device Functional Modes (continued)

8.4.1.4 Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as the CMOS voltage level, for every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. [Figure 101](#) depicts the CMOS output interface.

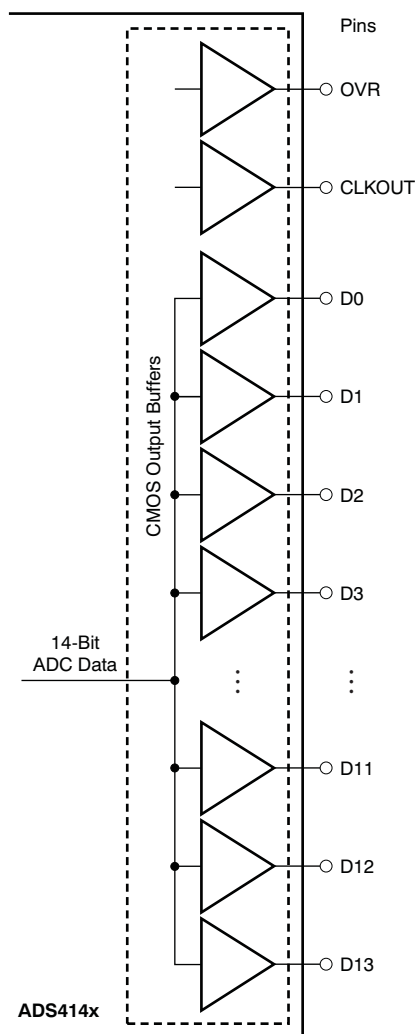


Figure 101. CMOS Output Interface

Device Functional Modes (continued)

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this degradation, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures a wide data stable window. TI recommends using short traces (one to two inches or 2.54 cm to 5.08 cm) terminated with less than 5-pF load capacitance, as shown in [Figure 102](#).

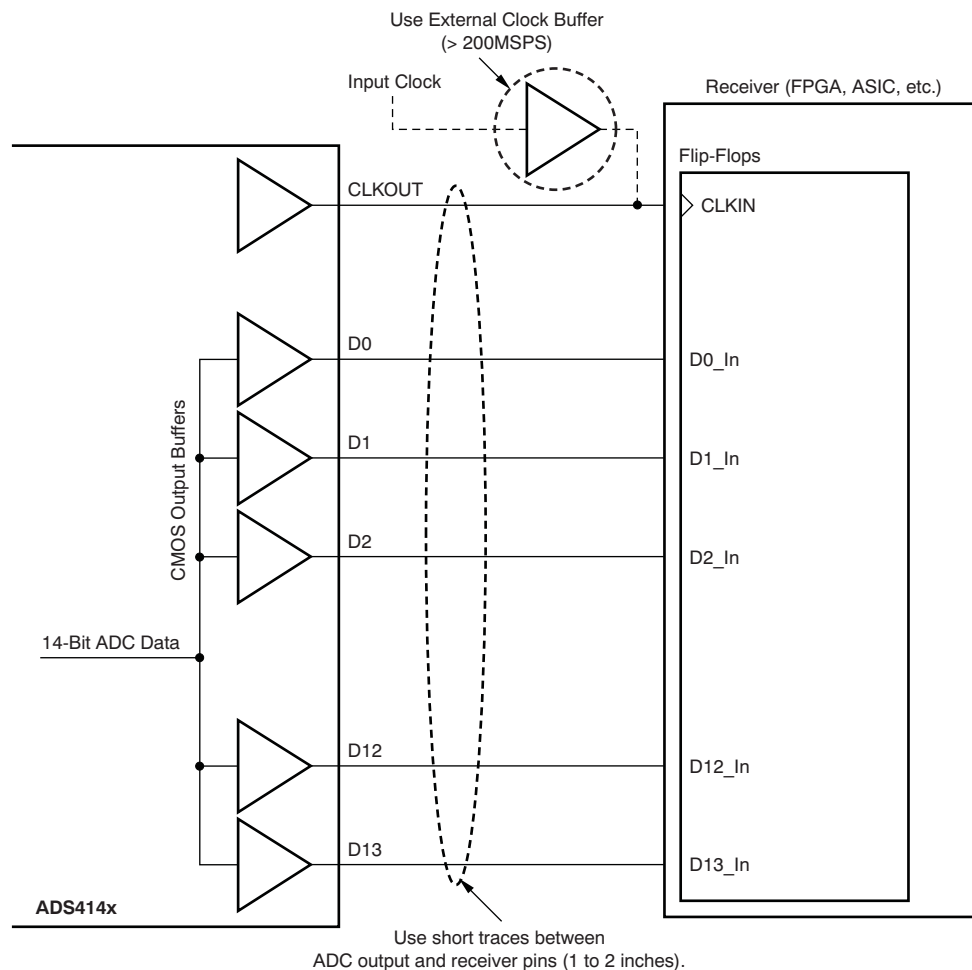


Figure 102. Using the CMOS Data Outputs

8.4.1.5 CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current is determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

$$\text{Digital Current as a Result of CMOS Output Switching} = C_L \times \text{DRVDD} \times (N \times f_{\text{AVG}})$$

where:

C_L = load capacitance,

$N \times F_{\text{AVG}}$ = average number of output bits switching.

(1)

[Figure 86](#) details the current across sampling frequencies at 2-MHz analog input frequency.

8.5 Programming

The performance of the ADS41xx can be enhanced by writing certain SPI registers bits with minimal impact (less than 10 mW) on power consumption. [Table 4](#) lists the device high-performance modes.

Table 4. High-Performance Modes⁽¹⁾⁽²⁾⁽³⁾

PARAMETER	DESCRIPTION
Mode 1	Set the MODE 1 register bits to get best performance across sample clock and input signal frequencies. Register address = 03h, register data = 03h
Mode 2	Set the MODE 2 register bit to get best performance at high input signal frequencies greater than 230 MHz. Register address = 4Ah, register data = 01h

- (1) TI recommends using these modes to obtain best performance. These modes can be set using the serial interface only.
(2) See the [Serial Interface](#) section for details on register programming.
(3) Note that these modes cannot be set when the serial interface is not used (when the RESET pin is tied high); see the [Device Configuration](#) section.

8.5.1 Device Configuration

The ADS412x and ADS414x have several modes that can be configured using a serial programming interface, as described in [Table 5](#), [Table 6](#), and [Table 7](#). In addition, the devices have two dedicated parallel pins for quickly configuring commonly used functions. The parallel pins are DFS (analog 4-level control pin) and OE (digital control pin). The analog control pins can be easily configured using a simple resistor divider (with 10% tolerance resistors).

Table 5. DFS: Analog Control Pin

VOLTAGE APPLIED ON DFS	DESCRIPTION (Data Format, Output Interface)
0, 100 mV, –0 mV	Twos complement, DDR LVDS
(3/8) AVDD ± 100 mV	Twos complement, parallel CMOS
(5/8) AVDD ± 100 mV	Offset binary, parallel CMOS
AVDD, 0 mV, –100 mV	Offset binary, DDR LVDS

Table 6. OE: Digital Control Pin

VOLTAGE APPLIED ON OE	DESCRIPTION
0	Output data buffers disabled
AVDD	Output data buffers enabled

When the serial interface is not used, the SDATA pin can also be used as a digital control pin to place the device in standby mode. To enable this functionality, the RESET pin must be tied high. In this mode, SEN and SCLK do not have any alternative functions. Keep SEN tied high and SCLK tied low on the board.

Table 7. SDATA: Digital Control Pin

VOLTAGE APPLIED ON SDATA	DESCRIPTION
0	Normal operation
Logic high	Device enters standby

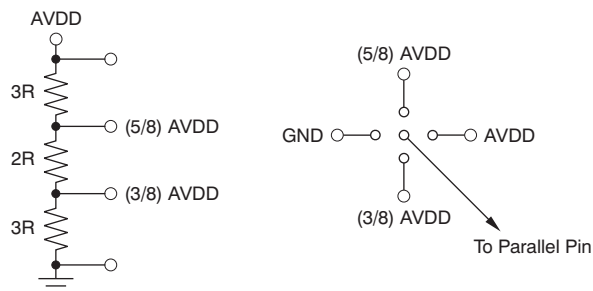


Figure 103. Simplified Diagram to Configure the DFS Pin

8.5.2 Serial Interface

The analog-to-digital converter (ADC) has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every falling edge of SCLK when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (a few hertz) and also with a non-50% SCLK duty cycle.

8.5.2.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

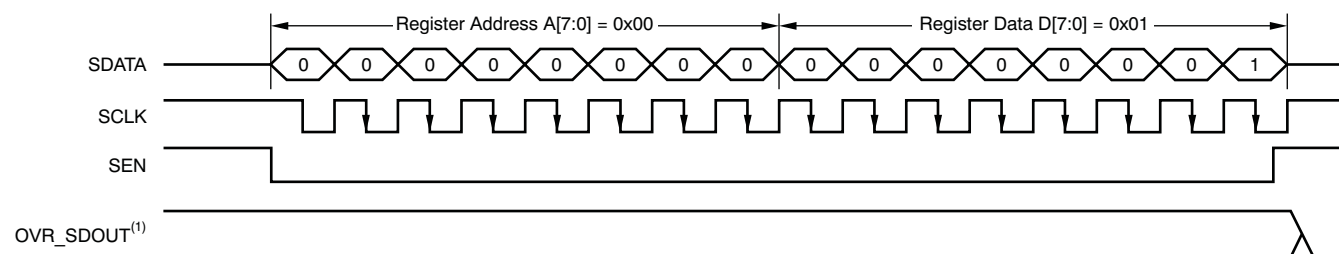
1. Either through hardware reset by applying a high pulse on RESET pin (of durations greater than 10 ns), as shown in [Figure 5](#); or
2. By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

8.5.3 Serial Register Readout

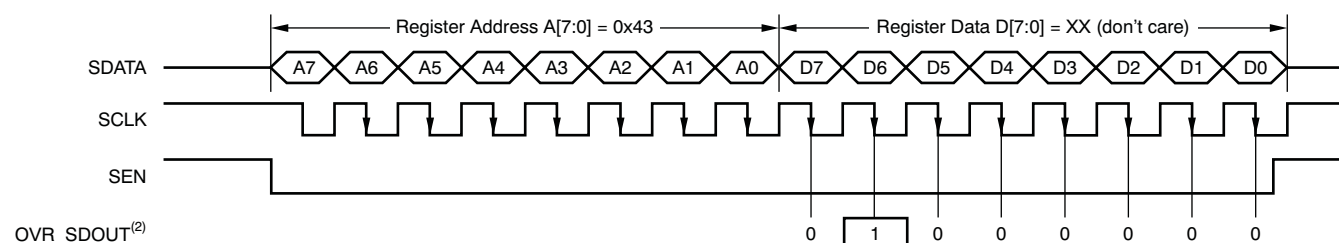
The serial register readout function allows the contents of the internal registers to be read back on the OVR_SDOUT pin. This readback may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

After power-up and device reset, the OVR_SDOUT pin functions as an over-range indicator pin by default. When the readout mode is enabled, OVR_SDOUT outputs the contents of the selected register serially:

1. Set the READOUT register bit to 1. This setting puts the device in serial readout mode and disables any further writes to the internal registers **except** the register at address 0. Note that the READOUT bit itself is also located in register 0. The device can exit readout mode by writing READOUT = 0. Only the contents of the register at address 0 cannot be read in the register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content must be read.
3. The device serially outputs the contents (D7 to D0) of the selected register on the OVR_SDOUT pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To exit the serial readout mode, the reset register bit READOUT = 0 enables writes into all registers of the device. At this point, the OVR_SDOUT pin becomes an over-range indicator pin.



a) Enable Serial Readout (READOUT = 1)



b) Read Contents of Register 0x43. This Register Has Been Initialized with 0x40 (device is put into global power-down mode).

The OVR_SDOUT pin functions as OVR (READOUT = 0).

The OVR_SDOUT pin functions as a serial readout (READOUT = 1).

Figure 104. Serial Readout Timing Diagram

8.6 Register Maps

8.6.1 Serial Register Map

Table 8 summarizes the functions supported by the serial interface.

Table 8. Serial Interface Register Map⁽¹⁾

REGISTER ADDRESS	DEFAULT VALUE AFTER RESET	REGISTER DATA							
A[7:0] (Hex)	D[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	00	0	0	0	0	0	0	RESET	READOUT
01	00	LVDS SWING						0	0
03	00	0	0	0	0	0	0	HIGH PERF MODE 1	
25	00	GAIN				DISABLE GAIN	TEST PATTERNS		
26	00	0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH
3D	00	DATA FORMAT		EN OFFSET CORR	0	0	0	0	0
3F	00	CUSTOM PATTERN HIGH D[13:6]							
40	00	CUSTOM PATTERN D[5:0]						0	0
41	00	LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL
42	00	CLKOUT FALL POSN		0	0	DIS LOW LATENCY	STBY	0	0
43	00	0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	
4A	00	0	0	0	0	0	0	0	HIGH PERF MODE 2
BF	00	OFFSET PEDESTAL						0	0
CF	00	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
DF	00	0	0	LOW SPEED		0	0	0	0

(1) Multiple functions in a register can be programmed in a single write operation.

8.6.2 Description of Serial Registers

For best performance, two special mode register bits must be enabled: HI PERF MODE 1 and HI PERF MODE 2.

Table 9. Register Address 00h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits[7:2] Always write 0

Bit 1 RESET: Software reset applied

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 READOUT: Serial readout

This bit sets the serial readout of the registers.

0 = Serial readout of registers disabled; the OVR_SDOOUT pin functions as an overvoltage indicator.

1 = Serial readout enabled; the OVR_SDOOUT pin functions as a serial data readout.

Table 10. Register Address 01h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits[7:2] LVDS SWING: LVDS swing programmability⁽¹⁾

000000 = Default LVDS swing; ± 350 mV with external 100- Ω termination

011011 = LVDS swing *increases* to ± 410 mV

110010 = LVDS swing *increases* to ± 465 mV

010100 = LVDS swing *increases* to ± 570 mV

111110 = LVDS swing *decreases* to ± 200 mV

001111 = LVDS swing *decreases* to ± 125 mV

Bits[1:0] Always write 0

(1) The EN LVDS SWING register bits must be set to enable LVDS swing control.

Table 11. Register Address 03h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HI PERF MODE 1	

Bits[7:2] Always write 0

Bits[1:0] HI PERF MODE 1: High performance mode 1

00 = Default performance after reset

01 = Do not use

10 = Do not use

11 = For best performance across sampling clock and input signal frequencies, set the HIGH PERF MODE 1 bits

Table 12. Register Address 25h (Default = 00h)

7	6	5	4	3	2	1	0
GAIN				DISABLE GAIN	TEST PATTERNS		

Bits[7:4] GAIN: Gain programmability

These bits set the gain programmability in 0.5-dB steps.

0000 = 0-dB gain (default after reset)

0001 = 0.5-dB gain

0010 = 1.0-dB gain

0011 = 1.5-dB gain

0100 = 2.0-dB gain

0101 = 2.5-dB gain

0110 = 3.0-dB gain

0111 = 3.5-dB gain

1000 = 4.0-dB gain

1001 = 4.5-dB gain

1010 = 5.0-dB gain

1011 = 5.5-dB gain

1100 = 6-dB gain

Bit 3 DISABLE GAIN: Gain setting

This bit sets the gain.

0 = Gain enabled; gain is set by the GAIN bits only if low-latency mode is disabled

1 = Gain disabled

Bits[2:0] TEST PATTERNS: Data capture

These bits verify data capture.

000 = Normal operation

001 = Outputs all 0s

010 = Outputs all 1s

011 = Outputs toggle pattern

In the ADS4122/25, output data D[11:0] is an alternating sequence of 010101010101 and 101010101010.

In the ADS4142/45, output data D[13:0] is an alternating sequence of 01010101010101 and 10101010101010.

100 = Outputs digital ramp

In ADS4122/25, output data increments by one LSB (12-bit) every fourth clock cycle from code 0 to code 4095

In ADS4142/45, output data increments by one LSB (14-bit) every clock cycle from code 0 to code 16383

101 = Output custom pattern (use registers 3Fh and 40h for setting the custom pattern)

110 = Unused

111 = Unused

Table 13. Register Address 26h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH

Bits[7:2] Always write 0

Bit 1 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength

This bit determines the external termination to be used with the LVDS output clock buffer.

0 = 100-Ω external termination (default strength)

1 = 50-Ω external termination (2x strength)

Bit 0 LVDS DATA STRENGTH: LVDS data buffer strength

This bit determines the external termination to be used with all of the LVDS data buffers.

0 = 100-Ω external termination (default strength)

1 = 50-Ω external termination (2x strength)

Table 14. Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
DATA FORMAT		EN OFFSET CORR	0	0	0	0	0

Bits[7:6] DATA FORMAT: Data format selection

These bits selects the data format.

00 = The DFS pin controls data format selection

10 = Twos complement

11 = Offset binary

Bit 5 ENABLE OFFSET CORR: Offset correction setting

This bit sets the offset correction.

0 = Offset correction disabled

1 = Offset correction enabled

Bits[4:0] Always write 0

Table 15. Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8	CUSTOM PATTERN D7	CUSTOM PATTERN D6

Bits[7:0] CUSTOM PATTERN⁽¹⁾

These bits set the custom pattern.

(1) For the ADS414x, output data bits 13 to 0 are CUSTOM PATTERN D[13:0]. For the ADS412x, output data bits 11 to 0 are CUSTOM PATTERN D[13:2].

Table 16. Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0	0	0

Bits[7:2] CUSTOM PATTERN⁽¹⁾

These bits set the custom pattern.

Bits[1:0] Always write 0

(1) For the ADS414x, output data bits 13 to 0 are CUSTOM PATTERN D[13:0]. For the ADS412x, output data bits 11 to 0 are CUSTOM PATTERN D[13:2].

Table 17. Register Address 41h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL

Bits[7:6] LVDS CMOS: Interface selection

These bits select the interface.

00 = The DFS pin controls the selection of either LVDS or CMOS interface

10 = The DFS pin controls the selection of either LVDS or CMOS interface

01 = DDR LVDS interface

11 = Parallel CMOS interface

Bits[5:4] CMOS CLKOUT STRENGTH

Controls strength of CMOS output clock only.

00 = Maximum strength (recommended and used for specified timings)

01 = Medium strength

10 = Low strength

11 = Very low strength

Bit 3 ENABLE CLKOUT RISE

0 = Disables control of output clock rising edge

1 = Enables control of output clock rising edge

Bits[2:1] CLKOUT RISE POSN: CLKOUT rise control

Controls position of output clock rising edge

LVDS interface:

00 = Default position (timings are specified in this condition)

01 = Setup reduces by 500 ps, hold increases by 500 ps

10 = Data transition is aligned with rising edge

11 = Setup reduces by 200 ps, hold increases by 200 ps

CMOS interface:

00 = Default position (timings are specified in this condition)

01 = Setup reduces by 100 ps, hold increases by 100 ps

10 = Setup reduces by 200 ps, hold increases by 200 ps

11 = Setup reduces by 1.5 ns, hold increases by 1.5 ns

Bit 0 **ENABLE CLKOUT FALL**

0 = Disables control of output clock fall edge

1 = Enables control of output clock fall edge

Table 18. Register Address 42h (Default = 00h)

7	6	5	4	3	2	1	0
CLKOUT FALL CTRL		0	0	DIS LOW LATENCY	STBY	0	0

Bits[7:6] **CLKOUT FALL CTRL**

Controls position of output clock falling edge

LVDS interface:

00 = Default position (timings are specified in this condition)

01 = Setup reduces by 400 ps, hold increases by 400 ps

10 = Data transition is aligned with rising edge

11 = Setup reduces by 200 ps, hold increases by 200 ps

CMOS interface:

00 = Default position (timings are specified in this condition)

01 = Falling edge is advanced by 100 ps

10 = Falling edge is advanced by 200 ps

11 = Falling edge is advanced by 1.5 ns

Bits[5:4] Always write 0

Bit 3 **DIS LOW LATENCY: Disable low latency**

This bit disables low-latency mode,

0 = Low-latency mode is enabled. Digital functions such as gain, test patterns and offset correction are disabled

1 = Low-latency mode is disabled. This setting enables the digital functions. See the [Digital Functions and Low Latency Mode](#) section.

Bit 2 **STBY: Standby mode**

This bit sets the standby mode.

0 = Normal operation

1 = Only the ADC and output buffers are powered down; internal reference is active; wake-up time from standby is fast

Bits[1:0] Always write 0

Table 19. Register Address 43h (Default = 00h)

7	6	5	4	3	2	1	0
0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	

Bit 0 Always write 0

Bit 6 PDN GLOBAL: Power-down

This bit sets the state of operation.

0 = Normal operation

1 = Total power down; the ADC, internal references, and output buffers are powered down; slow wake-up time.

Bit 5 Always write 0

Bit 4 PDN OBUF: Power-down output buffer

This bit set the output data and clock pins.

0 = Output data and clock pins enabled

1 = Output data and clock pins powered down and put in high- impedance state

Bits[3:2] Always write 0

Bits[1:0] EN LVDS SWING: LVDS swing control

00 = LVDS swing control using LVDS SWING register bits is disabled

01 = Do not use

10 = Do not use

11 = LVDS swing control using LVDS SWING register bits is enabled

Table 20. Register Address 4Ah (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HI PERF MODE 2

Bits[7:1] Always write 0

Bit[0] HI PERF MODE 2: High performance mode 2

This bit is recommended for high input signal frequencies greater than 230 MHz.

0 = Default performance after reset

1 = For best performance with high-frequency input signals, set the HIGH PERF MODE 2 bit

Table 21. Register Address BFh (Default = 00h)

7	6	5	4	3	2	1	0
OFFSET PEDESTAL						0	0

Bits[7:2] OFFSET PEDESTAL

These bits set the offset pedestal.

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits.

ADS414x VALUE
PEDESTAL

011111

31 LSB

011110

30 LSB

011101

29 LSB

—

—

000000

0 LSB

—

—

111111

–1 LSB

111110

–2 LSB

—

—

100000

–32 LSB

Bits[1:0] Always write 0

Table 22. Register Address CFh (Default = 00h)

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit 7 FREEZE OFFSET CORR

This bit sets the freeze offset correction.

0 = Estimation of offset correction is not frozen (bit EN OFFSET CORR must be set)

1 = Estimation of offset correction is frozen (bit EN OFFSET CORR must be set). When frozen, the last estimated value is used for offset correction every clock cycle. See the [Offset Correction](#) section.

Bit 6 Always write 0

Bits[5:2] OFFSET CORR TIME CONSTANT

These bits set the offset correction time constant for the correction loop time constant in number of clock cycles.

VALUE
TIME CONSTANT (Number of Clock Cycles)

0000

1M

0001

2M

0010

4M

0011

8M

0100

16M

0101

32M

0110

64M

0111

128M

1000

256M

1001

512M

1010

1G

1011

2G

Bits[1:0] Always write 0

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Table 23. Register Address DFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	LOW SPEED		0	0	0	0

Bits[7:6] Always write 0

Bits[5:4] LOW SPEED: Low-speed mode

For the ADS4122/42, the low-speed mode is enabled by default after reset.

00, 01, 10, 11 = Do not use

For the ADS4125/55 only:

00, 01, 10 = Low-speed mode disabled (default state after reset); this setting is recommended for sampling rates greater than 80 MSPS.

11 = Low-speed mode enabled; this setting is recommended for sampling rates less than or equal to 80 MSPS.

Bits[3:0] Always write 0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS412x and ADS414x are lower sampling speed members of the ADS41xx family of ultra-low-power analog-to-digital converters (ADCs). The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 10 clock cycles. The output is available as 14-bit data or 12-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary two's complement format.

9.1.1 Analog Input

The analog input consists of a switched-capacitor-based, differential, sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input INP and INM pin must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage). [Figure 105](#) shows an equivalent circuit for the analog input.

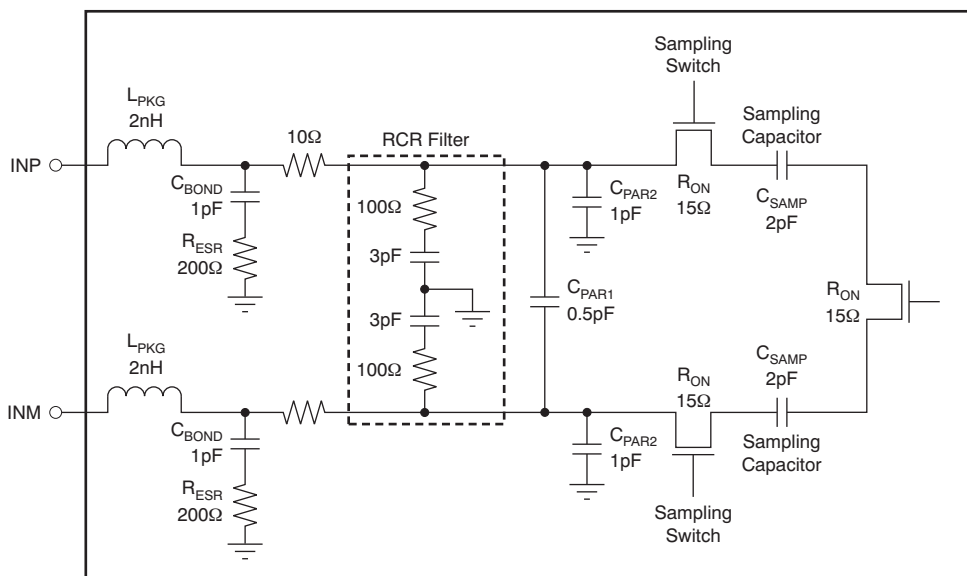


Figure 105. Analog Input Equivalent Circuit

9.1.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics. Low impedance (less than 50 Ω) must be present for the common-mode switching currents. This impedance can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

Application Information (continued)

Note that the device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but also reduces the input bandwidth and the maximum input frequency that can be supported. On the other hand, with no internal R-C filter, high input frequency can be supported but now the sampling glitches must be supplied by the external driving circuit. The inductance of the package bond wires limits the ability of the external driving circuit to support the sampling glitches.

In the ADS412x and ADS414x, the R-C component values are optimized when supporting high input bandwidth (550 MHz). However, in applications where very high input frequency support is not required, filtering of the glitches can be improved further with an external R-C-R filter; see [Figure 108](#) and [Figure 109](#).

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. When designing the drive circuit, the ADC impedance must be considered. [Figure 106](#) and [Figure 107](#) show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) looking into the ADC input pins.

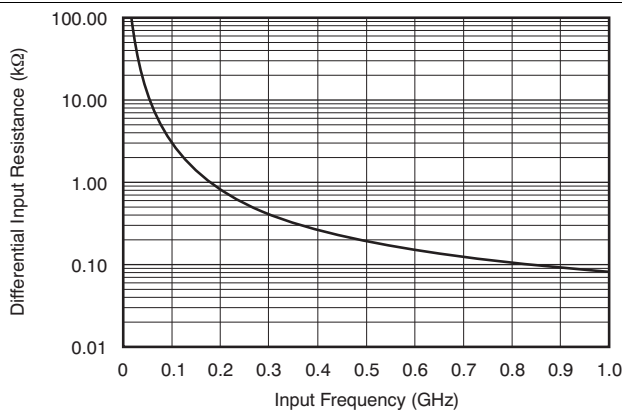


Figure 106. ADC Analog Input Resistance (R_{IN}) Across Frequency

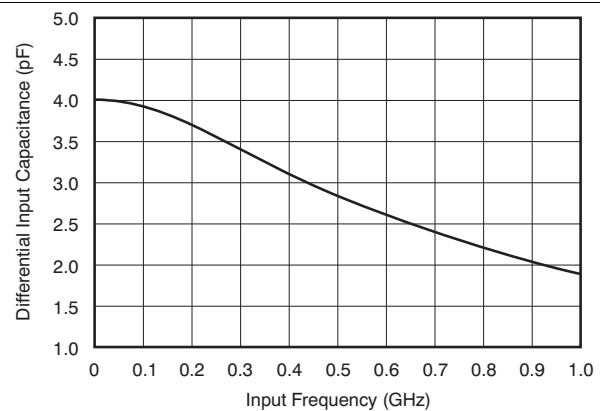


Figure 107. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Application Information (continued)

9.1.1.2 Driving Circuit

Two example driving circuit configurations are shown in [Figure 108](#) and [Figure 109](#)—one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies. In [Figure 108](#), an external R-C-R filter with 3.3 pF is used to help absorb sampling glitches. The R-C-R filter limits the bandwidth of the drive circuit, making the drive circuit suitable for low input frequencies (up to 250 MHz). Transformers such as ADT1-1WT or WBC1-1 can be used up to 250 MHz.

For higher input frequencies, the R-C-R filter can be dropped. Together with the lower series resistors (5 Ω to 10 Ω), this drive circuit provides higher bandwidth to support frequencies up to 500 MHz (as shown in [Figure 109](#)). A transmission line transformer such as ADTL2-18 can be used.

Note that both the drive circuits have been terminated by 50 Ω near the ADC side. The termination is accomplished by a 25- Ω resistor from each input to the 0.95-V common-mode (VCM) from the device. This termination allows the analog inputs to be biased around the required common-mode voltage.

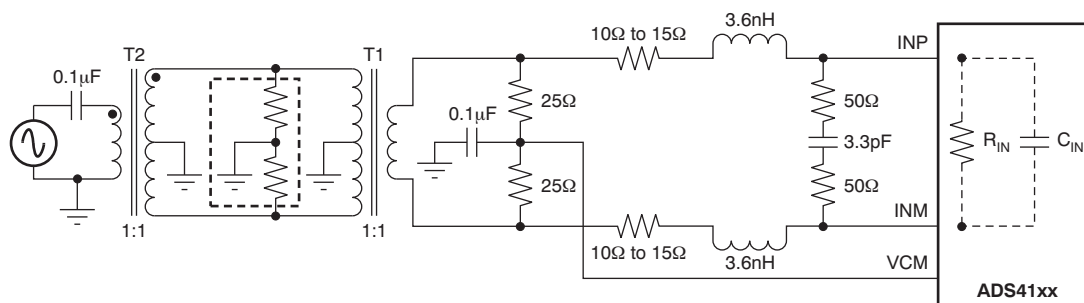


Figure 108. Drive Circuit With Low Bandwidth (for Low Input Frequencies)

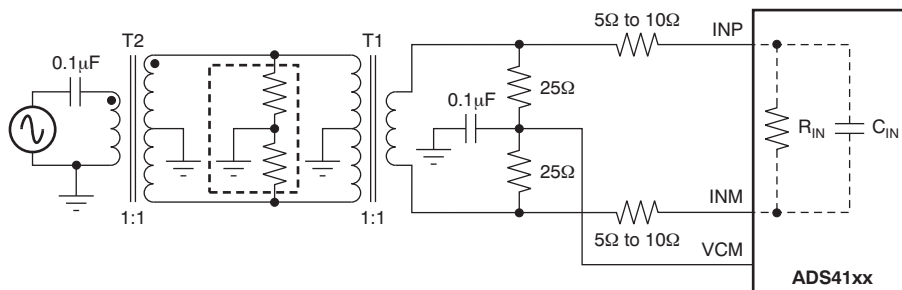


Figure 109. Drive Circuit With High Bandwidth (for High Input Frequencies)

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in [Figure 108](#) and [Figure 109](#). The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50- Ω source impedance).

[Figure 108](#) and [Figure 109](#) use 1:1 transformers with a 50- Ω source. As explained in the [Drive Circuit Requirements](#) section, this architecture helps to present a low source impedance to absorb sampling glitches. With a 1:4 transformer, the source impedance is 200 Ω . The higher source impedance is unable to absorb the sampling glitches effectively and can lead to degradation in performance (compared to using 1:1 transformers).

Application Information (continued)

In almost all cases, either a band-pass or low-pass filter is needed to obtain the desired dynamic performance, as shown in Figure 110. Such a filter presents low source impedance at the high frequencies corresponding to the sampling glitch and helps avoid the performance loss with the high source impedance.

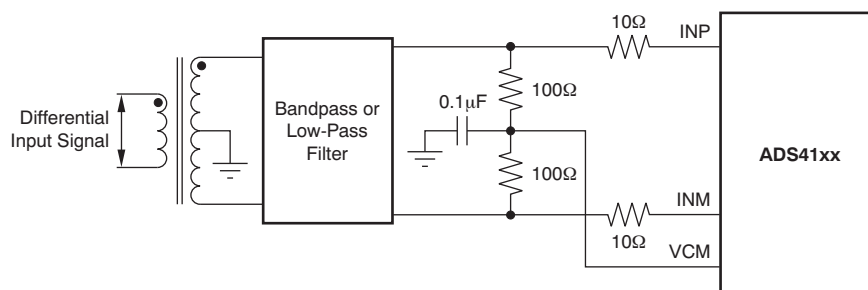


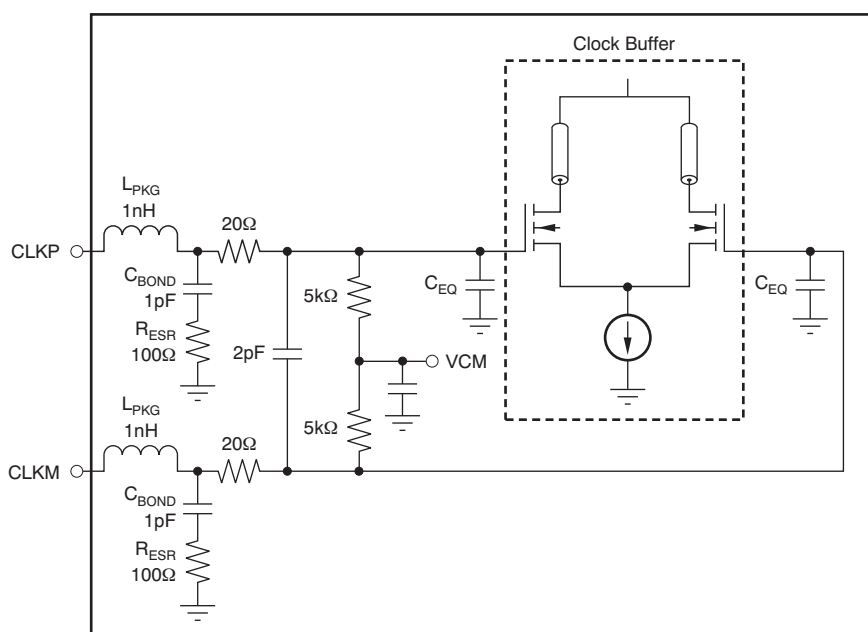
Figure 110. Drive Circuit With 1:4 Transformer

9.1.1.3 Input Common-Mode

To ensure a low-noise, common-mode reference, the VCM pin is filtered with a 0.1-μF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. Each ADC input pin sinks a common-mode current of approximately 0.6 μA per MSPS of clock frequency.

9.1.2 Clock Input

The ADS412x and ADS414x clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 111 shows an equivalent circuit for the input clock.



NOTE: C_{EQ} is 1 pF to 3 pF, and is the equivalent input capacitance of the clock buffer.

Figure 111. Input Clock Equivalent Circuit

Application Information (continued)

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1- μ F capacitor, as shown in Figure 112. For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 113 shows a differential circuit.

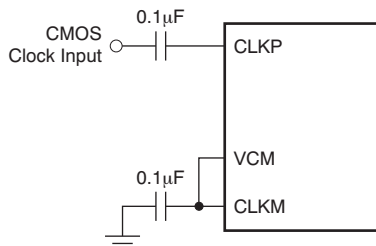


Figure 112. Single-Ended Clock Driving Circuit

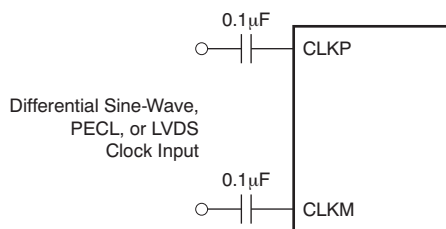


Figure 113. Differential Clock Driving Circuit

9.1.3 Input Overvoltage Indication (OVR Pin)

The device has an OVR pin that provides information about analog input overload. At any clock cycle, if the sampled input voltage exceeds the positive or negative full-scale range, the OVR pin goes high. The OVR remains high as long as the overload condition persists. The OVR pin is a CMOS output buffer (running off DRVDD supply), independent of the type of output data interface (DDR, LVDS, or CMOS).

For a positive overload, the D[13:0] output data bits are 3FFFh in offset binary output format and 1FFFh in twos complement output format. For a negative input overload, the output code is 0000h in offset binary output format and 2000h in twos complement output format.

Application Information (continued)

9.1.4 Using the ADS41xx at Low Sampling Rates

When ADS41xx is used at lower sampling rates (< 20 MSPS), set the LOW SPEED register bit (address DFh, bit[5:4]). At low sampling rates, use the device in CMOS interface mode which saves power and results in better setup and hold time compared to LVDS interface mode.

9.1.4.1 ADS412x (12-Bit Device)

ADS412x, 12-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted

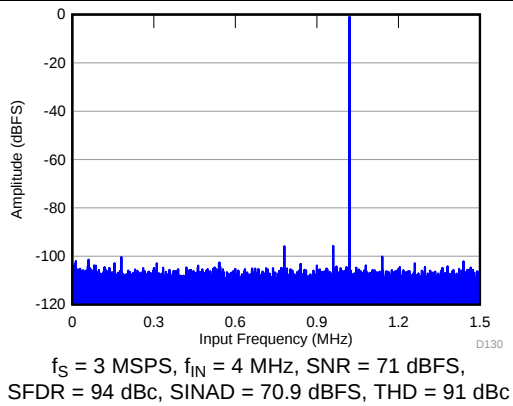


Figure 114. FFT for 3-MSPS Sampling Speed

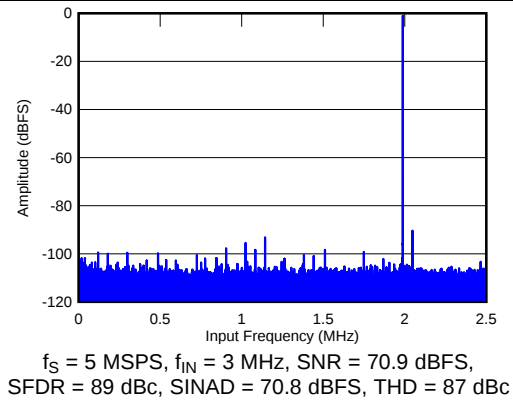


Figure 115. FFT for 5-MSPS Sampling Speed

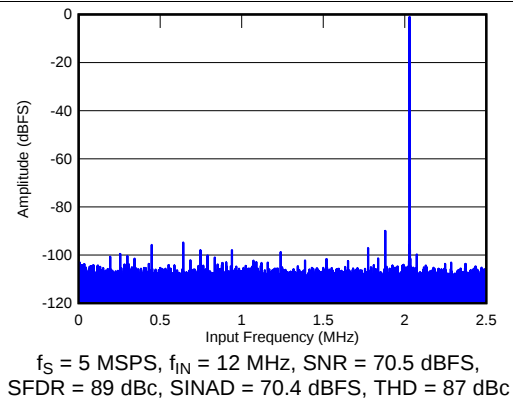


Figure 116. FFT for 5-MSPS Sampling Speed

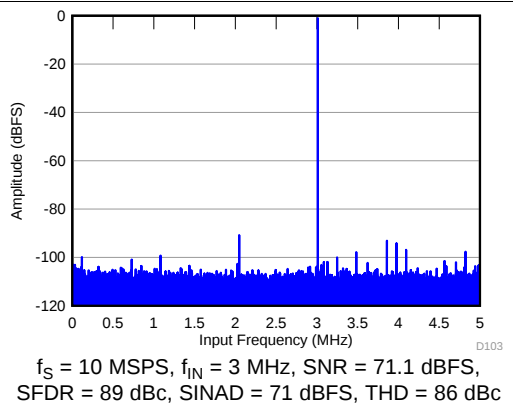
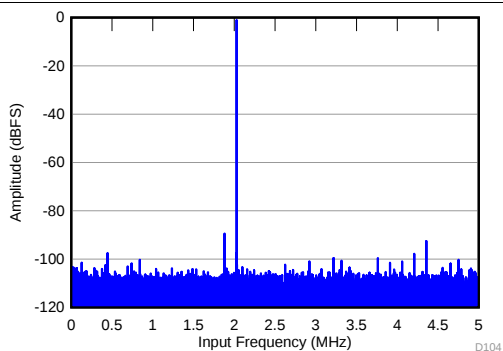


Figure 117. FFT for 10-MSPS Sampling Speed

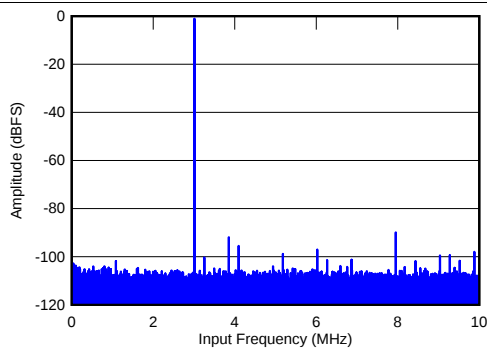
Application Information (continued)

ADS412x, 12-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted



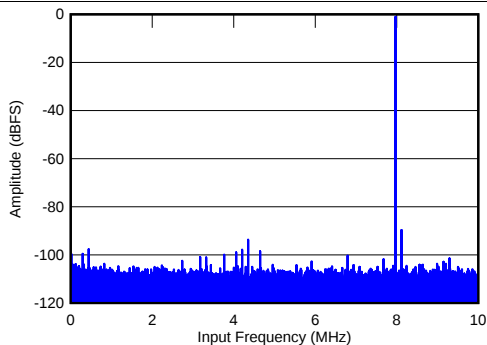
$f_S = 10$ MSPS, $f_{IN} = 12$ MHz, SNR = 70.9 dBFS, SFDR = 88 dBc, SINAD = 70.8 dBFS, THD = 86 dBc

Figure 118. FFT for 10-MSPS Sampling Speed



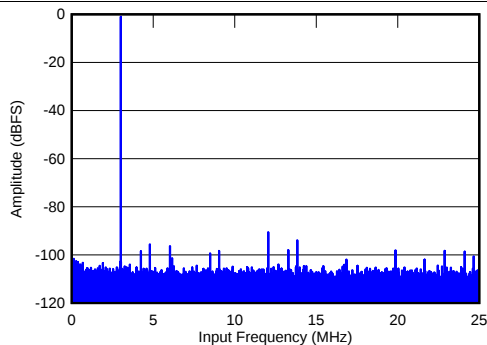
$f_S = 20$ MSPS, $f_{IN} = 3$ MHz, SNR = 71.1 dBFS, SFDR = 89 dBc, SINAD = 71 dBFS, THD = 87 dBc

Figure 119. FFT for 20-MSPS Sampling Speed



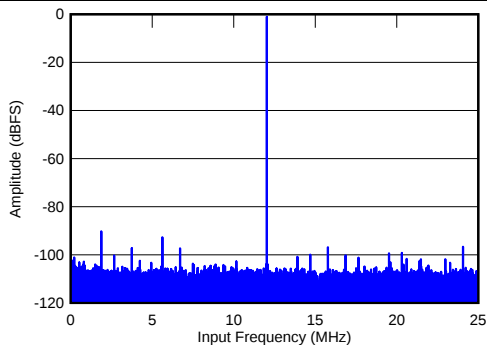
$f_S = 20$ MSPS, $f_{IN} = 12$ MHz, SNR = 71.1 dBFS, SFDR = 89 dBc, SINAD = 71 dBFS, THD = 87 dBc

Figure 120. FFT for 20-MSPS Sampling Speed



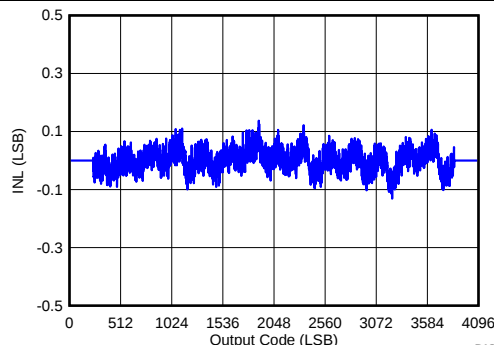
$f_S = 50$ MSPS, $f_{IN} = 3$ MHz, SNR = 71 dBFS, SFDR = 90 dBc, SINAD = 70.9 dBFS, THD = 87 dBc

Figure 121. FFT for 50-MSPS Sampling Speed



$f_S = 50$ MSPS, $f_{IN} = 12$ MHz, SNR = 71 dBFS, SFDR = 89 dBc, SINAD = 71.9 dBFS, THD = 87 dBc

Figure 122. FFT for 50-MSPS Sampling Speed



$f_S = 3$ MSPS, $f_{IN} = 4$ MHz

Figure 123. Integral Nonlinearity at 3-MSPS Sampling Speed

Application Information (continued)

ADS412x, 12-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted

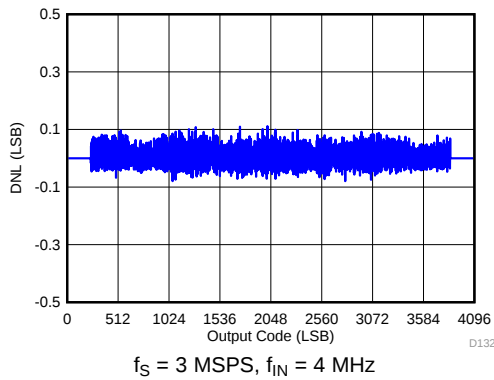


Figure 124. Differential Nonlinearity at 3-MSPS Sampling Speed

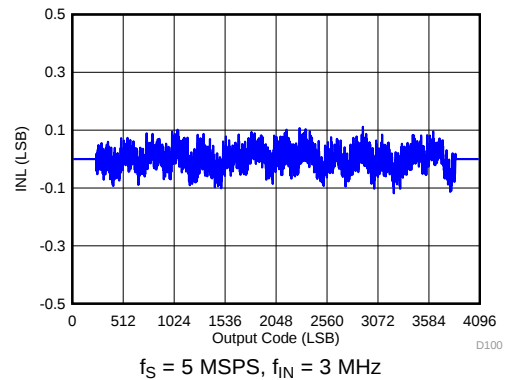


Figure 125. Integral Nonlinearity at 5-MSPS Sampling Speed

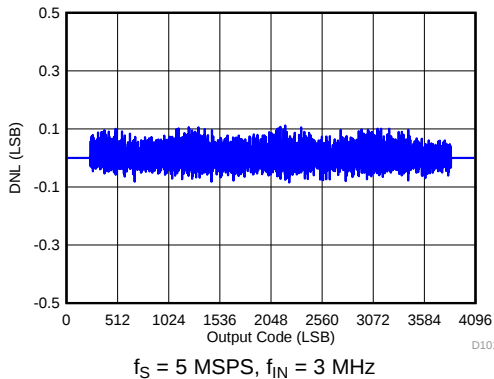


Figure 126. Differential Non-linearity at 5-MSPS Sampling Speed

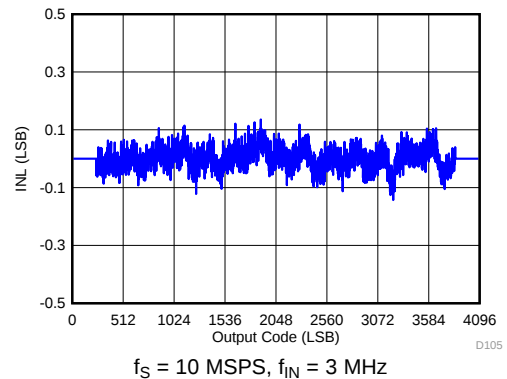


Figure 127. Integral Nonlinearity at 10-MSPS Sampling Speed

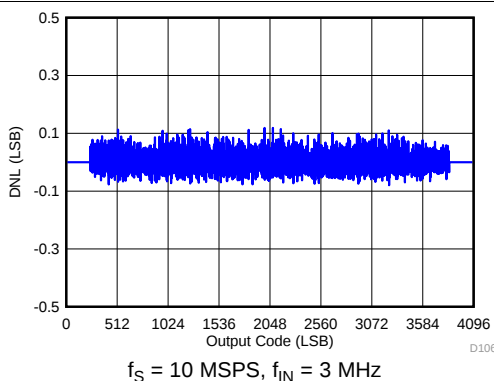


Figure 128. Differential Nonlinearity at 10-MSPS Sampling Speed

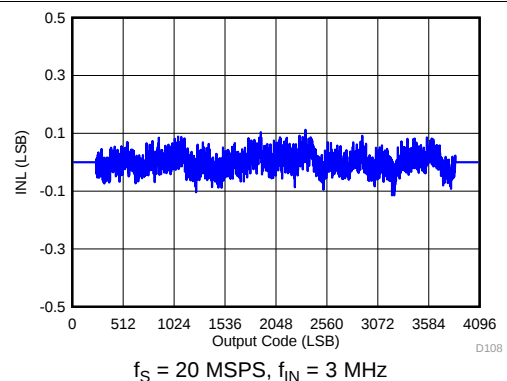


Figure 129. Integral Nonlinearity at 20-MSPS Sampling Speed

Application Information (continued)

ADS412x, 12-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted

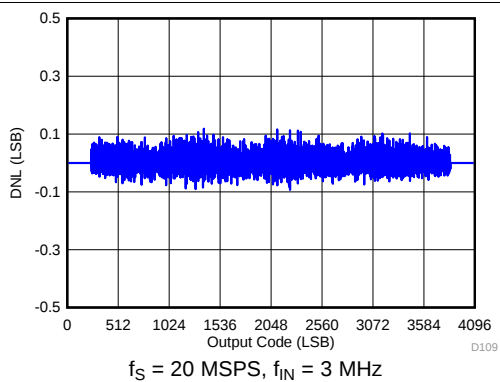


Figure 130. Differential Nonlinearity at 20-MSPS Sampling Speed

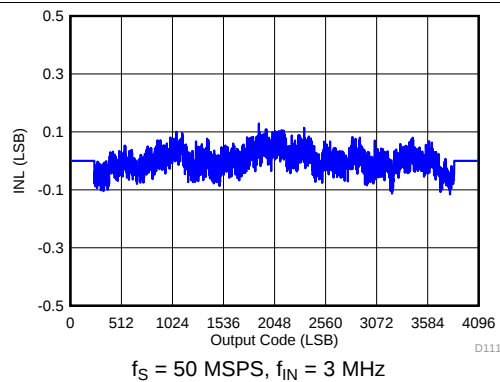


Figure 131. Integral Nonlinearity at 50-MSPS Sampling Speed

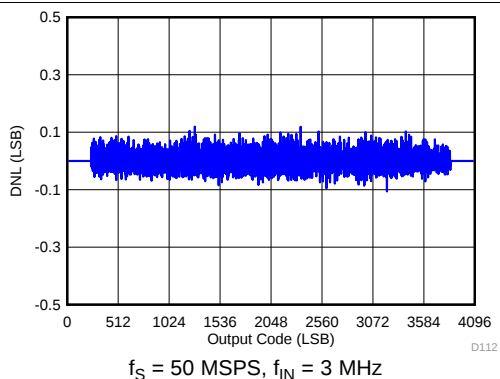


Figure 132. Differential Nonlinearity at 50-MSPS Sampling Speed

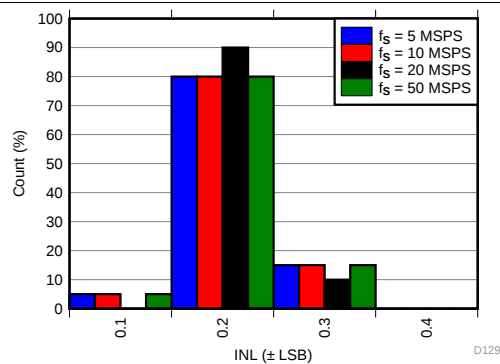


Figure 133. INL Histogram Across Sampling Speed

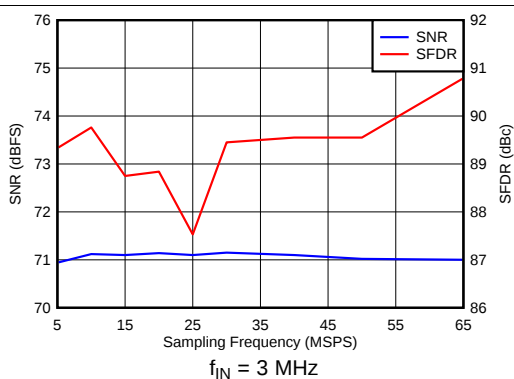


Figure 134. Performance Across Sampling Speed

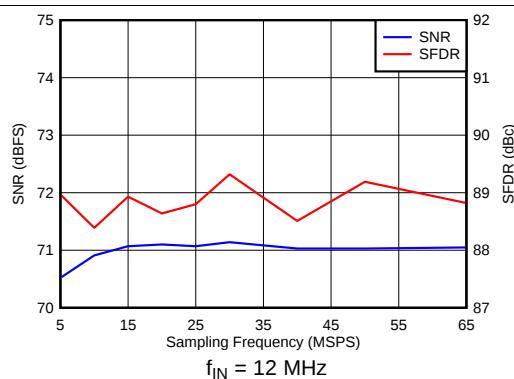


Figure 135. Performance Across Sampling speed

Application Information (continued)

ADS412x, 12-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted

9.1.4.2 ADS414x (14-Bit Device)

ADS414x, 14-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted.

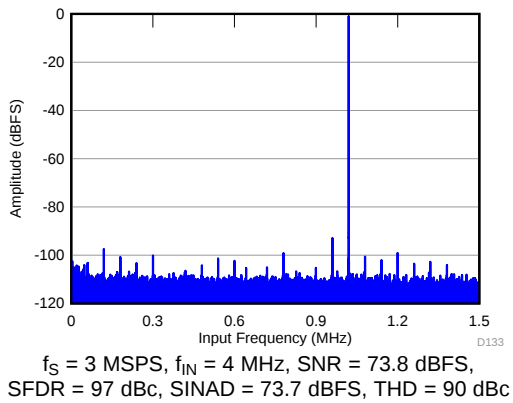


Figure 136. FFT for 3-MSPS Sampling Speed

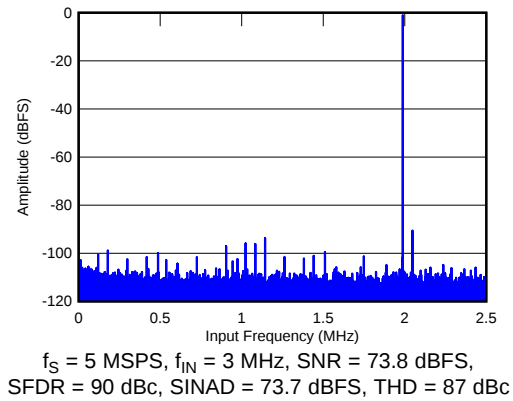


Figure 137. FFT for 5-MSPS Sampling Speed

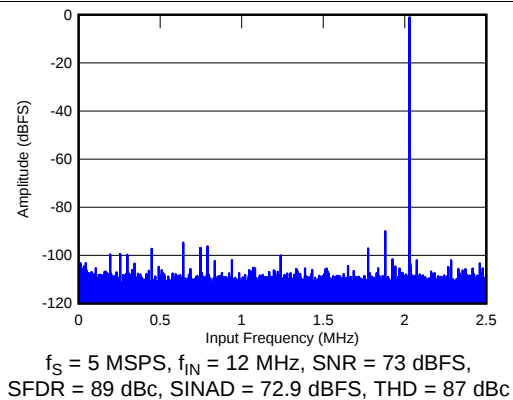


Figure 138. FFT for 5-MSPS Sampling Speed

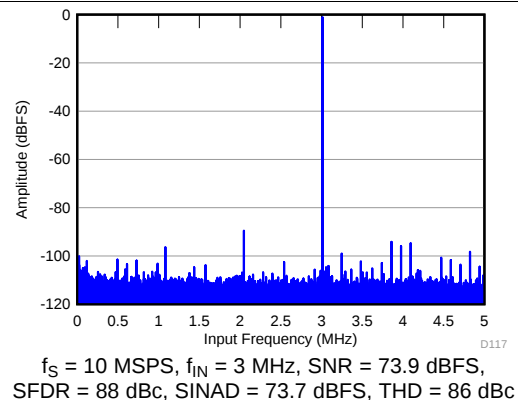


Figure 139. FFT for 10-MSPS Sampling Speed

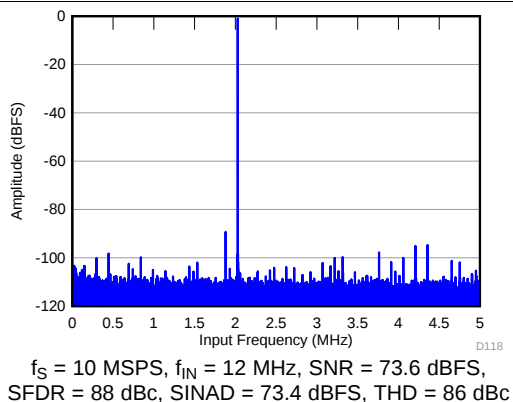


Figure 140. FFT for 10-MSPS Sampling Speed

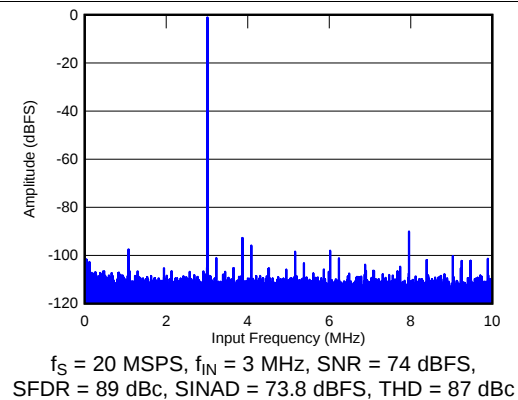
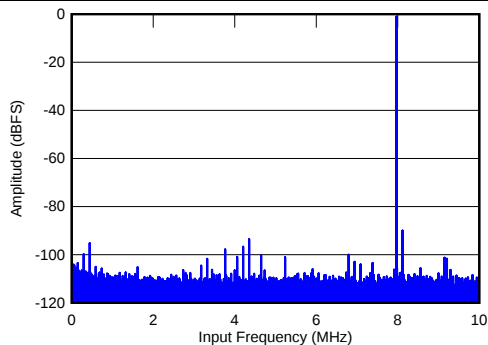


Figure 141. FFT for 20-MSPS Sampling Speed

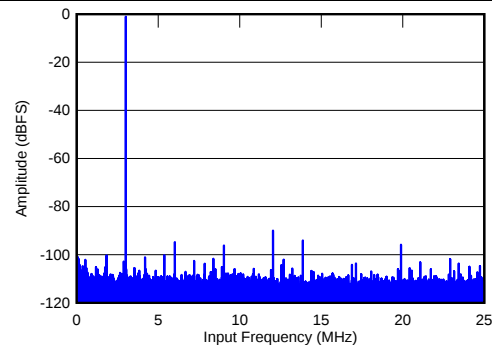
Application Information (continued)

ADS414x, 14-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted.



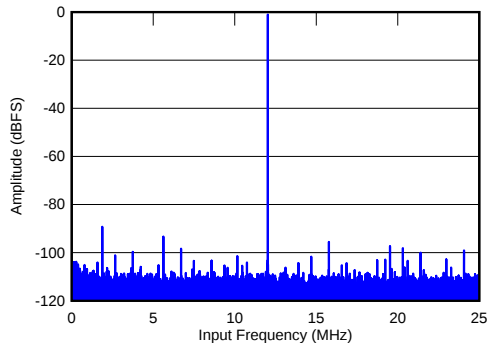
$f_S = 20$ MSPS, $f_{IN} = 12$ MHz, SNR = 73.9 dBFS, SFDR = 89 dBc, SINAD = 73.7 dBFS, THD = 87 dBc

Figure 142. FFT for 20-MSPS Sampling Speed



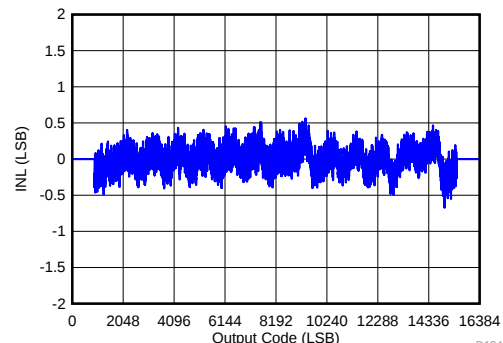
$f_S = 50$ MSPS, $f_{IN} = 3$ MHz, SNR = 73.8 dBFS, SFDR = 89 dBc, SINAD = 73.6 dBFS, THD = 86 dBc

Figure 143. FFT for 50-MSPS Sampling Speed



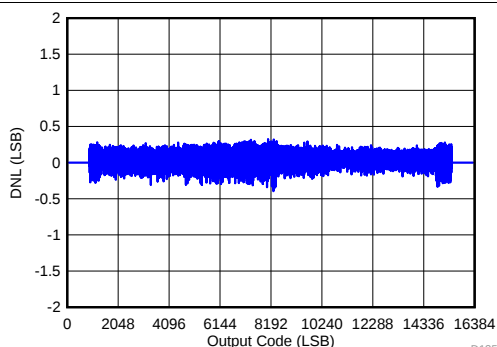
$f_S = 50$ MSPS, $f_{IN} = 12$ MHz, SNR = 73.8 dBFS, SFDR = 88 dBc, SINAD = 73.6 dBFS, THD = 86 dBc

Figure 144. FFT for 50-MSPS Sampling Speed



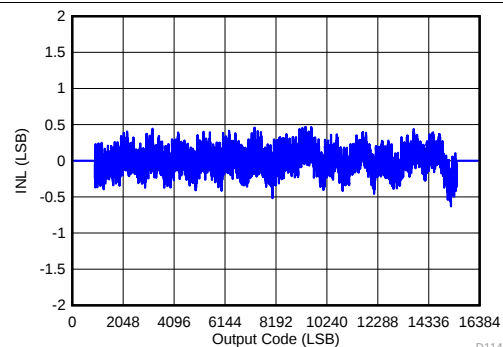
$f_S = 3$ MSPS, $f_{IN} = 4$ MHz

Figure 145. Integral Nonlinearity at 3-MSPS Sampling Speed



$f_S = 3$ MSPS, $f_{IN} = 4$ MHz

Figure 146. Differential Nonlinearity at 3-MSPS Sampling Speed



$f_S = 5$ MSPS, $f_{IN} = 3$ MHz

Figure 147. Integral Nonlinearity at 5-MSPS Sampling Speed

Application Information (continued)

ADS414x, 14-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted.

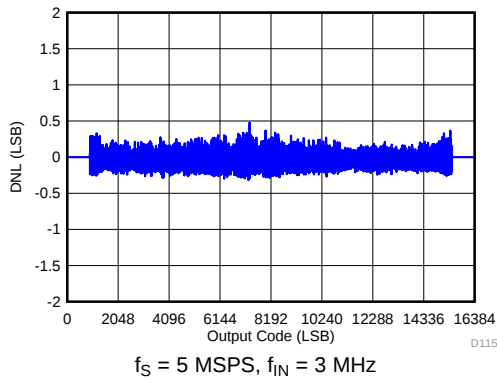


Figure 148. Differential Nonlinearity at 5-MSPS Sampling Speed

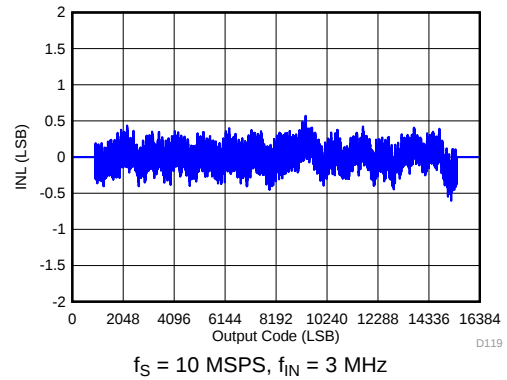


Figure 149. Integral Nonlinearity at 10-MSPS Sampling Speed

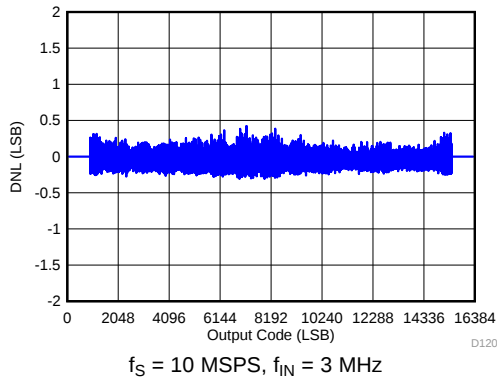


Figure 150. Differential Nonlinearity at 10-MSPS Sampling Speed

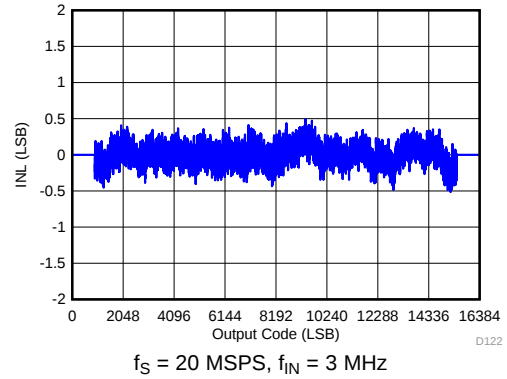


Figure 151. Integral Nonlinearity at 20-MSPS Sampling Speed

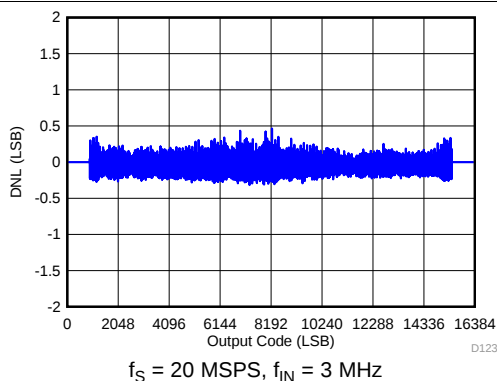


Figure 152. Differential Nonlinearity at 20-MSPS Sampling Speed

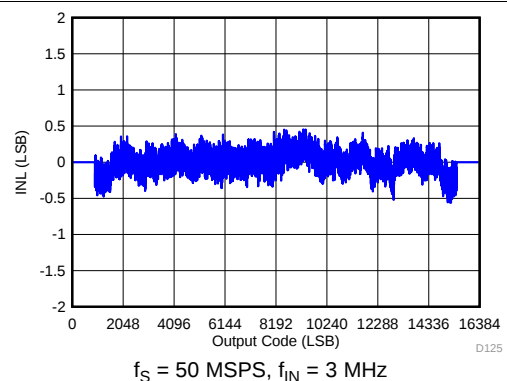


Figure 153. Integral Nonlinearity at 50-MSPS Sampling Speed

Application Information (continued)

ADS414x, 14-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted.

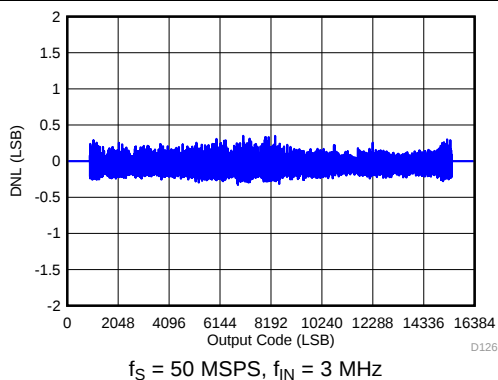


Figure 154. Differential Nonlinearity at 50-MSPS Sampling Speed

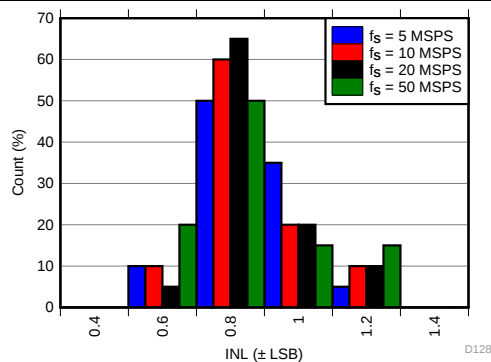


Figure 155. INL Histogram Across Sampling Speed

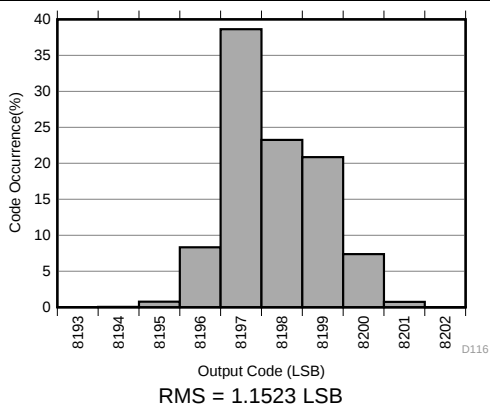


Figure 156. Output Noise Histogram (With Inputs shorted to VCM) at 5-MSPS Sampling Speed

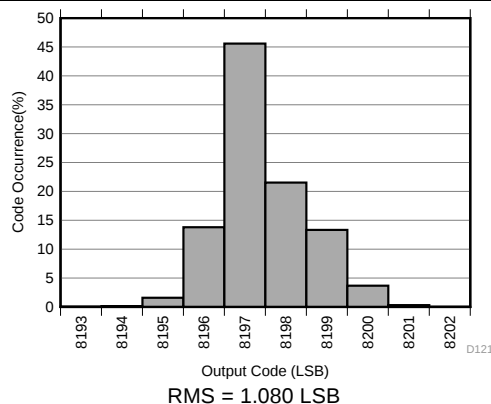


Figure 157. Output Noise Histogram (With Inputs shorted to VCM) at 10-MSPS Sampling Speed

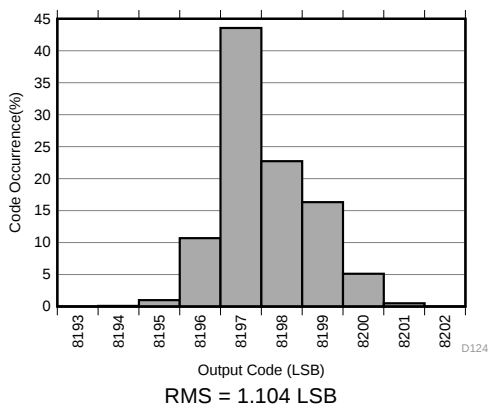


Figure 158. Output Noise Histogram (With Inputs shorted to VCM) at 20-MSPS Sampling Speed

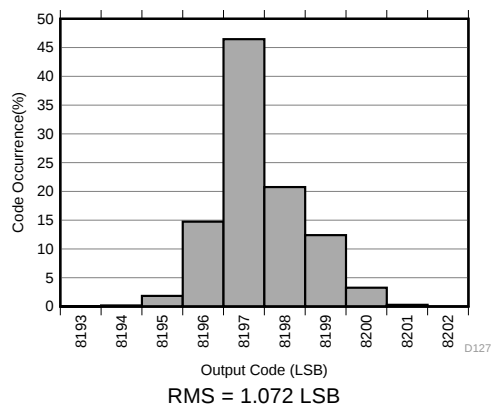


Figure 159. Output Noise Histogram (With Inputs shorted to VCM) at 50-MSPS Sampling Speed

Application Information (continued)

ADS414x, 14-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted.

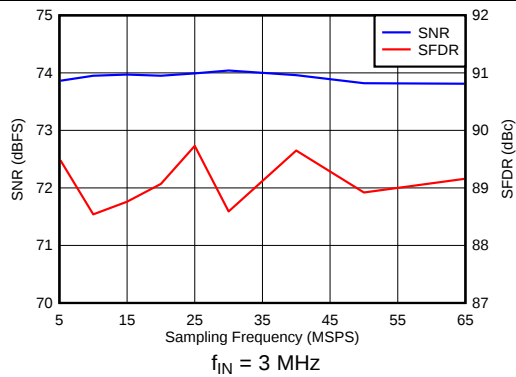


Figure 160. Performance Across Sampling Speed

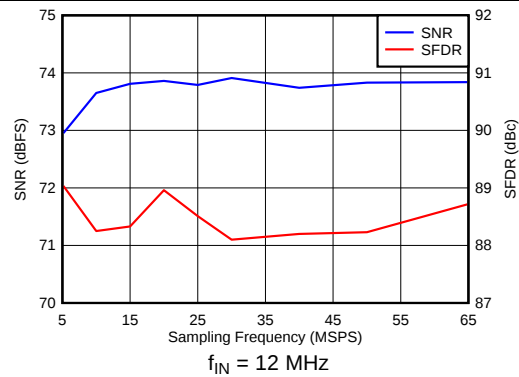


Figure 161. Performance Across Sampling Speed

Application Information (continued)

ADS414x, 14-Bit Resolution, at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sine wave input clock, 1.5-VPP differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, CMOS output interface, and 32k-point FFT, unless otherwise noted.

9.1.4.3 Power Consumption at Low Sampling Rates

Figure 162 shows typical power consumption at lower sampling rates on each supply.

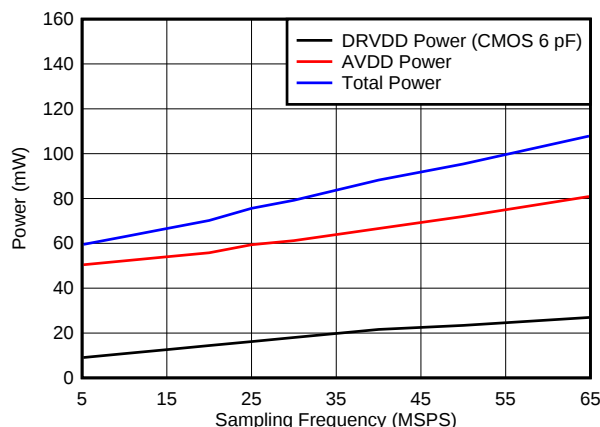


Figure 162. Power vs Sample Rate

9.1.4.4 Output Timing at Low Sampling Rates

Table 24 describes the set-up and hold times for the digital outputs of the ADS41xx with respect to the output clock at low sampling rates.

Table 24. Output Timing at Low Sampling Rates in CMOS Mode⁽¹⁾

SAMPLING FREQUENCY (MSPS)	SETUP TIME, t _{SU}			HOLD TIME, t _{HO}			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
CMOS (Low Latency Enabled)							
5	99.4	100.4		97.9	98.7		ns
10	49.0	49.7		48.5	49.3		ns
20	23.3	24.2		23.9	24.8		ns
30	15.0	15.8		15.7	16.6		ns
40	10.7	11.4		11.5	12.5		ns
50	8.2	9.0		9.1	10.0		ns
CMOS (Low Latency Disabled)							
5	99.6	100.3		97.8	98.5		ns
10	49.1	49.7		48.2	49.1		ns
20	23.6	24.2		23.6	24.6		ns
30	15.2	15.7		15.3	16.4		ns
40	10.9	11.4		11.2	12.3		ns
50	8.4	8.9		8.6	9.8		ns

(1) Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, C_{LOAD} = 5 pF. Minimum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

9.2 Typical Application

An example schematic for a typical application of the ADS414x is shown in [Figure 163](#).

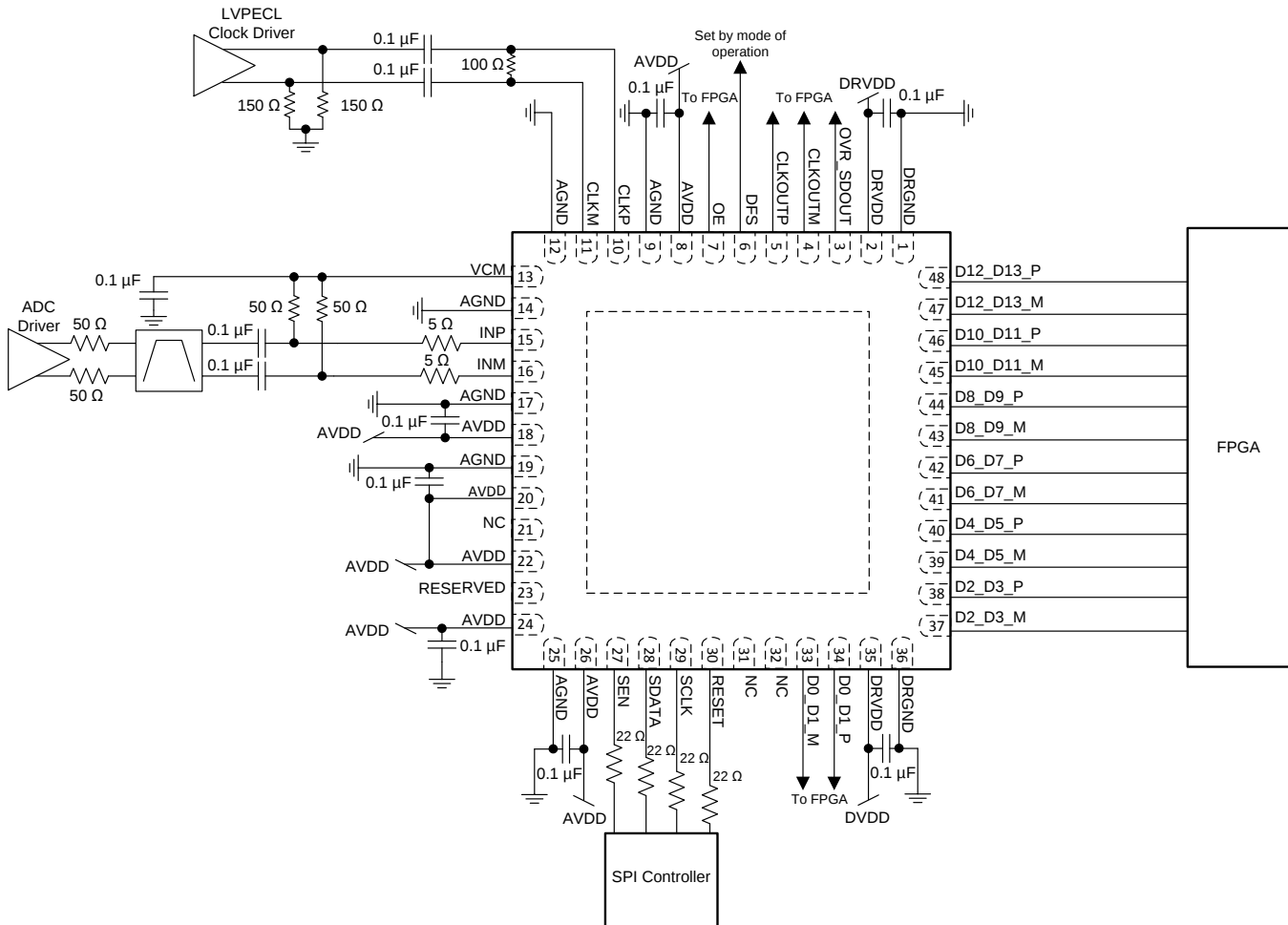


Figure 163. Example Schematic for the ADS414x

9.2.1 Design Requirements

Example design requirements are listed in [Table 25](#) for the ADC portion of the signal chain. These requirements do not necessarily reflect the requirements of an actual system, but rather demonstrate why the ADS412x and ADS414x can be chosen for a system based on a set of requirements.

Table 25. Example Design Requirements for the ADS412x and ADS414x

DESIGN PARAMETER	EXAMPLE DESIGN REQUIREMENT	ADS4125 CAPABILITY
Sampling rate	≥ 122.88 MSPS	Max sampling rate: 125 MSPS
Input frequency	> 125 MHz to accommodate full 2nd Nyquist zone	Large-signal, -3 -dB bandwidth: 400-MHz operation
SNR	> 68 dBFS at -1 dBFS, 170 MHz	72.2 dBFS at -1 dBFS, 170 MHz
SFDR	> 77 dBc at -1 dBFS, 170 MHz	81 dBc at -1 dBFS, 170 MHz
Input full scale voltage	$2 V_{PP}$	$2 V_{PP}$
Overload recovery time	< 3 clock cycles	1 clock cycle
Digital interface	Parallel LVDS	Parallel LVDS
Power consumption	< 200 mW per channel	153 mW per channel

9.2.2 Detailed Design Procedure

9.2.2.1 Analog Input

The analog input of the ADS412x and ADS414x is typically driven by a fully differential amplifier. The amplifier must have sufficient bandwidth for the frequencies of interest. The noise and distortion performance of the amplifier affect the combined performance of the ADC and amplifier. The amplifier is often ac-coupled to the ADC to allow both the amplifier and ADC to operate at the optimal common-mode voltages. The amplifier can be dc-coupled to the ADC if required. An alternate approach is to drive the ADC using transformers. DC coupling cannot be used with the transformer approach.

9.2.2.2 Clock Driver

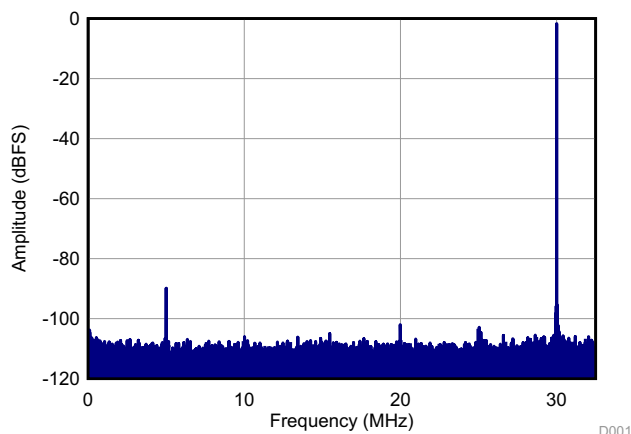
The ADS412x and ADS414x must be driven by a high-performance clock driver such as a clock jitter cleaner. The clock must have low noise to maintain optimal performance. LVPECL is the most common clocking interface, but LVDS and LVCMOS can be used as well. TI does not advise driving the clock input from an FPGA unless the noise degradation can be tolerated, such as for input signals near dc where the clock noise impact is minimal.

9.2.2.3 Digital Interface

The ADS412x and ADS414x supports both LVDS and CMOS interfaces. The LVDS interface must be used for best performance when operating at maximum sampling rate. The LVDS outputs can be connected directly to the FPGA without any additional components. When using CMOS outputs resistors must be placed in series with the outputs to reduce the output current spikes to limit the performance degradation. The resistors must be large enough to limit current spikes but not so large as to significantly distort the digital output waveform. An external CMOS buffer must be used when driving distances greater than a few inches to reduce ground bounce within the ADC.

9.2.3 Application Curve

Figure 164 shows the results of a 100-MHz signal sampled at 65 MHz captured by the ADS4122.



SNR = 70.11 dBFS, SFDR = 87.74 dBFS,
THD = 84.33 dB, SINAD = 70.03 dBFS

Figure 164. 100-MHz Signal Captured by the ADS4122

10 Power Supply Recommendations

The ADS412x and ADS414x have two power supplies, one analog (AVDD) and one digital (DRVDD) supply. Both supplies have a nominal voltage of 1.8 V. The AVDD supply is noise sensitive and the digital supply is not.

10.1 Sharing DRVDD and AVDD Supplies

For best performance, the AVDD supply must be driven by a low noise linear regulator and separated from the DRVDD supply. AVDD and DRVDD can share a single supply but must be isolated by a ferrite bead and bypass capacitors, in a PI-filter configuration, at a minimum. The digital noise is concentrated at the sampling frequency and harmonics of the sampling frequency and could contain noise related to the sampled signal. When developing schematics, leave extra placeholders for additional supply filtering.

10.2 Using DC-DC Power Supplies

DC-DC switching power supplies can be used to power DRVDD without issue. AVDD can be powered from a switching regulator. Noise and spurs on the AVDD power supply affect the SNR and SFDR of the ADC and show up near dc and as a modulated component around the input frequency. If a switching regulator is used, then the regulator must be designed to have minimal voltage ripple. Supply filtering must be used to limit the amount of spurious noise at the AVDD supply pins. Extra placeholders must be placed on the schematic for additional filtering. Optimization of filtering in the final system is likely needed to achieve the desired performance. The choice of power supply ultimately depends on the system requirements. For instance, if very low phase noise is required then use of a switching regulator is not recommended.

10.3 Power Supply Bypassing

Because the ADS412x and ADS414x already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. A 0.1- μ F capacitor is recommended near each supply pin. The decoupling capacitors must be placed very close to the converter supply pins.

11 Layout

11.1 Layout Guidelines

11.1.1 Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the [ADS414x, ADS412x EVM User Guide](#) for details on layout and grounding.

11.1.2 Supply Decoupling

Because the ADS412x and ADS414x already include internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise, so the optimum number of capacitors depends on the actual application. The decoupling capacitors must be placed very close to the converter supply pins.

11.1.3 Exposed Pad

In addition to providing a path for heat dissipation, the thermal pad is also electrically internally connected to the digital ground. Therefore, solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes, [QFN Layout Guidelines](#) (SLOA122) and [QFN/SON PCB Attachment](#) (SLUA271) that are both available for download at www.ti.com.

11.2 Layout Example

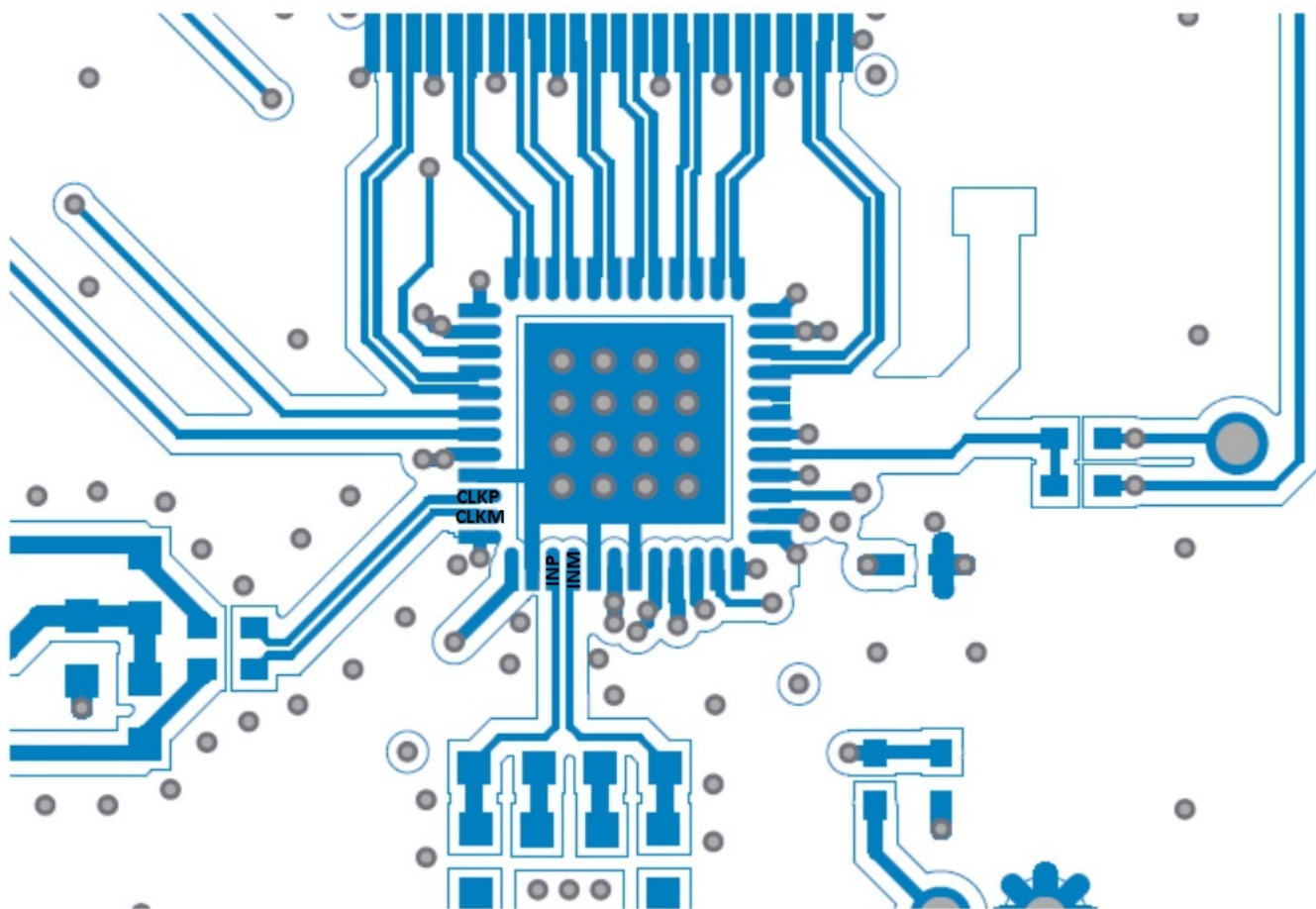


Figure 165. ADS412x and ADS414x EVM PCB Layout

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

模拟带宽 基频功率相对低频值下降 3dB 时的模拟输入频率。

孔径延时 从输入采样时钟的上升沿到实际发生采样之间的延迟时间。

该延迟在各通道中会有所不同。最大差值被定义为孔径延迟差异（通道间）。

孔径不确定性（抖动） 采样间的孔径延迟差异。

时钟脉冲宽度/占空比 时钟信号的占空比为时钟信号保持逻辑高电平的时间（时钟脉冲宽度）与时钟信号周期的比值。

占空比通常以百分比的形式表示。理想差分正弦波时钟的占空比为 50%。

最大转换速率 执行指定操作时所采用的最大采样率。

除非另外注明，否则所有参数测试均以该采样率执行。

最小转换速率 ADC 正常工作时的最小采样率。

微分非线性 (DNL) DNL 是指任意单个步长与这一理想值之间的偏差（以 LSB 为计量单位）。

理想 ADC 对模拟输入值进行编码转换时以 1 LSB 为步长。

积分非线性 (INL) INL 是 ADC 传递函数与其最小二乘法曲线拟合所确定的最佳拟合曲线的偏差（以 LSB 为计量单位）。

增益误差 增益误差是指 ADC 实际输入满量程范围与其理想值的偏差。

增益误差以理想输入满量程范围的百分比形式表示。增益误差包括两部分：基准不精确所导致的误差和通道所导致的误差。这两种误差分别定义为 E_{GREF} 和 E_{GCHAN} 。

对于一阶近似，总增益误差 $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$ 。

例如，如果 $E_{TOTAL} = \pm 0.5\%$ ，则满量程输入范围为 $(1 - 0.5 / 100) \times FS_{ideal}$ 至 $(1 + 0.5 / 100) \times FS_{ideal}$ 。

偏移误差 偏移误差是指 ADC 实际平均空闲通道输出编码与理想平均空闲通道输出编码之间的差值（以 LSB 数表示）。

该数量通常转换为毫伏。

温度漂移 温度漂移系数（相对于增益误差和偏移误差）指定参数从 T_{MIN} 到 T_{MAX} 每摄氏度的变化量。

温度漂移的计算方法是用参数在 T_{MIN} 至 T_{MAX} 范围内的最大变化量除以 $T_{MAX} - T_{MIN}$ 的值。

信噪比 SNR 是指基频功率 (P_S) 与噪底功率 (P_N) 的比值，后者不包括直流功率和前 9 个谐波的功率。

$$SNR = 10 \log_{10} \frac{P_S}{P_N} \quad (2)$$

当基频的绝对功率用作基准时，SNR 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SNR 以 dBFS（相对于满量程的分贝数）为单位。

信噪比和失真 (SINAD) SINAD 是指基频功率 (P_S) 与所有其他频谱成分（包括噪声 (P_N) 和失真 (P_D)，但不包括直流）功率的比值。

$$SINAD = 10 \log_{10} \frac{P_S}{P_N + P_D} \quad (3)$$

当基频的绝对功率用作基准时，SINAD 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SINAD 以 dBFS（相对于满量程的分贝数）为单位。

有效位数 (ENOB) ENOB 测量的是转换器相对于理论限值（基于量化噪声）的性能。

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (4)$$

器件支持 (接下页)

总谐波失真 (THD) THD 是指基频功率 (P_S) 与前 9 个谐波功率 (P_D) 的比值。

$$THD = 10 \log^{10} \frac{P_S}{P_N} \quad (5)$$

THD 通常以 dBc 为单位 (相对于载波的分贝数)。

无杂散动态范围 (SFDR) 基频功率与最高的其他频谱成分 (毛刺或谐波) 功率的比值。

SFDR 通常以 dBc 为单位 (相对于载波的分贝数)。

双频互调失真 IMD3 是指基频功率 (f_1 和 f_2 频率处) 与最差频谱成分 ($2f_1 - f_2$ 或 $2f_2 - f_1$ 频率处) 功率的比值。

当基频的绝对功率用作基准时, IMD3 以 dBc (相对于载波的分贝数) 为单位; 当基频功率被外推至转换器满量程范围时, IMD3 以 dBFS (相对于满量程的分贝数) 为单位。

直流电源抑制比 (DC PSRR) DC PSRR 是偏移误差变化量与模拟电源电压变化量的比值。

DC PSRR 通常以 mV/V 为单位进行表示。

交流电源抑制比 (AC PSRR) AC PSRR 测量的是 ADC 对电源电压变化的抑制能力。

如果 ΔV_{SUP} 表示电源电压的变化, ΔV_{OUT} 表示 ADC 输出编码的相应变化 (相对输入而言), 则:

$$PSRR = 20 \log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \quad (\text{Expressed in dBc}) \quad (6)$$

电压过载恢复 使过载的模拟输入端的误差恢复至 1% 以下所需的时钟数。

该技术参数的测试方法是分别施加具有 6dB 正过载和负过载的正弦波信号。然后记录下过载后前几个采样 (相对于期望值) 的偏差。

共模抑制比 (CMRR) CMRR 测量的是 ADC 对模拟输入共模变化的抑制能力。

如果 $\Delta V_{CM, IN}$ 表示输入引脚的共模电压变化, ΔV_{OUT} 表示 ADC 输出编码的相应变化 (相对输入而言), 则:

$$CMRR = 20 \log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \quad (\text{Expressed in dBc}) \quad (7)$$

串扰 (仅限多通道 ADC) 串扰测量的是目标通道与其相邻通道之间的内部信号耦合。串扰分两种情况: 一种是与紧邻通道 (近端通道) 之间的耦合, 另一种是与跨封装通道 (远端通道) 之间的耦合。

通常采用对邻近通道施加满量程信号的方式来测量串扰。串扰是指耦合信号功率 (在目标通道的输出端测得) 与邻近通道输入端所施加信号功率的比值。串扰通常以 dBc 为单位进行表示。

12.2 文档支持

12.2.1 相关文档

相关文档如下:

- [《QFN 布局指南》](#)
- [《QFN/SON PCB 连接》](#)
- [《ADS414x、ADS412x EVM 用户指南》](#)
- [《具有 DDR LVDS 和并行 CMOS 输出的 ADS61xx 14/12 位、250/210MSPS ADC》](#)

12.3 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件, 并且可通过快速访问立刻订购。

表 26. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
ADS4122	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS4125	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

相关链接 (接下页)

表 26. 相关链接 (接下页)

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
ADS4142	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS4145	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。请单击右上角的通知我 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 商标

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12.7 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS4122IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4122	Samples
ADS4122IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4122	Samples
ADS4125IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4125	Samples
ADS4125IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4125	Samples
ADS4142IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4142	Samples
ADS4142IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4142	Samples
ADS4145IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4145	Samples
ADS4145IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4145	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

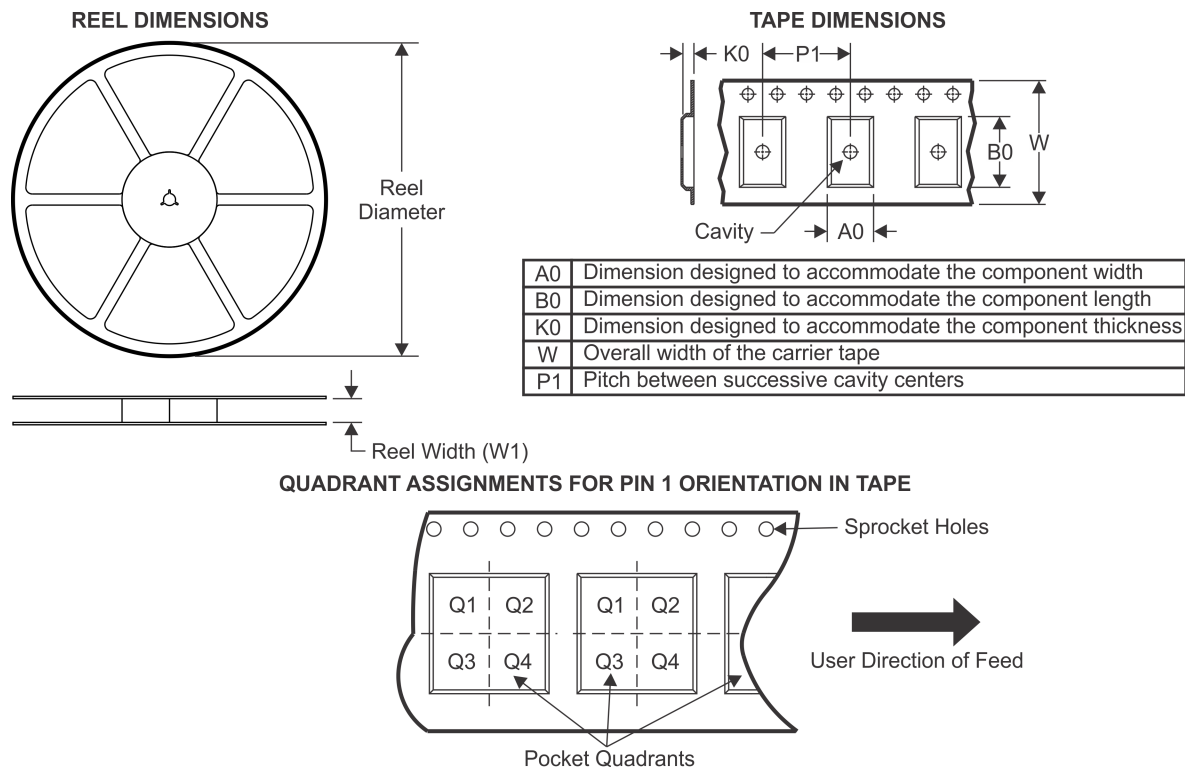
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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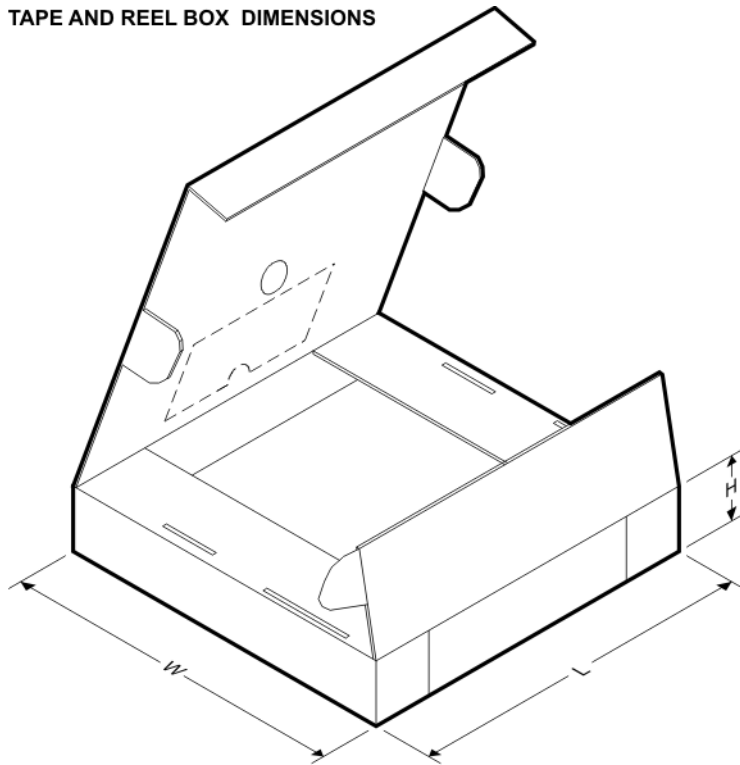
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS4122IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4122IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4125IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4125IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4142IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4142IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4145IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4145IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS4122IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS4122IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS4125IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS4125IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS4142IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS4142IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS4145IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS4145IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

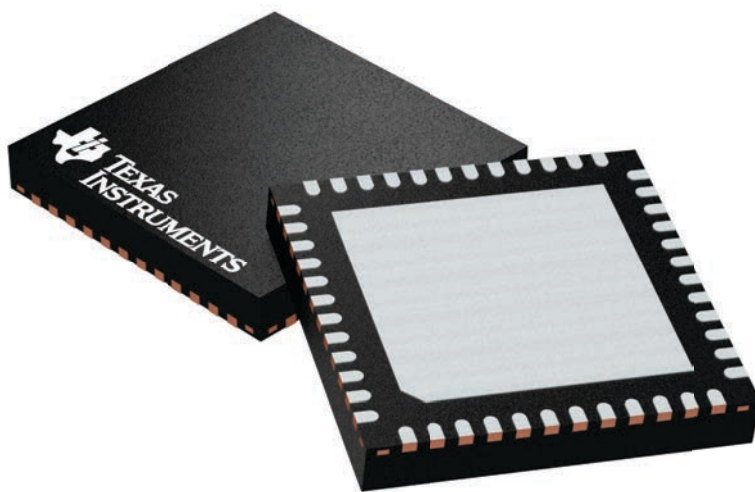
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

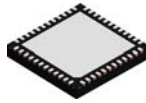
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

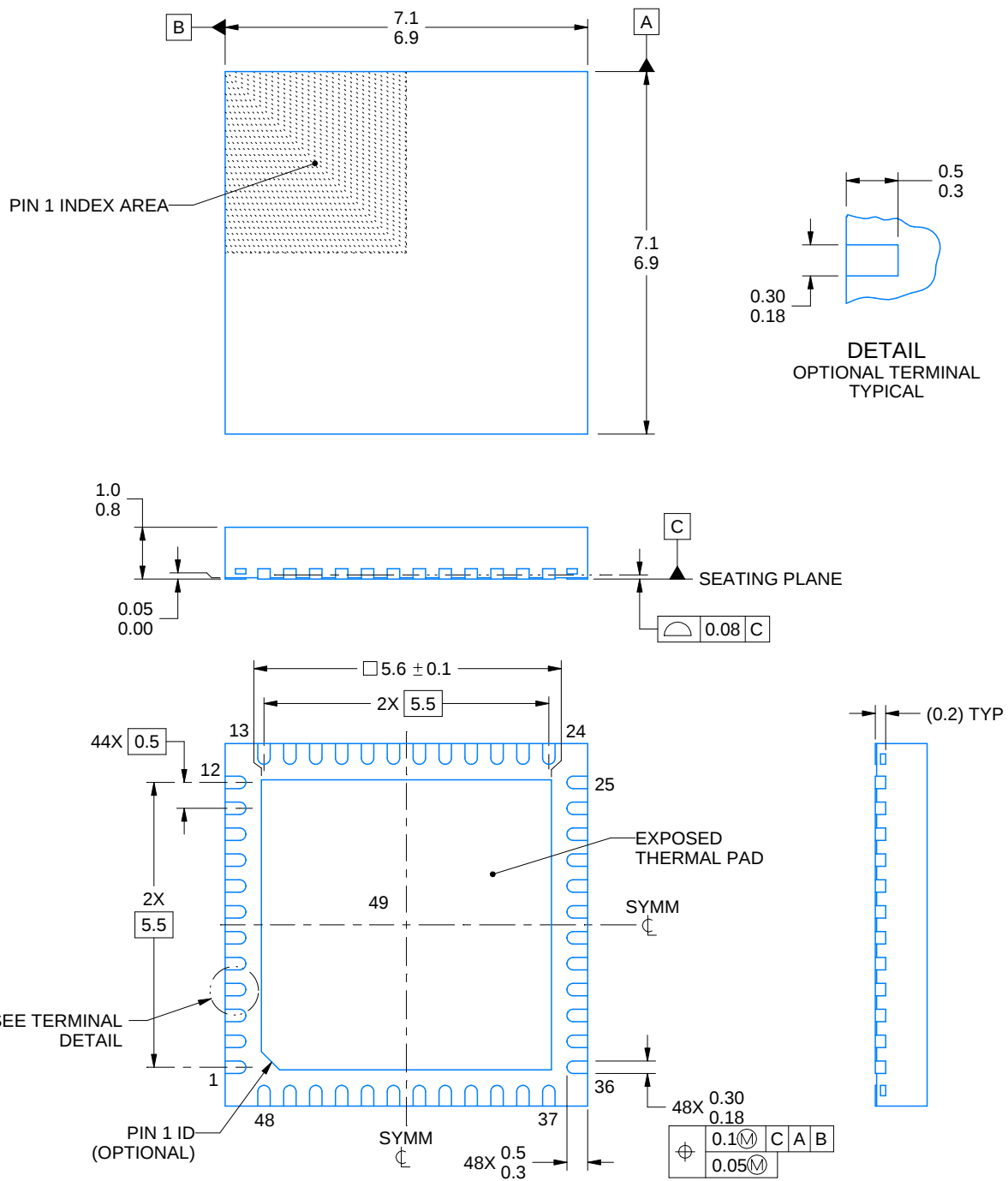
RGZ0048D



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219046/B 11/2019

NOTES:

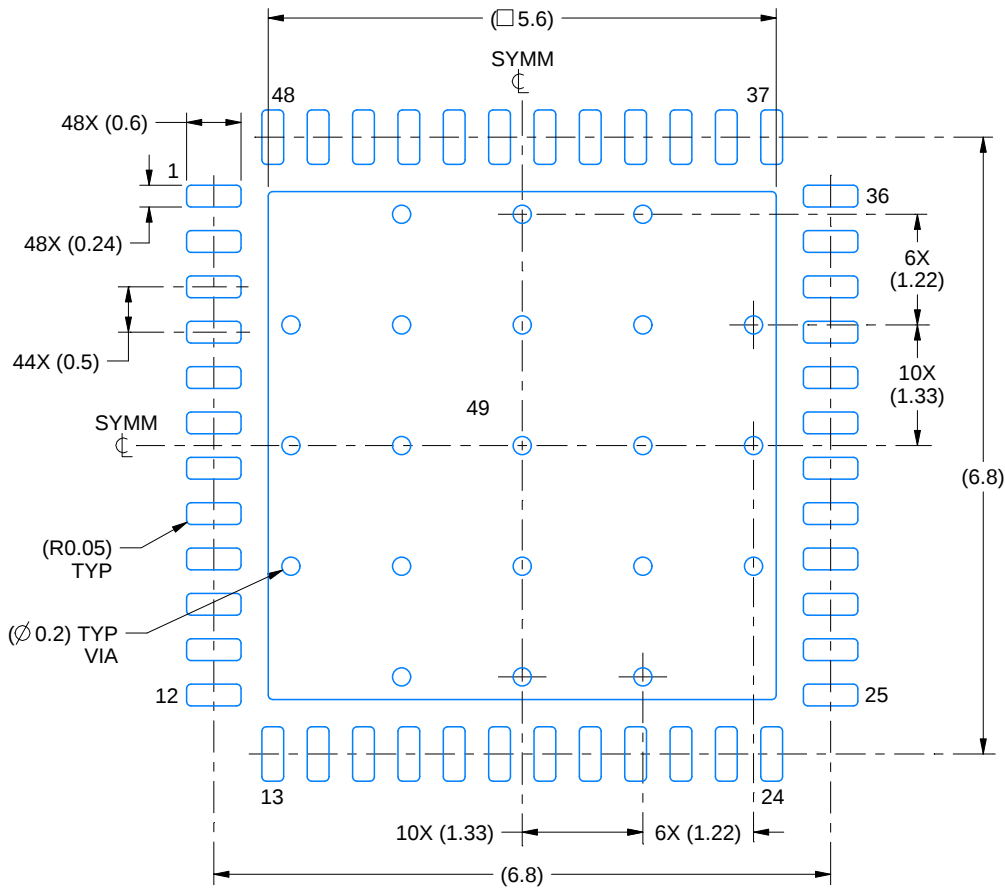
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

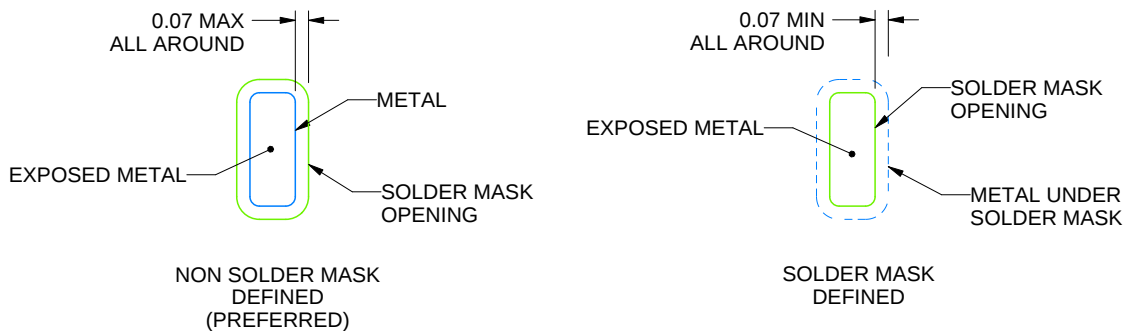
RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4219046/B 11/2019

NOTES: (continued)

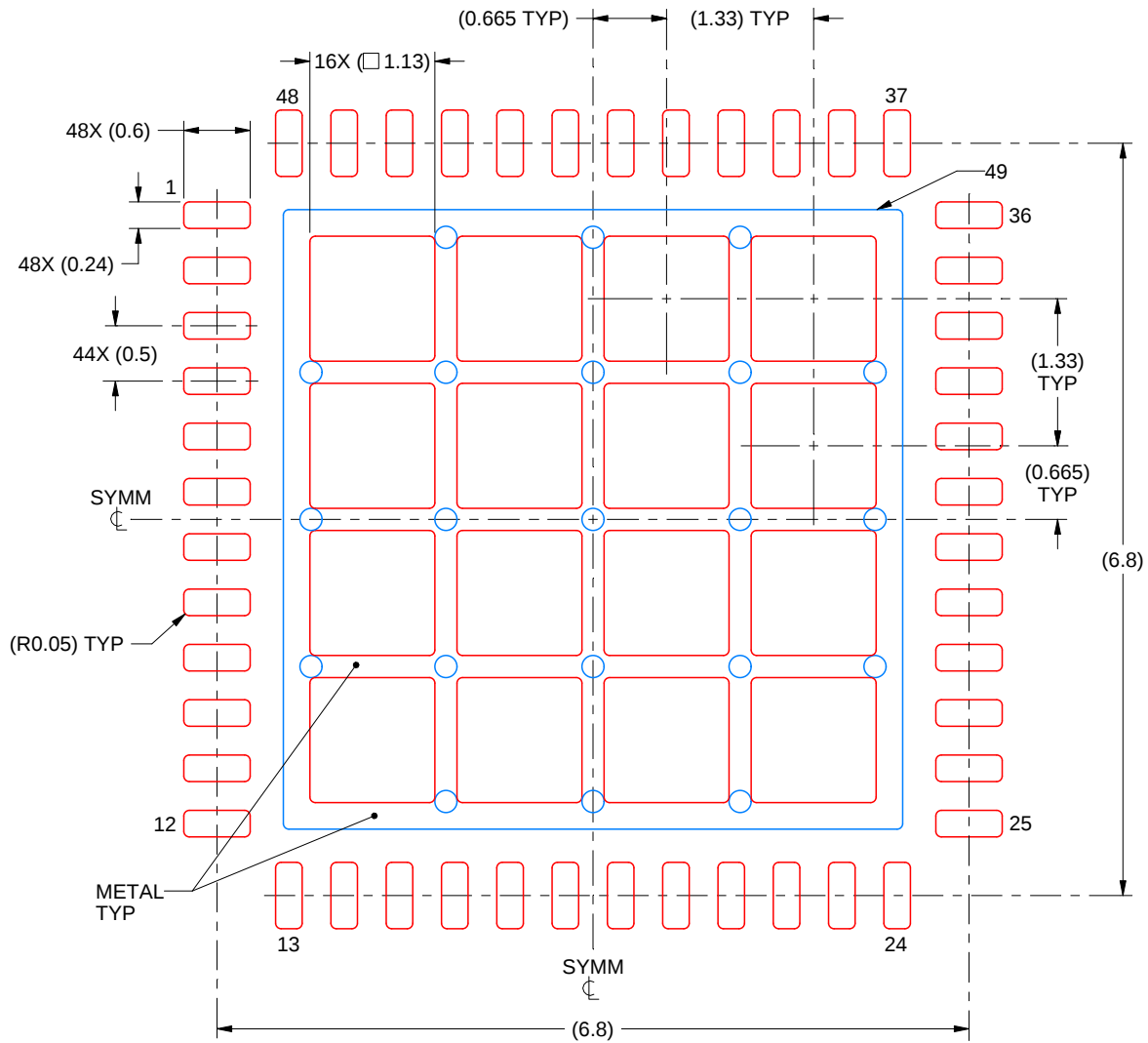
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4219046/B 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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