bq34110 适用于极少放电型应用的多化合物 CEDV 电池电量 监测计

1 特性

- 精准的放电结束 (EOS) 确定功能，适用于极少放电型应用中的 电池
- 补偿放电结束电压 (CEDV) 电池电量监测计，适用于单节和多节电池，可提供
  - 充电状态 (SOC)
  - 续航时间 (TTE)
  - 健康状况 (SOH)
  - 基于瓦时的充电终止
- 最高支持 65V 电压、32Ah 电容和 32 A 电流 - 可使用调节特性扩展这些参数级别
- 支持锂离子、磷酸铁锂、铅酸 (PbA)、镍氢和镍铬等化学成分
- 双路可配置主机中断或 GPO
- 寿命数据记录选项
- 精确的库伦计数器、电压和温度测量
- 电源使能控制
- 通过 I^2C™与主机通信
- 累加充电库伦计数和可配置中断
- 安全散列算法 (SHA-1) 认证

2 应用

- 不间断电源 (UPS) 备用系统
- 远程信息处理备用系统
- 应急电池供电模块
- 能量存储系统
- 资产跟踪
- 楼宇安全系统
- 视频监控
- 电子智能锁
- 远程和应急照明
- 服务器供电系统
- 机器人
- 玩具

3 说明

bq34110 CEDV 电池电量监测计可为单节和多节电池提供 CEDV 电量监测和放电结束 (EOS) 确定功能。该器件配有增强型 特性， 从而 为 各类备用系统中常用的始终保持满电量且极少放电的电池提供支持。Bq34110 电量监测计支持多种电池化学成分，包括锂离子、磷酸铁锂、铅酸 (PbA)、镍氢 (NiMH) 和镍铬 (NiCd)。

该电量监测计使用补偿放电结束电压 (CEDV) 技术获取电压、电流和温度数据，并借此提供充电状态 (SOC) 和健康状况 (SOH) 数据。这款电量监测计还整合了放电结束 (EOS) 确定功能，可在电池电量不足和即将完全放电时发出警报。

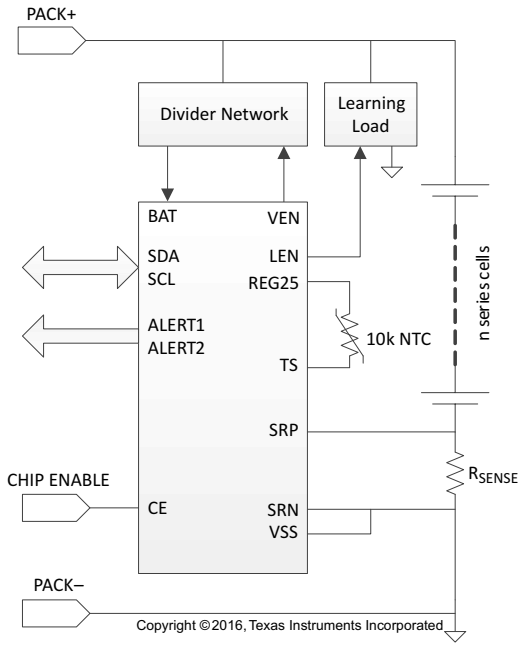
监测计中的数据可由主机通过 400kHz I^2C 总线读取。另外，还有两个 ALERT 输出可供使用，例如向主机发出中断或者实现其他功能，具体根据配置选项来决定。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq34110	TSSOP (14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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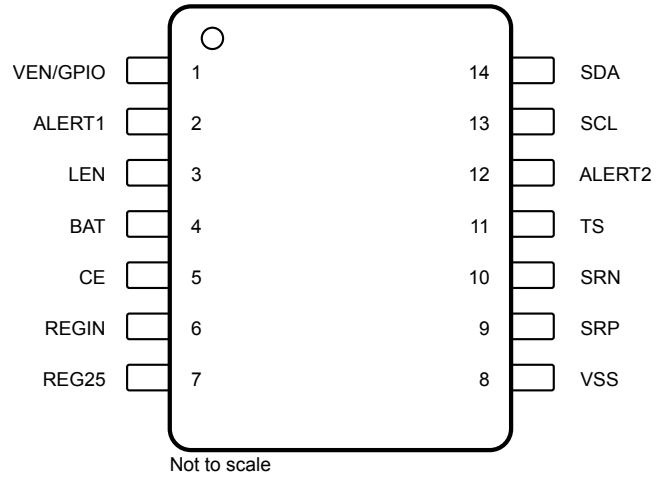
4 修订历史记录

日期	修订版本	注释
2016 年 11 月	B	产品预览至量产数据

5 Pin Configuration and Functions

14-Pin TSSOP (PW)
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VEN/GPIO	1	O(1)	Active High Voltage Translation Enable. This signal is used optionally to switch the input voltage divider on/off to reduce the power consumption (typ 45 μA) of the divider network. It can also be used as a general purpose output.
ALERT1	2	O	Open drain output for use as system alert or charger control. Pull-up voltage limited
LEN	3	O	Push-pull external voltage divider control output
BAT	4	P	Voltage measurement input
CE	5	I	Chip enable. Internal LDO is powered down when driven low.
REGIN	6	P	Internal integrated LDO input. Decouple with 0.1-μF ceramic capacitor to V_{SS}.
REG25	7	P	2.5-V output voltage of the internal integrated LDO. Decouple with 1-μF ceramic capacitor to V_{SS}.
VSS	8	P	Device ground
SRP	9	I	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN, where SRP is nearest the BAT– connection.
SRN	10	I	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN, where SRN is nearest the PACK– connection.
TS	11	I	Pack thermistor voltage sense (use 103AT-type thermistor)
ALERT2	12	O	Open drain output for use as system alert or charger control
SCL	13	I	Open drain slave I^2C serial communication clock input. Use with an external 10-kΩ pull-up resistor (typical).
SDA	14	I/O	Open drain slave I^2C serial communication data line. Use with an external 10-kΩ pull-up resistor (typical).

(1) AI = Analog Input, O = Output, I = Input, P = Power, I/O = Input/Output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{REGIN}	Regulator input range	–0.3	5.5	V
V_{CE}	CE input pin	–0.3	V_{REGIN} + 0.3	V
V_{REG25}	Supply voltage range	–0.3	2.75	V
V_{IOD}	Open-drain I/O pins (SDA, SCL, ALERT2)	–0.3	5.5	V
V_{BAT}	BAT input pin	–0.3	5.5	V
V_I	Input voltage range to all other pins (SRP, SRN, TS, ALERT1, VEN/GPIO, LEN)	–0.3	V_{REG25} + 0.3	V
T_A	Operating free-air temperature range	–40	85	°C
T_J	Operating junction temperature range	–40	100	°C
T_F	Functional temperature range	–40	100	°C
T_{STG}	Storage temperature range	–65	150	°C
	Lead temperature (soldering, 10 s)	–40	100	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, BAT pin(1)	±1500	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A= –40°C to 85°C, V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{REGIN}	Supply Voltage	No operating restrictions	2.7		4.5	V
		No FLASH writes	2.45		2.7	V
C_{REGIN}	External input capacitor for internal LDO between REGIN and VSS	Nominal capacitor values specified. Recommend a 10% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{REG25}	External output capacitor for internal LDO between VCC		0.47	1		µF
t_{PUCD}	Power-up communication			250		ms

6.4 Thermal Information

THERMAL METRIC(1)		bq34110 TSSOP (PW) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: Supply Current

T_A= –40°C to 85°C, V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC_NORMAL}	Normal operating current	Device in NORMAL mode, I_{LOAD} > ***Sleep Current***		133		µA
I_{SNOOZE} (1)	Sleep+ operation mode current	Device in SNOOZE mode, I_{LOAD} < ***Sleep Current***		53		µA
I_{SLEEP} (1)	Low-power SLEEP mode current	Device in SLEEP mode, I_{LOAD} < ***Sleep Current***		22		µA
$I_{SHUTDOWN}$	SHUTDOWN mode current	Fuel gauge in SHUTDOWN mode, CE pin < $V_{IL(CE)}$ max		0.01		µA

(1) Specified by design. Not production tested.

6.6 Electrical Characteristics: Digital Input and Output DC Characteristics

T_A= –40°C to 85°C, V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output voltage, low (SCL, SDA, VEN, LEN, ALERT1, ALERT2 pins)	I_{OL} = 3 mA			0.4	V
$V_{OH(PP)}$	Output voltage, high	I_{OH} = –1 mA	V_{REG25} – 0.5			V
$V_{OH(OD)}$	Output voltage, high (SDA, SCL, ALERT1, ALERT2 pins)	External pull-up resistor connected to V_{REG25}	V_{REG25} – 0.5			V
$V_{IH(ALERT1)}$	Input voltage, high (ALERT1 pin)		1.2		V_{REG25} + 0.3	V
V_{IL}	Input voltage, low		–0.3		0.6	V
$V_{IL(CE)}$	Input voltage, low (CE pin)	V_{REGIN} = 2.7 to 4.5 V			0.8	V
$V_{IH(CE)}$	Input voltage, high (CE pin)	V_{REGIN} = 2.7 to 4.5 V	2.65			V
$V_{IH(OD)}$	Input voltage, high (SDA, SCL, ALERT2 pins)		1.2		5.5	V
I_{LKG}	Input leakage current (I/O pins)				0.3	µA

6.7 Electrical Characteristics: Power-On Reset

T_A = –40°C to 85°C; typical values at T_A = 25°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going battery voltage input at REGIN			2.20		V
V_{HYS}	Power-on reset hysteresis			115		mV

6.8 Electrical Characteristics: LDO Regulator

T_A = 25°C, C_{REG25} = 1.0 µF, V_{REGIN} = 3.6 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage	2.7 V ≤ V_{REGIN} ≤ 4.5 V, I_{OUT} ≤ 16 mA T_A = –40°C to 85°C	2.3	2.5	2.7	V
		2.45 V ≤ V_{REGIN} < 2.7 V, I_{OUT} ≤ 3 mA T_A = –40°C to 85°C	2.3			
I_{SHORT} (2)	Short circuit current limit	V_{REG25} = 0 V T_A = –40°C to 85°C			250	mA

(1) LDO output current, I_{OUT}, is the total load current. Use the LDO regulator to power the internal fuel gauge only.
(2) Specified by design. Not production tested.

6.9 Electrical Characteristics: Internal Temperature Sensor

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{TEMP}	Internal temperature sensor voltage gain			–2		mV/°C

6.10 Electrical Characteristics: Low-Frequency Clock Oscillator

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(EIO)}$	Frequency error(1)(2)	T_A = 0°C to 60°C	–1.5%	0.25%	1.5%	
		T_A = –20°C to 70°C	–2.5%	0.25%	2.5%	
		T_A = –40°C to 85°C	–4%	0.25%	4%	
$t_{(SXO)}$	Start-up time(3)			500		µs

(1) The frequency drift is included and measured from the trimmed frequency at V_{REG25} = 2.5 V, T_A = 25°C.
(2) The frequency error is measured from 32.768 kHz.
(3) The start-up time is defined as the time it takes for the oscillator output frequency to be ±3%.

6.11 Electrical Characteristics: High-Frequency Clock Oscillator

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			8.389		MHz
$f_{(EIO)}$	Frequency error(1)(2)	T_A = 0°C to 60°C	–2%	0.38%	2%	
		T_A = –20°C to 70°C	–3%	0.38%	3%	
		T_A = –40°C to 85°C	–4.5%	0.38%	4.5%	
$t_{(SXO)}$	Start-up time(3)				5	ms

(1) The frequency drift is included and measured from the trimmed frequency at V_{REG25} = 2.5 V, T_A = 25°C.
(2) The frequency error is measured from 8.389 MHz.
(3) The start-up time is defined as the time it takes for the oscillator output frequency to be ±3%.

6.12 Electrical Characteristics: Integrating ADC (Coulomb Counter)

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SR)}$	Differential input voltage range	$V_{(SR)} = V_{(SRP)} – V_{(SRN)}$	–0.125		0.125	V
$V_{(SRP)}$, $V_{(SRN)}$	Input voltage range, $V_{(SRP)}$ and $V_{(SRN)}$		–0.125		0.125	V
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
$V_{OS(SR)}$	Input offset			10		µV
INL	Integral nonlinearity error			±0.007%		FSR(1)
$Z_{IN(SR)}$	Effective input resistance(2)		2.5			MΩ
$I_{LKG(SR)}$	Input leakage current(2)				0.3	µA

(1) Full-scale reference
(2) Specified by design. Not tested in production.

6.13 Electrical Characteristics: ADC (Temperature and Voltage Measurements)

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN((ADC)}$	ADC input voltage range for BAT measurement	Internal voltage divider inactive, internal V_{REF}	0.05		1	V
		Internal voltage divider activated, internal V_{REF}	0.05		4.5	V
	ADC input voltage for TS pin measurement		0		V_{REG25}	V
t_{ADC_CONV} (1)	Conversion time	Single conversion			125	ms
	Resolution		14		15	bits
$V_{OS(ADC)}$	Input offset			1		mV
Z_{ADC_TS}	Effective input resistance (TS with internal pull-down activated) (1)			5		kΩ
Z_{ADC_BAT}	Effective input resistance (BAT) (1)	When not measuring cell voltage (internal voltage divider inactive)		8		MΩ
		During measurement of cell voltage using internal divider (internal voltage divider active)		100		kΩ
$I_{LKG(ADC)}$	Input leakage current (1)				0.3	µA

(1) Specified by design. Not tested in production.

6.14 Electrical Characteristics: Data Flash Memory

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention (1)		10			Years
	Flash –programming write cycles (1)		20,000			Cycles
$t_{WORDPROG}$	Word programming time (1)				2	ms
I_{CCPROG}	Flash-write supply current (1)			5	10	mA

(1) Specified by design. Not tested in production.

6.15 Timing Requirements: I²C-Compatible Interface Timing Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REGIN} = V_{BAT} < 5 V; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_R	SCL/SDA rise time				300	ns
t_F	SCL/SDA fall time				300	ns
$t_{W(H)}$	SCL pulse width (high)		600			ns
$t_{W(L)}$	SCL pulse width (low)		1.3			µs
$t_{SU(STA)}$	Setup for repeated start		600			ns
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{SU(DAT)}$	Data setup time		100			ns
$t_{h(DAT)}$	Data hold time		0			ns
$t_{SU(STOP)}$	Setup time for stop		600			ns
t_{BUF}	Bus free time between stop and start		66			µs
f_{SCL}	Clock frequency				400	kHz

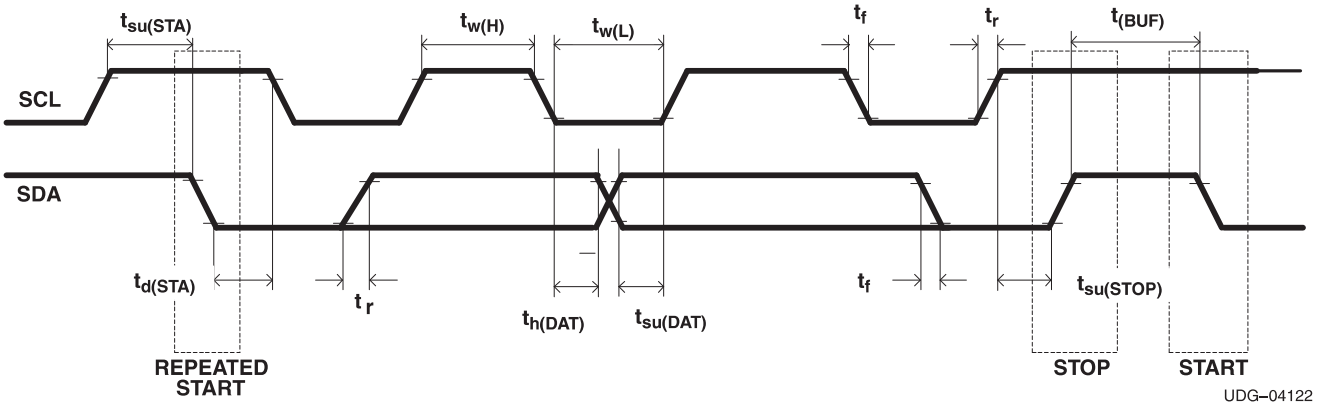


Figure 1. I²C-Compatible Interface Timing Diagram

6.16 Typical Characteristics

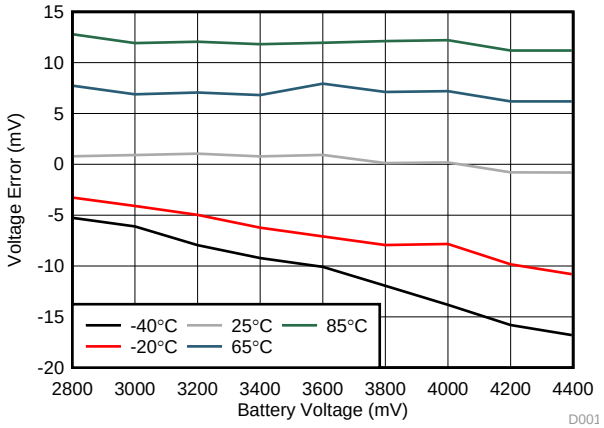


Figure 2. $V_{(Err)}$ Across VIN (0 mA)

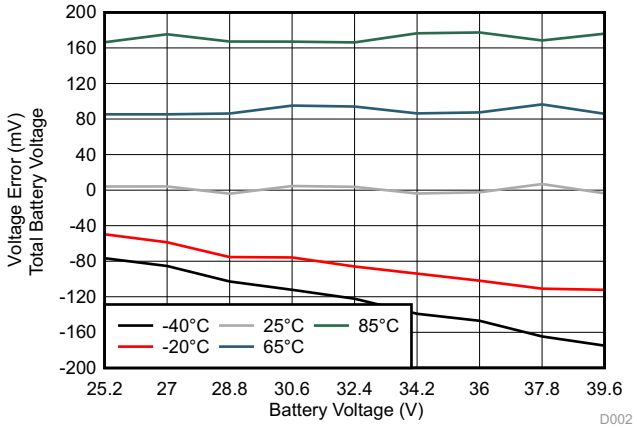


Figure 3. $V_{(Err)}$ Across VIN (0 mA) for a 9-Series Configuration

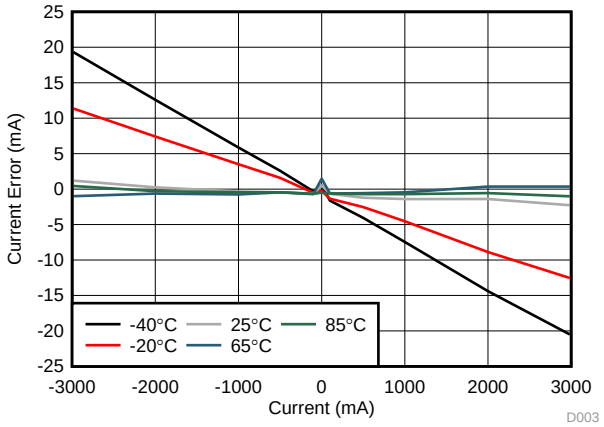


Figure 4. $I_{(Err)}$

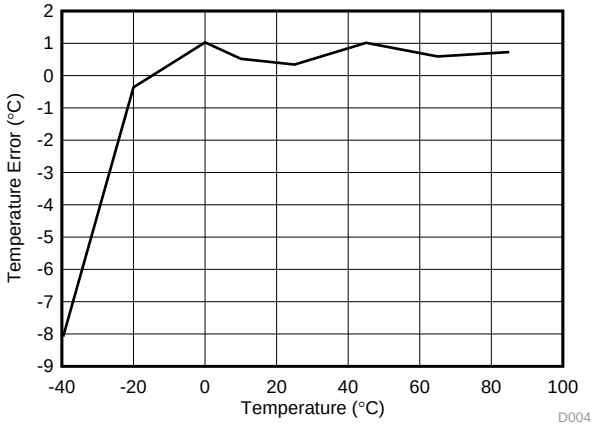


Figure 5. $T_{(Err)}$

7 Detailed Description

7.1 Overview

The bq34110 device incorporates multiple capabilities to provide detailed and sophisticated information on single-cell and multi-cell battery packs. Several different battery chemistries are supported, including Li-Ion, LiFePO4, lead-acid (PbA), Nickel Metal Hydride (NiMH), and Nickel Cadmium (NiCd). The device integrates a gas gauge for monitoring battery charge level, an End-Of-Service (EOS) Determination function to evaluate when a battery is nearing the end of its usable life, a specialized ***WHr Charge Termination*** function to enable battery charging to a targeted energy capacity, a charge control scheme using direct pin control, SHA-1/HMAC-based authentication, and lifetime data logging functionality.

NOTE

Formatting Conventions in This Document:

Commands: *italics* with parentheses and no breaking spaces; for example, *Control()*

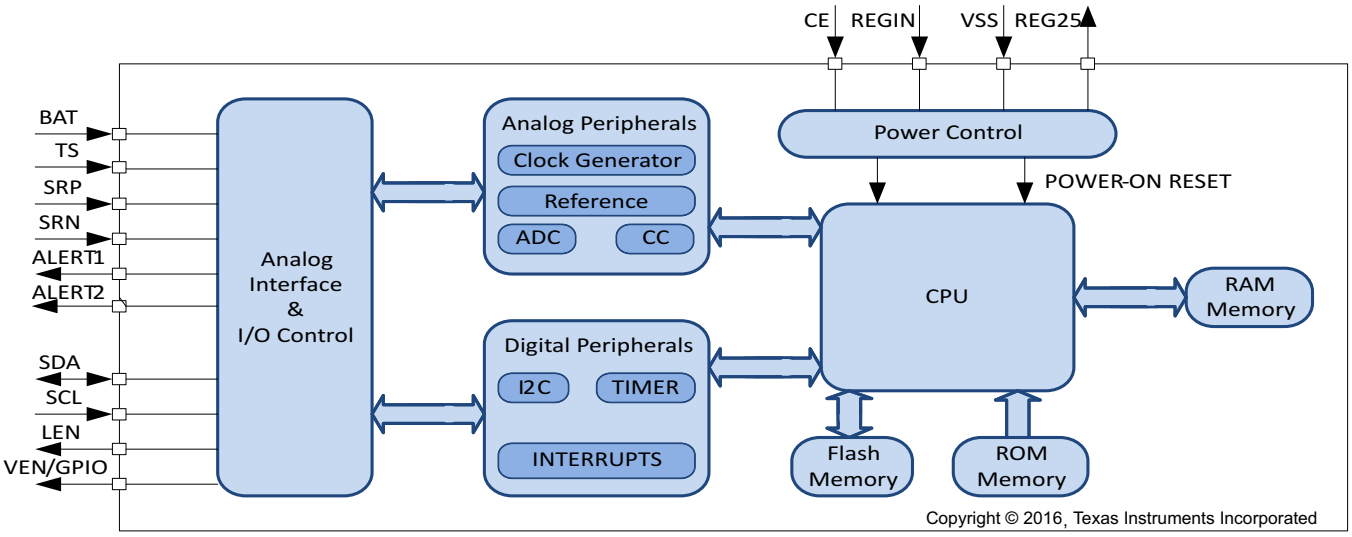
Data Flash: *italics*, **bold**, and breaking spaces; for example, ***Design Capacity***

Register Bits and Flags: brackets only; for example, [TDA]

Data Flash Bits: *italic* and **bold**; for example, ***[XYZ1]***

Modes and States: ALL CAPITALS; for example, UNSEALED mode

7.2 Functional Block Diagram



7.3 Feature Description

The bq34110 gas gauge uses Compensated End-of-Discharge Voltage (CEDV) technology to accurately predict the battery capacity and other operational characteristics of the battery, and can be interrogated by a host processor to provide cell information, such as remaining capacity, full charge capacity, and average current.

The integrated End-Of-Service (EOS) Determination function is specifically intended for applications where the battery is rarely discharged, such as in uninterruptible power supplies (UPS), enterprise server backup systems, and telecommunications backup modules. In such systems, the battery may remain in a fully (or near-fully) charged state for much of its lifetime, with it rarely or never undergoing a significant discharge. If the health of the battery in such a system is not monitored regularly, then it may degrade beyond the level required for a system backup/discharge event, and thus fail precisely at the time when it is needed most.

Feature Description (continued)

The EOS Determination function monitors the health of the battery through the use of infrequent Learning Phases, which involves a controlled discharge of ~1% capacity, and provides an alert to the system when the battery is approaching the end of its usable service. By coordinating battery charging with the Learning Phases, the battery capacity available to the system can be maintained above a preselected level to avoid compromising the ability for the battery to support a system discharge event.

The bq34110 device can support multi-cell battery configurations with maximum voltage up to 65 V through the use of external and internal resistive divider networks to reduce the voltage to an acceptable range for the device's integrated ADC. These resistive dividers are actively controlled to avoid unnecessary power dissipation when not needed. The device integrates an internal temperature sensor as well as support for an external NTC thermistor, such as a Semitec 103AT or Mitsubishi BN35-3H103FB-50.

The battery current is monitored by measuring the voltage across a series resistor, R_{SENSE}, which is placed in series with the battery pack and has a typical value of 5 mΩ to 20 mΩ. The bq34110 device integrates two ADCs, one of which is dedicated to current measurement, and the second used for measurement of several other parameters, including temperature and voltage.

Communication with the device is provided through an I^2C interface, supporting rates up to 400 kHz. Dual ALERT pins are provided with programmable configuration, which enables them to be used for such functions as a host interrupt/alert or controlling the battery charger.

To minimize power consumption, the bq34110 gauge has several power modes: NORMAL, SNOOZE, and SLEEP, which are under register or algorithm control. In addition, a separate chip enable (CE) pin is provided to control the internal LDO, which powers the bq34110 internal circuitry, and can put the device into SHUTDOWN mode.

Information is accessed through a series of commands called Data Commands, which are indicated by the general format *Command()*. These commands are used to read and write information in the bq34110 device's control and status registers, as well as its data flash locations.

Commands are sent from the host to the bq34110 device via I^2C and can be executed during application development, pack manufacture, or end-equipment operation. Cell information is stored in the bq34110 device in non-volatile flash memory. Many of the data flash locations are accessible during application development and pack manufacture. They cannot, generally, be accessed directly during end-equipment operation. Access to these locations is achieved by using the bq34110 device's companion evaluation software, through individual commands, or through a sequence of data flash access commands. To access a desired data flash location, the correct data flash subclass and offset must be known.

The bq34110 device provides 32 bytes of user-programmable data flash memory. This data space is accessed through a data flash interface. For specifics on accessing the data flash, see the *bq34110 Technical Reference Manual* (SLUUBF7).

A SHA-1/HMAC-based battery pack authentication feature is also implemented on the bq34110 device. When the device is in UNSEALED mode, authentication keys can be (re)assigned. A scratch pad area is used to receive challenge information from a host and to export SHA-1/HMAC encrypted responses. For more information on authentication, see the *bq34110 Technical Reference Manual* (SLUUBF7).

7.3.1 Communications

7.3.1.1 I^2C Interface

The bq34110 device supports the standard I^2C read, incremental read, one-byte write quick read, and functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively.

Feature Description (continued)

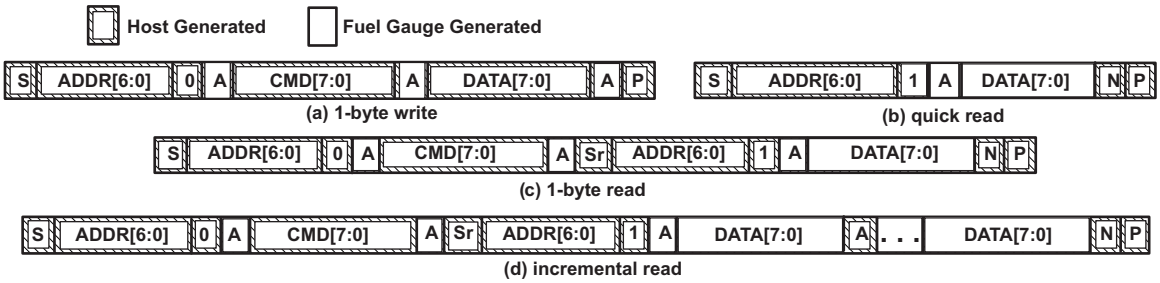


Figure 6. Supported I²C formats: (a) 1-byte write, (b) quick read, (c) 1 byte-read, and (d) incremental read (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The “quick read” returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, increments whenever data is acknowledged by the device or the I²C master. “Quick writes” function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as 2-byte commands that require two bytes of data).

Figure 7. Attempt to Write a Read-Only Address (Nack After Data Sent By Master)

Figure 8. Attempt to Read an Address Above 0x7F (NACK Command)

Figure 9. Attempt at Incremental Writes (Nack All Extra Data Bytes Sent)

Figure 10. Incremental Read at the Maximum Allowed Read Address

7.3.1.2 I²C Time Out

The I²C engine releases both SDA and SCL if the I²C bus is held low for a time programmed in data flash. If the device were holding the lines, releasing them frees the master to drive the lines.

Detailed examples of I²C transactions accessing gauge data can be found in the *Using I²C Communication with the bq275xx Series of Fuel Gauges Application Report* (SLUA467).

7.4 Device Functional Modes

The bq34110 device has four functional power modes: NORMAL, SNOOZE, SLEEP, and SHUTDOWN, based on firmware and/or host control.

- In NORMAL mode, the device is fully powered and can execute any allowable task.
- In SNOOZE mode, the device periodically wakes to take data measurements and updates the data set, after which it then returns directly to SNOOZE.
- In SLEEP mode, the device maintains the low-frequency oscillator but turns off the high-frequency oscillator and exists in a reduced-power state, periodically taking measurements and performing calculations.
- In SHUTDOWN mode, the device is fully powered down and can only be awakened using the chip enable (CE) pin.

8 Application and Implementation

NOTE

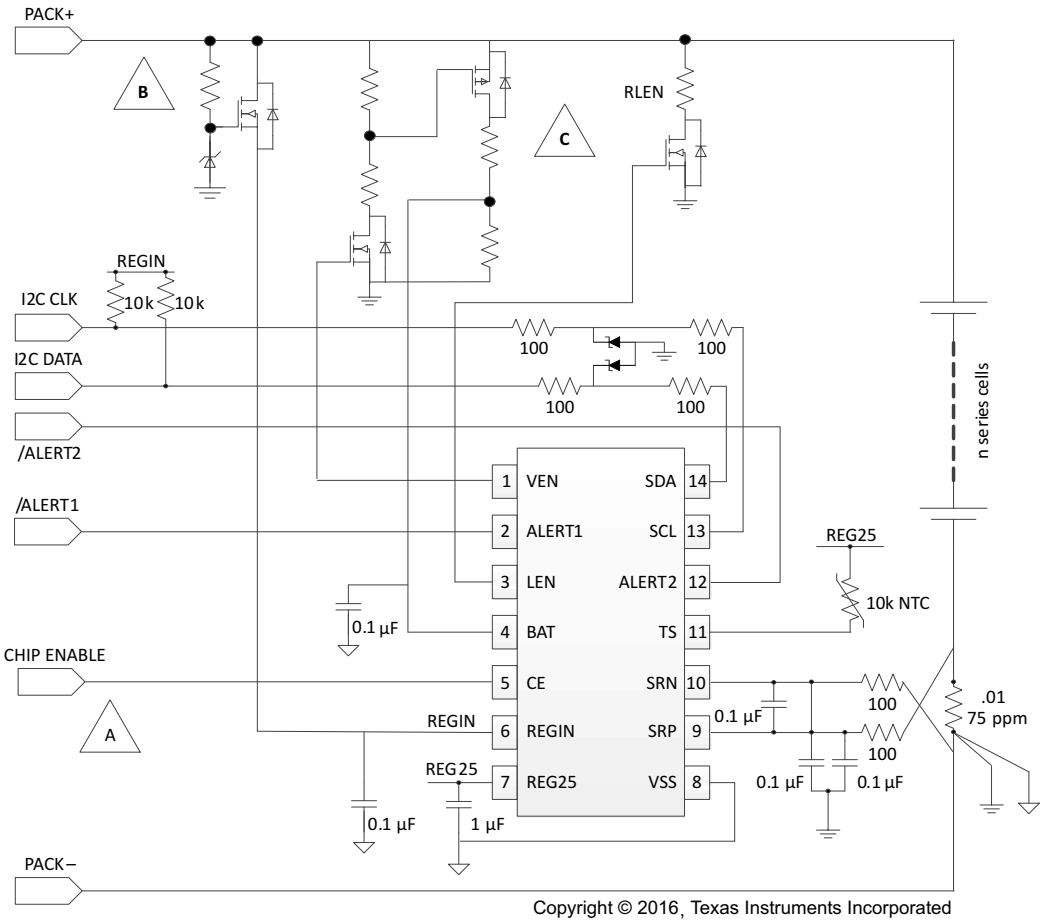
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq34110 gas gauge is a highly configurable device with multiple features that can be used individually or simultaneously (with some restrictions). The CEDV gas gauging function together with its support for an external voltage divider allows gauging of high voltage, multi-cell battery configurations of various chemistries. The EOS Determination function is intended for rarely discharged applications and evaluates the condition of the battery without requiring conventional maintenance cycles. These and additional features are described in detail in the *bq34110 Technical Reference Manual* (SLUUBF7).

8.2 Typical Applications

Figure 11 is a simplified schematic of the bq34110 system used in a multi-cell configuration.



A If power control of the gauge is not required by the system, then CE should be connected directly to REGIN.

B Required for applications of more than one-series cell; otherwise, REGIN can connect directly to single-cell BAT+ or an alternative power source.

C Required for applications of more than one-series cell; otherwise, BAT connects directly to single-cell BAT+ and VEN can be left unconnected.

Figure 11. bq34110 Simplified System Diagram

Typical Applications (continued)

Figure 12 shows the schematic of the bq34110 EVM, and depicts how the device can be used in the system.

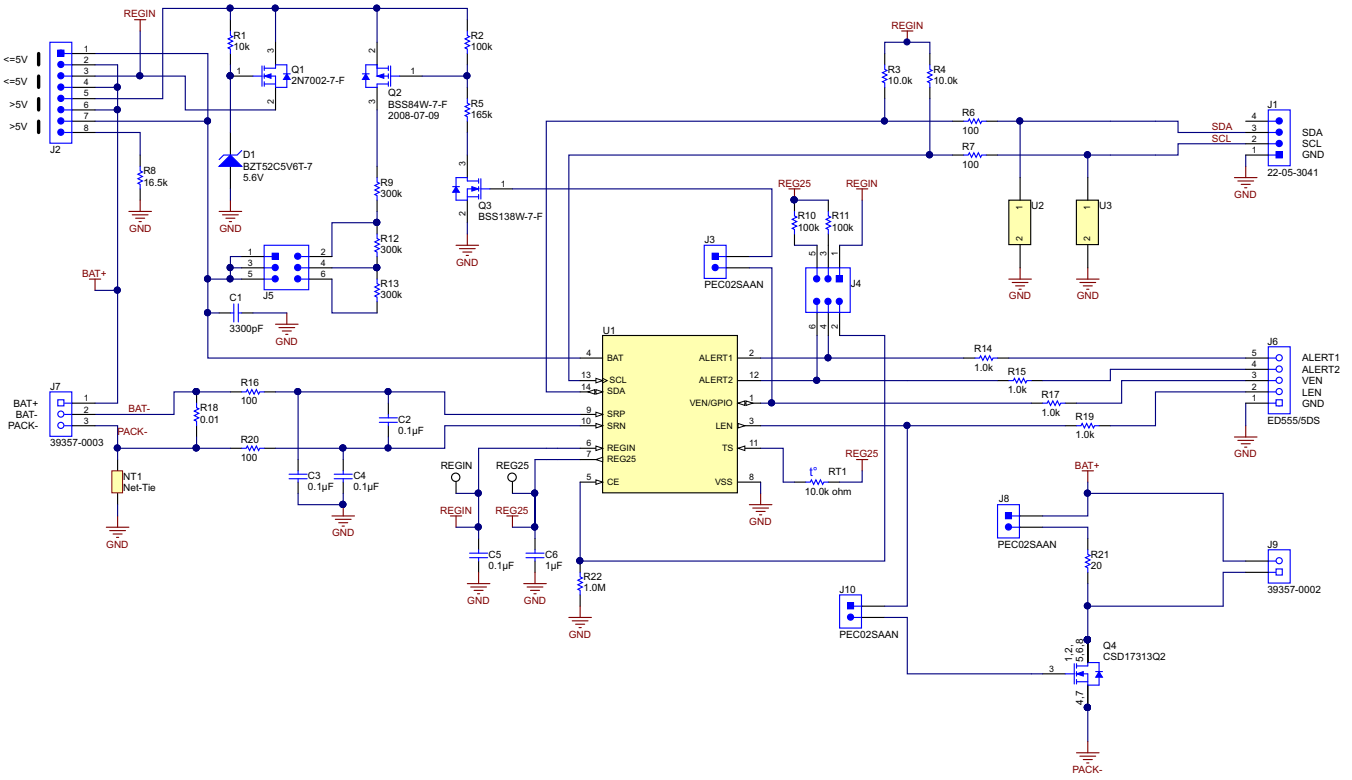


Figure 12. bq34110 EVM Schematic

8.2.1 Design Requirements

The bq34110 device supports several circuit configuration options that can be decided upon during the system design phase. Using the device with a single-cell battery versus a multi-cell configuration determines if there is a need for a battery divider and associated control using the VEN pin (as shown in Figure 11). The functions used within the bq34110 device also determine the pin usage, with the device incorporating flexibility to reuse pins for other purposes if the system configuration permits. For example, if a single-cell configuration is selected, then the VEN pin can be used as part of a direct charge control scheme. Similarly, the LEN, ALERT1, and/or ALERT2 pins can also be repurposed to support direct charge control. For additional design guidelines, refer to the *bq34110 EVM User's Guide* (SLUUBI1).

8.2.2 Detailed Design Procedure

8.2.2.1 BAT Voltage Sense Input

A ceramic capacitor at the input to the BAT pin is used to bypass AC voltage ripple to ground, greatly reducing its influence on battery voltage measurements. It proves most effective in applications with load profiles that exhibit high-frequency current pulses (that is, cell phones) but is recommended for use in all applications to reduce noise on this sensitive high-impedance measurement node. If the device is used in a multi-cell configuration with an external resistive voltage divider, it is recommended that the resistors used therein be selected with temperature coefficient of resistance (TCR) of 75-ppm or below. More detail on the design of the voltage divider network is discussed in the *bq34110 Technical Reference Manual* (SLUUBF7).

Typical Applications (continued)

8.2.2.2 SRP and SRN Current Sense Inputs

The filter network at the input to the coulomb counter is intended to improve differential mode rejection of voltage measured across the sense resistor. These components should be placed as close as possible to the coulomb counter inputs, and the routing of the differential traces length-matched to best minimize impedance mismatch-induced measurement errors.

8.2.2.3 Sense Resistor Selection

Any variation encountered in the resistance present between the SRP and SRN pins of the fuel gauge will affect the resulting differential voltage, and derived current, it senses. As such, it is recommended to select a sense resistor with minimal tolerance and temperature coefficient of resistance (TCR) characteristics. The standard recommendation based on the best compromise between performance and price is a 1% tolerance, 75-ppm drift sense resistor with a 1-W power rating.

8.2.2.4 TS Temperature Sense Input

Similar to the BAT pin, a ceramic decoupling capacitor for the TS pin is used to bypass AC voltage ripple away from the high-impedance ADC input, minimizing measurement error. It should be placed as close as possible to the respective input pin for optimal filtering performance.

8.2.2.5 Thermistor Selection

The fuel gauge temperature sensing circuitry is designed to work with a negative temperature coefficient-type (NTC) thermistor with a characteristic 10-kΩ resistance at room temperature (25°C). The default curve-fitting coefficients configured in the fuel gauge specifically assume a 103AT-2 type thermistor profile and so that is the default recommendation for thermistor selection purposes. Moving to a separate thermistor resistance profile (for example, JT-2 or others) requires an update to the default thermistor coefficients in data flash to ensure highest accuracy temperature measurement performance.

8.2.2.6 REGIN Power Supply Input Filtering

A ceramic capacitor is placed at the input to the fuel gauge internal LDO to increase power supply rejection (PSR) and improve effective line regulation. It ensures that voltage ripple is rejected to ground instead of coupling into the internal supply rails of the fuel gauge.

8.2.2.7 REG25 LDO Output Filtering

A ceramic capacitor is also needed at the output of the internal LDO to provide a current reservoir for fuel gauge load peaks during high peripheral utilization. It acts to stabilize the regulator output and reduce core voltage ripple inside the fuel gauge.

Typical Applications (continued)

8.2.3 Application Curves

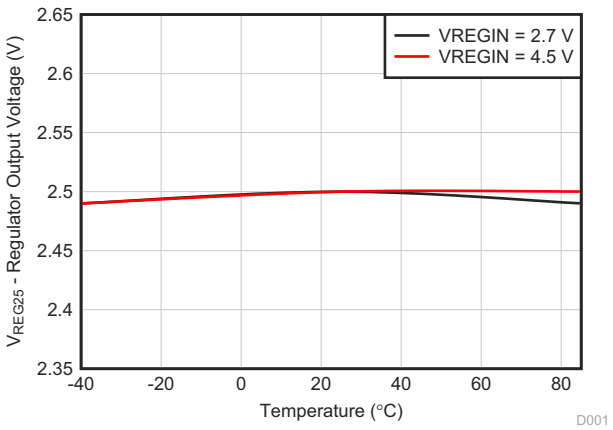


Figure 13. Regulator Output Voltage vs. Temperature

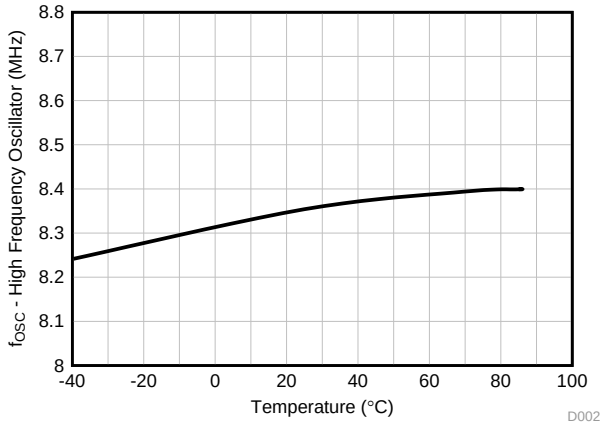


Figure 14. High-Frequency Oscillator Frequency vs. Temperature

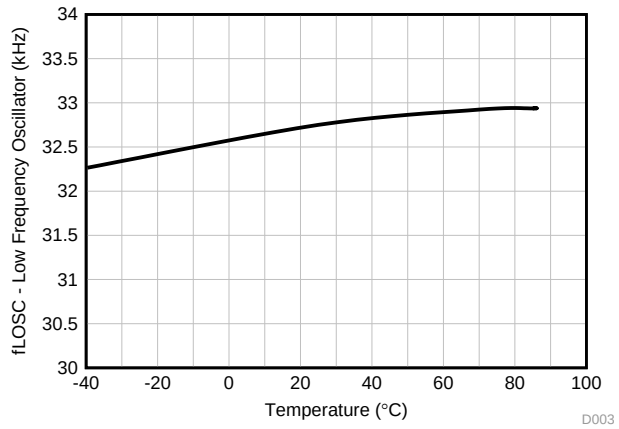


Figure 15. Low-Frequency Oscillator Frequency vs. Temperature

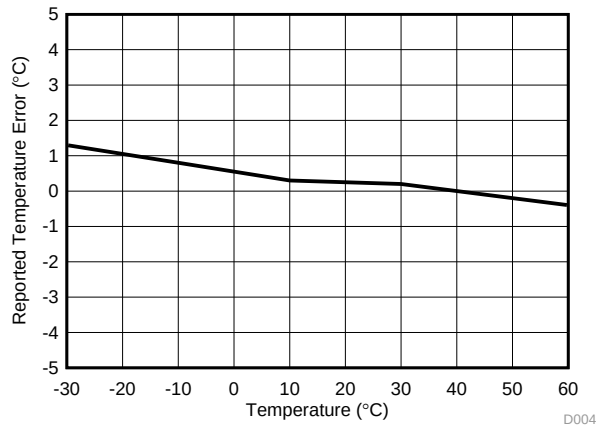


Figure 16. Reported Internal Temperature Measurement vs. Temperature

9 Power Supply Recommendations

Power supply requirements for the bq34110 device are simplified due to the presence of the internal LDO-voltage regulation. The REGIN pin accepts any voltage level between 2.7 V and 4.5 V, which is optimum for a single-cell Li-Ion application. For higher battery voltage applications, a simple preregulator can be provided to power the bq34110 device. Decoupling the REGIN pin should be done with a 0.1-µF 10% ceramic X5R capacitor placed close to the device. While the preregulator circuit is not critical, special attention should be paid to its quiescent current and power dissipation. The input voltage should handle the maximum battery stack voltage. The output voltage can be centered within the 2.7-V to 4.5-V range as recommended for the REGIN pin.

For high stack count applications, a commercially available LDO is often the best quality solution, but comes with a cost tradeoff. To lower the BOM cost, the following approaches are recommended.

In Figure 17, Q1 is used to drop the battery stack voltage to roughly 4 V to power the bq34110 device's REGIN pin. To avoid unwanted quiescent current consumption, R1 should be set as high as is practical. It is recommended to use a low-current Zener diode.

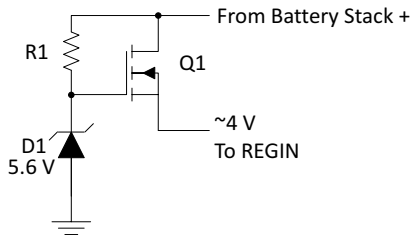


Figure 17. Q1 Dropping Battery Stack Voltage to 4 V

Alternatively, if the range of a high-voltage battery stack can be well-defined, a simple source follower based on a resistive divider can be used to lower the BOM cost and the quiescent current. For example:

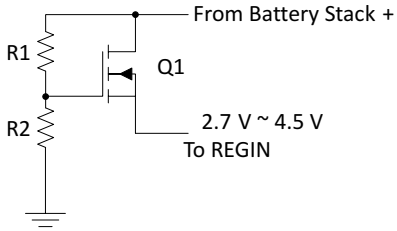


Figure 18. Source Follower on a Resistive Divider

10 Layout

10.1 Layout Guidelines

Attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that are not always trivial to solve. Some of the key areas of concern are described in the following sections and can help to enable success.

10.1.1 Power Supply Decoupling Capacitor

Power supply decoupling from REG25 to ground is important for optimal operation of the gas gauge. To keep the loop area small, place this capacitor next to the IC and use the shortest possible traces. A large loop area renders the capacitor useless and forms a small-loop antenna for noise pickup. Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSS pin to a ground plane layer.

10.1.2 Capacitors

Power supply decoupling for the gas gauge requires 0.1-μF ceramic capacitors for the BAT and REGIN pins. These should be placed reasonably close to the IC without using long traces back to VSS. The LDO voltage regulator, whether external or internal to the main IC, requires a 1-μF ceramic capacitor to be placed fairly close to the regulation output pin (REG25). This capacitor is for amplifier loop stabilization and as an energy well for the 2.5-V supply.

10.1.3 Communication Line Protection Components

5.6-V Zener diodes are included on the I^2C lines to protect the communication pins of the gas gauge from ESD. These diodes should be located as close as possible to the pack connector. The grounded end of these Zener diodes should be returned to the PACK(–) node rather than to the low-current digital ground system. This way, ESD is diverted away from the sensitive electronics as much as possible.

10.2 Layout Example

10.2.1 Ground System

The gas gauge requires a low-current ground system separate from the high-current PACK(–) path. ESD ground is defined along the high-current path from the PACK(–) terminal to the sense resistor. It is important that the low-current ground systems only connect to the PACK(–) path at the sense resistor Kelvin pick-off point. It is recommended to use an optional inner layer ground plane for the low-current ground system.

In Figure 19, the green area shows an example of using the low-current ground as a shield for the gas gauge circuit. Notice how it is kept separate from the high-current ground, which is shown in red. The high current path is joined with the low-current path only at one point, shown with the small blue connection between the two planes.

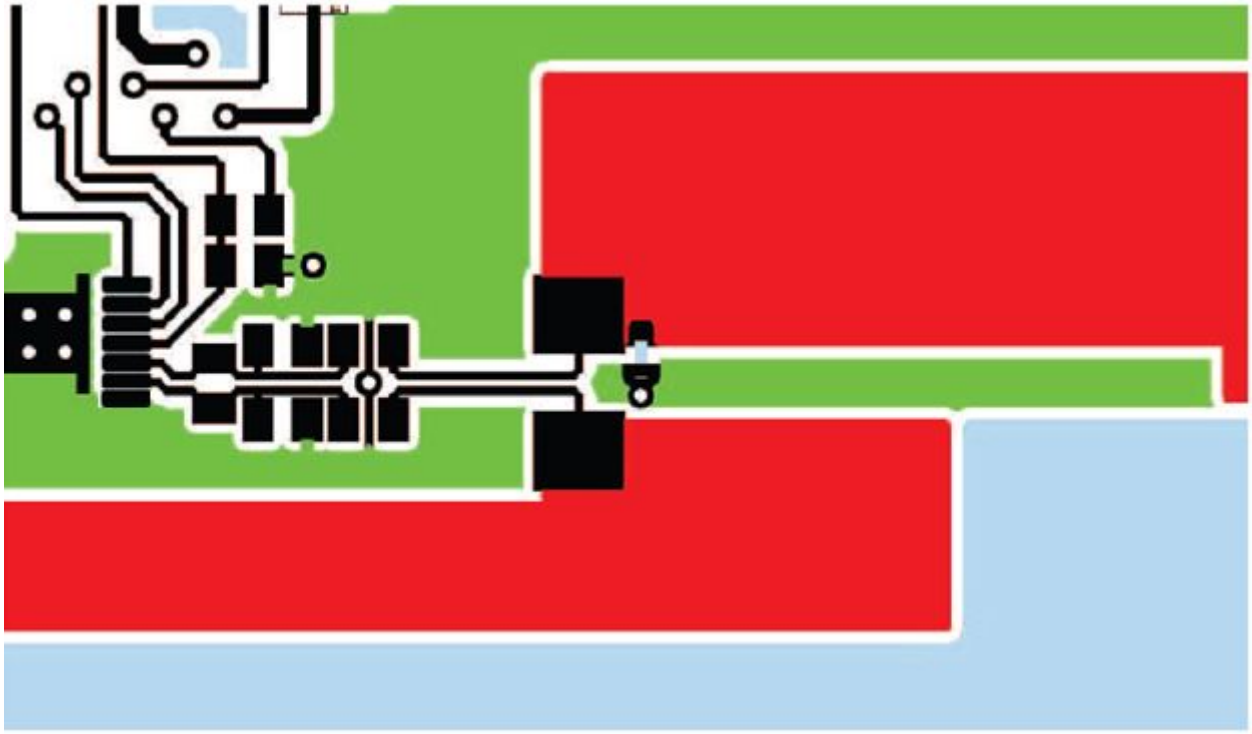


Figure 19. High-Current Versus Low-Current Ground Layout

10.2.2 Kelvin Connections

Kelvin voltage sensing is very important to accurately measure current and cell voltage. Note that in Figure 19 the differential connections at the sense resistor do not add any voltage drop across the copper etch that carries the high current path through the sense resistor.

10.2.3 Board Offset Considerations

Although the most important component for board offset reduction is the decoupling capacitor for REGIN, additional benefit is possible by using this recommended pattern for the coulomb counter differential low-pass filter network.

Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100-Ω resistors, as shown in Figure 20.

Layout Example (continued)

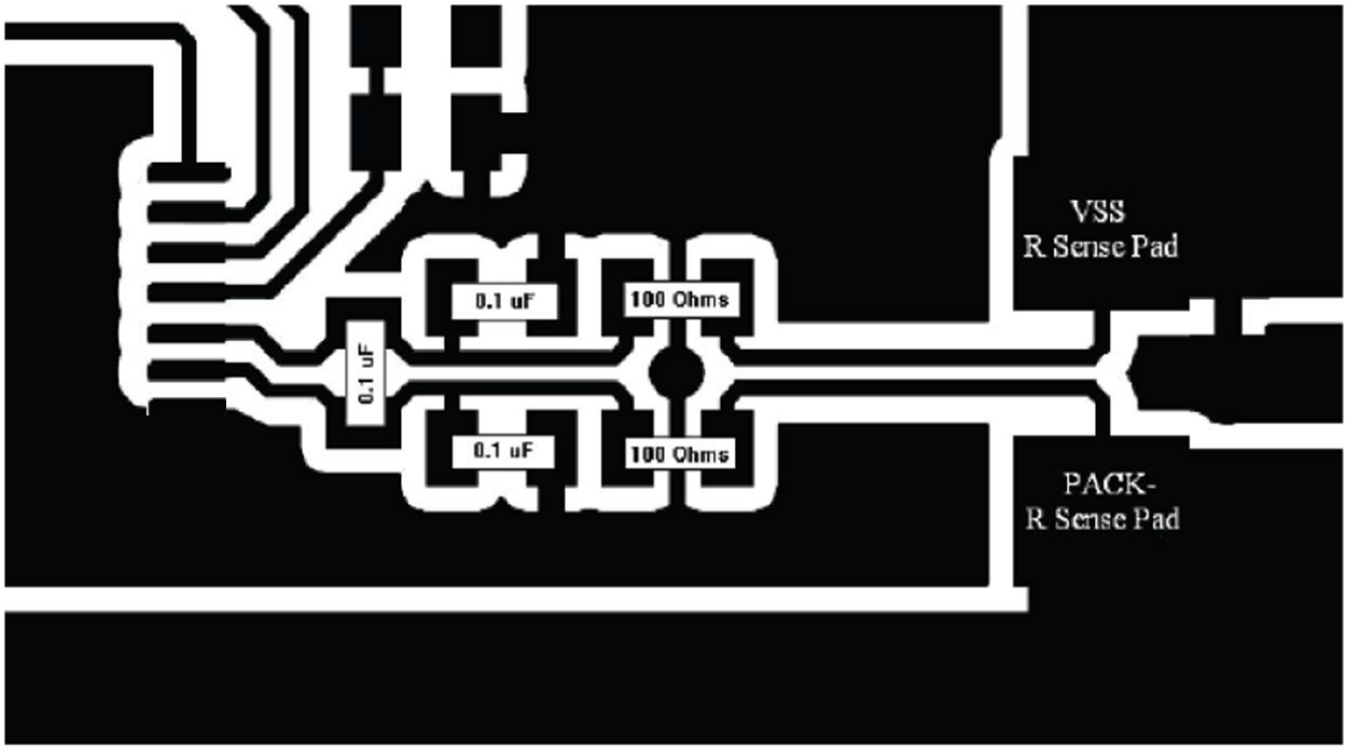


Figure 20. Differential Connection Between SRP and SRN Pins with Sense Resistor

10.2.4 ESD Spark Gap

Protect the communication lines from ESD with a spark gap at the connector. Figure 21 shows the recommended pattern with its 0.2-mm spacing between the points.

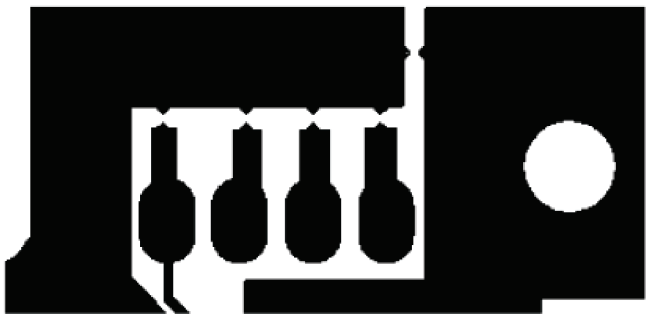


Figure 21. Recommended Spark-Gap Pattern Helps Protect Communication Lines from ESD

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

- 《*bq34110 技术参考手册*》（文献编号：SLUUBF7）
- 《*bq34110 EVM 用户指南*》（文献编号：SLUUBI1）
- 《*使用 I²C 与 bq275xx 系列电量监测计通信应用报告*》（文献编号：SLUA467）

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
通过 I²C is a trademark of NXP B.V. Corporation.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ34110PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ34110	Samples
BQ34110PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ34110	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

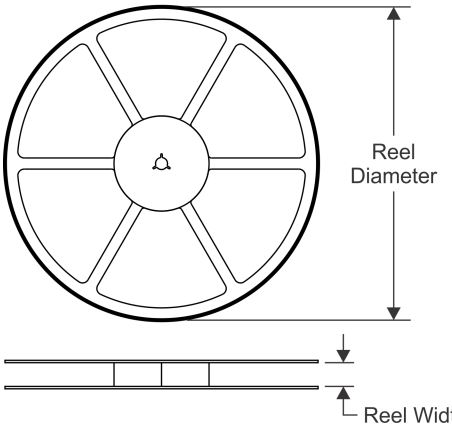
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

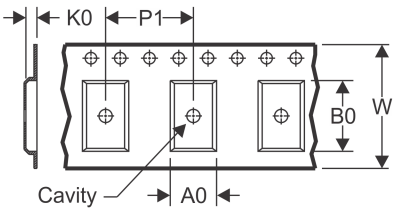
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

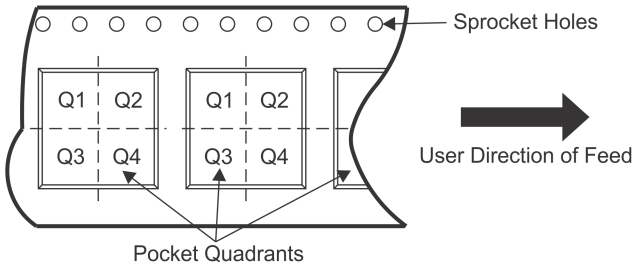


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

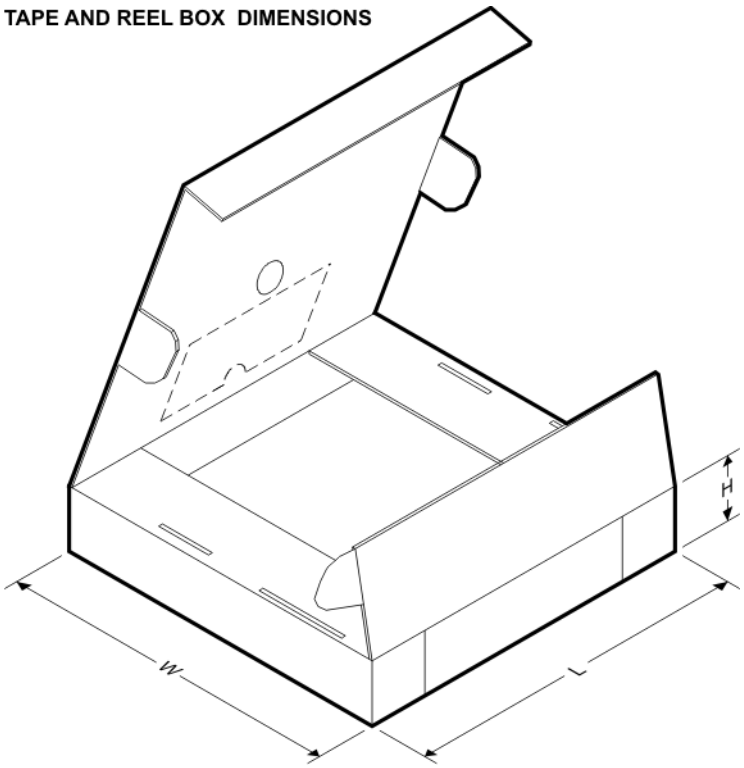
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ34110PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

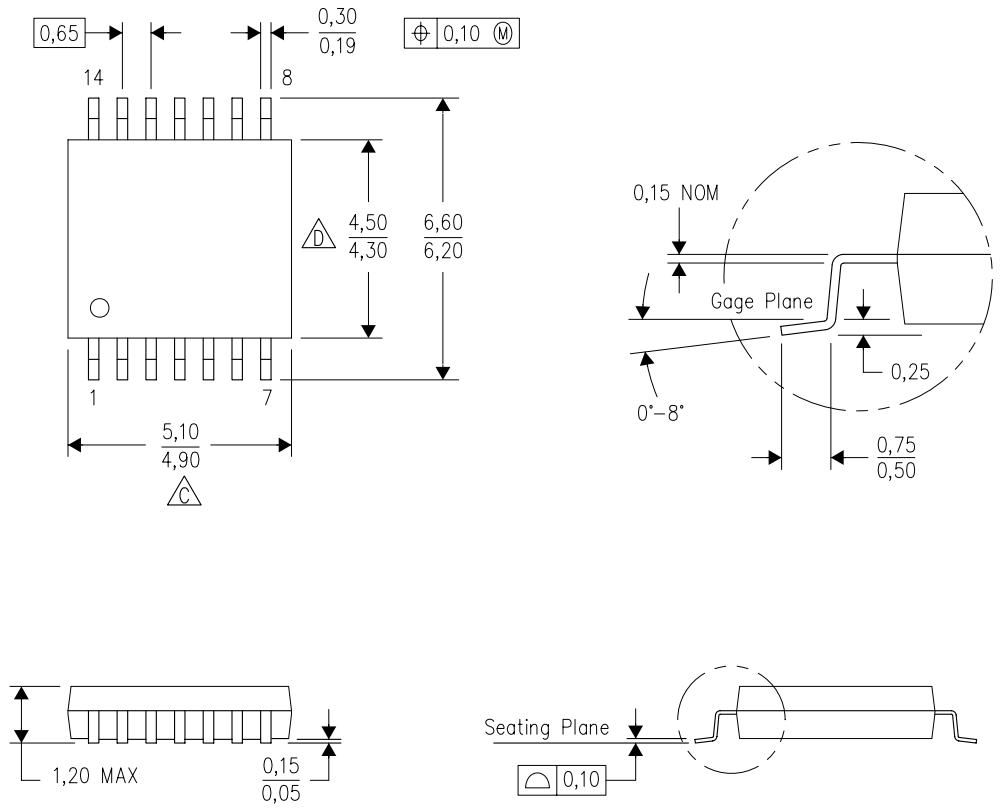
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ34110PWR	TSSOP	PW	14	2000	367.0	367.0	38.0

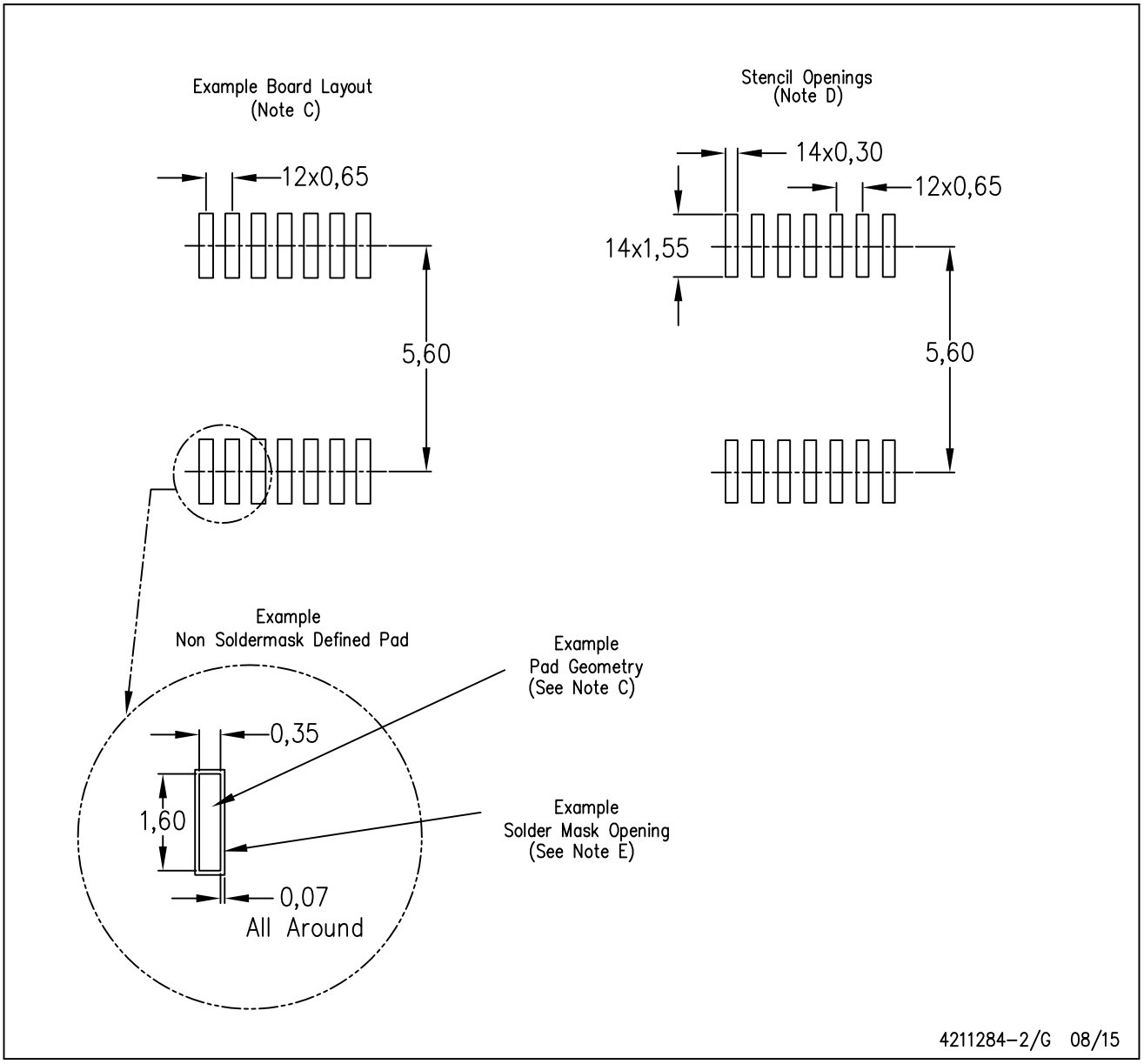
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122