P3S0200

I3C switch with hardware select and enable

Rev. 1.0 — 14 February 2022 Product data sheet

1 General description

The P3S0200 is ideally suited for the switching of high-speed I3C signals in communication and server applications, such as servers, workstations, and notebooks that have limited I3C I/Os. The wide bandwidth (52 MHz) of this switch allows signal to pass with minimum edge and phase distortion. The device multiplexes differential outputs from the I3C controller to one of two corresponding targets with hardware select pin. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation.

2 Features and benefits

- Wide supply voltage range from 2.3 V to 3.6 V
- Switch voltage accepts signals up to 5.5 V
- 1.8 V control logic at V_{CC} = 3.6 V
- Low-power mode when $\overline{OE}$ is HIGH (2 μA maximum)
- 6 Ω (maximum) ON resistance
- 0.1 Ω (typical) ON resistance mismatch between channels
- 6 pF (typical) ON-state capacitance
- High bandwidth (52 MHz typical)
- Latch-up performance exceeds 100 mA per JESD 78B Class II Level A
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 8000 V
  - CDM JESD22-C101E exceeds 1000 V
  - HBM exceeds 12000 V for I/O to GND protection
- Specified from -40 °C to +85 °C

3 Applications

- I3C or I^2C 2:1 or 1:2 mux with hardware select pin allowing bus voltage up to 5.5 V

4 Ordering information

Table 1. Ordering information

Type number	Topside marking [1]	Package		
		Name	Description	Version
P3S0200GM	x00	XQFN10	plastic extremely thin quad flat package; no leads; 10 terminals; body 2 × 1.55 × 0.5 mm	SOT1049-3

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method [1]	Minimum order quantity	Temperature
P3S0200GM	P3S0200GMX	XQFN10	REEL 7" Q1 NDP	5000	T_{amb} = -40 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

5 Functional diagram

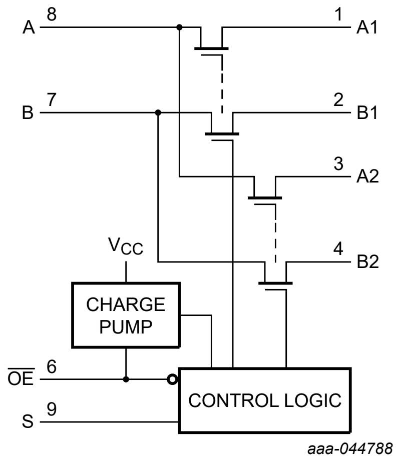


Figure 1. Logic symbol

6 Pinning information

6.1 Pinning

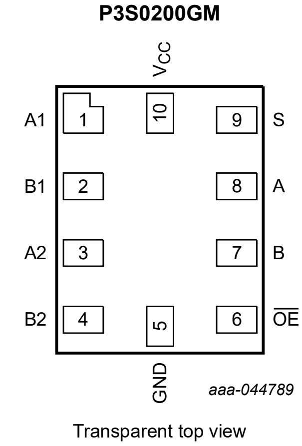


Figure 2. Pin configuration SOT1049-3 (XQFN10)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
A1	1	independent input or output
B1	2	independent input or output
A2	3	independent input or output
B2	4	independent input or output
GND	5	ground (0 V)
$\overline{OE}$	6	output enable input (active LOW)
B	7	common input or output
A	8	common input or output
S	9	select input
V_{CC}	10	supply voltage

7 Functional description

Table 4. Function table[1]

Input		Channel
S	$\overline{OE}$	
L	L	A = A1; B = B1
H	L	A = A2; B = B2
X	H	switches off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	S, $\overline{OE}$ input	[1]	-0.5	+7.0	V
V_{SW}	switch voltage		[2]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V		-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V		-50	-	mA
I_{SW}	switch current			-	±120	mA
I_{CC}	supply current			-	+100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C		-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			2.3	3.6	V
V_I	input voltage	S, $\overline{OE}$ input		0	V_{CC}	V
V_{SW}	switch voltage			0	5.5	V
T_{amb}	ambient temperature			-40	+85	°C

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); T_{amb} =-40 °C to +85 °C

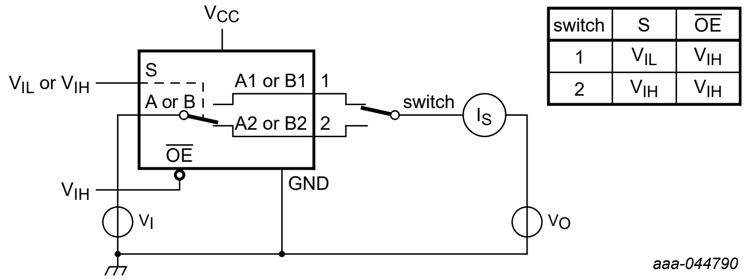
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	$0.46V_{CC}$	-	-	V
		V_{CC} = 2.7 V to 3.6 V	$0.46V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	-	$0.25V_{CC}$	V
		V_{CC} = 2.7 V to 3.6 V	-	-	$0.25V_{CC}$	V
V_{IK}	input clamping voltage	V_{CC} = 2.7 V, 3.6 V; I_I = -18 mA	-	-	-1.8	V
I_I	input leakage current	S, $\overline{OE}$ input; V_{CC} = 0 V, 2.7 V, 3.6; V_I = GND to 3.6 V	-	0.01	±1	μA
I_{OFF}	power-off leakage current	per pin; V_{CC} = 0 V				
		V_{SW} = 0 V to 2.7 V	-	0.01	±2.0	μA
		V_{SW} = 0 V to 3.6 V	-	0.01	±2.0	μA
		V_{SW} = 0 V to 5.25 V	-	0.01	±3.0	μA
$I_{S(OFF)}$	OFF-state leakage current	A and B ports; see Figure 3				
		V_{CC} = 2.7 V, 3.6 V	-	-	±1	μA
I_{CC}	supply current	V_{CC} = 2.7 V, 3.6 V				
		$\overline{OE}$ = GND	-	18.5	30	μA
		$\overline{OE}$ = V_{CC} (low-power mode)	-	0.01	2	μA
ΔI_{CC}	additional supply current	S, $\overline{OE}$ input; one input at 1.8 V; other inputs at GND or V_{CC}				
		V_{CC} = 2.7 V	-	0.8	1.8	μA
		V_{CC} = 3.6 V	-	12.5	20	μA
C_I	input capacitance	V_{SW} = GND or V_{CC}; V_{CC} = 2.5 V, 3.3 V	-	1	2.5	pF

Table 7. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground 0 V); T_{amb} =-40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{S(OFF)}$	OFF-state capacitance	V_{SW} = GND or V_{CC}; V_{CC} = 2.5 V, 3.3 V	-	3	5.0	pF
$C_{S(ON)}$	ON-state capacitance	V_{SW} = GND or V_{CC}; V_{CC} = 2.5 V, 3.3 V	-	6	7.5	pF

10.1 Test circuits



V_I = 0 V; V_O = 0 V to 5.25 V

Figure 3. Test circuit for measuring OFF-state leakage current

10.2 ON resistance

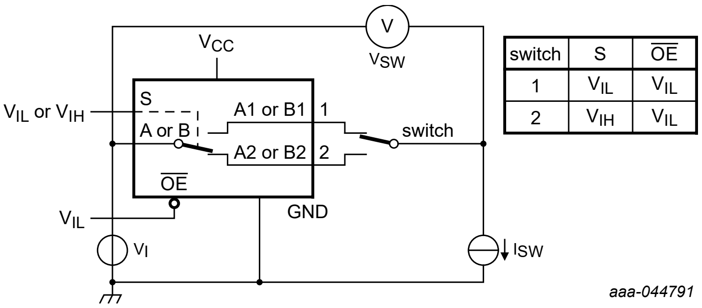
Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 5; T_{amb} =-40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
R_{ON}	ON resistance	V_{CC} = 2.3 V, 3.0 V see Figure 4					
		V_I = 0 V; I_I = 30 mA		-	3.6	6	Ω
		V_I = 2.4 V; I_I = -15 mA		-	4.3	7	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_{CC} = 2.3 V, 3.0 V	[2]				
		V_I = 0 V; I_I = 30 mA		-	0.1	-	Ω
		V_I = 1.7 V; I_I = -15 mA		-	0.1	-	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_{CC} = 2.3 V, 3.0 V; V_I = 0 V to V_{CC}	[3]				
		I_I = 30 mA		-	0.8	-	Ω
		I_I = -15 mA		-	0.7	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C.
[2] Measured at identical V_{CC}, temperature and input voltage.
[3] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3 ON resistance test circuit and waveforms



$R_{ON} = V_{SW} / I_{SW}$.

Figure 4. Test circuit for measuring ON resistance

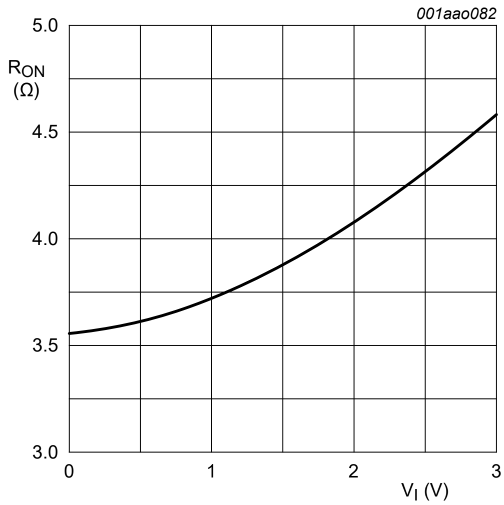


Figure 5. ON resistance as a function of input voltage

11 Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 9.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{pd}	propagation delay	A/B to An/Bn or An/Bn to A/B; see Figure 6	[2][3]				
		V_{CC} = 2.3 V to 2.7 V		-	0.25	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	0.25	-	ns
t_{en}	enable time	S to A/B, An/Bn; see Figure 8	[3]				
		V_{CC} = 2.3 V to 2.7 V		-	-	50	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	30	ns
		$\overline{OE}$ to A/B, An/Bn; see Figure 8	[3]				

Table 9. Dynamic characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 9.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
		V_{CC} = 2.3 V to 2.7 V		-	-	32	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	17	ns
t_{dis}	disable time	S to A/B, An/Bn; see Figure 8	[3]				
		V_{CC} = 2.3 V to 2.7 V		-	-	23	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	12	ns
		$\overline{OE}$ to A/B, An/Bn; see Figure 8	[3]				
		V_{CC} = 2.3 V to 2.7 V		-	-	12	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	10	ns
$t_{sk(o)}$	output skew time	see Figure 7	[4]				
		V_{CC} = 2.3 V to 2.7 V		-	0.1	0.2	ns
		V_{CC} = 3.0 V to 3.6 V		-	0.1	0.2	ns
$t_{sk(p)}$	pulse skew time	see Figure 6	[4]				
		V_{CC} = 2.3 V to 2.7 V		-	0.1	0.2	ns
		V_{CC} = 3.0 V to 3.6 V		-	0.1	0.2	ns

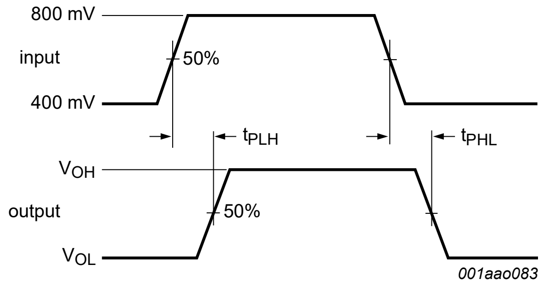
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 2.5 V and 3.3 V respectively.

[2] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[3] t_{pd} is the same as t_{PLH} and t_{PHL}.

[4] Guaranteed by design.

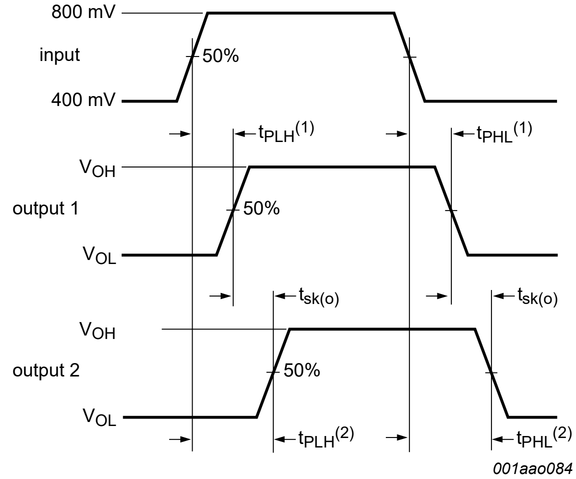
11.1 Waveforms, test circuit and graphs



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

$t_{sk(p)} = |t_{PHL} - t_{PLH}|$.

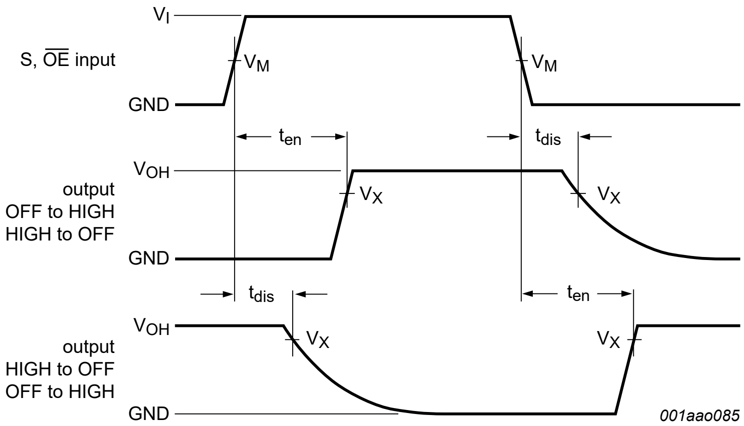
Figure 6. The data input to output propagation delay times and pulse skew time



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

$t_{sk(o)} = |t_{PLH}^{(1)} - t_{PLH}^{(2)}|$ or $|t_{PHL}^{(1)} - t_{PHL}^{(2)}|$.

Figure 7. Output skew time



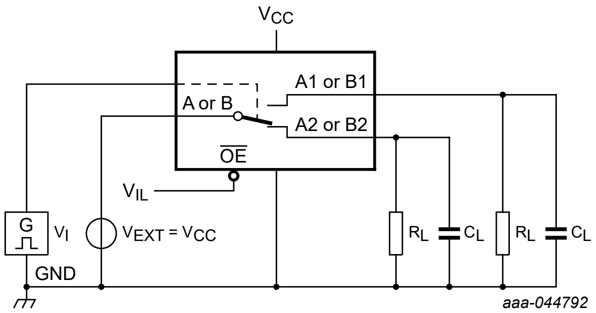
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 8. Enable and disable times

Table 10. Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_X
2.3 V to 3.6 V	$0.5V_I$	1. 8 V	$0.9V_{OH}$



Test data is given in Table 11.
Definitions test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
V_{EXT} = External voltage for measuring switching times.
V_I may be connected to S or $\overline{OE}$.

Figure 9. Test circuit for switching times

Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
2.3 V to 3.6 V	1.8 V	≤ 5 ns	50 pF	500 Ω

12 Power supply recommendations

Power to the device is supplied through the V_{CC} pin and should follow the I^2C and I3C standards.

NXP recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

13 Application information

13.1 Application and implementation: I3C or I^2C-bus

Information in the following application section is not part of the NXP component specification, and NXP does not warrant its accuracy or completeness.

NXP's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

13.1.1 Application information

There are many I3C or I^2C applications where there is the need for a single controller to connect to identical targets to avoid address conflict (Figure 10) or two controllers to connect to a shared target (Figure 11).

The P3S0200 acts like a wire that can be switched between the common input (A/B) to the shared output (A1/B1 or A2/B2) and is able to operate at any bus voltage between GND and 5.5 V (e.g,. I3C or I^2C bus max voltage can be any voltage up to 5.5 V regardless of V_{CC} supply voltage operating between 2.3 V and 3.6 V).

The P3S02000 doesn't provide any voltage level translation between A/B and An/Bn but it will isolate the capacitance for the bus that is not connected to A/B.

13.1.1.1 Typical application (A)

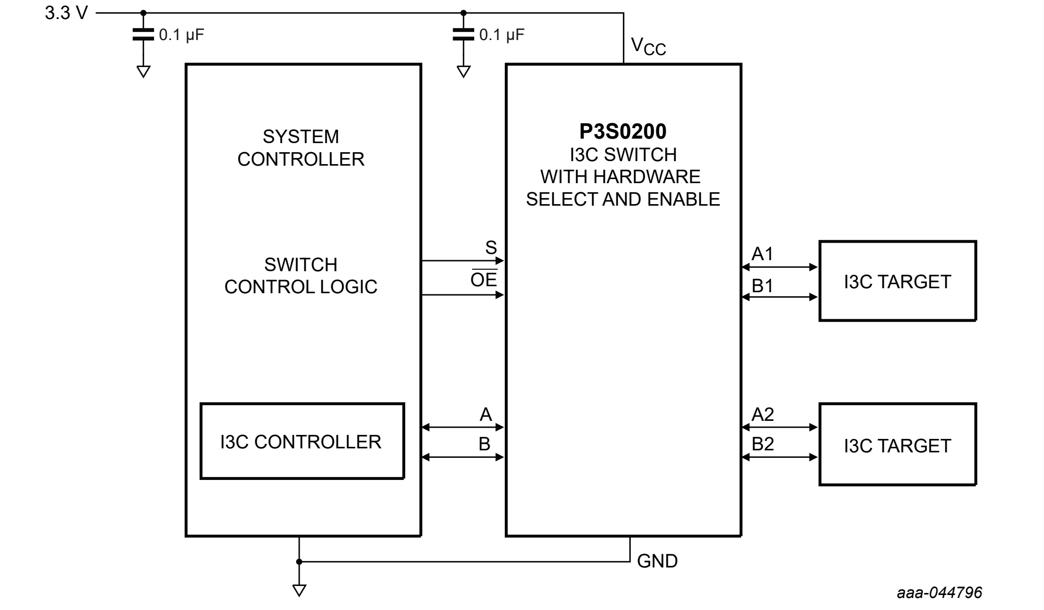


Figure 10. I3C controller to two I3C targets

13.1.1.2 Typical application (B)

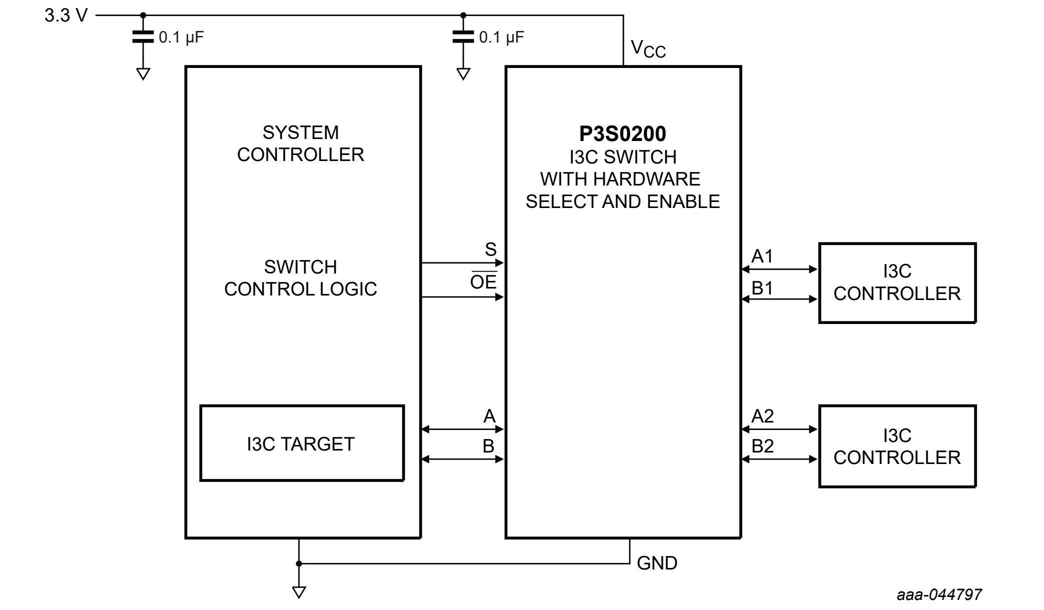


Figure 11. I3C target to two I3C controllers

13.1.2 Design requirements

Design requirements of the I^{2}C and I3C standards should be followed. NXP recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

13.1.3 Detailed design procedure

The P3S0200 can be properly operated without any external components. When used for I3C or I^{2}C there will not be any unused pins but if being used for example as single wire mux and using only one channel then it is recommended that unused pins should be connected to ground through a 50 Ω resistor to prevent signal reflections back into the device.

Design requirements of the I^{2}C and I3C standards should be followed. NXP recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

13.2 Layout

13.2.1 Layout guidelines

The I3C bus would benefit from these guidelines however the slower 12.5 MHz is much more forgiving if these guidelines can't be followed.

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the A/B traces.

Route the high-speed I3C signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities. Do not route I3C traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals. Avoid stubs on the high-speed I3C signals because they cause signal reflections.

Route all high-speed I3C signal traces over continuous planes (V_{CC} or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits. Due to high frequencies associated with the I3C, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 12.

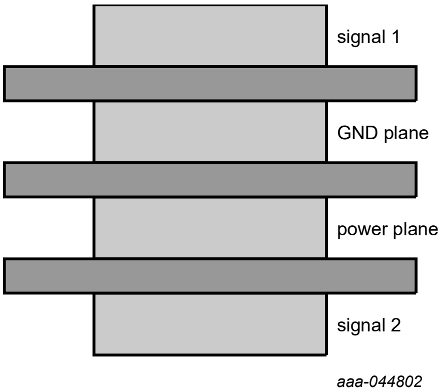


Figure 12. Four-layer board stackup

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

13.2.2 Layout example

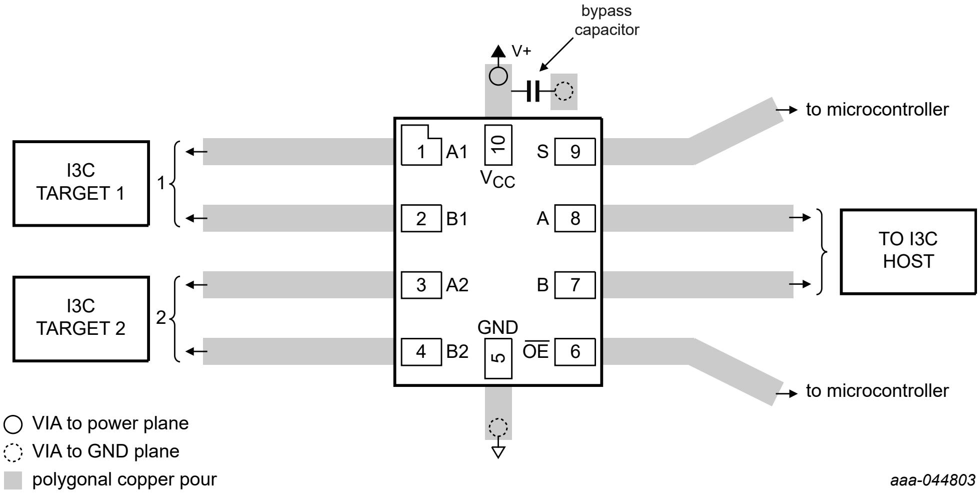
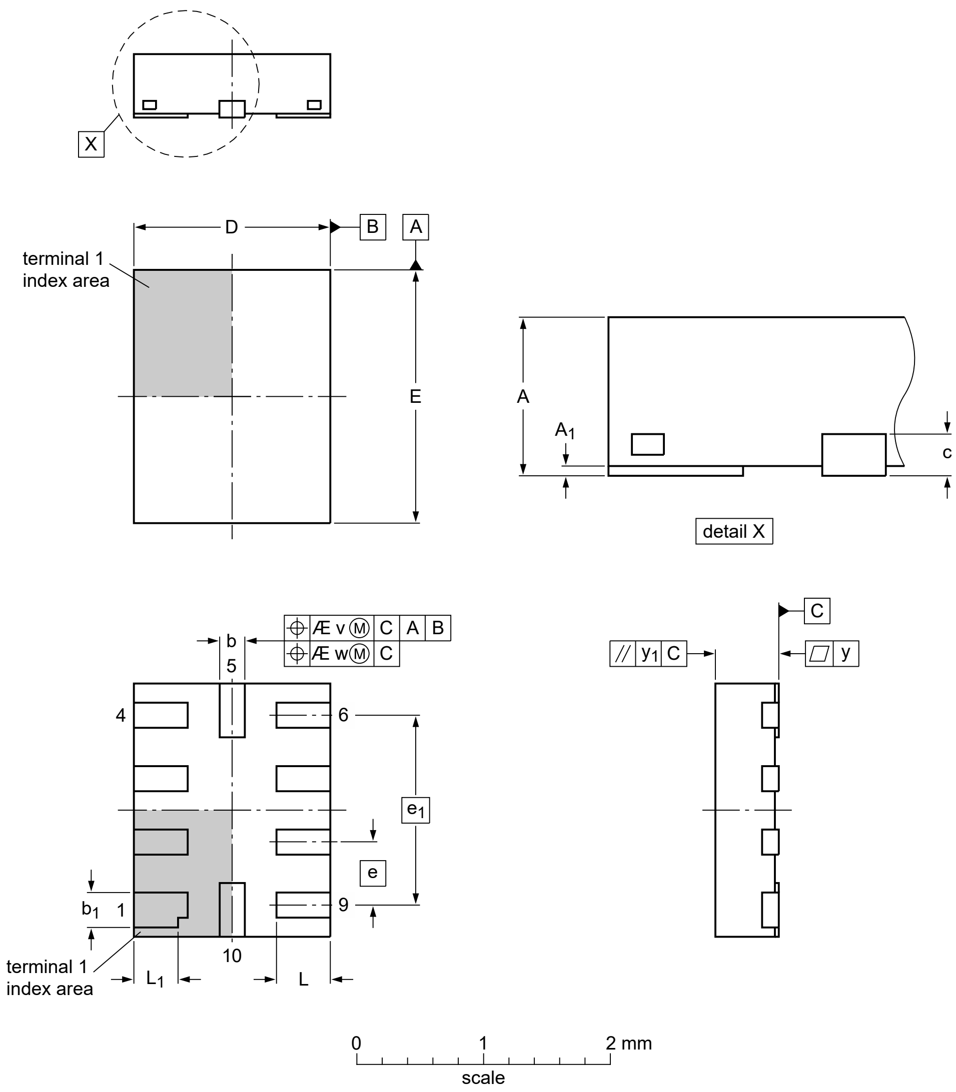


Figure 13. Package layout diagram

14 Package outline

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 x 2.00 x 0.50 mm **SOT1049-3**



Dimensions

Unit(1)		A	A_1	b	b_1	c	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	0.33		1.65	2.1			0.48	0.40				
	nom			0.20	0.28	0.127	1.55	2.0	0.5	1.5	0.43	0.35	0.1	0.05	0.05	0.05
	min		0.00	0.15	0.23		1.45	1.9			0.38	0.30				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1049-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1049-3	- - -	MO255	- - -			~~10-12-06~~ 11-03-30

Figure 14. Package outline SOT1049-3 (XQFN10)

15 Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

16 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P3S0200 v1.0	20220214	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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