PAC5256 Data Sheet

Power Application Controller®

Configurable Analog Front End™

Application Specific Power Drivers™

Arm® Cortex®-M0 Controller Core

TABLE OF CONTENTS

LIST OF TABLES

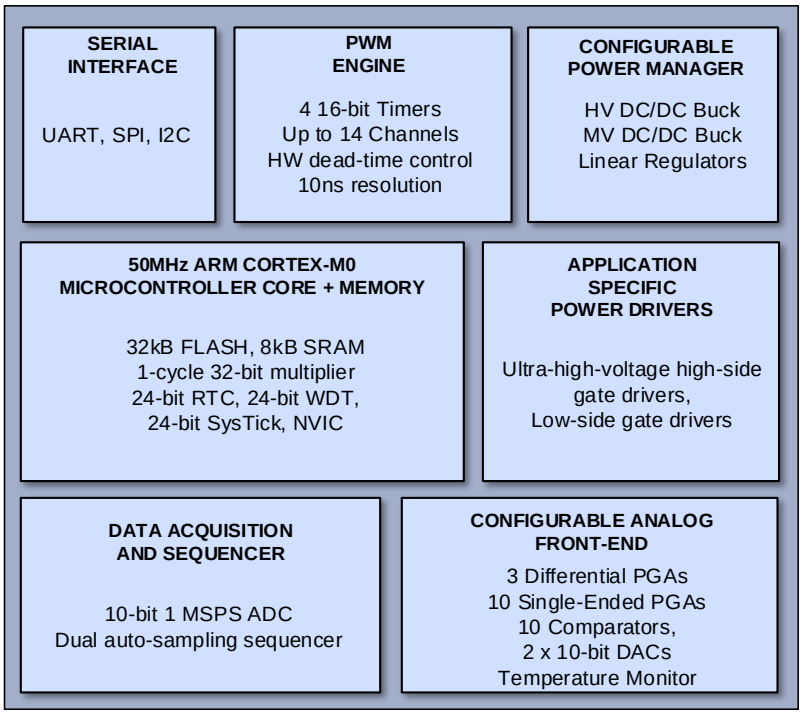
LIST OF FIGURES

1 GENERAL DESCRIPTION

The PAC5256 is a Power Application Controller® (PAC) product that is optimized for high-speed BLDC or PMSM motor control. The PAC5256 integrates a 50MHz Arm® Cortex®-M0 32-bit microcontroller core with a highly-configurable Power Manager, Active-Semi's Configurable Analog Front-End™ and Application Specific Power Drivers™ to form the most compact microcontroller-based power and motor control and drive solution available.

The PAC5256 microcontroller features 32kB of embedded FLASH and 8kB of SRAM memory, a 1MSPS analog-to-digital converter (ADC) with programmable auto-sequencer, 3.3V/5V IO, a flexible clock control system, PWM and general-purpose timers and several serial communications interfaces.

The Configurable Power Manager (CPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable high-voltage buck controller (HV-BUCK), a configurable medium-voltage switching regulator (MV-BUCK), and three linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are 600V power drivers designed for half bridge, H-bridge, 3-phase, and general-purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.



The PAC5256 is available in a 52-pin, 10x10mm QFN package.

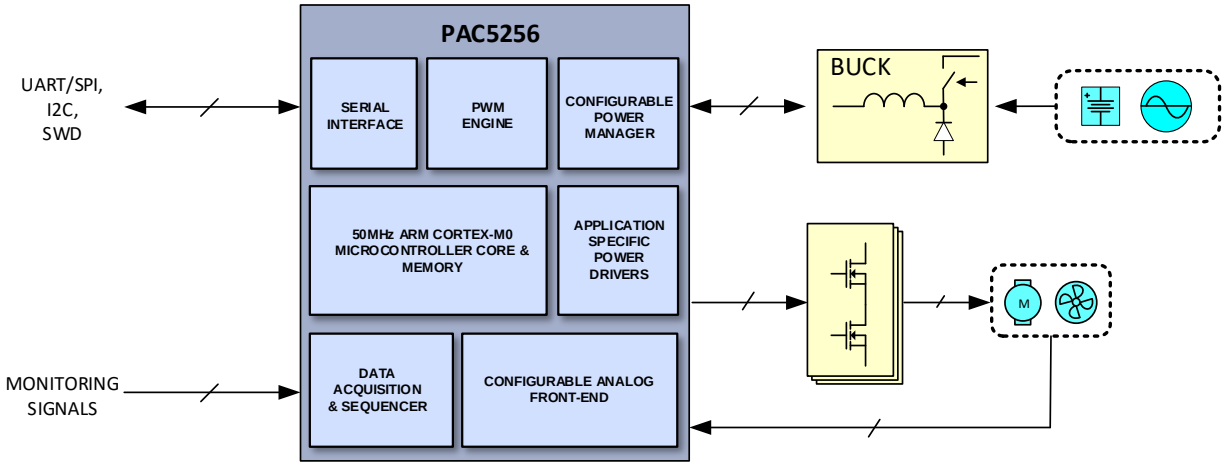
2 PAC FAMILY APPLICATIONS

The PAC5256 is ideal for 120VAC/240VAC or up to 600VDC powered BLDC or PMSM motor applications.

Target applications for this device include:

- AC Fans
- Ceiling Fans
- White Goods
- Compressors
- Water Pumps

Figure 2-1 Simplified Application Diagram



3 PRODUCT SELECTION SUMMARY

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END					APPLICATION SPECIFIC POWER DRIVERS		MICROCONTROLLER						PRIMARY APPLICATION
		INPUT VOLTAGE	CONFIGURABLE POWER MANAGER	DIFF-PGA	PGA	COMPARATOR	DAC	ADC CHANNEL	VBST/VSRC	POWER DRIVER	SPEED (MHz)	FLASH (kB)	SRAM (kB)	GPIO	PWM CHANNEL	COMM	
PAC5256	52-pin 10x10 QFN	Up to 600V	Y	3	10	10	2	12	630V/ 610V	3 LS @ 1A 3 HS @ 0.25A/0.5A	50	32	8	27	4 (3.3V /5V)	UART/SPI I2C SWD	3 half-bridge 3 phase control Sensored BLDC, Sensorless BEMF, Sensorless FOC

Notes: DIFF-PGA = differential programmable gain amplifier; HS = high-side, LS = low-side, PGA = programmable gain amplifier, VSRC = Bootstrap Voltage Source

4 ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
PAC5256QX	-40°C to 105°C	QFN1010-52	52 + Exposed Pad	Tray

5 FEATURES

5.1 Feature Overview

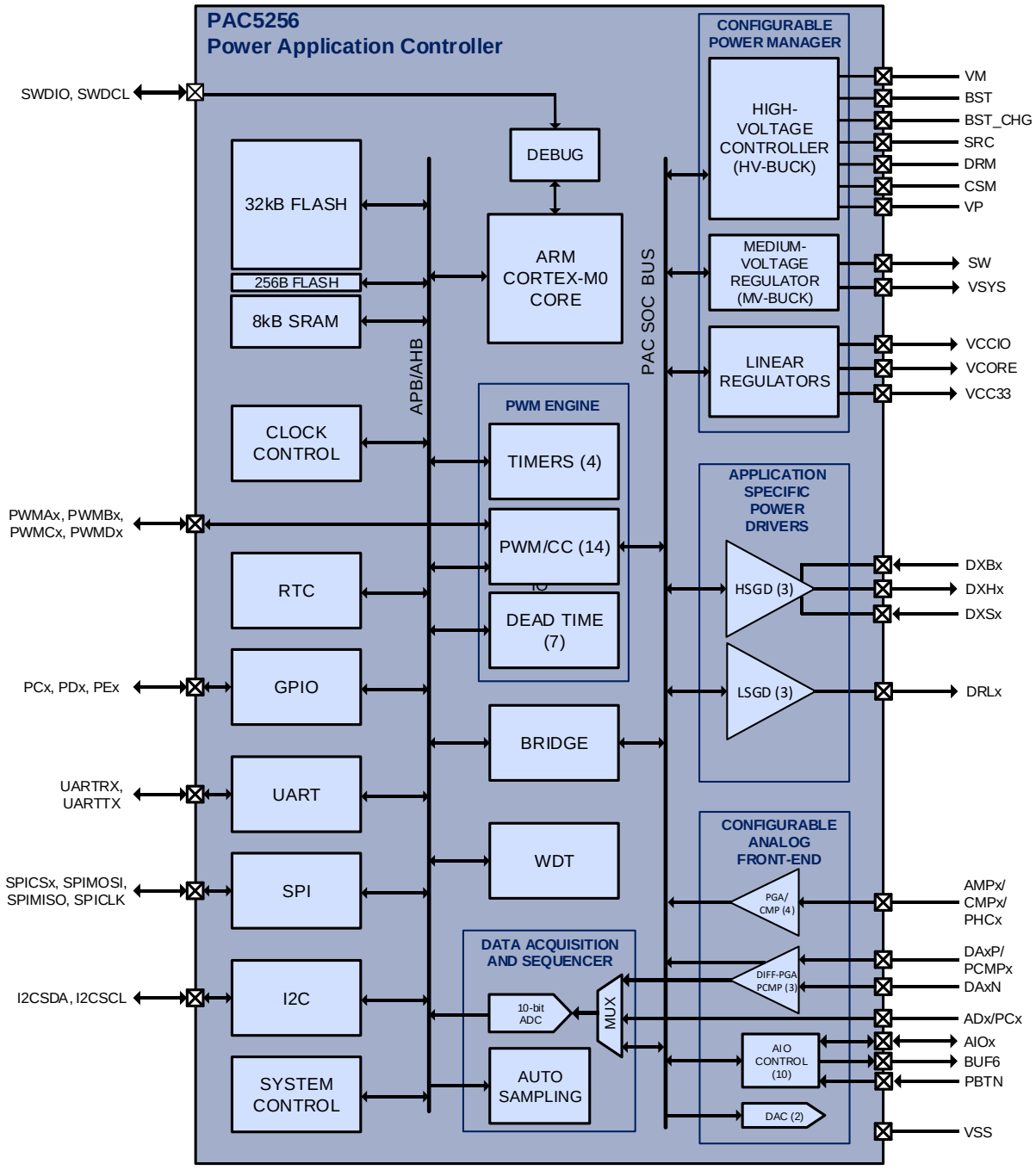
- **Configurable Power Manager**
  - AC line input or DC supply up to 600V
  - 8µA hibernate I_Q
  - 600V DC/DC buck controller (HV-BUCK)
  - 5V DC/DC buck regulator (MV-BUCK)
  - 3 Linear regulators with power and hibernate management
  - Power and temperature monitor, warning, fault detection
- **Proprietary Configurable Analog Front-End**
  - 10 Analog Front-End IO pins
  - 3 Differential Programmable Gain Amplifiers
  - 4 Single-ended Programmable Gain Amplifiers
  - Programmable Over-Current Protection
  - 10 Comparators, 2 DACs (10-bit)
  - Integrated VM ADC Sampling
- **Proprietary Application Specific Power Drivers**
  - 3 600V high-side gate drivers with 0.25A/0.5A gate driving capability
  - 3 low-side gate drivers with 1A/1A gate driving capability
  - Configurable fault protection
  - Cycle by cycle current limit control (CBCCTL)
- **50MHz Arm® Cortex®-M0 32-bit Microcontroller Core**
  - Single-cycle 32-bit hardware multiplier
  - Integrated sleep and deep sleep modes
  - Nested Vectored Interrupt Controller (NVIC) with 20 Interrupts with 3 levels of priority
  - 24-Bit SysTick Timer
  - Wake-up Interrupt Controller (WIC) allowing power-saving sleep modes
  - Clock-gating allowing low-power operation
- **Memory**
  - 32kB FLASH
  - 8kB SRAM
- **Analog to Digital Converter (ADC)**
  - 10-bit resolution, 1MSPS
  - Dual Programmable ADC Auto-Sequencers
- **3.3V I/Os**
  - 5 general-purpose I/Os with tri-state and dedicated analog input to ADC
- **True 5V I/Os**
  - 12 general-purpose I/Os with tri-state, pull-up, pull-down and dedicated I/O supply
  - Configurable as true 5V or 3.3V I/Os
- **Flexible clock and PLL from internal 2% oscillator, ring oscillator, external clock or crystal**

- **9 Timing Generators**
  - Four 16-bit timers with up to 16 PWM/CC blocks and 7 independent dead-time controllers
  - 24-bit watchdog timer, 4s or 8s watchdog timer
  - 24-bit real time clock
  - 24-bit SysTick timer
  - Wake-up timer for sleep modes from 0.125s to 8s
- **UART/SPI, I2C serial communication interfaces**
- **SWD debug interface with interface disable function**

6 ABSOLUTE MAXIMUM RATINGS

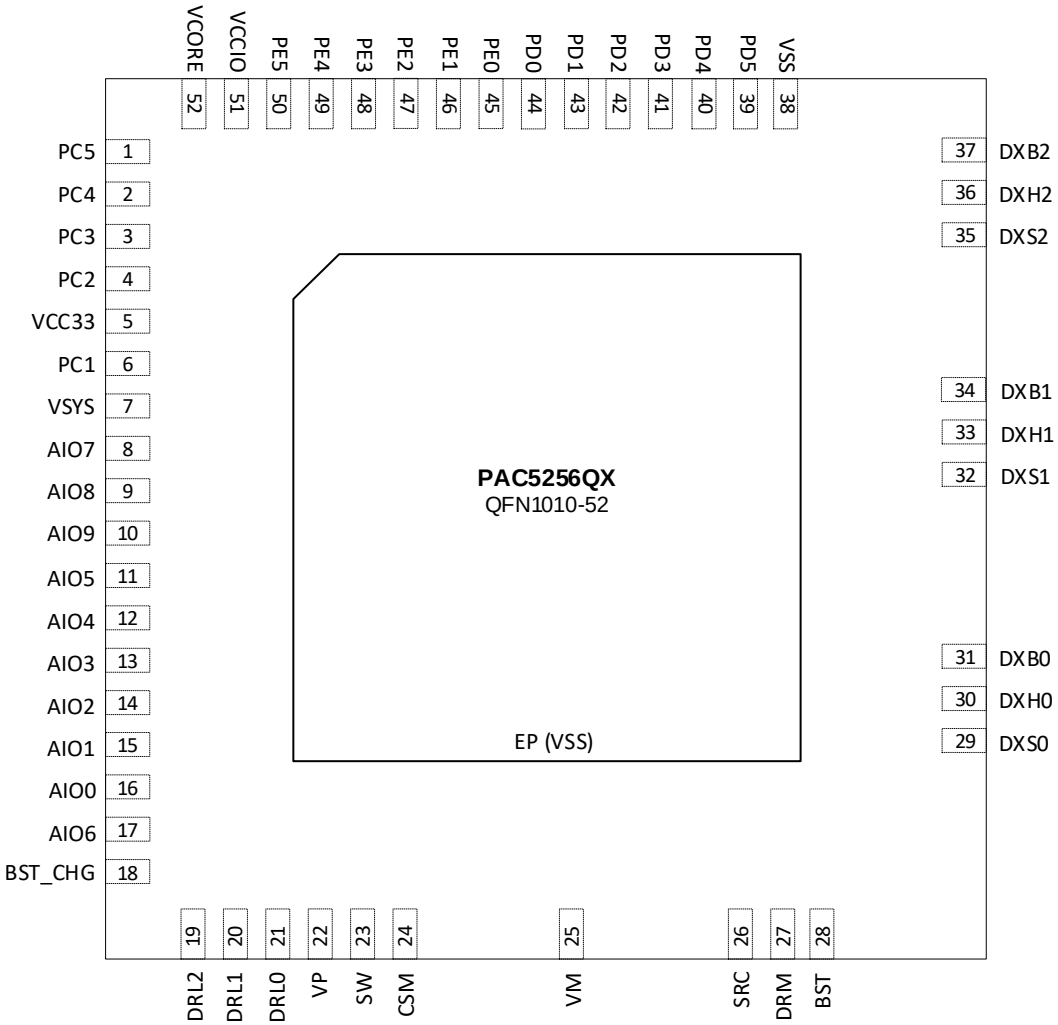
PARAMETER			VALUE	UNIT
VM to VSS			-0.3 to 605	V
BST/DXBx to VSS			-0.3 to 630	V
BST to SRC, DXBx to DXSx			-0.3 to 20	V
SRC/DXSx to VSS			-10 to 610	V
DRM to SRC, DXHx to DXSx			-0.3 to 20	V
DXSx allowable offset slew rate (dV_{DXSx}/dt)			-50 to 50	V/ns
DRLx to VSS			-0.3 to V_P + 0.3	V
VP to VSS			-0.3 to 18	V
SW to VSS			-0.3 to V_P + 0.3	V
CSM to VP			-0.3 to 0.3	V
CSM to VSS			-0.3 to V_P + 1.0	V
BST_CHG to VSS			-0.3 to 42	V
VSYS, VDDIO, AIO6 to VSS			-0.3 to 6	V
AIO<9:7>, AIO<5:0> to VSS			-0.3 to V_{SYS} + 0.3	V
PD<x>, PE<x> to VSS			-0.3 to V_{CCIO} + 0.3	V
PC<x>			-0.3 to V_{CC33} + 0.3	V
PA<x>, PB<x>, PC<x>, PD<x>, PE<x> pin injection current			7.5	mA
PA<x>, PB<x>, PC<x>, PD<x>, PE<x> sum of all pin injection current			25	mA
VCC33 to VSS			-0.3 to 4.1	V
VCORE to VSS			-0.3 to 2.5	V
VSS RMS Current			0.2	A_{RMS}
Operating temperature range			-40 to 105	°C
Electrostatic Discharge (ESD)	Human body model (JEDEC)	All pins (except VM)	2	kV
		VM	1	kV
	Charge device model (JEDEC)		1	kV

7 ARCHITECTURAL BLOCK DIAGRAM



8 PIN CONFIGURATION

8.1 PAC5256QX Pin Configuration (QFN1010-52 10x10mm Package)



9 PIN DESCRIPTION

9.1 Power and Ground Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VCC33	5	Power	Internally generated 3.3V power supply. Connect to a 2.2µF or higher value ceramic capacitor from V_{CC33} to V_{SSA}.
VSYS	7	Power	5V power supply for the medium-voltage buck regulator. Connect to a 22µF/6.3V or higher ceramic capacitor from V_{SYS} to V_{SS}.
BST_CHG	18	Power	Boot-strap capacitor charge pin. Connect to DC/DC boot-strap capacitor. Connect to a 220pF/50V ceramic bypass capacitor from BST_CHG to V_{SS}.
VP	22	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 4.7µF ceramic capacitor in parallel with a 220µF aluminum capacitor from V_P to V_{SS} for voltage loop stabilization. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
SW	23	Power	Switch node for the medium-voltage buck regulator.
CSM	24	Power	High-Voltage Buck Regulator Switching supply current sense input. Connect to the positive side of the current sense resistor.
VM	25	Power	High-Voltage Buck Regulator supply controller input. Connect a 0.1µF higher value ceramic capacitor from VM to VSS. This pin requires good capacitive bypass to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
SRC	26	Power	High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator.
DRM	27	Power	High-Voltage Buck Regulator gate driver. Connect to the gate of the high-side power MOSFET of the high-voltage buck regulator.
BST	28	Power	High-Voltage Buck Regulator bootstrap input. Connect a 2.2µF/25V or higher value ceramic capacitor from BST to SRC. The ceramic capacitor must be connected with a shorter than 10mm trace to the device pin.
VSS	38	Power	Ground.
VCCIO	51	Power	Internally generated digital I/O 3.3V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}.
VCORE	52	Power	Internally generated digital logic 1.9V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.

9.2 Signal Manager Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
AIO7	8	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AIO8	9	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AIO9	10	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.
AIO5	11	AIO5	I/O	Analog front end I/O 5.
		DA54P	Analog	Differential PGA 54 positive input.
		AMP5	Analog	PGA input 5.
AIO4	12	AIO4	I/O	Analog front end I/O 4.
		DA54N	Analog	Differential PGA 54 negative input.
		AMP4	Analog	PGA input 4.
AIO3	13	AIO3	I/O	Analog front end I/O 3.
		DA32P	Analog	Differential PGA 32 positive input.
		AMP3	Analog	PGA input 3.
AIO2	14	AIO2	I/O	Analog front end I/O 2.
		DA32N	Analog	Differential PGA 32 negative input.
		AMP2	Analog	PGA input 2.
AIO1	15	AIO1	I/O	Analog front end I/O 1.
		DA10P	Analog	Differential PGA 10 positive input.
		AMP1	Analog	PGA input 1.
AIO0	16	AIO0	I/O	Analog front end I/O 0.
		DA10N	Analog	Differential PGA 10 negative input.
		AMP0	Analog	PGA input 0.
AIO6	17	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.

9.3 Driver Manager Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DRL2	19	Analog	Low-side gate driver 2.
DRL1	20	Analog	Low-side gate driver 1.
DRL0	21	Analog	Low-side gate driver 0.
DXS0	29	Analog	Ultra-high-voltage high-side gate driver source 0.
DXH0	30	Analog	Ultra-high-voltage high-side gate driver 0.
DXB0	31	Analog	Ultra-high-voltage high-side gate driver bootstrap 0. Connect a 1µF or higher value ceramic capacitor from DXB0 to DXS0. This pin requires good capacitive bypass so it must be connected with a 10mm or shorter trace.
DXS1	32	Analog	Ultra-high-voltage high-side gate driver source 1.
DXH1	33	Analog	Ultra-high-voltage high-side gate driver 1.
DXB1	34	Analog	Ultra-high-voltage high-side gate driver bootstrap 1. Connect a 1µF or higher value ceramic capacitor from DXB1 to DXS1. This pin requires good capacitive bypass so it must be connected with a 10mm or shorter trace.
DXS2	35	Analog	Ultra-high-voltage high-side gate driver source 2.
DXH2	36	Analog	Ultra-high-voltage high-side gate driver 2.
DXB2	37	Analog	Ultra-high-voltage high-side gate driver bootstrap 2. Connect a 1µF or higher value ceramic capacitor from DXB2 to DXS2. This pin requires good capacitive bypass so it must be connected with a 10mm or shorter trace.

9.4 I/O Ports Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PC5	1	PC5	I/O	I/O port PC5.
		AD5	Analog	ADC input 5.
PC4	2	PC4	I/O	I/O port PC4.
		AD4	Analog	ADC input 4.
PC3	3	PC3	I/O	I/O port PC3.
		AD3	Analog	ADC input 3.
PC2	4	PC2	I/O	I/O port PC2.
		AD2	Analog	ADC input 2.
PC1	6	PC1	I/O	I/O port PC1.
		AD1	Analog	ADC input 1.
PD5	39	PD5	I/O	I/O port PD5.
		PWMA5	I/O	Timer A, PWM/Capture Unit 5.
		PWMC1	I/O	Timer C, PWM/Capture Unit 1.
PD4	40	PD4	I/O	I/O port PD4.
		PWMD1	I/O	Timer D, PWM/Capture Unit 1
PD3	41	PD3	I/O	I/O port PD3.
		PWMA5	I/O	Timer A, PWM/Capture Unit 5.
		PWMC1	I/O	Timer C, PWM/Capture Unit 1.
PD2	42	PD2	I/O	I/O port PD2.
		PWMA3	I/O	Timer A, PWM/Capture Unit 3.
		PWMA4	I/O	Timer A, PWM/Capture Unit 4.
		PWMB0	I/O	Timer B, PWM/Capture Unit 0.
PD1	43	PD1	I/O	I/O port PD1.
		SWDCL	I	SWD Serial Clock.
		EXTCLK	I	External Clock Input.
PD0	44	PD0	I/O	I/O port PD0.
		SWDIO	I/O	SWD Serial Data.
PE0	45	PE0	I/O	I/O port PE0.
		SPICLK	I/O	SPI Clock.
PE1	46	PE1	I/O	I/O port PE1.
		SPIMOSI	I/O	SPI Master-out, slave-in (MOSI)
		UARTTX	O	UART Transmit Output.
PE2	47	PE2	I/O	I/O port PE2.
		SPIMISO	I/O	SPI Master-in, slave-out (MISO)
		UARTRX	I	UART Receive Input.
PE3	48	PE3	I/O	I/O port PE3.
		SPICS0	O	SPI chip-select 0.
		nRESET1	I	Reset input 1 (active-low).

PE4	49	PE4	I/O	I/O port PE4.
		SPICS1	O	SPI chip-select 1.
		I2CSCL	I/O	I2C Serial Clock.
PE5	50	PE5	I/O	I/O port PE5.
		SPICS2	O	SPI chip-select 2.
		I2CSDA	I/O	I2C Serial Data.

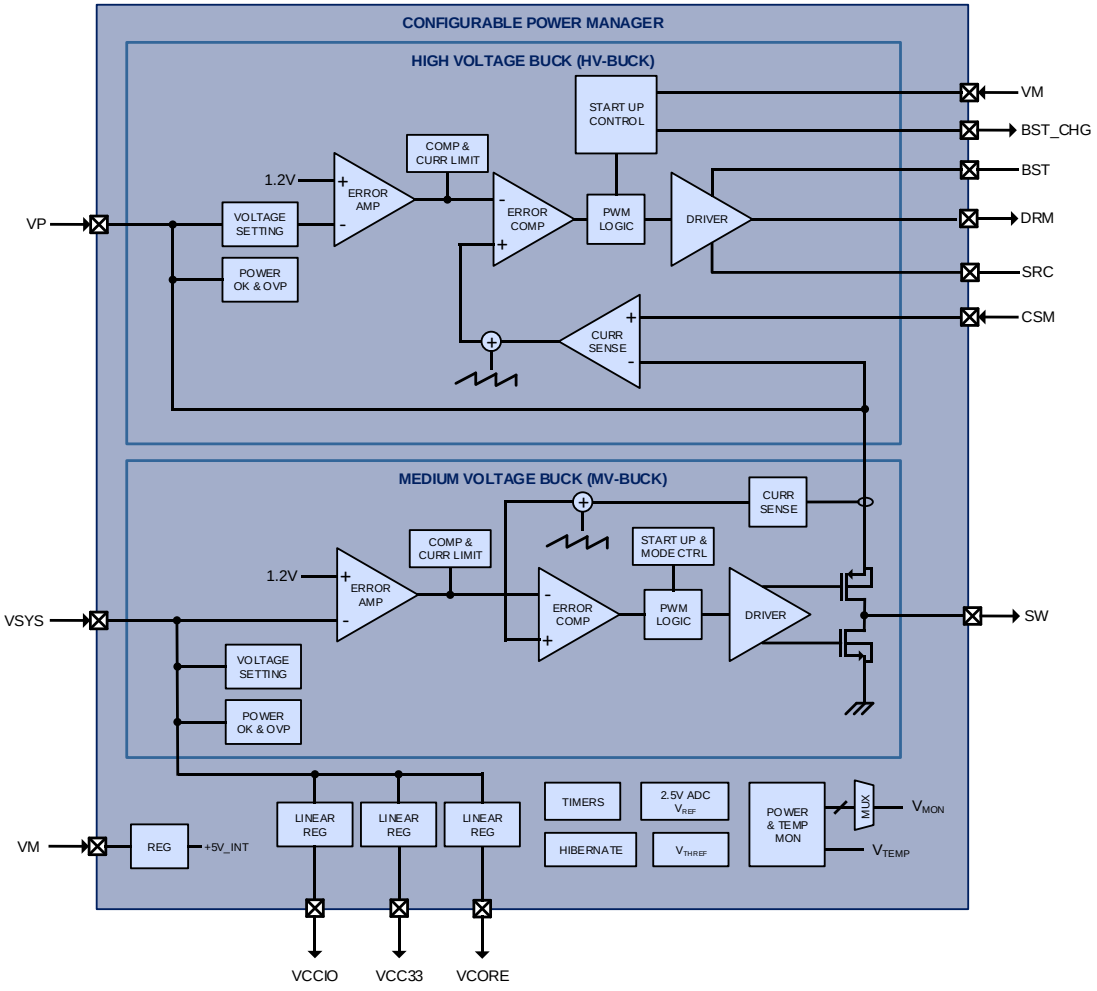
10 CONFIGURABLE POWER MANAGER (CPM)

10.1 Features

- 600V Switching Controller (HV-BUCK)
- 5V Switching Regulator (MV-BUCK) with integrated FET
- 3 linear regulators with power and hibernate management
- V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

10.2 Block Diagram

Figure 10-1 CPM Block Diagram



10.3 Functional Description

The Configurable Power Manager (Figure 10-1) is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a high-voltage DC/DC controller that is used to convert power from a DC input source to generate a main supply output V_P. There is also an integrated medium-voltage buck DC/DC regulator to generate V_{SYS}.

Three other linear regulators provide V_{CCIO}, V_{CC33}, and V_{CORE} supplies for 3.3V I/O, 3.3V mixed signal, and 1.9V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

10.4 High-Voltage Supply Controller (HV-BUCK)

The PAC5256 contains a 600V High-Voltage Supply Controller (Buck DC/DC). This power supply is used to supply the various regulators in the PAC5256, as well as generating the V_P gate drive voltage for the Application Specific Driver Manager (ASPD).

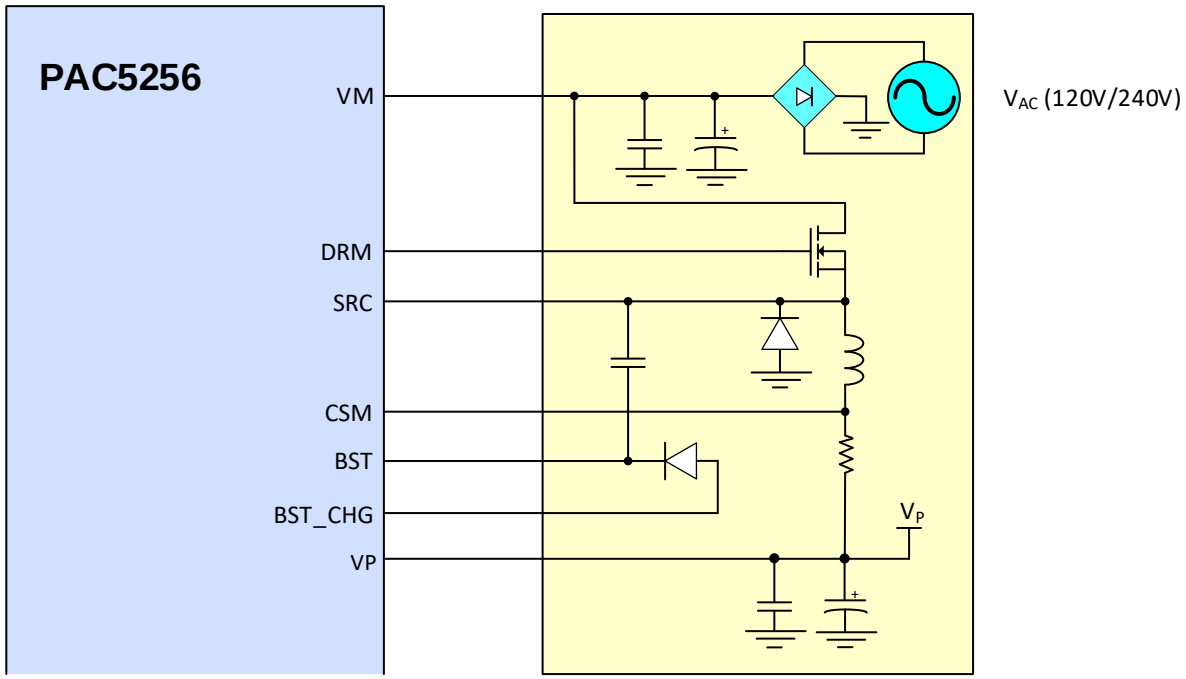
The HV-BUCK controller converts the motor voltage (V_M) to the gate driver and IC system supply (V_P). The VM input is the HV-BUCK supply regulator input and is connected to the rectified DC motor voltage source. The BST and SRC pins are connected to the boot-strap and source nodes of the power supply, respectively. The BST_CHG pin is used to initially charge the boot-strap capacitor in the HV-BUCK.

The V_P regulation voltage is initially set to 15V during start up, and may be reconfigured to be 12V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. The inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.2V.

The CPM may be used to supply both AC offline or DC supplied applications of up to 600VDC.

The diagram below shows an example of the PAC5256 with a 120Hz/240Hz AC application.

Figure 10-2 HV-BUCK with AC Supply



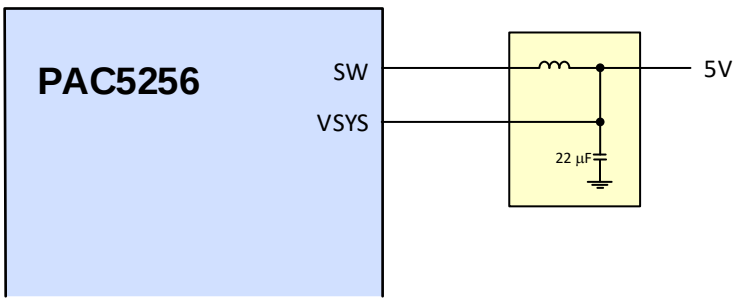
The switching frequency and output voltage of the HV-BUCK can be reconfigured by the MCU. The switching frequency can be configured to be between 25kHz and 125kHz and the gate drive output voltage can be configured to 12V or 15V.

10.5 Medium-Voltage Buck Regulator (MV-BUCK)

The PAC5256 contains a Medium-Voltage Buck Switching Regulator that generates a 5V/200mA supply for the device, as well as PCB functions.

The SW pin is the switch node of the Buck regulator. The Power MOSFET is integrated, so connect this pin to VSYS through an external inductor. The VSYS pin is the 5V regulator output, which should be bypassed to ground with a 22µF ceramic capacitor.

Figure 10-3 MV-BUCK Switching Regulator Example

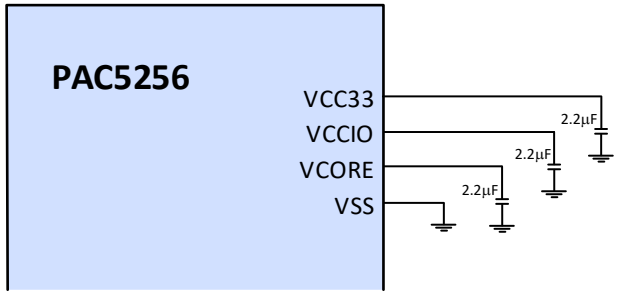


The output of the MV-BUCK is fixed at 5V and the switching frequency is 1.33MHz. This regulator supplies an external load on the PCB of at least 200mA - $I_{OP;VSYS}$ (The PAC operating V_{SYS} current).

10.6 Linear Regulators

The CPM includes three additional linear regulators. VSYS supplies these three regulators. Once VSYS is above 4V, these three additional 40mA linear regulators for VCCIO, VCC33, and VCORE supplies sequentially power up.

Figure 10-4 Linear Regulators Example



The figure above shows typical circuit connections for the linear regulators. The VCCIO regulator generates a dedicated 3.3V supply for IO. The VCC33 regulator generates a 3.3V supply for the analog peripherals in the MCU. The VCORE regulator generates a 1.9V supply for the MCU digital logic.

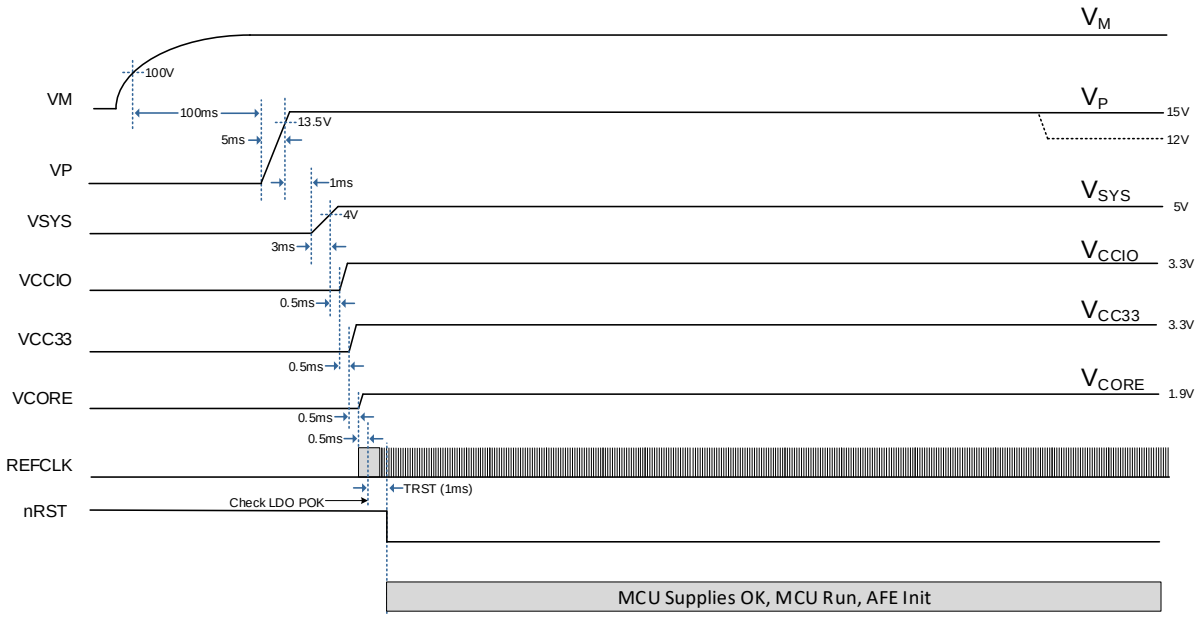
When VSYS, VCCIO, VCC33, and VCORE are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.

To enable true 5V IO in the PAC5256, the VCCIO and VSYS pins may be shorted together which will allow 5V drive output in all PAC5256 GPIO on the PD<x> and PE<x> pins.

10.7 Power-up Sequence

The CPM follows a typical power up sequence as in the Figure 10-5 below.

Figure 10-5 Power-Up Sequence



A typical sequence begins with power being applied to VM. When VM reaches 100V, the HV-BUCK controller is started. After the boot-strap capacitor is charged VP starts to rise. VP rises to 90% of the target setting of 15V (13.5V) within 5ms, then there is a 1ms delay and then the MV-BUCK is started. When the VSYS output of the MVBK rises to 4V, then there is a 0.5ms delay and the VCCIO LDO is enabled. Then there is a 0.5ms delay and the VCC33 LDO is enabled. Then there is a 0.5ms delay and the VCORE LDO is enabled.

There is then a 0.5ms delay and the power good threshold of all LDOs is checked. If all are OK, then there is an additional 1ms delay (TRST), then the POR signal is asserted to the MCU and it begins executing firmware.

During the firmware initialization process, the MCU may change the VP output voltage setting from the 15V default to 12V.

10.8 Hibernate Mode

The PAC5256 can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN, see *Push Button* description in *Configurable Analog Front End*). In hibernate mode, only a minimal amount of current is used by V_M (typically 8µA at 170VDC), and the CPM controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

10.9 Power Monitor

Whenever any of the V_{SYS}, V_{CCIO}, V_{CC33}, or V_{CORE} power supplies fall below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CORE} supplies are all good again and the reset time has expired.

These power supplies may also be monitored by the ADC. The PWRMON MUX allows the user to select which channels may be monitored by the ADC. The channels that may be monitored are shown below:

- V_{CORE}
- V_{CORE} * 4/10
- V_{CC33} * 4/10
- V_{CCIO} * 4/10
- V_{SYS} * 4/10
- VMS[1]
- VPTAT[2]
- VMS (buffered)

For details on how to select the power monitor channels using the ADC, see the section below on ADC Analog Input.

[1] VMS is the scaled value of the VM power supply input. For more information on how to convert this value to volts, see the PAC5256 User Guide.
[2] VPTAT is the internal temperature sensor value. For more information on how to convert this value to degrees C, see the PAC5256 User Guide.

10.10 Electrical Characteristics

Table 10-1 High-Voltage Buck Controller Electrical Characteristics

(V_M = 330V, V_P = 15V and T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_M	Motor voltage range			0		600	V
$I_{HIB;VM}$	V_M hibernate mode supply current	HIB = 1	VM = 170V		8	16	µA
			VM = 330V		18		µA
$V_{UVLOR;VM}$	V_M UVLO rising threshold				82		V
$V_{UVLOF;VM}$	V_M UVLO falling threshold				62		V
V_{SRC}	Level-shifted driver source voltage range	Repetitive, 10µs pulse		-10		605	V
		Steady state		0		600	V
V_{BST}	BST pin voltage range	Repetitive, 10µs pulse		1		625	V
$V_{BS;BST}$	Boot-strap supply voltage range	Steady state		9		620	V
		V_{BST}, relative to V_{SRC}		9		20	V
$V_{UVLOR;BST}$	Boot-strap UVLO rising threshold				7		V
$V_{UVLOF;BST}$	Boot-strap UVLO falling threshold				6.2		V
V_{DRM_MINON}	DRM minimum on time				200		ns
V_{DRM_MINOFF}	DRM minimum off time				1200		ns
$V_{REG;VP}$	V_P output regulation voltage	V_P = 15V		-5%	15	5%	V
$V_{POKR;VP}$	V_P power OK threshold	V_P rising			91		%
		V_P falling			87		%
$V_{OVPR;VP}$	V_P OV protection threshold	V_P rising			130		%
$f_{SWM;DRM}$	Switching frequency programmable range			25		125	kHz
I_{SRC}	Source node current output				100		mA
I_{SNK}	Sink node current output				200		mA
$V_{UVLOR;VP}$	V_P UVLO rising threshold				10		V
$V_{UVLOF;VP}$	V_P UVLO falling threshold				8		V
$V_{CSM;ILIM}$	CSM current limit threshold			-10%	0.2	10%	V
	HV-BUCK inductor value				680		µH
R_{DSG}	Discharge resistance				1		kΩ

Table 10-2 Medium-Voltage Buck Controller Electrical Characteristics

(V_M = 330V, V_P = 15V and T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VSYS}	V_{SYS} output voltage accuracy		-3%	5	3%	V
F_{SW}	Switching frequency		-5%	1.33	5%	MHz
$I_{VSYS;LIM}$	V_{SYS} peak current limit		320		450	mA
$V_{POK;VSYS}$	V_{SYS} power OK threshold	Rising	4.25	4.5	4.75	V
		Falling		4.2		V
	V_{SYS} power OK blanking delay			10		µs
	MV-BUCK inductor value	Current rating of at least 500mA	6.8 – 20%		10 + 20%	µH
$V_{UVLO;VSYS}$	V_{SYS} UVLO	Rising		4.5		V
		Falling		4.2		V
$V_{OVP;VSYS}$	V_{SYS} OVP	Rising		5.5		V
		Falling		5.2		V
$R_{DSCH;VSYS}$	V_{SYS} discharge resistance			2.5		kΩ

Table 10-3 Linear Regulators Electrical Characteristics

(V_P = 12V and T_A = -40°C to 105°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CCIO}	V_{CCIO} output voltage	Load = 1mA	-3%	3.3	3%	V
V_{CCIO}	V_{CCIO} output voltage	Load = 1mA	-3%	3.3	3%	V
V_{CORE}[3]	V_{CORE} output voltage	Load = 1mA	-3%	1.9	3%	V
$I_{LIM;VCCIO}$	V_{CCIO} current limit		40	65		mA
$I_{LIM;VCC33}$	V_{CC33} current limit		40	65		mA
$I_{LIM;VCORE}$	V_{CORE} current limit		40	65		mA
	LDO current fold back			50		%
$t_{POK;BLANK}$	Power OK blanking delay	V_{CCIO}, V_{CC33}, V_{CORE}		10		µs
R_{DISCH}	Output discharge resistance	LDO off		300		Ohm
C_{VCCIO}	VCCIO stable output capacitance		1		10	µF
C_{VCC33}	VCC33 stable output capacitance		1		10	µF
C_{VCORE}	VCORE stable output capacitance		1		10	µF
$V_{LDO;POK}$	LDO power OK rising threshold	Hysteresis = 10%	85	90	95	%

Table 10-4 Power Monitor Electrical Characteristics

(T_A = -40°C to 105°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
k_{MON}	Power monitoring voltage	V_{CORE}		1		V/V
		V_{SYS}, V_{CCIO}, V_{CC33}		0.4		

[3] Note that the VCORE LDO may not have any other loads. The only connection to the VCORE pin should be a bypass capacitor to ground.

10.11 Typical Performance Characteristics

(T_A = 25ºC unless otherwise specified)

Figure 10-6 VDDIO LDO Voltage vs. Current

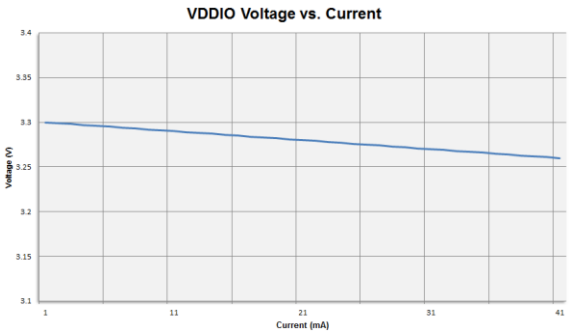


Figure 10-7 VCC33 LDO Voltage vs. Current

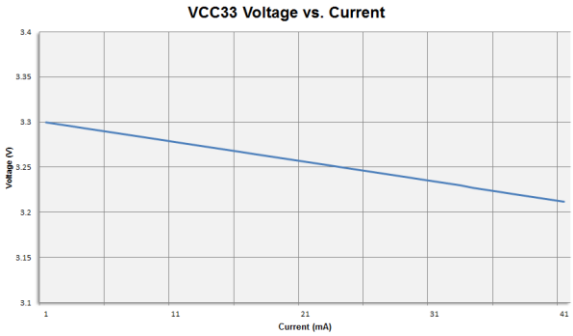
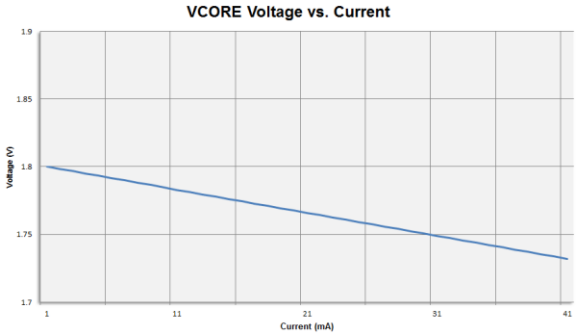


Figure 10-8 VCORE LDO Voltage vs. Current



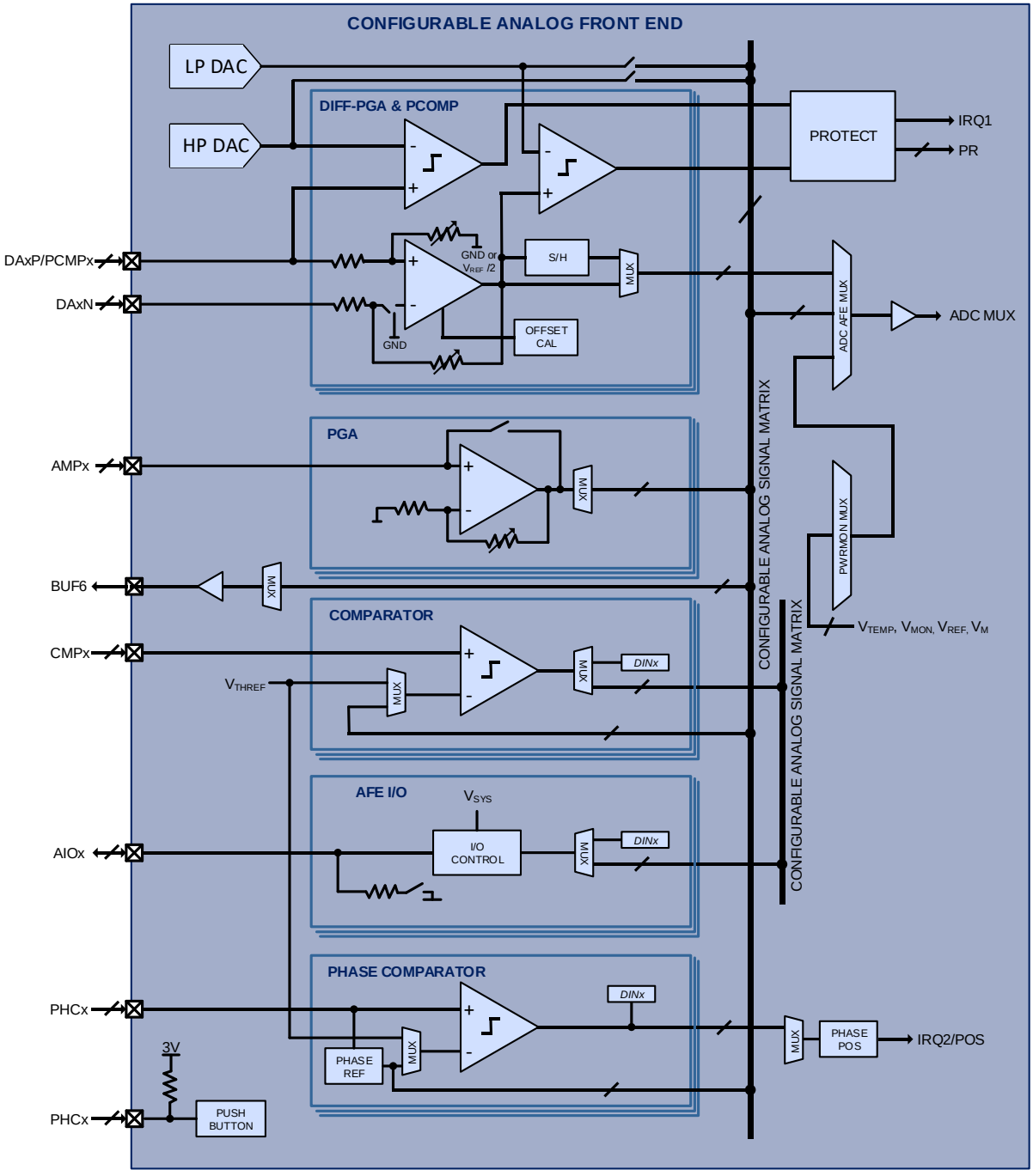
11 CONFIGURABLE ANALOG FRONT END (CAFE)

11.1 Features

- 10 Configurable Analog I/O signals
  - Gain mode, comparator mode, I/O mode, special mode
- 3 High-Performance, Configurable Differential Amplifiers
- 4 High-Performance, Configurable Single-Ended Amplifiers
- Two high-speed comparators with protection functions
- Phase to phase, phase to center-tap modes
- Bi-directional, asymmetric configurable comparator hysteresis
- Push-button input for entering/exiting hibernate mode
- Low-frequency Clock Output for safety applications
- Integrated VM sampling using ADC

11.2 Block Diagram

Figure 11-1 Configurable Analog Front End



11.3 Functional Description

The device includes a Configurable Analog Front End™ (CAFE, Figure 11-1) accessible through 10 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 10 protection comparators, and one buffer output.

Each of these pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

11.4 Differential Programmable Gain Amplifier (DA)

The DAxP and DAxN pin pair are positive and negative inputs, respectively, to a differential programmable gain amplifier. The differential gain can be programmable to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x for zero-ohm signal source impedance. The differential programmable gain amplifier has -0.3V to 2.5V input common mode range, and its output can be configured for routing directly to the ADC pre-multiplexer, or through a sample-and-hold circuit synchronized with the ADC auto-sampling mechanism. Each differential amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring. The programmable gain differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by 13.5k / (13.5k + R_{SOURCE}), where R_{SOURCE} is the matched source impedance of each input.

Each differential amplifier is connected to a pair of AIO pins on the PAC5256. AIO<1:0> are connected to one differential amplifier; AIO<3:2> are connected to one differential amplifier and AIO<5:4> are connected to one differential amplifier.

11.5 Single-Ended Programmable Gain Amplifier (AMP)

Each AMPx input goes to a single-ended programmable gain amplifier with signal relative to V_{SS}. The amplifier gain can be programmed to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x, or as analog feed-through. The programmable gain amplifier output is routed via a multiplexer to the configurable analog signal matrix CASM.

11.6 General Purpose Comparator (CMP)

The general-purpose comparator takes the CMPx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed via a multiplexer to either a data input bit or the configurable digital signal matrix CDSM.

11.7 Phase Comparator (PHC)

The phase comparator takes the PHCx input and compares it to either the programmable threshold voltage (VTHREF) or a signal from the configurable analog signal matrix CASM. The comparison signal can be set to a phase reference signal generated by averaging the PHCx input voltages. In a three-phase motor control application, the phase reference signal acts as a virtual center tap for BEMF detection. The PHCx inputs are optionally fed through to the CASM. The PHC inputs can be compared to the virtual center-tap, or phase to phase for the most efficient BEMF zero-cross detection. The phase comparators have configurable asymmetric hysteresis.

The phase comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed to a data input bit and to the phase/position multiplexer synchronized with the auto-sampling sequencers.

11.8 Protection Comparator (PCMP)

Two protection comparators are provided in association with each differential programmable gain amplifier, with outputs available to trigger protection events and accessible as read-back output bits. The high-speed protection (HP) comparator compares the AIO<n+1> pin to the 10-bit HP DAC output voltage, with full scale voltage of 2.5V. The limit protection (LP) comparator compares the differential programmable gain amplifier output to the 10-bit LP DAC output voltage, with full scale voltage of 2.5V.

Each protection comparator has a mask bit to prevent or allow it to trigger the main microcontroller interrupt IRQ1. Each protection comparator also has one mask bit to prevent or allow it to activate protection event PR. This protection event can be used directly by protection circuitry in the Application Specific Power Drivers (ASPD) to protect devices being driven.

11.9 Analog Output Buffer (BUF)

A subset of the signals from the configurable analog signal matrix CASM can be multiplexed to the AIO6 pin for external use. The buffer offset voltage can be minimized with the built-in swap function.

11.10 Analog Front End I/O (AIO)

The PAC5256 has 10 AIOx pins that are available. When in digital IO mode, each of these pins can be configured to be a digital input or digital open-drain output. The AIOx input or output signal can be set to a data input or output register bit, or multiplexed to one of the signals in the configurable digital signal matrix CDSM.

The signal can be set to active high (default) or active low, with V_{SYS} supply rail. Where $AIO_{6,7,8,9}$ supports microcontroller interrupt for external signals. Each has two mask bits to prevent or allow rising or falling edge of its corresponding digital input to trigger second microcontroller interrupt IRQ2.

11.11 Push Button (PBTN)

When the user commands the PAC5256 into hibernate mode, the device is put into a very low-power state and the MCU is not powered. To exit from hibernate mode, the user may use the push-button (PBTN) to wake the system up.

When enabled, the PBTN can be used to detect a user active-low push button event and will wake-up the system from hibernate mode.

In addition, PBTN can also be used as a hardware reset for the microcontroller when it is held low for longer than 8s during normal operation. The PBTN input is active low and has a 55kΩ pull-up resistor to 3V.

11.12 HP DAC and LP DAC

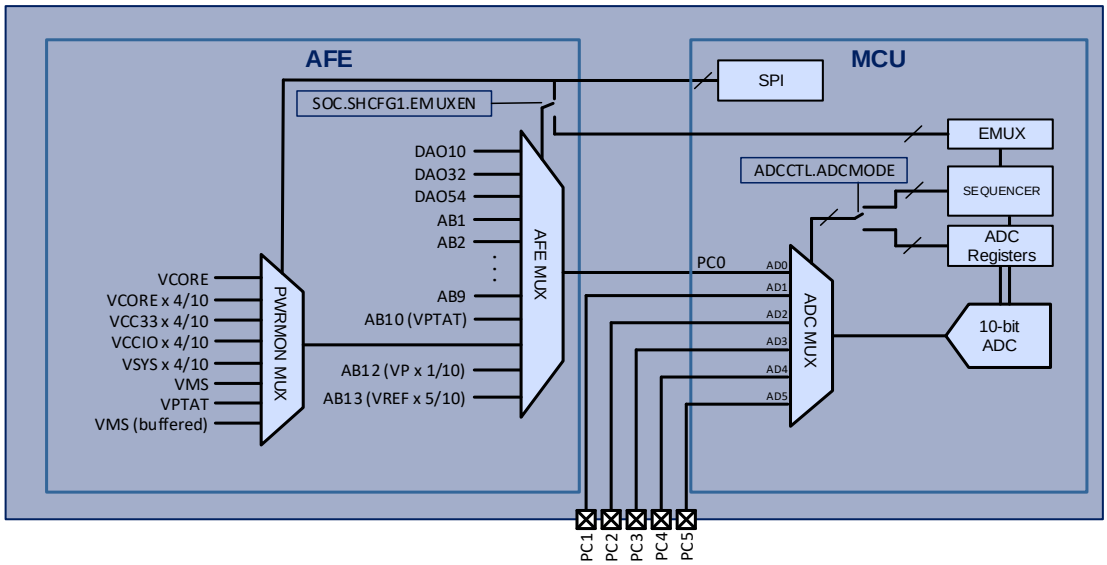
The 10-bit HP DAC can be used as the comparison voltage for the high-speed protection (HP) comparators, or routed for general purpose use via the AB2 signal in the CASM. The HP DAC output full scale voltage is 2.5V.

The 10-bit LP DAC can be used as the comparison voltage for the limit protection (LP) comparators, or routed for general purpose use via the AB3 signal in the CASM. The LP DAC output full scale voltage is 2.5V.

11.13 ADC Analog Input

The PAC5256 has a number of different Analog Input channels that may be used for analog-to-digital conversion. The diagram below shows the hierarchy of muxes that are available for analog signal sampling.

Figure 11-2 ADC Analog Input Muxes



The PAC5256 contains three hierarchical muxes:

- ADC MUX
- AFE MUX
- PWRMON MUX

The ADC MUX is an 8-channel MUX local to the ADC on MCU that is directly controlled by either by registers in the MCU, or automatically by the ADC sequencer. The output of the ADC MUX is sampled by the ADC. The AD0 input to the ADC MUX is connected to the AFE MUX. ADC MUX input channels AD1-AD5 are directly connected to package pins on the PAC5256.

The AFE MUX is a 16-to-1 multiplexer that selects between the 3 differential programmable gain amplifier outputs, AB1 through AB9, temperature monitor signal (VPTAT), power monitor signal (from the PWRMON MUX), attenuated VP voltage and VREF. The output of the AFE MUX is connected to channel AD0 on the ADC MUX on the MCU. The ADC AFE MUX can be directly controlled or automatically scanned by the ADC sequencer through the high-speed EMUX channel select.

The PWRMON MUX is an 8-channel MUX that selects between the internal regulators on the PAC5256 for diagnostic purposes. The output of the PWRMON MUX is connected to channel AB11 on the AFE MUX. The MUX channel select is available through the SPI SOC bus between the MCU and AFE.

For more information on controlling the various MUXes for ADC and ADC sequencer sampling, see the PAC5256 User Guide.

11.14 Configurable Analog Signal Matrix (CASM)

The CASM has 9 general purpose analog signals labeled AB1 through AB9 that can be used for:

- Routing the single-ended programmable gain amplifier or analog feed-through output to AB1 through AB9
- Routing an analog signal via AB1, AB2, or AB3 to the negative input of a general-purpose comparator or phase comparator
- Routing the 10-bit HP DAC output to AB2
- Routing the 10-bit LP DAC output to AB3
- Routing analog signals via AB1 through AB12 to the ADC pre-multiplexer
- Routing phase comparator feed-through signals to AB7, AB8, and AB9, and averaged voltage to AB1

11.15 Configurable Digital Signal Matrix (CDSM)

The CDSM has 7 general purpose bi-directional digital signals labeled DB1 through DB7 that can be used for:

- Routing the AIOx input to or output signals from DB1 through DB7
- Routing the general-purpose comparator output signals to DB1 through DB7

11.16 Low-Frequency Clock Output

The PAC5256 has a configurable low-frequency clock output. When enabled, the device will output a 250Hz, 50% duty cycle clock to the CLKOUT pin.

The supported clock frequencies are 250Hz, 500Hz, 1kHz or 2kHz.

11.17 Cycle-by-cycle Current Limit

The PAC5256 contains hardware support for cycle by cycle current limit. The user may configure this feature to use the LPCOMP DAC as the current threshold. The CAFE will automatically perform duty cycle truncation to lower current at any time the associated phase current is greater than the setting of the LPCOMP DAC.

11.18 Integrated VM ADC Sampling

The PAC5256 contains integrated sampling of the VM (motor voltage) input using the ADC without having to dedicate an external pin to this sampling circuit on the PCB.

To sample the VM motor voltage (called VMS), the user should select the VMS voltage on the PWRMON MUX, and set the ADC AFE MUX to AB11 (PWRMON) and may use the ADC to sample channel AD0 to read this value.

In INFO FLASH, there are two linear sampling points for the VM ADC input: VMS100 and VMS200. These contain calibrated values for two sample points of VM = 100V and VM = 200V.

To calculate the actual VM sampling point, using the equation below.

- VM = 100 * (VMS_ADC[4] - VMS100) / (VMS200 - VMS100) + 100V

These can be used to calibrate the measured VM voltage and can be used by algorithms that need an accurate VM voltage for control.

For more information on how to set the device registers to read VMS, see the Application Note on this topic.

11.19 Temperature Warnings and Faults

The PAC5256 integrates a temperature sensor that is used for temperature protection and monitoring. The PAC5256 monitors the device temperature during operation for temperature warnings and faults.

If the device temperature reaches 140°C, the device enters the temperature warning state. When in this state, the device will continue to operate normally. The user may enable a maskable interrupt to notify the MCU of this event. While in the temperature warning state, if the temperature falls below 125°C, the device exits the temperature warning state.

If the device temperature reaches 170°C, the device enters the temperature fault state. When this state is entered, the Power Manager disables all of the power supplies, the ASPD and CAFE are disabled. The Power Manager will also set fault bits for the over-temperature and power supply failure conditions. While in this state, if the temperature falls below 155°C then the device will re-start the power supplies and the MCU will re-start. The MCU may check the fault bits to determine that this condition occurred when it is initializing itself.

For more details on temperature warning and fault handling, see the PAC5256 User Guide.

[4] Power monitor sampled VMS voltage in ADC counts

11.20 Temperature Monitoring

The PAC5256 has an integrated temperature sensor that may be sampled by the ADC in the MCU.

The voltage of the temperature sensor is called VPTAT. The PAC5256 stores calibration values for the temperature sensor in INFO FLASH. The MCU may calculate the device temperature by sampling VPTAT and using the calibration values stored in INFO FLASH.

For more information on how to calculate device temperature from VPTAT see the PAC5256 User Guide.

For details on how to select the temperature sensor channel using the ADC, see the section below on ADC Analog Input and the PAC5256 User Guide.

11.21 Voltage Reference

The reference block includes a 1.2V high-precision reference voltage used internally and for all the LDOs. There is also a high-accuracy 2.5V programmable reference for the ADC V_{REF} on the MCU. There is also a 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).

11.22 Electrical Characteristics

Table 11-1 Differential Programmable Gain Amplifier (DA) Electrical Characteristics (AIO<5:0>)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;DA}$	Input common mode range		-0.3		2.5	V
$V_{OLR;DA}$	Output linear range		0.1		V_{SYS} – 0.1	V
$V_{SHR;DA}$	Sample and hold range		0.1		3.5	V
$I_{CC;DA}$	Operating supply current	Each enabled amplifier		150	300	µA
$V_{OS;DA}$	Input offset voltage	Gain = 8x	-8		8	mV
$k_{CMRR;DA}$	Common mode rejection ratio		50	80		dB
	Slew rate	Gain = 8x	10			V/µs
$R_{INDIF;DA}$	Differential input impedance			27		kΩ
$t_{ST;DA}$	Settling time	To 1% of final value			360	ns
$A_{VZI;DA}$	Differential amplifier gain (zero ohm source impedance)	Gain = 1x		1		
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{DAxP}=V_{DAxN}=0V, T_A = 25°C	-2		2	%
		Gain = 8x		8		
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		

Table 11-2 Single-Ended Programmable Gain Amplifier (AMP) Electrical Characteristics (AIO<9:6>)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;AMP}$	Input common mode range		0		V_{SYS}	V
$V_{OLR;AMP}$	Output linear range		0.1		V_{SYS} - 0.1	V
$I_{CC;AMP}$	Operating supply current	Each enabled amplifier		80	120	µA
$V_{OS;AMP}$	Input offset voltage	Gain = 8x	-10		10	mV
	Slew rate	Gain = 1x	10			V/µs
$t_{ST;AMP}$	Settling time	To 1% of final value			360	ns
$A_{V;AMP}$	Amplifier gain	Gain = 1x		1		%
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{AMPx}=125mV, T_A = 25°C	-2		2	
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		
$t_{ST;AMP}$	Settling time	To 1% of final value			360	ns

Table 11-3 General Purpose Comparator (CMP) Electrical Characteristics (AIO<9:6>)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;CMP}$	Input common mode range		0		V_{SYS}	V
$I_{CC;CMP}$	Operating supply current	Each enabled comparator		35	70	µA
$V_{OS;CMP}$	Input offset voltage		-10		10	mV
$V_{HYS;CMP}$	Hysteresis			22		mV
$t_{DEL;CMP}$	Comparator delay				1	µs
$t_{DELMODE;CMP}$	Mode change blanking delay			10		µs

Table 11-4 Phase Comparator (PHC) Electrical Characteristics (AIO<9:6>)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;PHC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;PHC}$	Operating supply current	Each enabled comparator		35	70	µA
$V_{OS;PHC}$	Input offset voltage		-10		10	mV
$V_{HYS;PHC}$	Hysteresis			22		mV
$t_{DEL;PHC}$	Comparator delay	10mV difference input			1	µs

Table 11-5 Special Mode Electrical Characteristics (AIO<9:7>)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;SPEC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;SPEC}$	Operating supply current	Each enabled comparator		80	120	µA
$V_{HSYS;SPEC}$	Comparator Hysteresis, HYSMODE = 0	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (5mV)	4	6	8	mV
		AIO<9:7>HYS = 10b (10mV)	9	12	15	mV
		AIO<9:7>HYS = 11b (20mV)	18	24	30	mV
	Comparator Hysteresis, HYSMODE = 1	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (20mV)	18	24	30	mV
		AIO<9:7>HYS = 10b (40mV)	36	48	60	mV
		AIO<9:7>HYS = 11b (80mV)	72	96	120	mV

Table 11-6 Special Mode Electrical Characteristics (AIO6)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;SPEC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;SPEC6}$	Operating supply current			60	120	µA
$V_{INOFF;SPEC6}$	Input offset voltage		-20		20	mV
$I_{OUT;SPEC6}$	Output current			2		mA

Table 11-7 Analog Front End (AIO) Electrical Characteristics (AIO<9:0>)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{AIO}	Pin voltage range		0		5	V
$V_{IH;AIO}$	High-level input voltage	Input mode	2.2			V
$V_{IL;AIO}$	Low-level input voltage	Input mode			0.8	V
$R_{PD;AIO}$	Pull-down resistance	Input mode		1		MΩ
$V_{OL;AIO}$	Low-level output voltage	I_{AIOx}=10mA, open-drain output mode			0.3	V
$I_{OL;AIO}$	Low-level output sink current	V_{AIOx} = 0.4V, open-drain output mode	6	14		mA
$I_{LK;AIO}$	High-level output leakage current	V_{AIOx} = 5V, open-drain output mode		0	10	µA

Table 11-8 Push Button (PBTN) Electrical Characteristics (AIO6)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I;PBTN}$	Input voltage range		0		5	V
$V_{IH;PBTN}$	High-level input voltage		2.2			V
$V_{IL;PBTN}$	Low-level input voltage				0.8	V
$R_{PU;PBTN}$	Pull-up resistance	To 3V, push-button input mode		50		kΩ

Table 11-9 HP DAC and LP DAC Electrical Characteristics

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DACREF}	DAC reference voltage	TA = 25°C	-0.5%	2.5	0.5%	V
		TA = -40°C to 105°C	-0.9%	2.5	0.9%	
	HP 10-bit DAN INL		-2		2	LSB
	HP 10-bit DAC DNL		-1		1	LSB
	LP 10-bit DAC INL		-2		2	LSB
	LP 10-bit DAC DNL		-1		1	LSB

Table 11-10 Low-Frequency Clock Output (CLKOUT)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
F_{CLKOUT}	Low-speed clock output frequency	CLKOUT 250Hz		250		Hz
$F_{CLKOUT;ERR}$	Low-speed clock output frequency error	T_A = 25°C	-10		10	%
		T_A = -40°C - 105°C	-15		15	%

Table 11-11 Temperature Protection

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{WARN}	Temperature warning threshold			140		ºC
$T_{WARN;HYS}$	Temperature warning hysteresis			15		ºC
$T_{WARN;BLANK}$	Temperature warning blanking			10		µs
T_{FAULT}	Temperature fault threshold			165		ºC
$T_{FAULT;HYS}$	Temperature fault hysteresis			15		ºC
$T_{FAULT;BLANK}$	Temperature fault blanking			10		µs

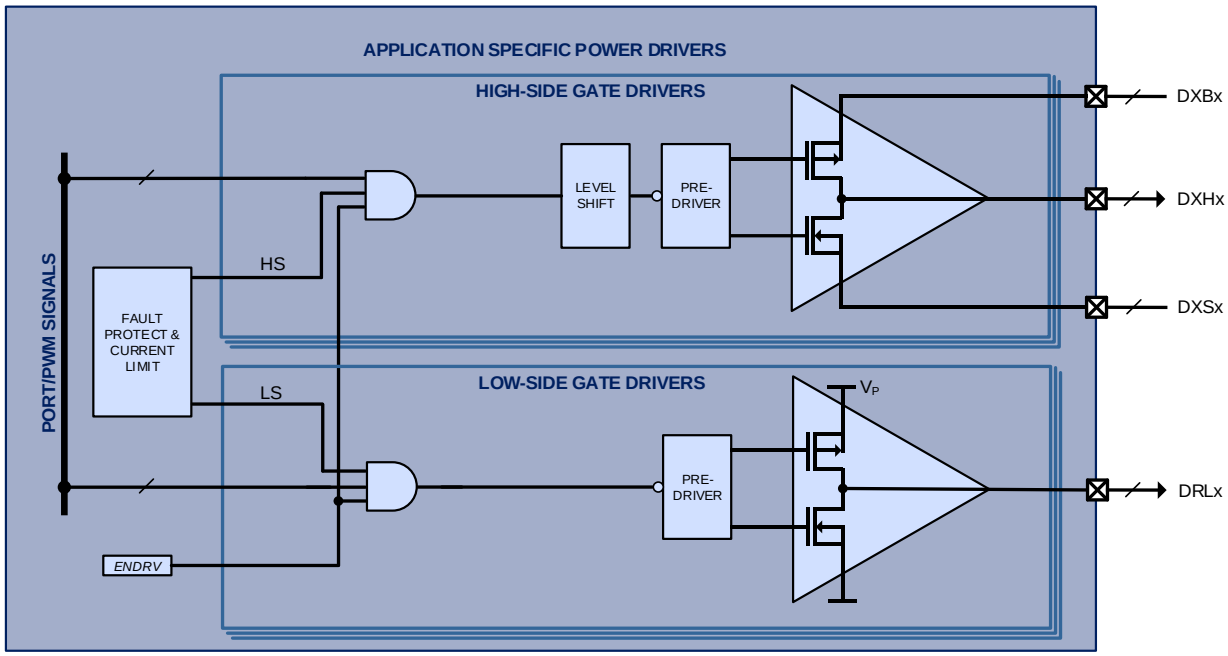
12 APPLICATION SPECIFIC POWER DRIVERS (ASPD)

12.1 Features

- 3 high-side gate drivers with 250mA source and 500mA sink current
- 3 low-side gate drivers with 1A source and 1A sink current
- Fast fault protection
- Cycle-by-cycle current limit function
- Configurable driver break-before-make (BBM) safety function

12.2 Block Diagram

Figure 12-1 Application Specific Power Drivers



12.3 Functional Description

The Application Specific Power Drivers™ (ASPD, Figure 12-1) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three ultra-high-side gate drivers (DXHx). Each gate driver can drive an external IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

Figure 12-2 below shows typical gate driver connections and Table 12-1 shows the ASPD available resources. The ASPD gate drivers support up to a 600V source supply.

Figure 12-2 Typical Gate Driver Connections

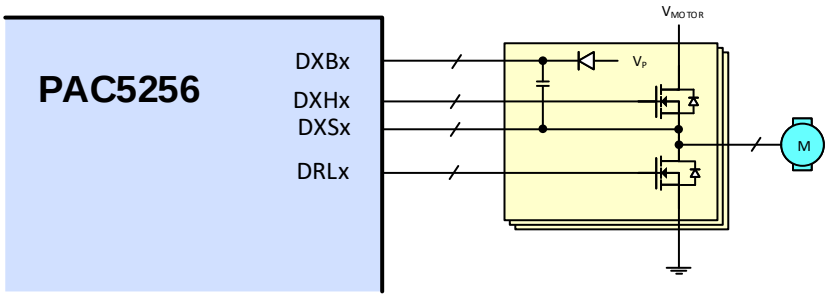


Table 12-1 Power Driver Resources

PART NUMBER	LOW-SIDE GATE DRIVER		HIGH-SIDE GATE DRIVER		
	DRLx	SOURCE/SINK CURRENT	DXHx	SOURCE/BOOTSTRAP SUPPLY	SOURCE/SINK CURRENT
PAC5256	3	1A/1A	3	610V/630V	0.25A/0.5A

When the ASPD is not enabled, the high-side and low-side gate drivers are pulled-down to a safe state.

12.4 Low-Side Gate Driver

The DRLx low-side gate driver drives the gate of an external IGBT switch between the low-level power ground rail and high-level V_P supply rail. The DRLx output pin has sink and source output current capability of 1A. Each low-side gate driver is controlled by a microcontroller port signal.

12.5 High-Side Gate Driver

The DXHx high-side gate driver drives the gate of an external MOSFET or IGBT switch between its low-level DXSx driver source rail and its high-level DXBx bootstrap rail. The DXSx pin can go up to 610V. The DXHx output pin has source output current capability of 0.25A and sink output current capability of 0.5A. The DXBx bootstrap pin can have a maximum operating voltage of up to 20V relative to the DXSx pin. The DXSx pin is designed to tolerate momentary switching negative spikes down to -10V without affecting the DXHx output state. Each high-side gate driver is controlled by a microcontroller port signal.

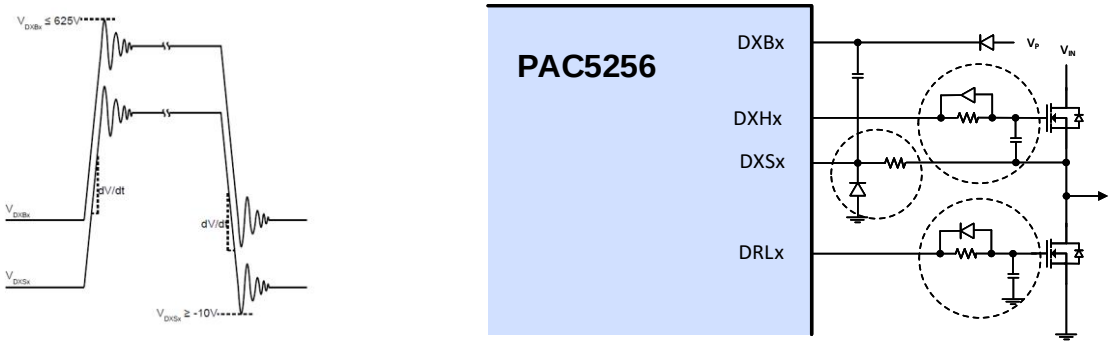
For bootstrapped high-side operation, connect an appropriate capacitor between DXBx and DXSx and a properly rated bootstrap diode from V_P to DXBx.

12.6 High-Side Switching Transients

Typical high-side switching transients are shown in Figure 10-1. To ensure functionality and reliability, the DXSx and DXBx pins must not exceed the peak and undershoot limit values shown. This should be verified by probing the DXSx and DXBx pins directly relative to VSS pin. A small resistor and diode clamp for the DXSx pin can be used to make sure that the pin voltage stays within the negative limit value. In addition, the high-side slew rate dV/dt must be kept within ±50V/ns for DXSx. This can be achieved by adding a resistor-diode pair in series, and an optional capacitor in parallel with the power switch gate. The parallel capacitor also provides a low impedance and close gate shunt against coupling from the switch drain.

These optional protection and slew rate controls are shown in Figure 10-1.

Figure 12-3 Gate Driver Switching Transients



(a) High-Side Switching Transients

(b) Optional Transient Protection and Slew Rate Control

12.7 Gate Driver Fault Protection

The ASPD incorporates a configurable fault protection mechanism using protection signal from the Configurable Analog Front End (CAFE), designated as protection event 1 (PR) signal.

The DRL0/DRL1/DRL2 drivers are designated as low-side group 1. The DXH0/DXH1/DXH2 gate drivers are designated as high-side group 1. The PR signal from the CAFE can be used to disable low-side group 1, high-side group 1, or both depending on the PR mask bit settings.

12.8 Gate Driver Pull Down

When the PAC5256 is powered-up, the input PWM from the MCU to the ASPD can be in an unknown state. To avoid any incorrect gate driver output, the ASPD includes pull-down resistors for the gate driver output as follows.

The high-side gate driver (DXHx) is pulled down to its source (DXSx) with a 5k resistor. The low-side gate driver (DRLx) is pulled down to ground using a 5k resistor.

12.9 Electrical Characteristics

Table 12-2 Gate Driver Electrical Characteristics

(V_M = 330V, V_P = 15V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Low-Side Gate Drivers (DRLx pins)						
$V_{OH;DRL}$	High-level output voltage	I_{DRLx} = -50mA	V_P-0.5			V
$V_{OL;DRL}$	Low-level output voltage	I_{DRLx} = 50mA			0.35	V
$I_{OHPK;DRL}$	Output high source current	10µs pulse		-1		A
$I_{OLPK;DRL}$	Output low sink current	10µs pulse		1		A
High-Side Gate Drivers (DXHx, DXBx and DXSx pins)						
V_{DXS}	Level-shift driver source voltage range	Repetitive, 10µs pulse	-10		605	V
		Steady state	0		600	V
V_{DXB}	Bootstrap pin voltage range	Repetitive, 10µs pulse	1		625	V
		Steady state	9		620	V
$V_{BS;DXB}$	Bootstrap supply voltage range	V_{DXBx}, relative to V_{DXSx}	9		20	V
$V_{UVLO;DXB}$	Bootstrap UVLO threshold	V_{DXBx} rising, relative to respective V_{DXSx}, Hysteresis = 0.5V	7	8	9	V
$I_{BS;DXB}$	Bootstrap supply current			25	50	µA
$I_{OS;DXB}$	Offset supply current	V_{DXBx} = V_{DXSx} = 600V			10	µA
$V_{OH;DXH}$	High-Level output voltage	I_{DXHx} = -50mA	V_{DXBx}-1			V
$V_{OL;DXH}$	Low-level output voltage	I_{DXHx} = 50mA			V_{DXSx}+0.6	V
$I_{OHPK;DXH}$	High-level pulsed peak source current	10µs pulse		-0.25		A
$I_{OLPK;DXH}$	Low-level pulsed peak sink current	10µs pulse		0.5		A

13 SOC CONTROL SIGNALS

The MCU has access to the Analog Sub-system on the PAC5256 through certain digital peripherals. The functions that the MCU may access from the Analog Sub-System are:

- High-side and Low-side Gate Drivers
- SPI Interface for Analog Register Access
- ADC EMUX
- Analog Sub-system Interrupts
- CLKOUT low-speed clock

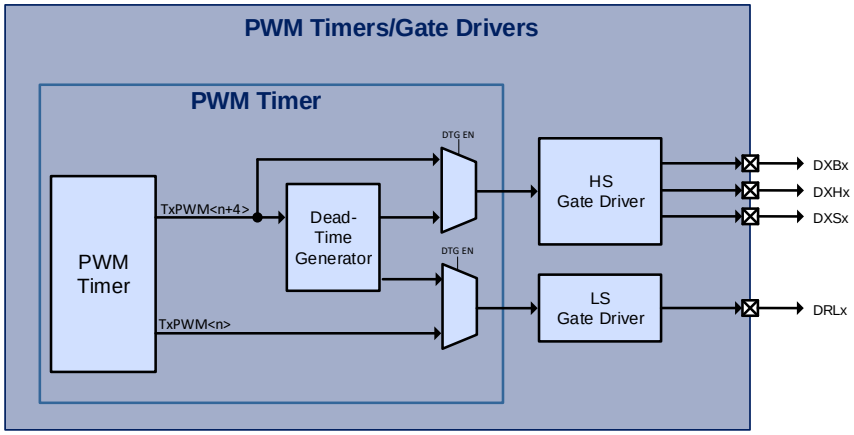
13.1 High-side and Low-Side Gate Drivers

The high-side and low-side gate drivers on the PAC5256 are controlled by PWM outputs of the timer peripherals on the MCU. The timer peripheral generates the PWM output. The PWM timer may be configured to generate a complementary PWM output (high-side and low-side gate drive signals) with hardware controlled dead-time.

These signals are sent to the gate drivers in the Analog Sub-system that create the high and low side gate drivers for the external inverter.

The user may choose to enable or not enable the DTG (Dead-time Generator). The diagram below shows the block diagram of the PWM timer, DTG and ASPD gate drivers.

Figure 13-1 SOC Signals for Gate Drivers



Each timer peripheral that drives the DTG and ASPD Gate Drivers has two PWM outputs that are connected to the gate drivers: TxPWM<n> and TxPWM<n+4>. If the Dead-Time Generator is disabled TxPWM<n> is connected to the DRLx gate driver output and TxPWM<n+4> is connected to the DXHx gate driver output. If the DTG is enabled, the TxPWM<n+4> is used to generate the complementary high-side and low-side output to the gate driver. For applications that drive half-bridge or full-bridge topologies, the DTG will be enabled to allow a complementary output with dead-time insertion.

Table 13-1 PWM to ASPD Gate Driver Options

Gate Driver	Timer PWM Input	GPIO Port/Pin
Complementary Pair		
DXH0	TAPWM4	PA6
DRL0	TAPWM0	PA0
Complementary Pair		
DXH1	TAPWM5	PA7
DRL1	TAPWM1	PA1
Complementary Pair		
DXH2	TAPWM6	PD7
DRL2	TAPWM2	PA2

Note in the table above that each phase has a complementary pair that is optimized for driving one half-bridge. Each half-bridge uses a pair of timer outputs that have dead-time insertion between them. The complementary pairs are grouped together in this table.

13.2 SPI SOC Bus

The SPI SOC bus is used for reading and writing registers in the Analog Sub-System. The table below shows which peripherals and which IO pins should be used for this interface.

Table 13-2 SPI SOC Bus Connections

SPI Signal	IO Pin
SCLK	PB4
MOSI	PB3
MISO	PB2
SS	PB1

13.3 CLKOUT Low-Speed Clock

The CLKOUT low-speed clock is an independent clock source that is generated by the AFE that can be used by applications that require a 2nd independent clock source.

The CLKOUT low-speed clock is available on the PA3 IO, which has the PWMA3, PWMA4 and PWMB0 CCR units available.

13.4 ADC EMUX

The ADC EMUX is a write-only serial bus that the ADC sequencer uses for instructing the CAFE to perform MUX changes, activate Sample and Hold, etc.

The table below shows the MCU pins that are used by the ADC EMUX in the PAC5256.

Table 13-3 SPI SOC Bus Connections

EMUX Signal	Description	IO Pin
EMUXC	EMUX Clock	PB5
EMUXD	EMUX Data	PB6

13.5 Analog Interrupts

The Analog sub-system has two interrupts that it can generate for different conditions. The table below shows the two different interrupts, the interrupt conditions and the IO pin that the interrupts are connected to.

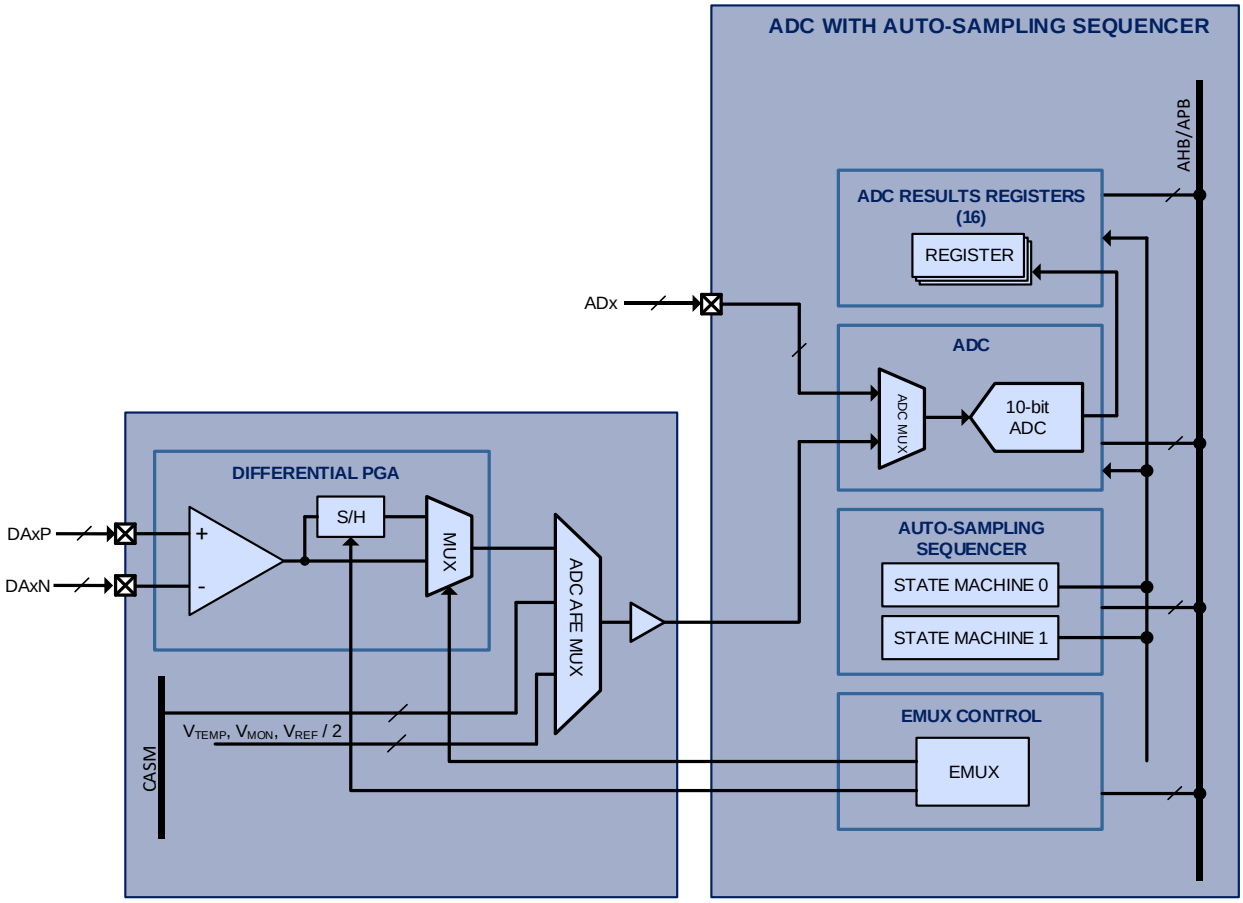
Table 13-4 Analog Interrupts

Analog IRQ	Interrupt Conditions	IO Pin
IRQ1	HPCOMP/LPCOMP Comparator Protection for Over-current and Over-Voltage events	PB0
IRQ2	BEMF and Special Mode Comparator, including phase to phase comparator, AIO6/AIO7/AIO8/AIO9 interrupt	PB7

14 ADC

14.1 ADC Block Diagram

Figure 14-1 ADC with Sequencer



14.2 Functional Description

14.2.1 ADC

The analog-to-digital converter (ADC) is a 10-bit successive approximation register (SAR) ADC with 1µs conversion time and up to 1MSPS capability. The ADC input clock has a user-configurable divider from /1 to /8 of the system clock. The integrated analog multiplexer allows selection from up to 5 direct ADx inputs, and from up to 10 analog inputs signals in the Configurable Analog Front End (CAFE), including up to 3 differential input pairs. The ADC can be configured for repeating or non-repeating conversions and can interrupt the microcontroller when a conversion is finished.

14.2.2 Auto-Sampling Sequencer

Two independent and flexible auto-sampling sequencer state machines allow signal sampling using the ADC without interaction from MCU. Each auto-sampling sequencer state machine can be programmed to take and store up to 8 samples each in the ADC result registers from different analog inputs, is able to control the ADC MUX and ADC AFE MUX as well as the precise timing of the S/H in the Configurable Analog Front-End (CAFE). The sampling start of the auto-sampling sequencer can be precisely triggered using timers A, B, C, or D or any of their associated PWM edges (high-to-low or low-to-high). It also supports manual start or a ping-pong-scheme, where one auto-sampling sequencer state machine triggers the other when it finishes sampling.

The auto-sampling sequencer can interrupt the microcontroller when either conversion sequence is finished.

14.2.3 EMUX Control

A dedicated low latency interface controllable by the auto-sampling sequencer or register control allows changing the ADC pre-multiplexer and asserting/de-asserting the S/H circuit in the Configurable Analog Front-End (CAFE), allowing back to back conversions of multiple analog inputs without MCU interaction.

For more information on the ADC and Auto-Sequencer, see the PAC5256 User Guide.

14.3 Electrical Characteristics

Table 14-1 ADC and Sequencer Electrical Characteristics

(V_{CCIO} = 5V and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ADC						
f_{ADCCLK}	ADC conversion clock input				16	MHz
$f_{ADCCONV}$	ADC conversion time	f_{ADCCLK} = 16MHz			1	µs
	ADC resolution			10		bits
	ADC effective resolution		9.2			bits
	ADC differential non-linearity (DNL)			±0.5		LSB
	ADC integral non-linearity (INL)			±1		LSB
	ADC offset error			0.6		%FS
	ADC gain error			0.12		%FS
REFERENCE VOLTAGE						
V_{REFADC}	ADC reference voltage input	V_{REF} = 2.5V	-0.5%	2.5	0.5%	V
SAMPLE AND HOLD						
t_{ADCSH}	ADC sample and hold time	f_{ADCCLK} = 16MHz		188		µs
C_{ADCIC}	ADC input capacitance	ADC MUX input		1.3		pF
INPUT VOLTAGE RANGE						
V_{ADCIN}	ADC input voltage range	ADC MUX input	0		V_{REFADC}	V
EMUX CLOCK SPEED						
$f_{EMUXCLK}$	EMUX engine clock input				50	MHz

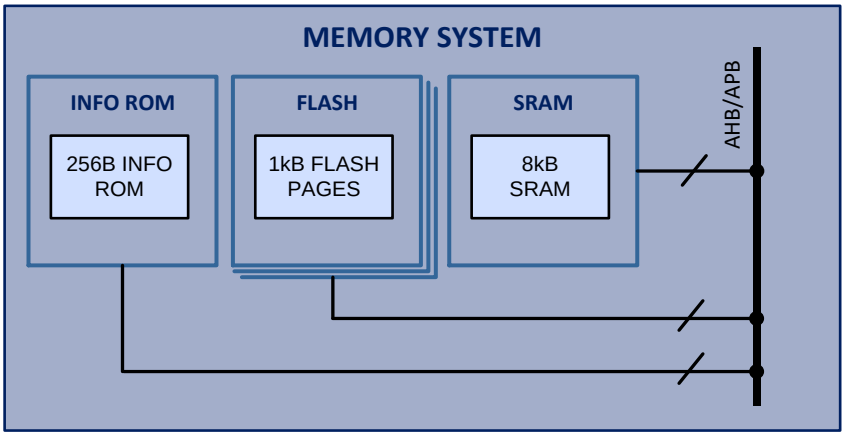
15 MEMORY SYSTEM

15.1 Features

- 32kB Embedded FLASH
  - 100,000 program/erase cycles
  - 10 years data retention
- 256B INFO Embedded FLASH
  - Device ID, calibration data
- 8kB SRAM
  - 50MHz read/write
  - Data storage or code execution
- SWD code protection

15.2 Memory System Block Diagram

Figure 15-1 Memory System



15.3 Functional Description

The PAC5256 has multiple banks of embedded FLASH memory, SRAM memory as well as peripheral control registers that are program-accessible in a flat memory map.

15.4 Program FLASH

The PAC5256 Memory Controller provides access to 32 1kB pages of main program FLASH for a total of 32kB of FLASH through the system AHB bus. Each page may be individually erased or written while the MCU is executing instructions from SRAM.

15.5 INFO FLASH

The PAC5256 Memory Controller contains a 256B read-only INFO memory. This memory contains device-specific information such as the device ID and calibration data for the device.

15.6 SRAM

The PAC5256 Memory Controller provides access to the 8kB SRAM for non-persistent data storage. The SRAM memory supports word (4B), half-word (2B) and byte addresses with aligned access.

The PAC5256 Memory Controller can read or write data from RAM up to 50MHz. This can be a benefit for time-critical applications. This memory can also be used for program execution when modifying the contents of FLASH.

For more information on the PAC5256 Memory Controller, see the PAC5256 User Guide.

15.7 SWD Protection

The PAC5256 allows the user to blow a fuse that prohibits use of the SWD serial interface.

This will prevent unauthorized users from accessing the contents of the device after customer production.

15.8 Electrical Characteristics

Table 15-1 Memory System Electrical Characteristics

(V_{CCIO} = 5V, T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Embedded FLASH						
$t_{READ;FLASH}$	FLASH read time		40			ns
$t_{WRITE;FLASH}$	FLASH write time		20			µs
$t_{PERASE;FLASH}$	FLASH page erase time				10	ms
$N_{PERASE;FLASH}$	FLASH program/erase cycles			100k		cycles
$t_{DR;FLASH}$	FLASH data retention		10			years
SRAM						
$t_{ACC;SRAM}$	SRAM access time	Word (32-bits), aligned	20			ns

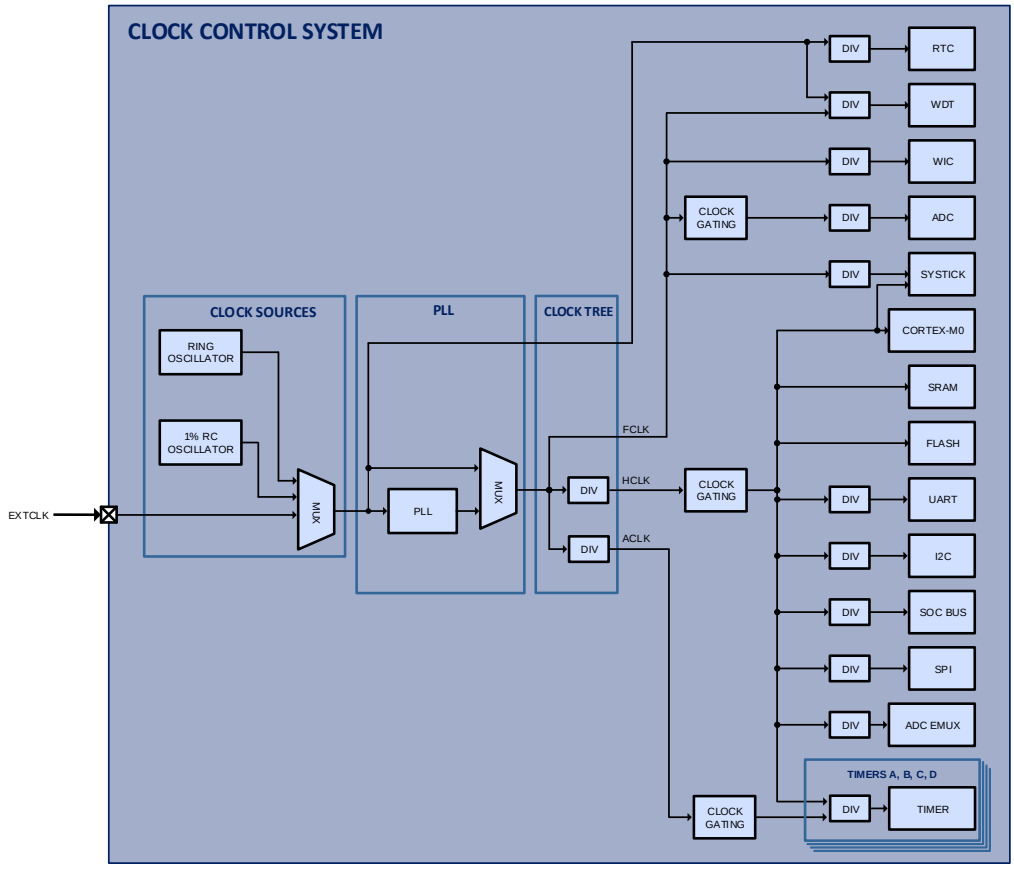
16 SYSTEM AND CLOCK CONTROL

16.1 Features

- Ring oscillator with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings
- High accuracy 1.25% trimmed 4MHz RC oscillator
- External clock input up to 10MHz
- PLL with 1MHz to 25 MHz input, and 3.5MHz to 100MHz output
- /1 to /8 clock divider for HCLK
- /1 to /128 clock divider for ACLK

16.2 Block Diagram

Figure 16-1 Clock Control System



16.3 Functional Description

16.3.1 Free-Running Clock (FRCLK)

The free running clock (FRCLK) is generated from one of the 3 clock sources: ring oscillator, trimmed RC oscillator or external clock input. The FRCLK is used for the real-time clock (RTC), watchdog timer (WDT), input to the PLL, or FCLK source to clock the system in low power and sleep mode.

16.3.2 Auxiliary Clock (ACLK)

The auxiliary clock (ACLK) is derived from FCLK with a /1, /2, to /128 divider, and supplies the timer and dead-time blocks. It can be clocked faster or slower than HCLK and can go as high as 100MHz.

16.3.3 Clock Gating

The clock tree supports clock gating in deep-sleep mode for the timer block, ADC, SPI interface, I^2C interface, UART interface, memory subsystem and the Arm® Cortex®-M0 itself.

16.3.4 Ring Oscillator (ROSC)

The integrated ring oscillator (ROSC) is the default clock for the PAC5256. ROSC provides 4 different clocks with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings. After reset, the clock tree always defaults to this clock input with the lowest frequency setting.

16.3.5 Trimmed 4MHz RC Oscillator

The 1.25% trimmed 4MHz RC oscillator provides an accurate clock suitable for many applications. It is also used to derive the clock for the Multi-Mode Power Manager.

16.3.6 External Clock Input

The clock tree can be supplied with an external clock up to 10MHz.

16.3.7 PLL

The integrated PLL input clock is supplied by the FRCLK with an input frequency range of 1MHz to 25MHz. The PLL output frequency is adjustable from 3.5MHz to 100MHz.

16.4 Electrical Characteristics

Table 16-1 CCS Electrical Characteristics

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Clock Tree (FRCLK, FCLK, ACLK, and HCLK)						
f_{FRCLK}	Free-running clock frequency				50	MHz
f_{FCLK}	Fast clock frequency				100	MHz
f_{ACLK}	Auxiliary clock frequency	After divider			100	MHz
f_{HCLK}	System clock frequency	After divider			50	MHz
Internal Oscillators						
f_{ROSC}	Ring oscillator frequency	Frequency setting = 11b		7.5		MHz
		Frequency setting = 10b		9.6		
		Frequency setting = 01b		13.8		
		Frequency setting = 00b		25.7		
f_{TRIM}	Trimmed RC oscillator frequency	T_A = 25°C	3.95	4	4.05	MHz
			-1.25		1.25	%
		T_A = -40°C to 105°C	3.90	4	4.08	MHz
			2.5		2.0	%
	Trimmed RC oscillator clock jitter	T_A = -40°C to 85°C		0.5		%
External Clock Input (EXTCLK)						
f_{EXTCLK}	External Clock Input Frequency				40	MHz
$t_{HIGH;EXTCLK}$	External Clock High Time		10			ns
$t_{LOW;EXTCLK}$	External Clock Low Time		10			ns
$V_{IH;EXTCLK}$	External Clock Input high-level input voltage		2.1			V
$V_{IL;EXTCLK}$	External Clock Input low-level input voltage				0.825	V
PLL						
f_{INPLL}	PLL input frequency range		2		25	MHz
f_{OUTPLL}	PLL output frequency range		3.5		100	MHz
	PLL setting time			0.5		ms
	PLL period jitter	RMS		30		ps
		Peak to peak		±150		ps

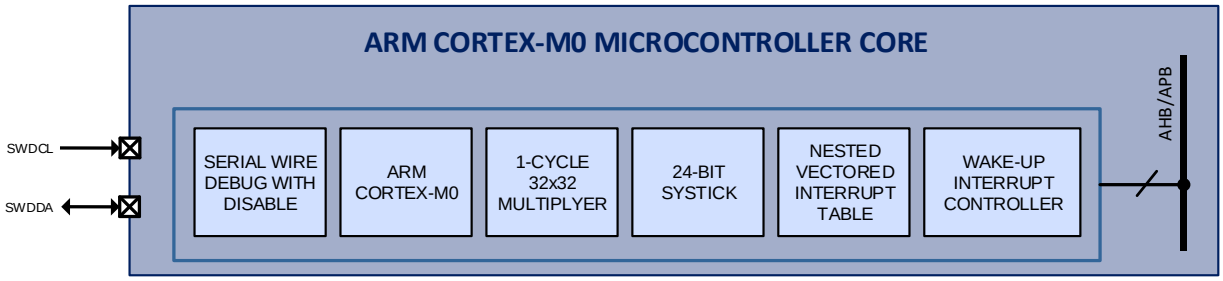
17 ARM® CORTEX®-M0 MCU CORE

17.1 Features

- Arm® Cortex®-M0 core
- Fast single-cycle 32-bit x 32-bit multiplier
- 24-bit SysTick timer
- Up to 50MHz operation
- Serial wire debug (SWD), with 4 break-point and 2 watch-point unit comparators
- Nested vectored interrupt controller (NVIC) with 25 external interrupts
- Wake-up interrupt controller (WIC) with GPIO, real-time clock (RTC) and watchdog timer (WDT) interrupts enabled
- Sleep and deep-sleep mode with clock gating

17.2 Block Diagram

Figure 17-1 Arm® Cortex®-M0 Microcontroller Core



17.3 Functional Description

The Arm® Cortex®-M0 microcontroller core is configured for little endian operation and includes the fast single-cycle 32-bit multiplier and 24-bit SysTick timer and can operate at a frequency of up to 50MHz.

The microcontroller nested vectored interrupt controller (NVIC) supports 25 external interrupts for the device's peripherals and sub-systems. For low-latency interrupt processing, the NVIC also supports interrupt tail-chaining. The wake-up interrupt controller (WIC) is able to wake up the device from low-power modes using any GPIO interrupt, as well as from the RTC or WDT. The Arm® Cortex®-M0 supports both sleep and deep-sleep low-power modes. The deep-sleep mode supports clock gating to limit standby power even further.

Firmware debug support includes 4 break-point and 2 watch-point unit comparators using the serial wire debug (SWD) protocol. The serial wire debug mechanism can be disabled to prevent device access to the firmware in the field.

For more information on the detailed operation of the Microcontroller Core in the PAC5256, see the PAC5256 User Guide.

17.4 Electrical Characteristics

Table 17-1 MCU and Clock Control System Electrical Characteristics

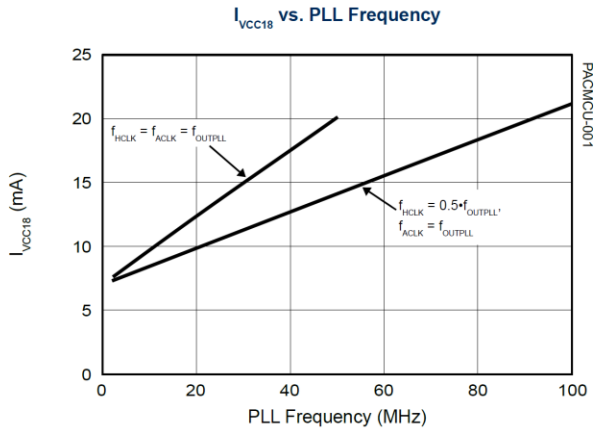
(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{HCLK}	Microcontroller Clock	HCLK			50	MHz
$I_{OP;VSYS}$	V_{SYS} operating supply current	f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 11b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled		3.4		mA
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 10b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled		4		
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 01b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled		5.3		
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 00b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled		9		
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = CLKREF, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled		2.3		
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = 10MHz XTAL, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled		4.5		
		f_{FRCLK} = 4MHz CLKREF, f_{HCLK} = 50MHz, f_{ACLK} = f_{OUTPLL} = 100MHz, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled		23.3		

17.5 Typical Performance Characteristics

(V_{SYS} = V_{CCIO} = 5V, T_A = -40°C to 105°C unless otherwise specified.)

Figure 17-2 MCU Performance Characteristics



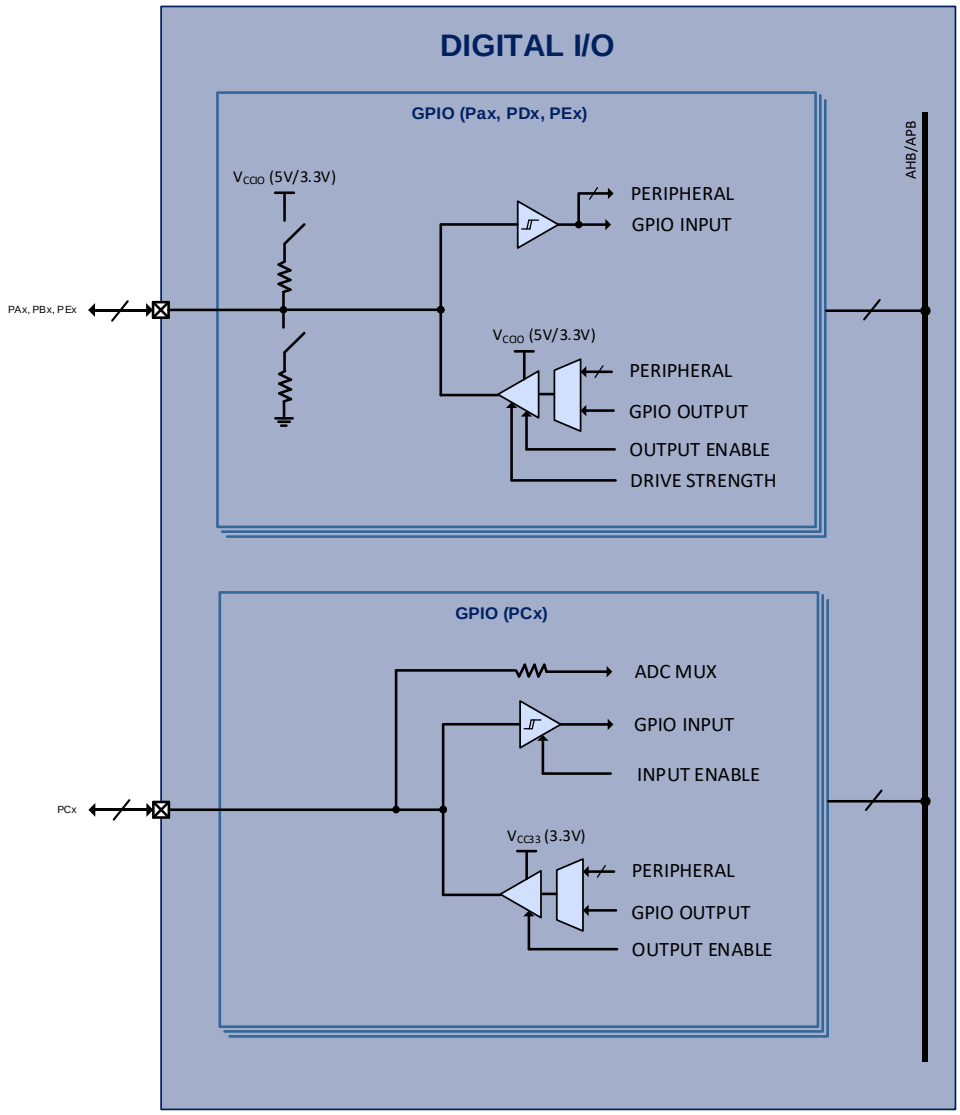
18 IO CONTROLLER

18.1 Features

- 5V-compliant I/O PAx, PDx, PEx
- 3.3V-compliant I/O PCx
- Configurable drive strength on PAx, PDx, PEx
- Configurable pull-up or pull-down on PAx, PDx, PEx

18.2 Block Diagram

Figure 18-1 IO Controller Block Diagram



18.3 Functional Description

The PAC can support up to 4 ports with 8 I/Os each from PAx, PCx, PDx, and PEx, in addition to the I/Os on the analog front end. All PAx, PCx, PDx, and PEx ports have interrupt capability with configurable interrupt edge.

PAx, PDx, and PEx I/Os use V_{CCIO} as the I/O supply voltage that is 5V on default parts (and 3.3V available from factory).

The drive current can be configured as 8mA or 16mA. They also support weak pull-up and pull-down to save external components.

PCx uses V_{CC33} as its I/O supply voltage. The drive current is fixed to 8mA. PC0 to PC5 are also associated with analog inputs AD0 to AD5 to the ADC.

18.4 GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply[5]. Current will be injected into the GPIO when the GPIO pin voltage is less than -0.3V or when greater than GPIO supply + 0.3V.

In order provide a robust solution when this situation occurs, the PAC52XX family of products allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than -0.3V may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.

[5] VCC33 is the supply for any PC GPIO pin and VCCIO is the supply for any other GPIO pins.

18.5 Electrical Characteristics

Table 18-1 IO Controller Electrical Characteristics

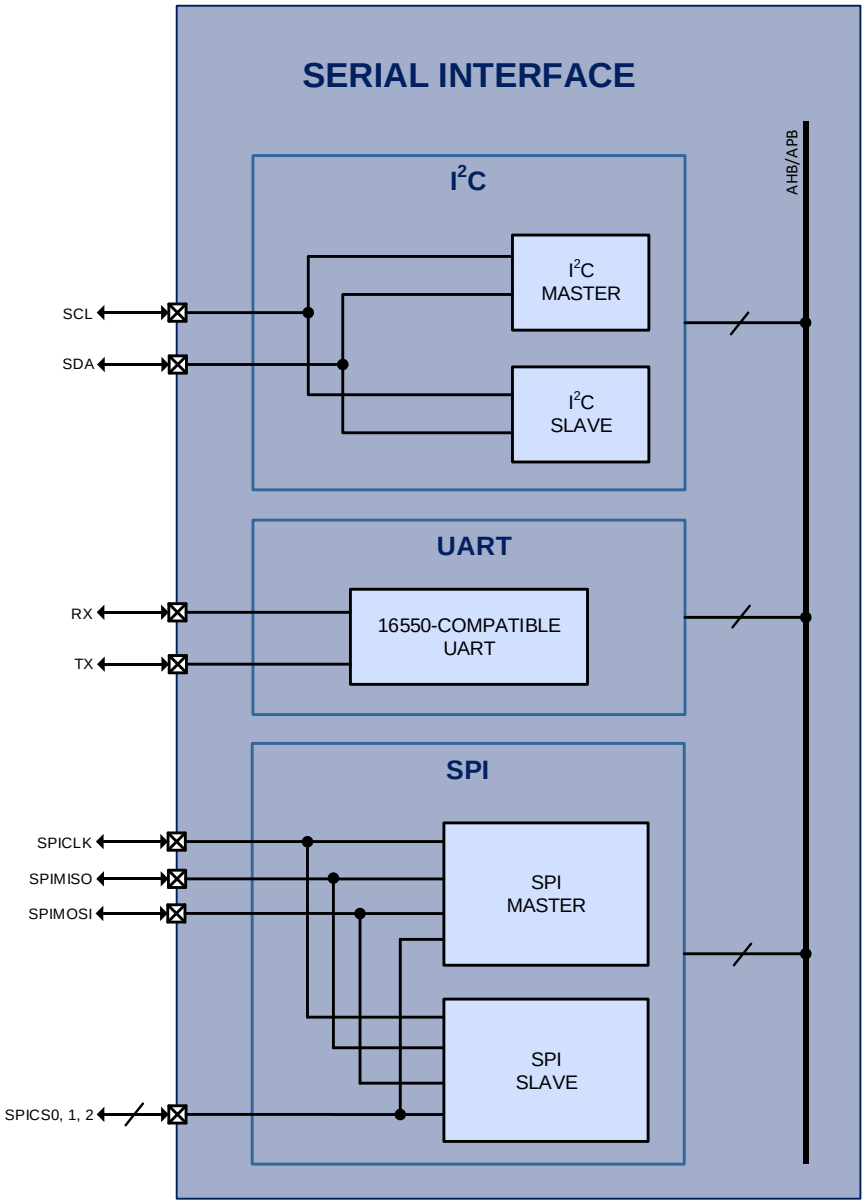
(V_{SYS} = V_{CCIO} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
PAx, PDx, PEx (3.3V Operation)							
V_{IH}	High-level input voltage			3			V
V_{IL}	Low-level input voltage					0.8	V
I_{OL}	Low-level output sink current (Limited by I_{VSYS})	V_{OL} = 0.4V	Drive Strength = 0b	7			mA
			Drive Strength = 1b	15			
I_{OH}	High-level output source current (Limited by I_{VSYS})	V_{OH} = 2.4V	Drive Strength = 0b			-7	mA
			Drive Strength = 1b			-15	
R_{PU}	Weak pull-up resistance	V_{CCIO} = 3.3V, pull-up enabled		47	74	104	kΩ
R_{PD}	Weak pull-down resistance	V_{CCIO} = 3.3V, pull-down enabled		50	84	121	kΩ
I_{IL}	Input leakage current			-10		10	µA
PCx (3.3V Operation)							
V_{IH}	High-level input voltage	V_{CC33} = 3.3V		2			V
V_{IL}	Low-level input voltage	V_{CC33} = 3.3V				0.8	V
I_{OL}	Low-level output sink current	V_{CC33} = 3.3V, V_{OL} = 0.4V		7			mA
I_{OH}	High-level output source current	V_{CC33} = 3.3V, V_{OH} = 2.4V				-7	mA
I_{IL}	Input leakage current	T_A = 125°C		-10	0	10	µA

19 SERIAL INTERFACE

19.1 Block Diagram

Figure 19-1 Serial Interface Block Diagram



19.2 Functional Description

The PAC5256 has up to three serial interfaces: I²C, UART and SPI.

19.3 I²C Controller

The I₂C controller is a configurable peripheral that can support various modes of operation:

- I²C master operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Single and multi-master
  - Synchronization (multi-master)
  - Arbitration (multi-master)
  - 7-bit or 10-bit slave addressing
- I²C slave operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Clock stretching
  - 7-bit or 10-bit slave addressing

The I₂C peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

19.4 UART Controller

The UART peripheral is a configurable peripheral that can support various features and modes of operation:

- Programmable clock selection
- National Instruments PC16550D compatible
- 16-deep transmit and receive FIFO and fractional clock divisor
- Up to 3.125Mbps communication speed (with HCLK = 50MHz)

The UART peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

19.5 SPI Controller

The device contains an SPI controller that can each be used in either master or slave operation, with the following features:

- SPI master operation
  - Control of up to three different SPI slaves
  - Operation up to 25MHz
  - Flexible multiple transmit mode for variable-size SPI data with user-defined chip-select behavior
  - Chip select “shaping” through programmable additional delay for chip-select setup, hold and wait time
  - for back-to-back transfers

- SPI master or slave operation
  - Supports clock phase and polarity control
  - Data transmission/reception can be on 8-, 16-, 24- or 32-bit boundary
  - Selectable data bit ordering (LSB or MSB first)
  - Programmable chip select polarity
  - Selectable “auto-retransmit” mode

The SPI peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

19.6 Dynamic Characteristics

Table 19-1 Serial Interface Dynamic Characteristics

(V_{SYS} = V_{CCIO} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I²C						
f_{I2CCLK}	I²C input clock frequency	Standard mode (100kHz)	2.8			MHz
		Full-speed mode (400kHz)	2.8			MHz
		Fast mode (1MHz)	6.14			MHz
UART						
$f_{UARTCLK}$	USART input clock frequency				f_{HCLK}/16	MHz
	UART baud rate	f_{HCLK} = 50MHz			3.125	Mbps
SPI						
f_{SPICLK}	USART input clock frequency	Master mode			f_{HCLK}/2	MHz
		Slave mode			f_{HCLK}/2	MHz

Table 19-2 I²C Dynamic Characteristics

(V_{SYS} = V_{CCIO} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Full-speed mode	0		400	kHz
		Fast mode	0		1000	kHz
t_{LOW}	SCL clock low	Standard mode	4.7			µs
		Full-speed mode	1.3			µs
		Fast mode	0.5			µs
t_{HIGH}	SCL clock high	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{HD;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Full-speed mode	0		0.9	µs
		Fast mode	0			µs
$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
		Full-speed mode	100			ns
		Fast mode	50			ns
$t_{SU;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Full-speed mode	1.3			µs
		Fast mode	0.5			µs
t_r	Rise time for SDA and SCL	Standard mode			1000	ns
		Full-speed mode	20		300	ns
		Fast mode			120	ns
t_f	Fall time for SDA and SCL	Standard mode			300	ns
		Full-speed mode			300	ns

		Fast mode	120	ns
C_b	Capacitive load for each bus line	Standard mode, full-speed mode	400	pF
		Fast mode	550	pF

Figure 19-2 I²C Timing Diagram

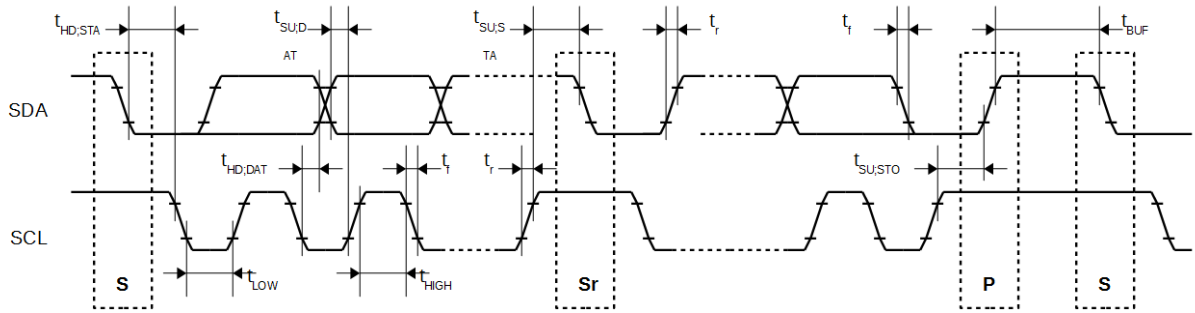
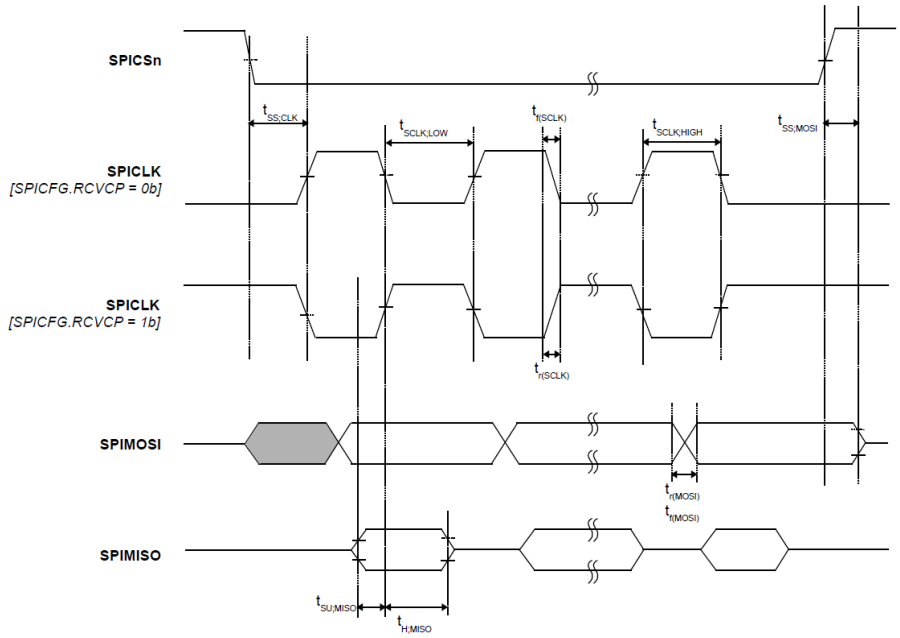


Table 19-3 SPI Dynamic Characteristics

(V_{SYS} = V_{CCIO} = 5V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SCLK;HIGH}$	SPICLK Input High Time	SPICLK = 25MHz	30			ns
$t_{SCLK;LOW}$	SPICLK Input low Time		30			ns
$t_{SS;SCLK}$	SPICSn to SPICLK Time		120			ns
$t_{SS;MOSI}$	SPICSn to SPIMISO High-impedance time		10		50	ns
$t_{r(SCLK)}$	SPICLK Rise Time			10	25	ns
$t_{f(SCLK)}$	SPICLK Fall Time			10	25	ns
$t_{r(MOSI)}$	SPIMOSI Rise Time			10	25	ns
$t_{f(MOSI)}$	SPIMOSI Fall Time			10	25	ns
$t_{r(MISO)}$	SPIMISO Rise Time			10	25	ns
$t_{f(MISO)}$	SPIMISO Fall Time			10	25	ns
$t_{SU;MISO}$	SPIMISO Setup Time		20			ns
$t_{H;MISO}$	SPIMISO Hold Time		20			ns

Figure 19-3 SPI Timing Diagram



20 TIMERS

20.1 Block Diagram

Figure 20-1 PWM Timers Block Diagram

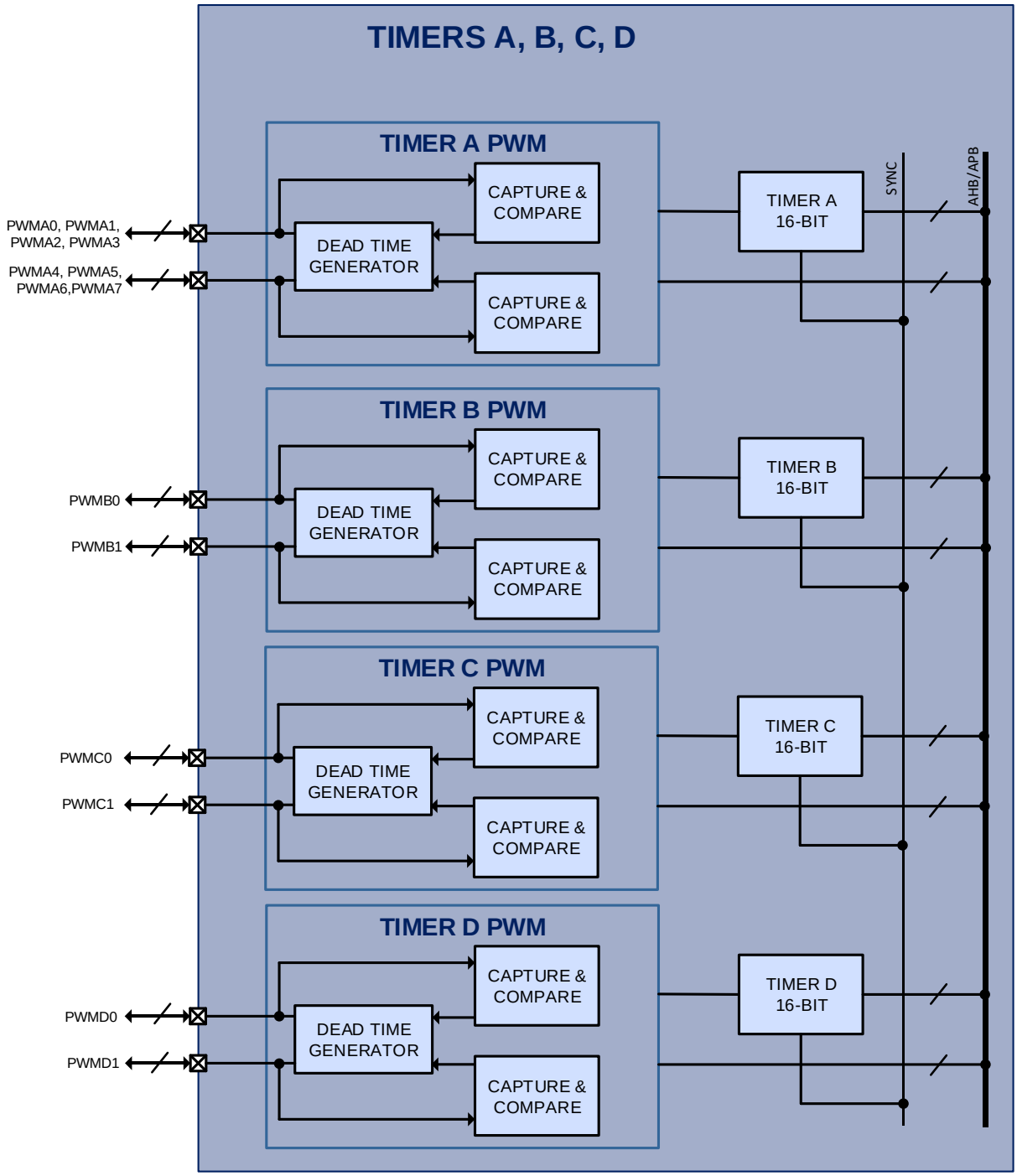


Figure 20-2 SOC Bus Watchdog and Wake-Up Timer

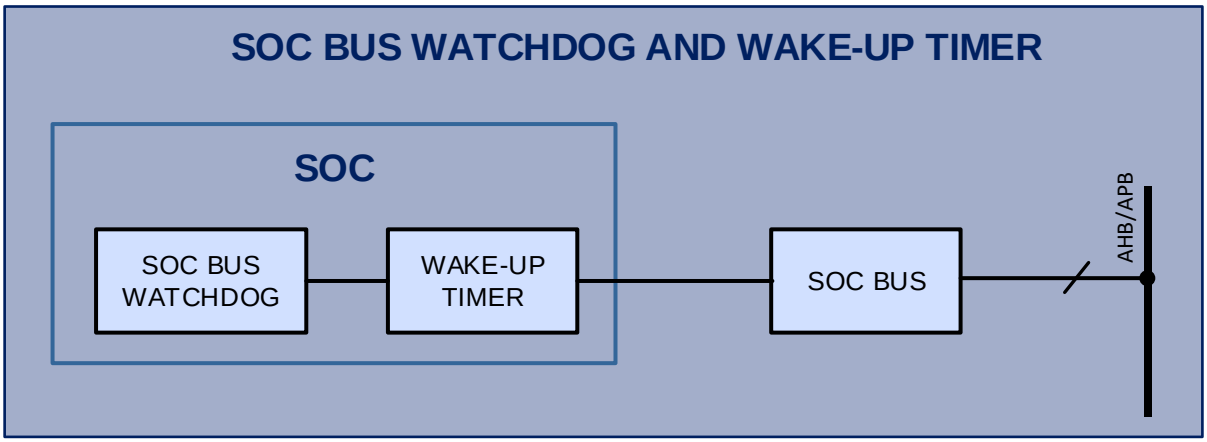
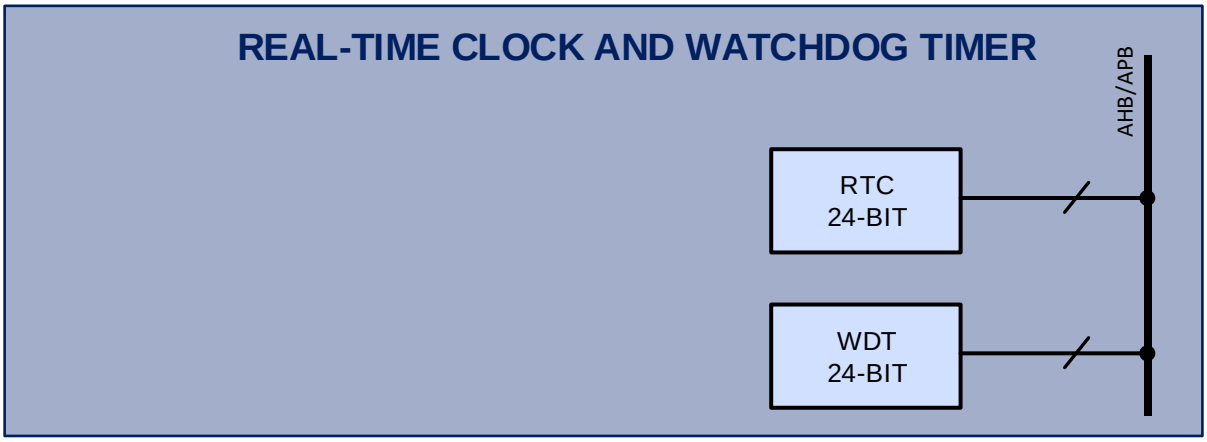


Figure 20-3 Real-Time Clock and Watchdog Timer



20.2 Functional Description

The device includes 9 timers: timer A, timer B, timer C, timer D, watchdog timer 1 (WDT), watchdog timer 2, wake-up timer, real-time clock (RTC), and SysTick timer. The device supports up to 14 different PWM signals and has up to 7 dead-time controllers. Timers A, B, C and D can be concatenated to synchronize to a single clock and start/stop signal for applications that require a synchronized timer period between timers.

20.2.1 Timer A

Timer A is a general purpose 16-bit timer with 8 PWM/capture and compare units. It has 4 pairs of PWM signals going into 4 dead-time controllers. Timer A can be concatenated with timers B, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

20.2.2 Timer B

Timer B is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller, as well as 2 additional compare units that can be used for additional system time bases for interrupts. Timer B can be concatenated with timers A, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

20.2.3 Timer C

Timer C is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer C can be concatenated with timers A, B, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

20.2.4 Timer D

Timer D is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer D can be concatenated with timers A, B, and C to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

20.2.5 Watchdog Timer

The 24-bit watchdog timer (WDT) can be used for long time period measurements or periodic wake up from sleep mode.

The watchdog timer can be used as a system watchdog, or as an interval timer, or both. The watchdog timer can use either FRCLK or FCLK as clock input with an additional clock divider from /2 to /65536.

20.2.6 SOC Bus Watchdog Timer

The watchdog timer 2 is used to monitor internal SOC Bus communication. It will trigger device reset if there is no SOC Bus communication to the AFE for 4s or 8s.

20.2.7 Wake-Up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically.

It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

20.2.8 Real-Time Clock

The 24-bit real-time clock (RTC) can be used for time measurements when an accurate clock source is used. This timer can also be used for periodic wake up from sleep mode. The RTC uses FRCLK as clock input with an additional clock divider from /2 to /65536.

21 THERMAL CHARACTERISTICS

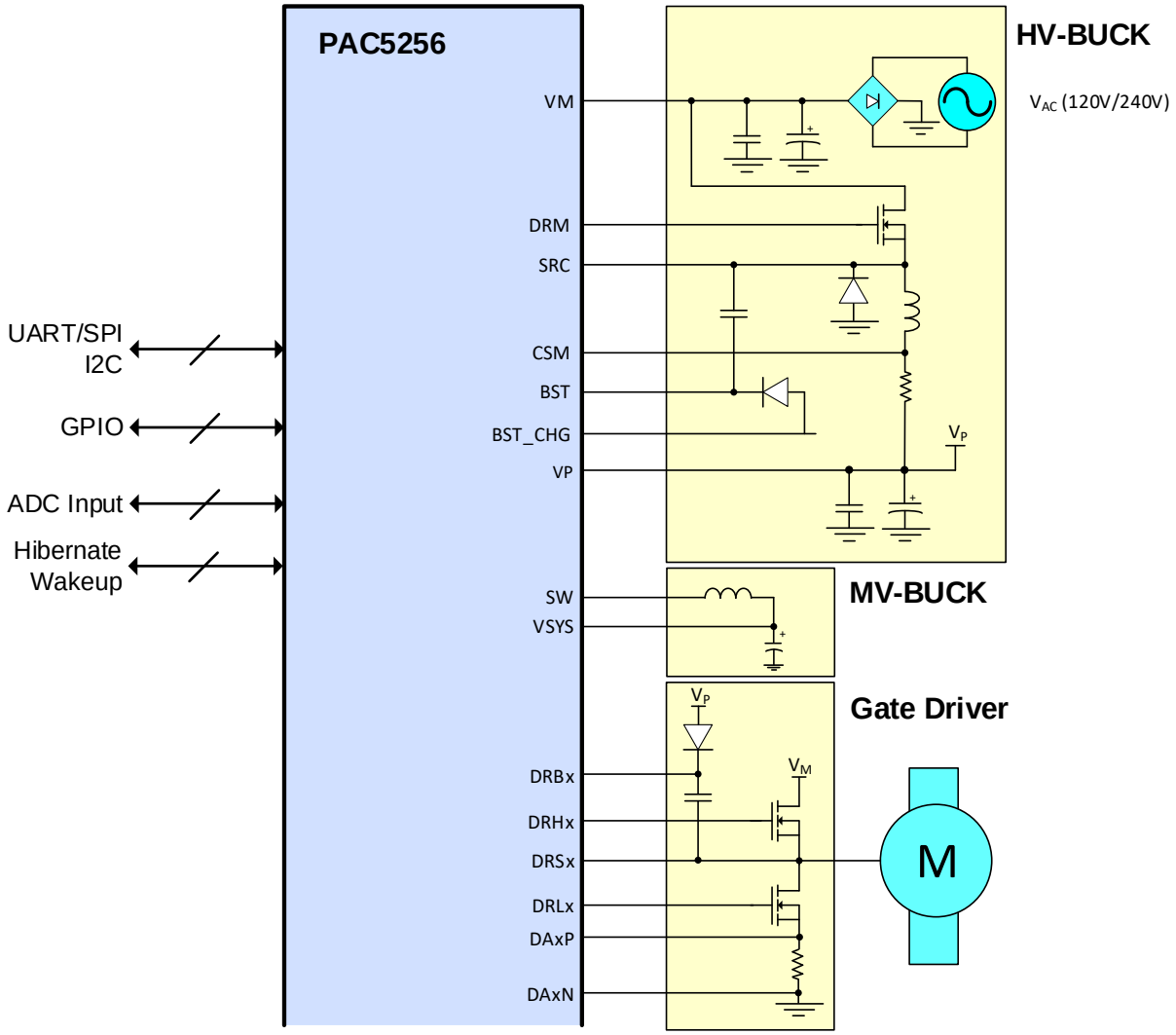
Table 21-1 Thermal Characteristics

PARAMETER	VALUE	UNIT
Operating ambient temperature range	-40 to 105	°C
Operating junction temperature range	-40 to 125	°C
Storage temperature range	-55 to 150	°C
Lead temperature (Soldering, 10 seconds)	300	°C
Junction-to-case thermal resistance (Θ_{JC})	2.897	°C/W
Junction-to-ambient thermal resistance (Θ_{JA})	23.36	°C/W

22 APPLICATION EXAMPLES

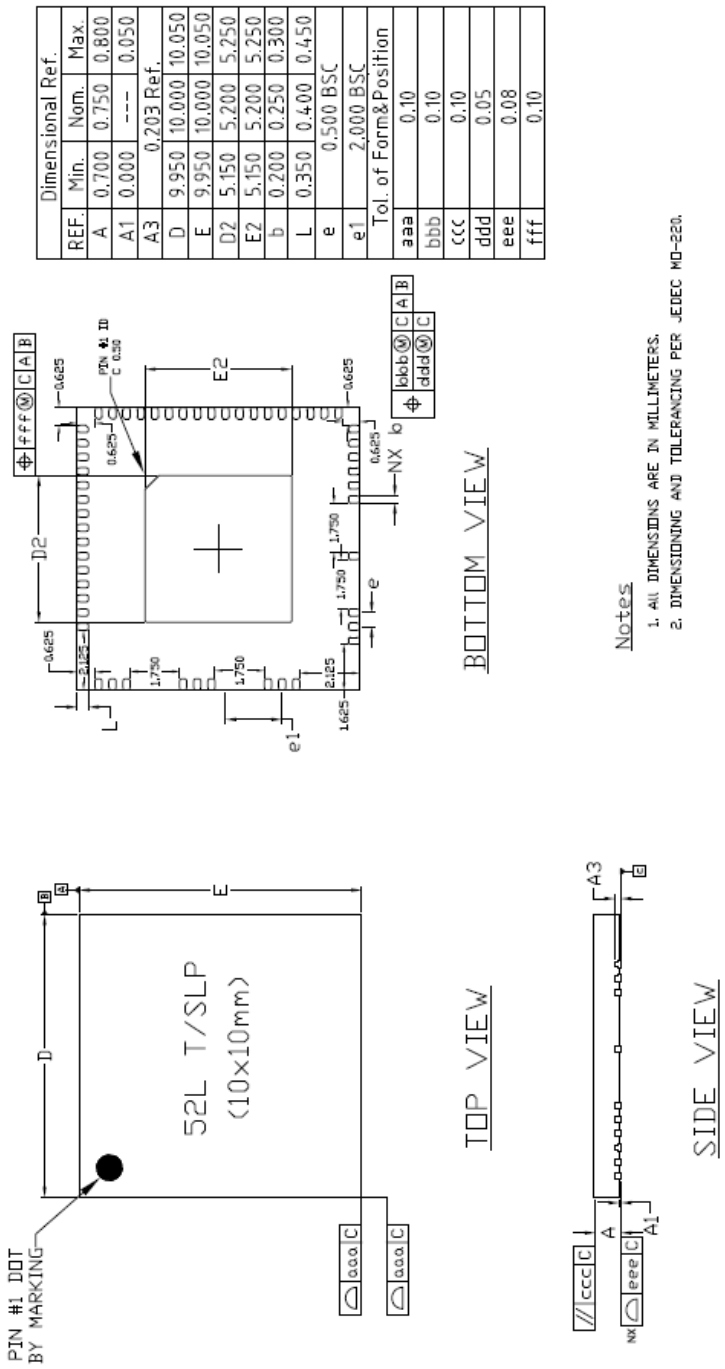
The following simplified diagram shows an example of a 3-phase BLDC or PMSM motor application for FOC or BEMF control.

Figure 22-1 BLDC/PMSM Motor Application Example



23 PACKAGE OUTLINE AND DIMENSIONS

23.1 QFN1010-52 Package Outline and Dimensions



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

Important Notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE**.

Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.