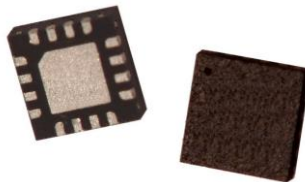


Applications

- Base Station receivers
- Tower-mounted amplifiers

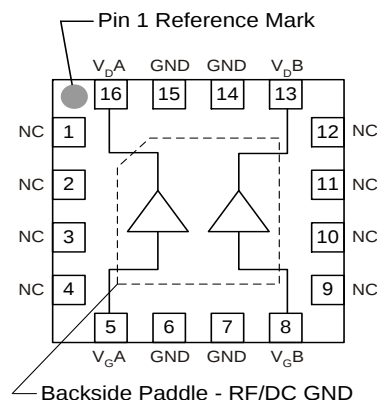


16-pin 4 x 4 mm Leadless SMT Package

Product Features

- 0.36 dB Noise Figure (Single Channel)
- 1700 – 2000 MHz
- 17.9 dB Gain (Single Channel)
- +13.4 dBm IIP3 (Single Channel)
- Compact 4 x 4 mm Package
- RoHS Compliant, Pb-free

Functional Block Diagram



General Description

The TQP3M6005 is a low noise dual pHEMT discrete device operating from 1700 – 2000 MHz. Noise figure is typically 0.36 dB per channel and 0.54 dB when used in a balanced configuration with a balun.

The TQP3M6005 consists of a single monolithic GaAs die mounted in a compact 4 x 4 QFN package. This device is a dual discrete LNA intended to be used as a balanced pair in wireless networks applications. The TQP3M6005 is packaged in a Pb-free/RoHS-compliant, compact 4 x 4 mm surface-mount leadless package.

The TQP3M6005 is useful in a number of different applications, and is particularly well suited for cellular base station or tower-mounted amplifier products.

Pin Configuration

Pin No.	Label
1, 2, 3, 4, 9, 10, 11, 12	NC (No Connect)
6, 7, 14, 15	GND (Ground)
5	V _{GA}
8	V _{GB}
13	V _{DB}
16	V _{DA}
Backside Paddle	RF / DC Ground

Ordering Information

Part No.	Description
TQP3M6005	Mid Band Dual LNA

Standard T/R size = 2500 pieces on a 13" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
Drain Voltage	+5 V
Gate Voltage	-1.0 to +0.5 V
Drain Current (Per Channel)	330 mA
Gate Current (Per Channel)	5 mA
RF Input Power (Balanced)	+10 dBm
Power Dissipation	1.1 W
Operating Channel Temperature	150 °C
Mounting Temperature (10 Seconds)	260 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _D		+4.5		V
I _D (Per Channel)		50		mA
Operating Temp. Range	-35		+105	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

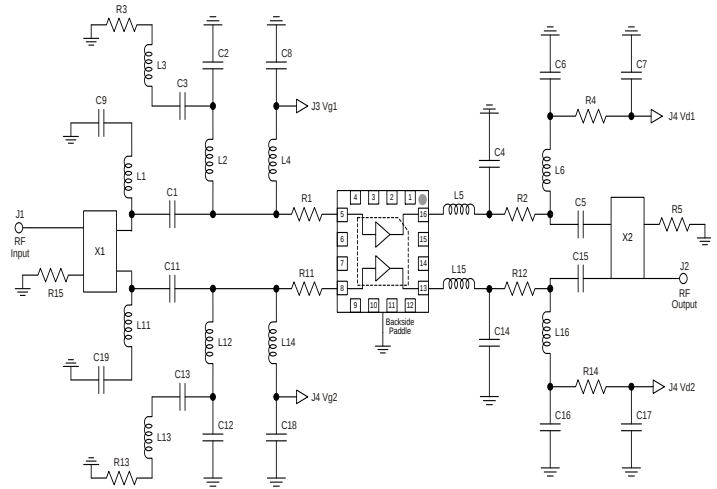
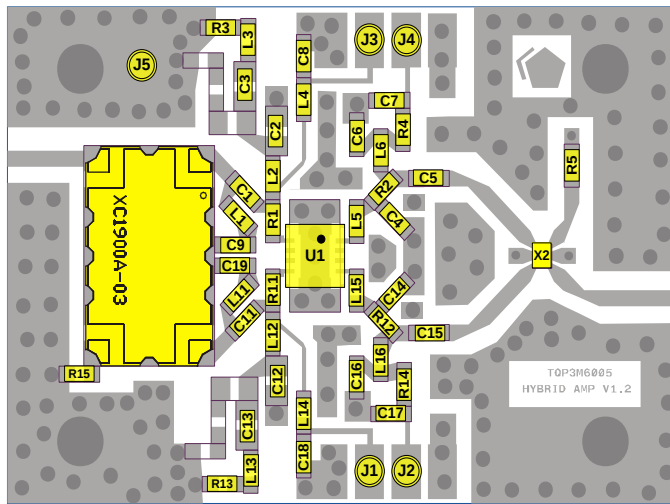
Test conditions unless otherwise noted: V_D= +4.5 V, Freq.= 1850 MHz, I_D= 50 mA per channel, T_A= 25 °C

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1700		2000	MHz
Drain Voltage ⁽¹⁾ , V _D		+2	+4.5	+5	V
Gain dual channel ⁽²⁾		16.0	17.7		dB
Noise Figure Dual Channel ⁽²⁾			0.54	0.72	dB
Noise Figure Per Channel			0.36	0.50	dB
Reverse Isolation		20	22		dB
Output P1dB Dual Channel ⁽²⁾			+21.6		dBm
Input IP3 Dual Channel ^(2,3)	F=1700 MHz	12	+14		dBm
Input IP3 Dual Channel ^(2,3)	F=1850 MHz		+15		dBm
Input IP3 Per Channel ⁽³⁾	F=1700 MHz		+9.5		dBm
Input IP3 Per Channel ⁽³⁾	F=1850 MHz		+13.4		dBm
Isolation Between Gate 1 and Gate 2			26		dB
Isolation Between Drain 1 and Drain 2			24		dB
Thermal Resistance (jnc. to case) θ_{jc}				146	°C / W

Notes:

- V_D is set based on a 1.5 Ω resistor in the drain path. See test diagram or schematic.
- Balanced pair, with baluns
- Pin / tone = -13 dBm, 8 MHz tone spacing

TQP3M6005-PCB Evaluation Board (1700 – 2000 MHz)



Notes:

1. See PC Board Layout, page 4 for more information.
2. Zero ohm jumpers may be replaced with copper traces in the target application layout.
3. Though not shown on reference design, grounding recommended on pins 6, 7, 14 & 15 for optimal isolation between amp A and B.

Bill of Material – TQP3M6005-PCB

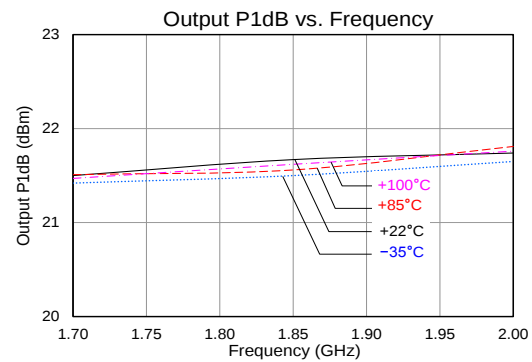
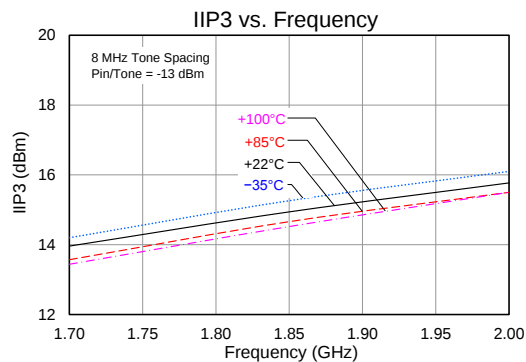
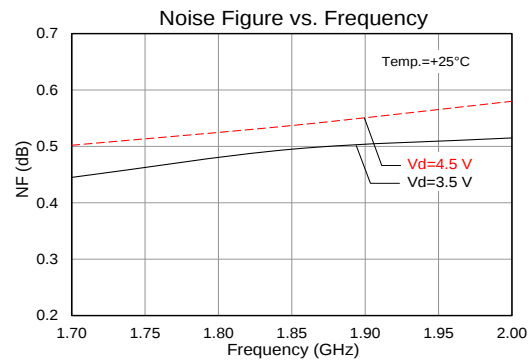
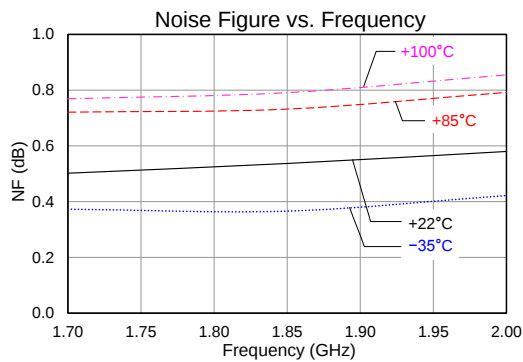
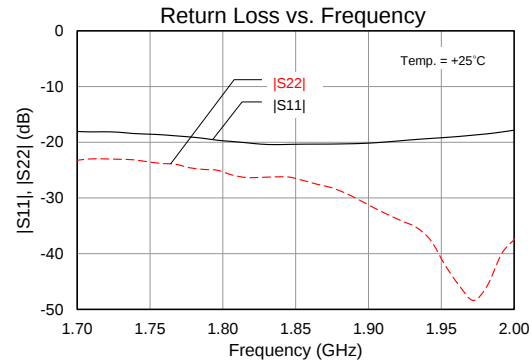
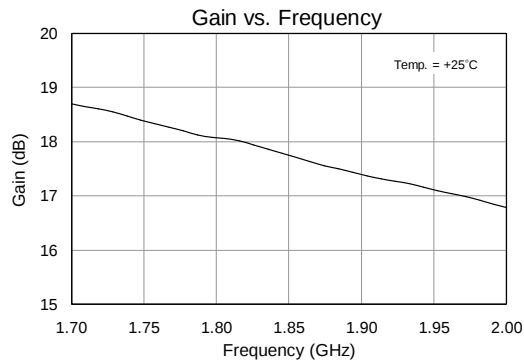
Reference Des.	Value	Description	Manuf.	Part Number
U1	N/A	Mid Band Dual LNA	TriQuint	TQP3M6005
C1, C10	2.4 pF	Capacitor, 0603, ± 0.1 pF NPO	Various	
C2, C12	10 pF	Capacitor, 0603, 5%, NPO	Various	
C3, C13	22 pF	Capacitor, 0603, 5%, NPO	Various	
C4, C14	1.2 pF	Capacitor, 0603, ± 0.1 pF NPO	Various	
C5, C15	12 pF	Capacitor, 0603, 5%, NPO	Various	
C6, C16	2.2 pF	Capacitor, 0603, ± 0.1 pF NPO	Various	
C7, C17	1 μ F	Capacitor, 0603, 10%, X5R	Various	
C8, C18	10 μ F	Capacitor, 0603, 20%, X5R	Various	
C9, C19	0.01 μ F	Capacitor, 0603, 10%, X7R	Various	
R1, R2, R11, R12	0 Ω	Resistor, 0603, 5%, 1/16W	Various	
R3, R13	8.2 Ω	Resistor, 0603, 5%, 1/16W	Various	
R4, R14	1.5 Ω	Resistor, 0603, 5%, 1/16W	Various	
R5, R15	50 Ω	Resistor, 0603, 5%, 1/16W	Various	
L1, L11	10 nH	Inductor, 0603, 5%	Coilcraft	0603CS-10NXJLW
L2, L12	3.6 nH	Inductor, 0603, 5%	Coilcraft	0603CS-3N6XJLW
L3, L13	2.2 nH	Inductor, 0603, 5%	Coilcraft	0603CS-2N2XJLW
L4, L14	33 nH	Inductor, 0603, 5%	Coilcraft	0603CS-33NXJLW
L5, L15	1.2 nH	Inductor, 0402, 5%	Coilcraft	0402CS-1N2XJLW
L6, L16	43 nH	Inductor, 0603, 5%	Coilcraft	0603CS-43NXJLW
X1	N/A	Hybrid Coupler, 3 dB, 90°	Anaren	XC1900A-03
X2	N/A	Hybrid Coupler, 3 dB, 90° 0805	Anaren	C1720J5003A00

Typical Performance (Balanced Configuration)

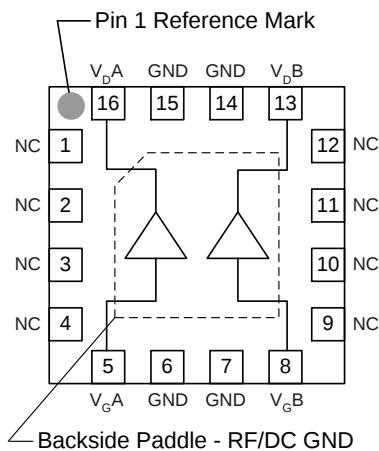
Test conditions unless otherwise noted: $V_d = +4.35$ V, $I_d = 57$ mA, Temp. = +25°C

Parameter	Typical Value			Units
Frequency	1700	1850	2000	MHz
Gain	18.7	17.7	16.8	dB
Input Return Loss	-18	-20	-18	dB
Output Return Loss	-23	-26	-38	dB
Output P1dB	+21.5	+21.6	+21.7	dBm
Input IP3 at P_{IN} / Tone = -13 dBm, 8 MHz tone spacing	+14	+15	+15.9	dBm
Noise Figure	0.5	0.54	0.58	dB

Performance Plots (Balanced Configuration)



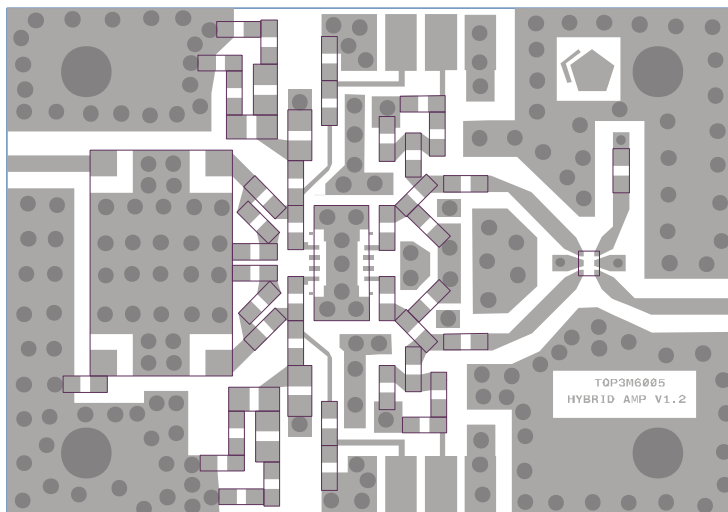
Pin Configuration and Description



Pin No.	Label	Description
1, 2, 3, 4, 9, 10, 11, 12	NC (No Connect)	No electrical connection. Land pads should be provided for PCB mounting integrity.
6, 7, 14, 15	GND (Ground)	Grounding recommended for optimal isolation between amp A and B
5	V _{GA}	RF Input – Channel A
8	V _{GB}	RF Input – Channel B
13	V _{DB}	RF Output – Channel B
16	V _{DA}	RF Output – Channel A
Backside Paddle	RF/DC Ground	RF/DC ground. Provide recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

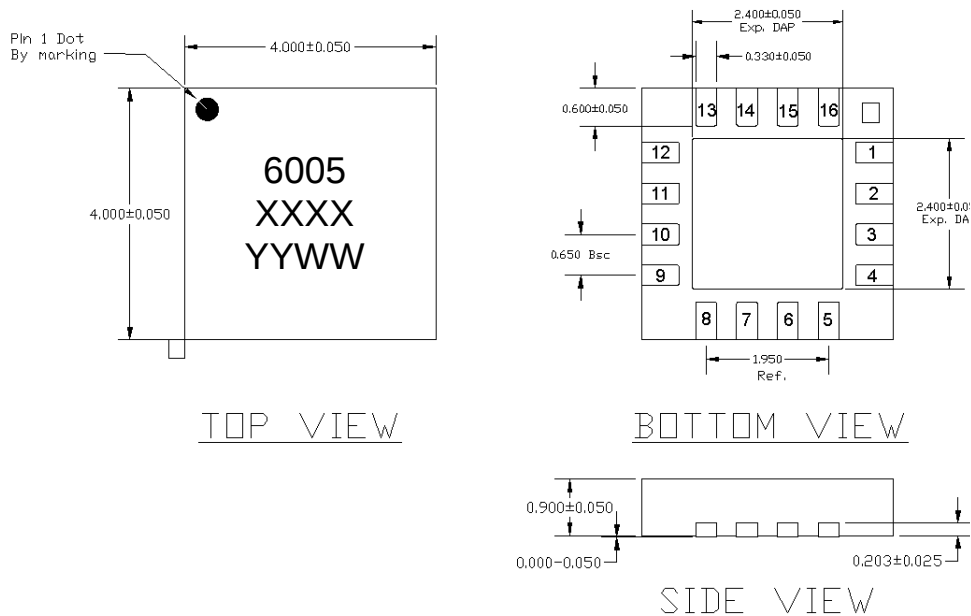
PCB Material (stackup)
Single-layer, 20 mil thick Rogers RO4350B
2.8 mil copper top and bottom



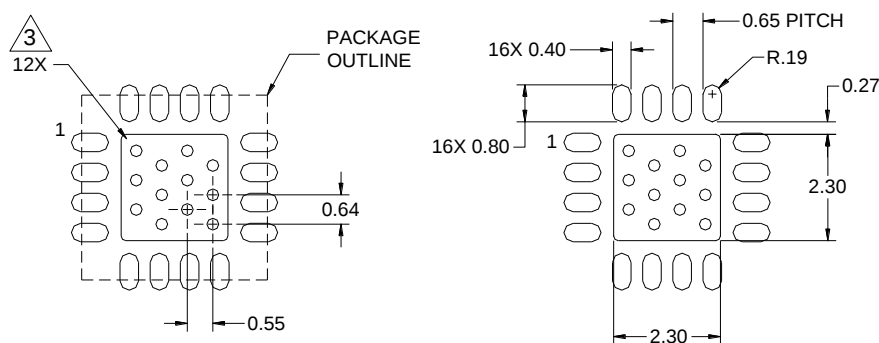
Mechanical Information

Package Marking and Dimensions

Marking: Part number – 6005
Year, week - YYWW CCCC
Assembly code - AaXXXX



PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: ≥ 250 V to < 500 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class C2
Value: ≥ 500 V to < 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: Matte Tin

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($\text{C}_{15}\text{H}_{12}\text{Br}_4\text{O}_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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Tel: 877-800-8584

For information about the merger of RFMD and TriQuint as Qorvo:

Web: www.qorvo.com

For technical questions and application information:

Email: sjcapapplications.engineering@qorvo.com

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